TAN-042

Designing the XRT71D00 and the XRT73L00 Devices to operate in the Host Mode, and to be accessed via a single Chip Select pin.

Preliminary

October 19, 2001

Revision 1.05

DESIGNING THE XRT71D00 AND THE XRT73L00 DEVICES TO OPERATE IN THE HOST MODE, AND TO BE ACCESSED VIA A SINGLE CHIP SELECT PIN

Designing the XRT71D00 and the XRT73L00 Devices to operate in the Host Mode, and to be accessed via a single Chip Select pin.

Preliminary

October 19, 2001

Revision 1.05

DESIGNING THE XRT71D00 AND THE XRT73L00 DEVICES TO OPERATE IN THE HOST MODE, AND TO BE ACCESSED VIA A SINGLE CHIP SELECT PIN

TABLE OF CONTENTS

Designing the XRT71D00 and the XRT73L00 Devices to operate in the Host Mode, and to be accessed via a single Chip Select pin.

Preliminary

October 19, 2001

Revision 1.05

1.0 INTRODUCTION

The purpose of this Applications Note is two-fold.

a. To describe a possible approach that one can use to interface the XRT71D00 DS3/E3/STS-1 Jitter Attenuator to the XRT73L00 DS3/E3/STS-1 LIU IC, while operating each device in the "Host" Mode. In particular, this Applications Note describes how to design a system, such that a Microprocessor can perform READ/WRITE access to both the XRT71D00 and the XRT73L00 device with a single Chip-Select (CS) signal.

b. To provide some "Power Conditioning" recommendations for designs using the XRT71D00 and the XRT73L00 devices.

2.0 BACKGROUND INFORMATION ON THE XRT73L00 AND XRT71D00 DEVICES

The next couple of sections present a detailed description of both the XRT73L00 and the XRT71D00 devices.

2.1 BACKGROUND INFORMATION – THE XRT73L00 1-CHANNEL DS3/E3/STS-1 LIU IC

The XRT73L00 device is a single Channel DS3/E3/STS-1 LIU IC that was designed to operate at 3.3V. Further this device can be configured via two possible approaches.

a. The Hardware Mode
b. The Host Mode.

If the XRT73L00 device has been configured to operate in the "Hardware" Mode, then all Mode/Configuration selection is achieved by setting certain input pins either "HIGH" or "LOW". If the user configures the XRT73L00 device to operate in the "Hardware" Mode, then the user can configure the XRT73L00 device into a wide variety of modes, via the following external input pins.

- REQDIS – Receive Equalizer Enable/Disable Input pin
- TXLEV – Transmit Line Build-Out Circuit Enable/Disable Input pin.
- LLB & RLB – Loop Mode Select input pins.
- STS-1/DS3* & E3 – Data Rate Select Input pins.
- ENDECDIS – B3ZS/HDB3 Encoder & Decoder Block Enable/Disable Input pin.
- DR/SR* - Dual-Rail/Single-Rail Select Input pin.
- TxOFF – Transmit Shut Off Input pin.
- TAOS – Transmit All Ones Enable Input pin
- RCLK2INV – RCLK2 Invert/Non-Invert Select Input pin.

Therefore, for Hardware Mode operation, the XRT73L00 device provides the user with 11 input pins that can be used to control various operational aspects of the XRT73L00 device.

If the XRT73L00 device has been configured to operate in the Host Mode, then all Mode/Configuration selection is achieved by writing data into the on-chip Command Registers (via the Microprocessor Serial Interface block). The Microprocessor Serial Interface block consists of the following pins.

- SDI – Serial Data In
- SDO – Serial Data Out
- SCLK – Serial Clock In
- CS* - Chip Select Input
- REG_RESET* - Register Reset Input.

A more detailed description of each of these pins is presented in Appendix C.

Therefore, for Host Mode operation, the XRT73L00 device provides the user with 5 pins (4 input and 1 output) that can be used to control various operational aspects of the XRT73L00 device.

The bit-format of the Command Register set, within the XRT73L00 LIU device is presented below in Figure 1.

			Register Bit-Format				
Address	**Command Register**	**Type**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	RO	RLOL	RLOS	ALOS	DLOS	DMO
0x01	CR1	R/W	TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
0x02	CR2	R/W	Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
0x03	CR3	R/W	RNRZ	LOSMUT	RCLK2/ LCV*	RCLK2INV	RCLK1INV
0x04	CR4	R/W	Reserved	STS-1/ DS3*	E3	LLB	RLB
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x08	CR8	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Figure 1, The Bit Format of the Command Registers, within the XRT73L00 Device.

A detailed discussion of each of these command register bits is presented in Appendix A.

2.2 BACKGROUND INFORMATION – THE XRT71D00 1-CHANNEL DS3/E3/STS-1 JITTER ATTENUATOR IC

The XRT71D00 device is a single-channel DS3/E3/STS-1 Jitter Attenuator IC that was designed to operate at either 3.3V or 5V. Further, this device can be configured via two possible approaches.

a. The Hardware Mode
b. The Host Mode

If the XRT71D00 device has been configured to operate in the "Hardware" Mode, then all Mode/Configuration selection is achieved by setting certain input pins either "HIGH" or "LOW". If the user configures the XRT71D00 device to operate in the "Hardware" Mode, the user can configure the XRT71D00 device into a wide variety of modes, via the following external input pins.

- FSS – FIFO Size Select
- DJA – Disable (Jitter Attenuator PLL) Select
- CLKES – Clock Edge Select
- BWS – (Jitter Attenuator PLL) Bandwidth Select
- DS3*/E3 – Data Rate Select Input pin
- STS-1 – Data Rate Select Input pin.

Therefore, for Hardware Mode operation, the XRT71D00 device provides the user with 6 input pins that can be used to control various operational aspects of the XRT71D00 device.

If the XRT71D00 device has been configured to operate in the "Host" Mode, then all Mode/Configuration is achieved by writing data into the on-chip Command Registers (via the Microprocessor Serial Interface block). The Microprocessor Serial Interface block consists of the following pins.

- SDI – Serial Data In
- SDO – Serial Data Out
- SCLK – Serial Clock Input
- CS* - Chip Select Input
- RST* - Reset Input

A more detailed description of each of these pins is presented in Appendix C.

Therefore, for Host Mode Operation, the XRT71D00 device provides the user with five (5) pins (4 inputs and 1 output) that can be used to control various aspects of the XRT71D00 device.

The bit-format of the Command Register set, within the XRT71D00 Jitter Attenuator device is presented below in Figure 2.

			Register Bit-Format						
Addr.	**Command Register**	**Type**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
			Channel 0 Registers						
0x06	CR6	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES	FSS
0x07	CR7	R/O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FL
			Channel 1 Registers						
0x0E	CR14	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES	FSS
0x0F	CR15	R/O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FL
			Channel 2 Registers						
0x16	CR22	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES	FSS
0x17	CR23	R/O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FL

Figure 2, The Bit Format of the Command Registers, within the XRT71D00 Device.

A detailed discussion of each of these Command Register bits are presented in Appendix B.

3.0 THE CHANNEL ASSIGNMENT FEATURE OF THE XRT71D00 DEVICE

The "Channel Assignment" feature, within the XRT71D00 device, permits the user to perform "READ/WRITE" access to the following sets of devices, with only one Chip Select pin.

- 1- XRT73L00 1-Channel DS3/E3/STS-1 LIU IC and 1-XRT71D00 DS3/E3/STS-1 Jitter Attenuator IC.
- 1-XRT7300 1-Channel DS3/E3/STS-1 LIU IC and 1-XRT71D00 DS3/E3/STS-1 Jitter Attenuator IC.
- 1- XRT73L02 2-Channel DS3/E3/STS-1 LIU IC and 2-XRT71D00 DS3/E3/STS-1 Jitter Attenuator Devices.
- 1-XRT7302 2-Channel DS3/E3/STS-1 LIU IC and 2-XRT71D00 DS3/E3/STS-1 Jitter Attenuator Devices.
- 1-XRT73L03 3-Channel DS3/E3/STS-1 LIU IC and 3-XRT71D00 DS3/E3/STS-1 Jitter Attenuator Devices.

Figure 2 presents the bit format of the Command Registers, within the XRT71D00 device. In this figure, the Command Register set is sub-divided into "Channels". Command Registers CR6 and CR7 are allocated to "Channel 0"; Command Registers CR14 and CR15 are allocated to "Channel 1"; and finally, Command Registers CR22 and CR23 have been allocated to "Channel 2". The XRT71D00 device contains two external input pins, which are relevant to this discussion.

- Ch_Addr_0 (Pin 28)
- Ch_Addr_1 (Pin 15)

A XRT71D00 device (within a given system) can be assigned a "Channel Number" by setting the "Ch_Addr_0" and "Ch_Addr_1" input pins either high or low. The relationship between the states of the "Ch_Addr_0" and the "Ch_Addr_1" input pins, and the "Assigned Channel" is presented below in Table 1.

Table 1, The Relationship between the Logic States of the "Ch_Addr_0" and "Ch_Addr_1" input pins, and the "Assigned Channel"

Ch_Addr_1	Ch_Addr_0	Assigned Channel
0	0	Channel 0
0	1	Channel 1
1	0	Channel 2
1	1	Not Valid

If a given XRT71D00 device is assigned to "Channel 0" then it will only respond to READ/WRITE operations to Address locations 0x06 and 0x07 (within the device). If the Microprocessor attempts to perform write operations to address locations "0x0E" and "0x16", then the XRT71D00 device will ignore this particular operation. Further, if the Microprocessor attempts to perform read operations to address locations "0x0E", "0x0F", "0x16" and "0x17", then the XRT71D00 device will simply ignore these particular operations and will continue to tri-state its "SDO" output pin.

Similarly, if a given XRT71D00 device is assigned to "Channel 1" then it will only respond to READ/WRITE operations to Address locations 0x0E and 0x0F (within the device). If the Microprocessor attempts to perform write operations to address locations "0x06" and "0x16", then the XRT71D00 device will ignore this particular operation. Further, if the Microprocessor attempts to perform read operations to address locations "0x06", "0x07", "0x16" and "0x17", then the XRT71D00 device will simply ignore these particular operations and will continue to tri-state its "SDO" output pin.

This Applications Note discusses how to interface a single XRT71D00 device to the XRT73L00 device. Therefore, the Jitter Attenuator IC (within this Applications Note) will be assigned to "Channel 0".

When the XRT71D00 device has been assigned to "Channel 0" and has been interfaced with the XRT73L00 device (as shown in Figure 3); then the resulting composite Command Register Address Map is as presented below.

			Register Bit-Format						
Addr.	**Command Register**	**Type**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	R/O	Res.	Res.	RLOL	RLOS	ALOS	DLOS	DMO
0x01	CR1	R/W	Res.	Res.	TXOFF	TAOS	TXCLK INV	TXLEV	TXBIN
0x02	CR2	R/W	Res.	Res.	Res.	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
0x03	CR3	R/W	Res.	Res.	RNRZ	LOSMUT	RCLK2/ LCV*	RCLK2 INV	RCLK1 INV
0x04	CR4	R/W	Res.	Res.	Res.	STS-1/ DS3*	E3	LLB	RLB
0x05	CR5	R/W	Res.	Res.	Res.	Res.	Res.	Res.	Res.
0x06	CR6	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES	FSS
0x07	CR7	R/O	Res.	Res.	Res.	Res.	Res.	Res.	FL

Figure 3, The Bit-Format of the "Composite Set" of Command Registers (from the XRT73L00 and the XRT71D00 Device).

NOTE: The "shaded" register bits (within Figure 4) actually reside within the XRT71D00 device. Conversely, the "un-shaded" register bits actually reside within the XRT73L00 device.

4.0 HARDWARE DESIGN CONSIDERATIONS

Figures 4 and 6 each presents a schematic design of the XRT71D00 device being interfaced to the XRT73L00 device. In these schematics, both the XRT73L00 and the XRT71D00 devices have been configured to operate in the "Host" Mode. In the case of Figure 4, the XRT71D00 device has been designed to operate in the Receive Path. Additionally, in the case of Figure 6, the XRT71D00 device has been designed to operate in the Transmit Path.

There are numerous other things to note about Figures 4 and 6.

1. The XRT71D00 and the XRT73L00 devices are each connected to the following signals.

a. HW_RESET*

This signal is tied to the "RST*" input pin of the XRT71D00 device and the "REG_RESET*" input pin of the XRT73L00 device. Therefore, pulsing the "HW_RESET*" input signal "low" will command a "Hardware RESET" to both the Jitter Attenuator and the LIU IC.

b. JA_LIU_CS*

This signal is tied to the CS* (Chip-Select) input pins of both the XRT71D00 and the XRT73L00 devices. Therefore, pulsing the "JA_LIU_CS*" input signal "low" asserts Chip Select for both of these devices, simultaneously.

c. JA_LIU_SCLK_IN

This input signal is tied to the "SCLK" input pins of both the XRT71D00 and the XRT73L00 devices. Hence, applying a clock signal to this input signal permits the clock signal to be applied to the "SCLK" input pins of both devices, simultaneously.

d. JA_LIU_SDI_IN

This input signal is tied to the "SDI" input pins of both the XRT71D00 and the XRT73L00 devices. Hence, applying data (via this signal) permits this signal to be applied to the "SDI" input pins of both devices, simultaneously.

e. JA_LIU_SDO_OUT

This output signal is tied to the "SDO" output pins of both the XRT71D00 and the XRT73L00 device. Therefore, either the "SDO" output pin of the XRT73L00 device, or that of the XRT71D00 device can drive this output signal.

Designing the XRT71D00 and the XRT73L00 Devices to operate in the Host Mode, and to be accessed via a single Chip Select pin.

Preliminary

October 19, 2001

Revision 1.05

IMPORTANT INFORMATION ABOUT THE SDO OUTPUT PINS OF THE XRT71D00 AND THE XRT73L00 DEVICE

Earlier, this Applications Note states that since the XRT71D00 device has been assigned to "Channel 0", then it will only respond to READ operations to address locations "0x06" and "0x07". Additionally, the XRT71D00 device will also tri-state its SDO output pin during READ operations to any other address location. The purpose behind this feature is to prevent the XRT71D00 device from contending with the XRT73L00 device over the JA_LIU_SDO_OUT" line, by pulling its SDO output pin to GND. By designing the XRT71D00 device to tri-state its SDO output, whenever the Microprocessor performs a READ operation to other address locations (e.g., within the XRT73L00 Command Register); this prevents the XRT71D00 device from pulling the entire "JA_LIU_SDO_OUT" line to GND, and corrupting the data that needs to be read via from the XRT73L00 LIU Device.

Unfortunately, the XRT73L00 LIU IC does not have this same "tri-stating of the SDO output pin" feature. Further, the content of any Command Register bit (within the XRT73L00 device) other than those at address locations "0x00" through "0x04"; are set to "0". Therefore, whenever the Microprocessor performs a READ operation to any address location, other than locations "0x00" through "0x04", then the XRT73L00 LIU IC will automatically pull its SDO output pin to GND.

HOW TO SOLVE THIS PROBLEM

This issue with the SDO output pins means that simply tying the SDO output pins, of the two devices together, is not a prudent thing to do. Instead, we recommend that the user route the SDO output (of the XRT73L00 LIU device) through a 475 Ω resistor, prior to being connected to the trace carrying the SDO output of the XRT71D00 device. This 475 Ω resistor serves to isolate the data, being output via the SDO output pin, of the XRT71D00 device; from the SDO output pin of the XRT73L00 device.

2. The XRT71D00 device has been designed to operate in the Receive Path (Figure 4)

Figure 4 presents a schematic design in which the Jitter Attenuator is placed in the "Receive Path" such that the "RPOS", "RNEG" and "RCLK" output signals (from the XRT73L00 LIU IC) are being routed to the "RPOS", "RNEG" and "RCLK" input signals of the XRT71D00 Jitter Attenuator IC.

3. The XRT71D00 device has been designed to operate in the Transmit Path (Figure 6).

It should be noted that it is entirely acceptable to design a board such that the Jitter Attenuator is placed in the "Transmit Path"; as is shown in Figure 6. Please note that in this case, the "RRPOS", "RRNEG" and "RRCLK" outputs (from the XRT71D00 Jitter Attenuator IC) are being routed to the "TPDATA", "TNDATA" and "TCLK" input signals of the LIU IC.

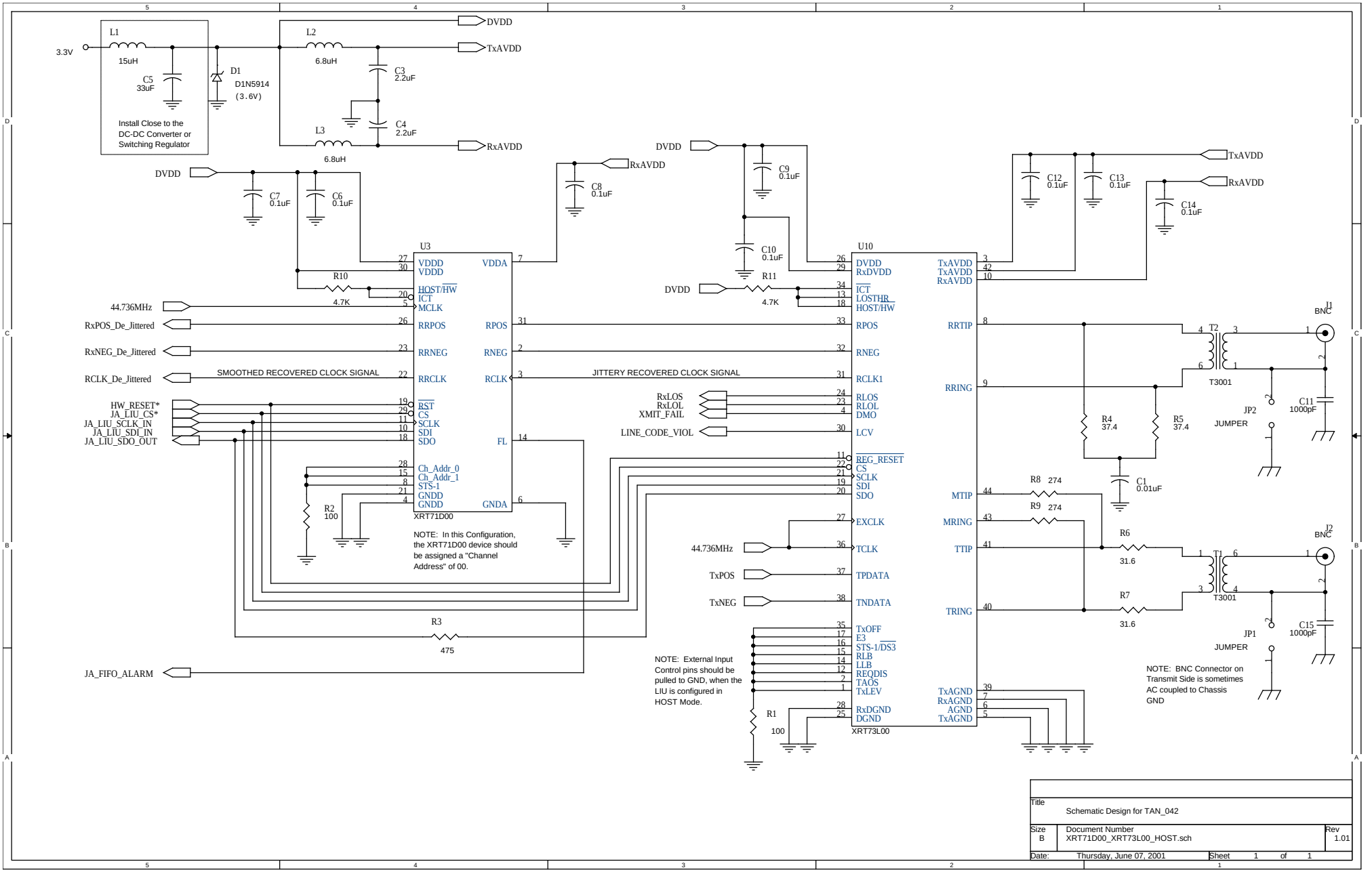
4.1 DESIGN CONSIDERATIONS WHEN THE JITTER ATTENUATOR IS DESIGNED IN THE RECEIVE PATH

If the user has designed his/her board such that the XRT71D00 device is operating in the "Receive Path" (as illustrated in Figure 4), then it is imperative that the two devices be configured such that the "set-up" and "hold" time requirements (of the RPOS/RNEG inputs of the XRT71D00 device) are met.

By default, the XRT73L00 device will update its "recovered" data, via the "RPOS" and "RNEG" output pins, upon the rising edge of "RCLK1" and "RCLK2". According to the XRT73L00 Data Sheet, the "RCLK to RPOS/RNEG" output delay is about 4ns (maximum). Therefore, the user is advised to configure the XRT71D00 device to sample the data, via its "RPOS" and "RNEG" input pins, upon the falling edge of the "RCLK" input signal. According to the XRT71D00 Data Sheet, the "RPOS/RNEG" to "RCLK" set-up and hold time requirements are each 3ns (maximum).

In order to achieve this configuration, the user must insure that the "RCLK1" or "RCLK2" bit-fields (within the XRT73L00 device) are set to "0", and that the "CLKES" bit-field (within the XRT71D00 device) is set to "1"; as illustrated below.

FIGURE 4, SCHEMATIC DESIGN OF XRT71D00 DEVICE BEING INTERFACED TO THE XRT73L00 DEVICE (IN THE RECEIVE PATH)


3.3V
L1
15uH
C5
33uF
Install Close to the DC-DC Converter or Switching Regulator
D1
D1N5914
(3.6V)
L2
6.8uH
C3
2.2uF
C4
2.2uF
L3
6.8uH
DVDD
TxAVDD
RxAVDD
C7
0.1uF
C6
0.1uF
C8
0.1uF
C9
0.1uF
C10
0.1uF
C12
0.1uF
C13
0.1uF
C14
0.1uF
U3
VDDD
VDDD
VDDA
HOST/HW
ICT
MCLK
RRPOS
RPOS
RRNEG
RNEG
RRCLK
RCLK
RST
CS
SCLK
SDI
SDO
FL
Ch_Addr_0
Ch_Addr_1
STS-1
GNDD
GNDD
GNDA
XRT71D00
R10
4.7K
R11
4.7K
R2
100
R3
475
R1
100
44.736MHz
RxPOS_De_Jittered
RxNEG_De_Jittered
RCLK_De_Jittered
SMOOTHED RECOVERED CLOCK SIGNAL
JITTERY RECOVERED CLOCK SIGNAL
HW_RESET*
JA_LIU_CS*
JA_LIU_SCLK_IN
JA_LIU_SDI_IN
JA_LIU_SDO_OUT
JA_FIFO_ALARM
NOTE: In this Configuration, the XRT71D00 device should be assigned a "Channel Address" of 00.
U10
DVDD
RxDVDD
ICT
LOSTHR
HOST/HW
RPOS
RNEG
RCLK1
RLOS
RLOL
DMO
LCV
REG_RESET
CS
SCLK
SDI
SDO
EXCLK
TCLK
TPDATA
TNDATA
TxOFF
E3
STS-1/DS3
RLB
LLB
REQDIS
TAOS
TxLEV
RxDGND
DGND
XRT73L00
RxLOS
RxLOL
XMIT_FAIL
LINE_CODE_VIOL
TxPOS
TxNEG
NOTE: External Input Control pins should be pulled to GND, when the LIU is configured in HOST Mode.
TxAVDD
TxAVDD
RxAVDD
RRTIP
RRING
MTIP
MRING
TTIP
TRING
TxAGND
RxAGND
AGND
TxAGND
R8
274
R9
274
R6
31.6
R7
31.6
R4
37.4
R5
37.4
C1
0.01uF
T2
T3001
T1
T3001
J1
BNC
J2
BNC
JP2
JUMPER
JP1
JUMPER
C11
1000pF
C15
1000pF
NOTE: BNC Connector on Transmit Side is sometimes AC coupled to Chassis GND
Title
Schematic Design for TAN_042
Size
B
Document Number
XRT71D00_XRT73L00_HOST.sch
Rev
1.01
Date:
Thursday, June 07, 2001
Sheet
1
of
1

Designing the XRT71D00 and the XRT73L00 Devices to operate in the Host Mode, and to be accessed via a single Chip Select pin.

Preliminary

October 19, 2001

Revision 1.05

			Register Bit-Format						
Addr.	**Command Register**	**Type**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	R/O	Res.	Res.	RLOL	RLOS	ALOS	DLOS	DMO
0x01	CR1	R/W	Res.	Res.	TXOFF	TAOS	TXCLK INV	TXLEV	TXBIN
0x02	CR2	R/W	Res.	Res.	Res.	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
0x03	CR3	R/W	Res.	Res.	RNRZ	LOSMUT	RCLK2/ LCV*	RCLK2 INV 0	RCLK1 INV 0
0x04	CR4	R/W	Res.	Res.	Res.	STS-1/ DS3*	E3	LLB	RLB
0x05	CR5	R/W	Res.	Res.	Res.	Res.	Res.	Res.	Res.
0x06	CR6	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES 0	FSS
0x07	CR7	R/O	Res.	Res.	Res.	Res.	Res.	Res.	FL

Figure 5, The Recommended Bit-Format of the "Composite Set" of Command Registers (from the XRT73L00 and the XRT71D00 Device), when the XRT71D00 device is configured to operate in the "Receive Path".

If the above-mentioned configuration is implemented, then the XRT71D00 device will be provided with the following set-up and hold times, for each of the three (3) data rates.

Table 2, The "RPOS/RNEG" to "RCLK" Set-up and Hold Times provided to the XRT71D00 Device, when configured as presented in Figure 4.

Data Rate	RPOS/RNEG to RCLK Set-up Time Provided	RCLK to RPOS/RNEG Hold Time Provided
E3	10.5ns	18.5ns
DS3	7ns	15ns
STS-1	5.5ns	13.5ns

NOTES:

1. Minimum "RPOS/RNEG to RCLK Set-up Time" Requirements of XRT71D00 Device = 3ns.
2. Minimum "RCLK to RPOS/RNEG Hold-Time Requirements of the XRT71D00 Device = 3ns.

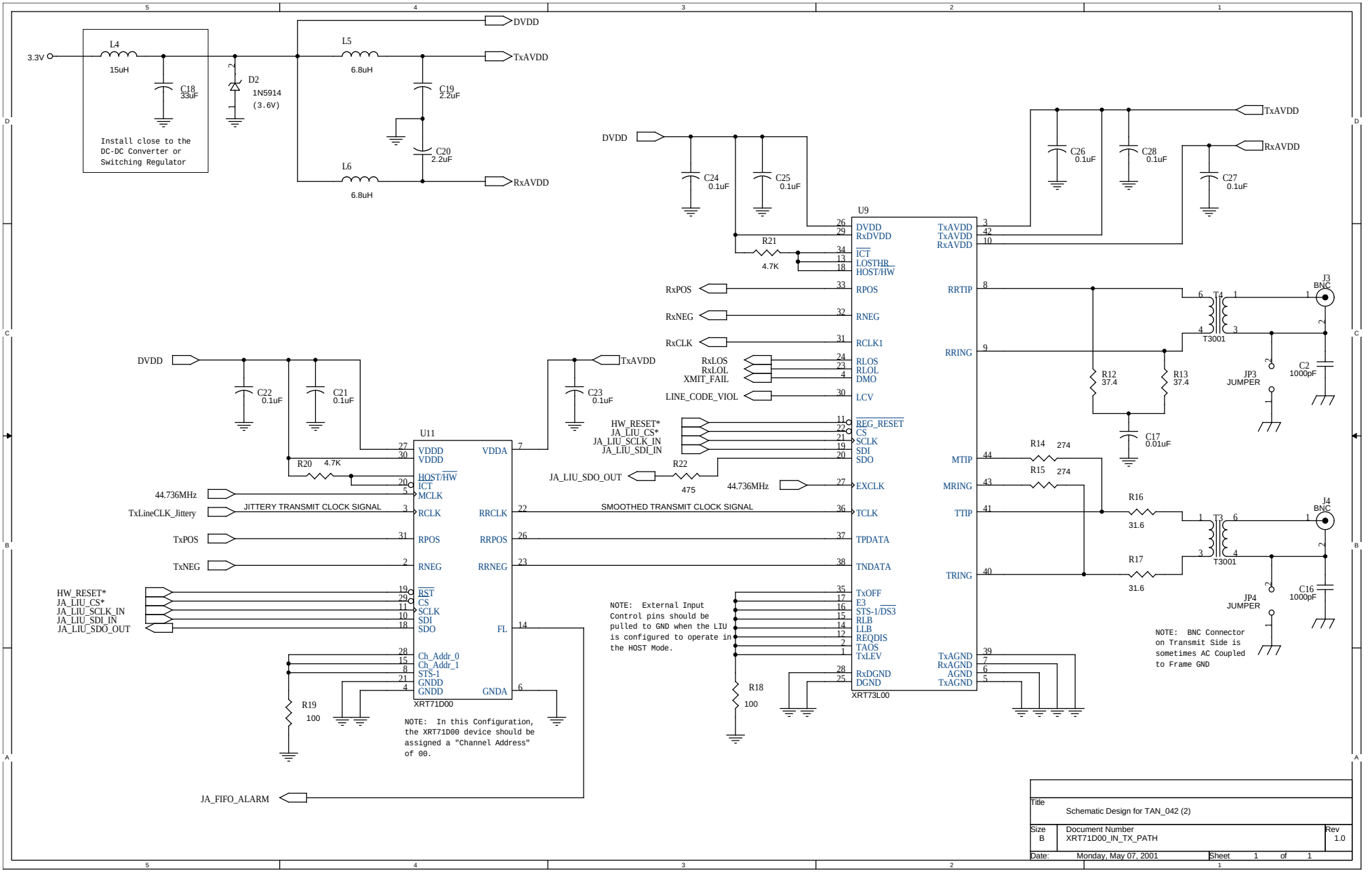
4.2 DESIGN CONSIDERATIONS WHEN THE JITTER ATTENUATOR IS DESIGNED IN THE TRANSMIT PATH

If the user has designed his/her board such that the XRT71D00 device is operating in the "Transmit Path" (as illustrated in Figure 6), then it is imperative that the two devices be configured such that the "set-up" and "hold" time requirements (of the TPDATA/TNDATA inputs of the XRT73L00 device) are met.

By default, the XRT73L00 device will sample the data, input at the "TPDATA/TNDATA" pins, upon the falling edge of "TCLK". According to the XRT73L00 Data Sheet, the "TPDATA/TNDATA to TCLK" set-up time requirements are 3ns (minimum). Additionally, the "TCLK to TPDATA/TNDATA" hold time requirements are also 3ns (minimum). According to the XT71D00 Data Sheet, the "RRPOS/RRNEG to RRCLK" output delay is 5ns (maximum). Therefore, the user is advised to configure the XRT71D00 device to output the "RRPOS/RRNEG" data upon the rising edge of "RRCLK".

In order to achieve this configuration, the user must insure that the "TXCLK INV" bit-field (within the XRT73L00 device) is set to "0", and that the "CLKES" bit-field (within the XRT71D00 device) is set to "1"; as illustrated below.

FIGURE 6, SCHEMATIC DESIGN OF XRT71D00 DEVICE BEING INTERFACED TO THE XRT73L00 DEVICE (IN THE TRANSMIT PATH)



Title	Schematic Design for TAN_042 (2)	
Size B	Document Number XRT71D00_IN_TX_PATH	Rev 1.0
Date: Monday, May 07, 2001	Sheet 1 of 1	

			Register Bit-Format						
Addr.	**Command Register**	**Type**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	R/O	Res.	Res.	RLOL	RLOS	ALOS	DLOS	DMO
0x01	CR1	R/W	Res.	Res.	TXOFF	TAOS	TXCLK INV 0	TXLEV	TXBIN
0x02	CR2	R/W	Res.	Res.	Res.	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
0x03	CR3	R/W	Res.	Res.	RNRZ	LOSMUT	RCLK2/ LCV*	RCLK2 INV	RCLK1 INV
0x04	CR4	R/W	Res.	Res.	Res.	STS-1/ DS3*	E3	LLB	RLB
0x05	CR5	R/W	Res.	Res.	Res.	Res.	Res.	Res.	Res.
0x06	CR6	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES 0	FSS
0x07	CR7	R/O	Res.	Res.	Res.	Res.	Res.	Res.	FL

Figure 7, The Recommended Bit-Format of the "Composite Set" of Command Registers (from the XRT73L00 and the XRT71D00 Device), when the XRT71D00 device is configured to operate in the "Transmit Path".

If the above-mentioned configuration is implemented, then the XRT71D00 device will be provided with the following set-up and hold times, for each of the three (3) data rates.

Table 3, The "TPDATA/TNDATA" to "TCLK" Set-up and Hold Times provided to the XRT71D00 Device, when configured as presented in Figure 6.

Data Rate	TPDATA/TNDATA to TCLK Set-up Time Provided	TCLK to TPDATA/TNDATA Hold Time Provided
E3	9.5ns	19.5ns
DS3	6ns	16ns
STS-1	4.5ns	14.5ns

NOTES:

1. Minimum "TPDATA/TNDATA to TCLK Set-up Time" Requirements of XRT73L00 Device = 3ns.
2. Minimum "TCLK to TPDATA/TNDATA Hold-Time Requirements of the XRT73L00 Device = 3ns.

5.0 POWER CONDITION CONSIDERATIONS FOR THE XRT73L00 AND THE XRT71D00 DEVICES

The XRT73L00 is a 1-Channel DS3/E3/STS-1 Transceiver (Line Interface Unit) IC that is designed for use in multi-standard Networking and Transmission Systems. Likewise, the XRT71D00 is a 1-Channel DS3/E3/STS-1 Jitter Attenuator IC that is also designed for use in these same multi-standard Networking and Transmission Systems.

The XRT73L00 device is a mixed signal device that supports the transmission and reception of data at the DS3, E3 and STS-1 rates. Hence, this chip handles both digital inputs and output signals (which switch at very fast rates and generate a lot electrical and radio frequency noise). Additionally, this chip also consists of an independent sensitive analog receiver. As a consequence, the user must be careful in how to handle the VDD and GND pins, in order to ensure high-quality performance of the XRT73L00 device.

The XRT71D00 device is also a mixed signal device. This particular device consists of an Analog and Digital PLL. Each of these PLLs is used to generate high-speed signals that support loop filtering within the Jitter Attenuator IC. This loop filtering essentially defines the Jitter Transfer Characteristics of the XRT71D00 device. As a consequence, the user must also be careful in how to handle the VDD and GND pins, in order to ensure high-quality performance of the XRT71D00 device.

In particular, the user's PCB layout and handling of the VDD and GND signals must accomplish the following:

1. It must provide good isolation between the Transmit and Receive signals.
2. It must provide good isolation between the Analog and Digital signals.
3. It must provide good isolation between signals from other components on the board.

In many networking or transmission systems, the source of power is a DC-to-DC converter, which uses a switching converter to transform a –48VDC input to a +3.3VDC output. The switching converter typically uses a switching frequency from 20kHz to 1MHz and the 3.3VDC power normally carries a significant amount of "ripple" noise at this switching frequency. This ripple noise can adversely affect performance of analog circuits in the mixed signals devices (e.g., XRT73L00 and XRT71D00).

This section presents some guidelines on how to layout and filter the VDD and GND signals that are fed to the XRT73L00 and XRT71D00 devices.

The XRT73L00 and XRT71D00 "GND" Pins

Tie all XRT73L00 and XRT71D00 "GND" pins to the system ground plane. In cases where there are separate analog and digital ground planes, tie all "GND" pins to the analog ground. Do not insert any impedance (in the form of an inductor or ferrite bead) between the analog and digital ground pins of the XRT73L00 and XRT71D00 devices.

The XRT73L00 and XRT71D00 "POWER" Pins

The XRT73L00 device contains five (5) power supply pins. Pin 10 is the Receive Analog Section power supply pin. Pins 3 and 42 are the Transmit Analog Section power supply pins. Finally, pins 26 and 29 are the digital power supply pins.

Likewise, the XRT71D00 device contains three (3) power supply pins. Pin 7 is the Analog power supply pin. Pins 27 and 30 are the digital power supply pins.

The Receive Analog Power supply pin (e.g., pin 10) of the LIU is the most critical, as it powers the Clock Recovery PLL. Therefore, the power to this pin should be as clean as possible.

It is also desirable to keep the Transmit Power Supply noise isolated from the Receive Power supply. Further, it is also desirable to keep the other components, on the board isolated from each other, in order to minimize cross-talk.

The attached schematics (e.g., Figures 4 and 6) illustrate Exar's recommendation on how to connect the Analog and Digital VDD pins (of the XRT73L00 and the XRT71D00 devices) to a 3.3V power supply. Exar's approach recommends the use of two-stage LC filtering.

STAGE 1 – A LARGE LC FILTER (consisting of L1 and C5)

This particular LC filter consists of a 15uH inductor and a 33uF capacitor. The purpose of this LC filter is to eliminate much of the "DC-to-DC Converter-induced" low frequency ripple, within the 3.3V power supply line, prior to being routed to any of the VDD pins of the XRT73L00 and the XRT71D00 devices.

NOTES ABOUT THIS LC FILTER:

1. This LC filter should be placed close to the output of the DC-to-DC Converter.

2. Only one such LC filter is needed, per board (even in multi-channel applications). However, multi-channel designs may still have to use multiple instantiations of this LC filter due to large voltage drops across the inductor (due to the increased amount of current draw of multiple XRT73L00 and XRT71D00 devices and the dc resistance of the inductor), or because of the maximum operating current limit of this inductor as well.
3. This LC filter may not be necessary if the 3.3V Power Supply is already filtered elsewhere in the system.

COMPONENT SELECTION FOR L1 AND C5

The XRT73L00 device draws approximately 140mA and the XRT71D00 device draws approximately 30mA. Therefore, this combined solution draws about 170mA. We recommend that the user select a High-Current Inductor that has a small enough DC resistance such that the voltage drop across the inductor will not exceed 50mV. Therefore, the user should select a 15uH inductor that has a DC resistance of less than 0.294Ω.

An example of an acceptable inductor for L1 is the 4922-15L from API-Delevan. This particular inductor has a maximum dc resistance of 0.089Ω, and has a maximum current rating of 2.11A. Contact information for API-Delevan is presented in Appendix D, at the end of this Applications Note.

The capacitor, C5, should be a 33uF 10V Tantalum capacitor, which is supplied by various manufacturers. Digikey PCT2336CT-ND or equivalent would be acceptable.

STAGE 2 – SMALLER LC FILTERING FOR RECEIVE AND TRANSMIT ANALOG VDD PINS

After the Power Supply signal passes through the large LC filter (consisting of L1 and C5), it should then be routed to three different points, in parallel (in order to support both the XRT73L00 and the XRT71D00 device).

- Directly to the Digital VDD pins of the XRT73L00 and the XRT71D00 devices.
- To an LC filter (consisting of L3 and C4), prior to being routed to the Receive Analog VDD pin of the XRT73L00 LIU IC (pin 10) and the Analog VDD pin of the XRT71D00 Jitter Attenuator IC (pin 7).
- To an LC filter (consisting of L2 and C3) prior to being routed to the Transmit Analog VDD pins of the XRT73L00 LIU IC (pins 3 and 42).

The purpose of this LC filter is three-fold.

1. To provide some isolation and filtering between the Digital VDD and the Analog VDD lines.
2. To provide some isolation (and reduce cross-talk) between the Transmit and Receive Analog VDD lines.
3. To provide some isolation (and reduce cross-talk) between each of the components of the line card.

NOTE: In contrast to the LC filter (consisting of Inductor L1 and capacitor C5), these LC filters must not be shared with other LIU or Jitter Attenuator Devices.

COMPONENT SELECTION FOR L2, L3 AND C3, C4

As mentioned above, each of the LC filters (consisting of Inductors L2 and L3 and capacitors C3 and C4) are used to filter and isolate the power supply line, going to the LIU Receive Analog VDD/Jitter Attenuator Analog VDD pins and the LIU Transmit Analog VDD pins. Each of these inductors should be of the value 6.8uH, and each of these capacitors should be of value 2.2uF.

The current consumption (via each of the Power Supply pins, of the XRT73L00 device) is presented below in Table 4.

Table 4, The Current Consumption via each of the XRT73L00 Power Supply Pins

Pin Number	Description	Amount of Current
3	Transmit Analog VDD	4.7mA
10	Receive Analog VDD	59.3mA
26	EXCLK_VDD	1.45mA
29	Receive Digital VDD	16.9mA
42	Transmit Analog VDD	49.9mA
Total Current Consumption – Channel 0		**132.25mA**

NOTE: Current consumption measurements were made while the XRT73L00 device was operating in the "STS-1" Mode, and transmitting/receiving an "All Ones" pattern.

Similarly, the current consumption (via each of the Power Supply pins, of the XRT71D00 device) is presented below in Table 5.

Table 5, A Listing of the Amount of Current Consumed via each of the VDD pins within the XRT71D00 device (3.3V operation)

Pin Number	Pin Name	Current Consumption
7	VDDA (Analog VDD)	15.57mA
27	VDDD (Digital VDD)	4.18mA
30	VDDD (Digital VDD)	9.1mA
Total Current Consumption		**28.85mA**

NOTE: Current measurements were made when the XRT71D00 device was operating in the STS-1 Mode, and powered at 3.35V.

For inductors L2 and L3, the user should select as large a value as the selected size (0805, 1210 or 1812 etc.) will allow while keeping the DC resistance of each inductor to less than 2 ohms. The goal is to keep the power supply voltage (at the VDD pins of the XRT73L00 and the XRT71D00 devices) above 3.135 volts.

An example of an acceptable inductor would be the 1210-682J or the S1210-682K (each of size 1210) from API-Delevan. The 1210-682J inductor is spec'd to have a maximum dc resistance of 1.8 ohms. Additionally, the 1210-682J inductor has a maximum current rating of 321mA. The S1210-682K inductor is spec'd to have a maximum dc resistance of 1.5ohms. Further, the S1210-682K has a maximum current rating of 372mA.

THE ZENER DIODE

It is strongly recommended that a 3.6V 400mW Zener Diode be connected from the +3.3V supply to Power GND to suppress power supply transient in case of excessive charge injection into the Ground Plane. These transients can occur while connecting the remote terminal or test equipment to the board via coaxial cable. Such transients can expose integrated circuit devices to momentary "reverse' polarity or excessive (7V to 10V) power supply voltages. Most regulators are too slow to respond to such transient conditions.

NOTE: This zener diode is also useful for suppressing peak overshoots and ringing (in the power supply line) following a rapid ramp in the power supply voltage, due to events such as "hot-swapping", etc.

An example of an acceptable 3.6V zener diode would be the 1N5914, which is available from various suppliers.

Designing the XRT71D00 and the XRT73L00 Devices to operate in the Host Mode, and to be accessed via a single Chip Select pin.

Preliminary

October 19, 2001

Revision 1.05

DECOUPLING CAPACITORS

We strongly recommend that the user provide de-coupling capacitors for each VDD pin of the XRT73L00 device (Analog as well as Digital). The placement and routing of these decoupling capacitors must be such to minimize the trace length (and in-turn, inductance) between the capacitor and the corresponding VDD pin, and the capacitor and the corresponding via (which connects to the GND plane).

MISCELLANEOUS NOTES

The component values shown for capacitors and inductors are to be used as guidelines only. Use the following guidelines for selecting components.

For decoupling capacitors use X7R for ceramic non-polar capacitors, solid tantalum for polar capacitors. Avoid Z5U and electrolytic capacitors.

6.0 THE BNC CONNECTOR SHIELDS

As a general rule, we highly recommend that the customer either AC or DC couple the BNC connector shield to Frame or Chassis Ground. In the schematic design, we recommend that the customer AC couple the BNC connectors (on both the Transmit and Receive Sides) to Frame GND. Further, we also recommend that the customer also design in a Jumper, which permits installation personnel to DC couple the BNC connector shield to Frame GND, when set.

Component selection for the for the Capacitor (used to AC couple the BNC Connector Shield to GND)
The characteristics of a capacitor, to be used in this role are as follows.

- This capacitor must be rated for high voltages.
- This capacitor must impose minimum AC impedance to Frame GND.

Therefore, the optimum choice for such a capacitor would be a capacitor that has a very high voltage rating and very large capacitance. The best capacitor that we could find that has both of these characteristics is a 1000pF capacitor that has a working voltage of 2000V.

SOME ACCEPTABLE CAPACITORS for AC Coupling the BNC Connector to Frame GND

Any of the following capacitors are suitable for this applicable. In all cases, these are Ceramic, X7R, 1000pF, 2kV, 10% capacitors which come in a 1812 case size.

Manufacturer	**Part Number**
AVX	1812GC102KA11A
AVX	1812GC102KAT2A
CALCHIP	CHV1812N2K0102KXT
JARO	CC1812XR102JN202ER
JARO	CC1812XR102KN202ER
MURATA	GRM43-2X7R102K2KVAL
JOHANSON	202S43W102KV4E

APPENDIX A – REGISTER DESCRIPTION FOR THE XRT73L00 DS3/E3/STS-1 LIU IC

The Bit Format of the Command Registers, within the XRT73L00 device is presented below in Figure A1.

			Register Bit-Format				
Address	**Command Register**	**Type**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	RO	RLOL	RLOS	ALOS	DLOS	DMO
0x01	CR1	R/W	TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
0x02	CR2	R/W	Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
0x03	CR3	R/W	RNRZ	LOSMUT	RCLK2/ LCV*	RCLK2INV	RCLK1INV
0x04	CR4	R/W	Reserved	STS-1/ DS3*	E3	LLB	RLB
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x08	CR8	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Figure A1, The Bit Format of the Command Registers, within the XRT73L00 Device.

A brief description/definition of each of these bit-fields are presented below.

Command Register CR0

Bit D0 – DMO (Drive Monitor Output)
This "Read-Only" Bit indicates whether or not the "Transmit Drive Monitor" is currently detecting a "Transmit Line Fault" condition or not. If the user has connected the MTIP and MRING input pins (of the LIU IC) the TTIP and TRING line (as shown in Figure A2), then this bit-field will toggle and remain "high" anytime the Transmit Drive Monitor (via the MTIP and MRING input pins) has detected an absence of bipolar pulses for 128 consecutive bit periods. This bit-field will be reset to "0" the instant that the Transmit Drive Monitor detects a bipolar pulse via the TTIP/TRING outputs.

NOTE: This Register bit is only valid if the user has tied the MTIP and MRING input pins to the TTIP and TRING line, as shown below in Figure A2.

Designing the XRT71D00 and the XRT73L00 Devices to operate in the Host Mode, and to be accessed via a single Chip Select pin.

Preliminary

October 19, 2001

Revision 1.05

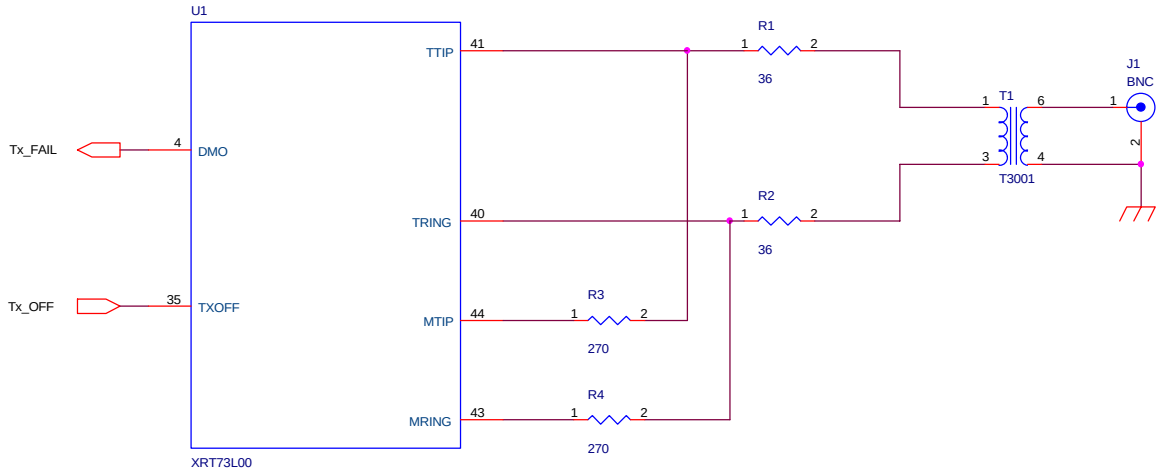


Figure A2, Illustration of the Required Connection, between the MTIP/MRING and TTIP/TRING pins, in order to permit "Transmit Drive Monitoring" via the DMO Bit-field.

Bit D1 – DLOS (Digital Loss of Signal)
This "Read-Only" bit-field indicates whether or not the Digital LOS Detector is currently declaring an LOS condition.

If this bit-field is set to "1" then the "Digital LOS Detector" is currently declaring an LOS condition. Conversely, if this bit-field is set to "0", then the Digital LOS Detector is NOT currently declaring an LOS condition.

Bit D2 – ALOS (Analog Loss of Signal)
This "Read-Only" bit-field indicates whether or not the Analog LOS Detector is currently declaring an LOS condition.

If this bit-field is set to "1" then the "Analog LOS Detector" is currently declaring an LOS condition. Conversely, if this bit-field is set to "0", then the Analog LOS Detector is NOT currently declaring an LOS condition.

Bit D3 – RLOS (Receive Loss of Signal)
This "Read-Only" bit-field indicates whether or not the XRT73L00 device is currently declaring an LOS condition.

NOTES:

1. For DS3 and STS-1 applications, the state of the "RLOS" bit-field is simply the "wired-OR" of both the "DLOS" and "ALOS" bit-fields.
2. For E3 applications, a special "ITU-T G.775 LOS Detector" is used to declare and clear LOS.

If this bit-field is set to "1" then the LIU device is currently declaring an LOS condition. Conversely, if this bit-field is set to "0", then the Analog LOS Detector is NOT currently declaring an LOS condition.

Bit D4 – RLOL (Receive Loss of Lock)
This "Read-Only" bit-field indicates whether or not the Clock Recovery PLL (within the Receive Section of the LIU IC) is declaring a "Loss of Lock" condition or not. If the Clock Recovery PLL is currently declaring a "Loss of Lock" condition, then it will set this bit-field to "1". Conversely, if the Clock Recovery PLL is currently NOT declaring a "Loss of Lock" condition, then it will set this bit-field to "0".

The Clock Recovery PLL will declare a Loss of Lock condition whenever the frequency of the Recovered Clock deviates from that of the EXCLK by 0.5% (5000ppm) or more.

NOTES:

1. Whenever the Clock Recovery PLL is declaring a Loss of Lock, then the Clock Recovery PLL will cease using the "receive line signal" in order to derive and synthesize the "RCLK" signal, The Clock Recovery PLL will, instead, use the EXCLK clock signal as the timing source, when generating the Recovered Clock signal (RCLK).
2. If the user is interested in monitoring a signal that truly indicates when the Receive Line signal is truly non-discernable, then the RLOL bit-field or output pin is the signal of choice.

Command Register CR1

Bit D0 – TXBIN (Transmitter - Single Rail Enable/Disable)
This "Read/Write" bit-field permits the user to configure the Transmit Section of the LIU IC to operate in either the Single-Rail or Dual-Rail Mode.

If the Transmit Section is configured to operate in the "Single-Rail" Mode, then it will only accept and latch data that is applied to the LIU IC via the "TPDATA" input pin. Data, which is applied to the "TNDATA", input pin is ignored.

If the Transmit Section is configured to operate in the "Dual-Rail" Mode, then it will accept and latch data that is applied to the LIU IC via both the "TPDATA" and "TNDATA" input pins. In this case the state of the "TNDATA" input pin will NOT be ignored.

NOTE:
If the user configures the Transmit Section of the LIU to operate in the "Single-Rail" Mode, then is imperative that the user to enable both the B3ZS/HDB3 Encoder and Decoder blocks by setting the "ENDECDIS" bit-field to "0".

Bit D1 – TXLEV (Transmit Line Build-Out Enable/Disable)
This "Read/Write" bit-field permits the user to enable or disable the "Transmit Line Build-Out" circuit within the Transmit Section of the LIU IC.

The "Transmit Line Build-Out" circuit should be enabled if the cable length between the Line Card (containing the XRT73L00 device) and the DSX-3/STSX-1 location is less than 225 feet.

Conversely, the "Transmit Line Build-Out" circuit should be disabled if the cable length between the Line Card (containing the XRT73L00 device) and the DSX-3/STSX-1 location is greater than 225 feet.

Setting this bit-field to "0" enables the "Transmit Line Build-Out" circuit. Conversely, setting this bit-field to "1" disables the "Transmit Line Build-Out" circuit.

NOTE: This bit-field is ignored if the XRT73L00 device has been configured to operate in the E3 Mode.

Bit D2 – TXCLKINV (Transmit Clock Invert)
This "Read/Write" bit-field permits the user to configure the Transmit Section of the LIU IC to latch the contents of the "TPDATA/TNDATA" input pin upon either the rising or falling edge of TXCLK.

Setting this bit-field to "0" configures the Transmit Section to latch the TPDATA/TNDATA signal upon the falling edge of TXCLK. Conversely, setting this bit-field to "1" configures the Transmit Section to latch the TPDATA/TNDATA signal upon the rising edge of TXCLK.

Bit D3 – TAOS (Transmit All Ones)
This "Read/Write" bit-field permits the user to configure the Transmit Section of the LIU IC to transmit an "All Ones" pattern onto the line.

Setting this bit-field to "1" configures the Transmit Section to transmit an "All Ones" pattern onto the line. Setting this bit-field to "0" configures the Transmit Section to transmit data based that which is sampled via the TPDATA/TNDATA input pins.

Bit D4 – TXOFF (Transmit Shut OFF)
This "Read-Write" bit-field permits the user to turn on or turn-off the Transmit Output Driver of the XRT73L00 device.

When the user turns on the Transmit Output Driver of the XRT73L00, then the LIU will generate and output a bipolar line signal (via the TTIP and TRING output pins), based upon the data that it samples on the TPDATA/TNDATA input pin via the TCLK clock signal. When the user turn off the Transmit Output Driver of the XRT73L00, then no bipolar line signal will be output onto the line. Further, the TTIP and TRING output pins will be "tri-stated".

NOTE: In contrast to most of the other hardware-mode external input pins, the state of the "TxOFF" input pin is NOT ignored, whenever the XRT73L00 device is configured to operate in the "HOST" Mode. Therefore, if the user wishes to control the "ON/OFF" of the Transmit Output Driver, via the Microprocessor Serial Input; he/she must ensure that the "TxOFF" input pin is tied to "GND".

Command Register CR2

Bit D0 – REQDIS (Receive Equalizer Enable/Disable)
This "Read/Write" bit-field permits the user to enable or disable the Receive Equalizer within the XRT73L00 device.

Setting this bit-field to "0" enables the Receive Equalizer within the Receive Section of the XRT73L00 device. Conversely, setting this bit-field to "1" disables the Receive Equalizer.

NOTE: For most DS3, E3 and STS-1 applications, the user is advised to enable the Receive Equalizer for all mandated cable lengths.

Bit D1 – DLOSDIS (Digital LOS Detector Disable)
This "Read/Write" bit-field permits the user to enable or disable the "Digital LOS" Detector, within the LIU IC.

Setting this bit-field to "0" enables the "Digital LOS" Detector. Conversely, setting this bit-field to "1" disables the "Digital LOS" Detector.

NOTE: This bit-field is ignored if the XRT73L00 device has been configured to operate in the "E3" Mode.

Bit D2 – ALOSDIS (Analog LOS Detector Disable)
This "Read/Write" bit-field permits the user to enable or disable the "Analog LOS" Detector, within the LIU IC.

Setting this bit-field to "0" enables the "Analog LOS" Detector. Conversely, setting this bit-field to "1" disables the "Analog LOS" Detector.

Bit D3 – ENDECDIS (B3ZS/HDB3 Encoder & Decoder Block Enable/Disable)
This "Read/Write" bit-field permits the user to enable or disable both the B3ZS/HDB3 Encoder and Decoder blocks within the XRT73L00 LIU IC.

Setting this bit-field to "0" enables both the B3ZS/HDB3 Encoder and Decoder blocks within the LIU IC. Conversely, setting this bit-field to "1" disables both the B3ZS/HDB3 Encoder and Decoder blocks.

Command Register CR3

Bit D0 – RCLK1INV (RCLK1 Invert)
This "Read/Write" bit-field permits the user to configure the Receive Section of the LIU to update the "output" data (via the RPOS and RNEG output pins) upon the rising or falling edge of the RCLK1 signal.

Setting this bit-field to "0" configures the LIU to update the "RPOS" and "RNEG" output pins, upon the rising edge of the RCLK1 signal. Conversely, setting this bit-field to "1" configures the LIU to update the "RPOS" and "RNEG" output pins upon the falling edge of the RCLK1 signal.

Bit D1 – RCLK2 INV (RCLK2 Invert)
This "Read/Write" bit-field permits the user to configure the Receive Section of the LIU to update the "output" data (via the RPOS and RNEG output pins) upon the rising or falling edge of the RCLK2 signal.

Setting this bit-field to "0" configures the LIU to update the "RPOS" and "RNEG" output pins, upon the rising edge of the RCLK2 signal. Conversely, setting this bit-field to "1" configures the LIU to operate the "RPOS" and "RNEG" output pins upon the falling edge of the RCLK2 signal.

NOTE: This bit-field is ignored if the "RCLK2/LCV" output pin has been configured to function as the "LCV" (Line Code Violation) output pin.

Bit D2 – RCLK2/LCV (RCLK2 or LCV Output Select)
This "Read/Write" bit-field permits the user to configure the "RCLK2/LCV" output pin to function as either the "RCLK2" or the "LCV" output pin.

Setting this bit-field to "1" configures this pin to function as the "RCLK2" output pin. Conversely, setting this bit-field to "0" configures this pin to function as the "LCV" output pin.

NOTES:

1. If the "RCLK2/LCV" output pin is configured to function as the "LCV" output pin, then the "D1" (RCLK2) bit-field is ignored.
2. If the "RCLK2/LCV" output pin is configured to function as the "LCV" output pin, then the LCV output pin will be updated on either the rising or falling edge of "RCLK1" (depending upon the state of the "D0" [RCLK1] bit-field).

Bit D3 – LOSMUT (MUTING upon LOS Enable/Disable)
This "Read/Write" bit-field permits the user to enable or disable the "MUTing-upon-LOS" feature within the XRT73L00 device. When this feature is enabled, then the XRT73L00 device will automatically pull the "RPOS" and "RNEG" output pins to GND, anytime the LIU declares an LOS condition.

Setting this bit-field to "1" enables the "MUTing-upon-LOS" feature. Conversely, setting this bit-field to "0" disables the "MUTing-upon-LOS" feature.

Bit D4 – RNRZ (Receiver – Single Rail Mode Enable/Disable)
This "Read/Write" bit-field permits the user to configure the Receive Section of the LIU to operate in either the Single-Rail or Dual-Rail Mode.

If the Receive Section is configured to operate in the "Single-Rail" Mode, then it will output all recovered data via the "RPOS" output pin. The "RNEG" output pin will be inactive.

If the Receive Section is configured to operate in the "Dual-Rail" Mode, then it will output the recovered data via both the "RPOS" and "RNEG" output pins.

Command Register CR4

Bit D0 – RLB (Loop-back Select)
This "Read/Write" bit-field, along with "D1" (LLB) permits the user to configure the XRT73L00 device to operate in either the "Analog-Local", "Digital-Local" or "Remote" Loop-back Modes.

The following table presents the relationship between the states of these two bit-fields and the corresponding loop-back mode of the XRT73L00 device.

Table A1, The Relationship between the states of bits D0 (RLB), D1 (LLB) and the corresponding Loop-back Modes of the XRT73L00 Device

D0 (RLB)	D1 (LLB)	Resulting Loop-back Mode
0	0	No Loop-back Mode (Normal Operation)
0	1	Analog Local Loop-back Mode
1	0	Remote Loop-back Mode
1	1	Digital Local Loop-back Mode

Bit D1 – LLB (Loop-back Select)
This "Read/Write" bit-field, along with "D0" (RLB) permits the user to configure the XRT73L00 device to operate in either the "Analog-Local", "Digital-Local" or "Remote" Loop-back Modes.

The following table presents the relationship between the states of these two bit-fields and the corresponding loop-back mode of the XRT73L00 device.

Table A2, The Relationship between the states of bits D0 (RLB), D1 (LLB) and the corresponding Loop-back Modes of the XRT73L00 Device

D0 (RLB)	D1 (LLB)	Resulting Loop-back Mode
0	0	No Loop-back Mode (Normal Operation)
0	1	Analog Local Loop-back Mode
1	0	Remote Loop-back Mode
1	1	Digital Local Loop-back Mode

Bit D2 – E3 (E3 Mode Select)
This "Read/Write" bit-field, along with bit D3 (STS-1/DS3*) permits the user to configure the XRT73L00 device to operate in either the DS3, E3 or STS-1 Mode.

Setting this bit-field to "1" configures the XRT73L00 device to operate in the "E3" Mode.

NOTE: In this setting, the state of the "D3" (STS-1/DS3*) bit-field will be ignored.

Setting this bit-field to "0" configures the XRT73L00 device to operate in either the "DS3" or the "STS-1" Modes. In this setting the state of the "D3" (STS-1/DS3*) bit-field will dictate whether the chip is operating in the DS3 or STS-1 Mode.

Bit D3 – STS-1/DS3* (STS-1 or DS3 Mode Select)
This "Read/Write" bit-field, along with bit D2 (E3) permits the user to configure the XRT73L00 device to operate in either the DS3, E3 or STS-1 Mode.

Setting this bit-field to "1" configures the XRT73L00 device to operate in the STS-1 Mode. Conversely, setting this bit-field to "0" configures the XRT73L00 device to operate in the "DS3" Mode.

NOTE: The state of this bit-field is ignored if bit D2 (E3) is set to "1".

APPENDIX B – REGISTER DESCRIPTION FOR THE XRT71D00 DS3/E3/STS-1 JITTER ATTENUATOR IC

The Command Register Format for the XRT71D00 device is presented below in Figure B1.

			Register Bit-Format						
Addr.	**Command Register**	**Type**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
			Channel 0 Registers						
0x06	CR6	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES	FSS
0x07	CR7	R/O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FL
			Channel 1 Registers						
0x0E	CR14	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES	FSS
0x0F	CR15	R/O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FL
			Channel 2 Registers						
0x16	CR22	R/W	STS-1	0	E3/DS3*	DJA	BWS	CLKES	FSS
0x17	CR23	R/O	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FL

Figure B1, The Bit Format of the Command Registers, within the XRT71D00 Device.

A brief description/definition of each of these bit-fields are presented below.

Command Register CR6 (CR14 or CR22)

Bit D0 – FSS (FIFO Size Select)
This "Read/Write" bit-field permits the user to configure the XRT71D00 device to operate with either a 16-bit or 32-bit FIFO depth.

Setting this bit-field to "0" configures the Jitter Attenuator IC to operate with a FIFO Depth of 16-bits. Conversely, setting this bit-field to "1" configures the Jitter Attenuator IC to operate with a FIFO Depth of 32-bits.

D1 – CLKES (Clock Edge Select)

This "Read/Write" bit-field permits the user to configure the following.

a. Which edge of RCLK that the XRT71D00 device will sample the data (applied at the "RPOS" and "RNEG" input pins).
b. Which edge of RRCLK that the XRT71D00 device will output the data (via the "RRPOS" and "RRNEG" output pins).

Setting this bit-field to "0" configures the XRT71D00 device to do the following.

a. To latch the state of the "RPOS/RNEG" input pins, upon the rising edge of the "RCLK" input signal.
b. To update the output data (via the "RRPOS/RRNEG" output pins) upon the falling edge of the "RRCLK" output signal

Conversely, setting this bit-field to "1" configures the XRT71D00 device to do the following.

a. To latch the state of the "RPOS/RNEG" input pins, upon the falling edge of the "RCLK" input signal.
b. To update the output data (via the "RRPOS/RRNEG" output pins) upon the rising edge of the "RRCLK" output signal.

D2 – BWS (Bandwidth Select)

This "Read/Write" bit-field permits the user to configure the Jitter Attenuator PLL to operate with either a "Narrow-" or "Wide-" band loop-filter. If the Jitter Attenuator PLL is configured to operate with a "Narrow-band" loop-filter, then the "Corner Frequency" (of the Jitter Transfer Characteristic curve) will occur at about 30Hz. If the Jitter Attenuator PLL is configured to operate with a "Wide-band" loop-filter, then the "Corner Frequency" (of the Jitter Transfer Characteristic curve) will occur at about 300Hz.

Setting this bit-field to "0" configures the Jitter Attenuator PLL to operate with a "Narrow-Band" loop-filter. Conversely, setting this bit-field to "1" configures the Jitter Attenuator PLL to operate with a "Wide-Band" loop-filter.

NOTE: This bit-field is ignored if the Jitter Attenuator PLL is disabled (e.g., if bit-field "D3" [DJA], within this Command Register is set to "1").

D3 – DJA (Disable Jitter Attenuator PLL)
This "Read/Write" bit-field permits the user to either enable or disable the "Jitter Attenuator" PLL within the XRT71D00 device. If the Jitter Attenuator PLL is enabled, then the Jitter Attenuator IC will attenuate the jitter within the "RCLK" input signal (in a manner as specified by the "BWS" bit-field). If the Jitter Attenuator PLL is disabled, then the Jitter Attenuator IC will NOT attenuate the jitter within the "RCLK" input signal. Whatever jitter, is present within the "RCLK" will also be present at the "RRCLK" output signal.

Setting this bit-field to "0" enables the Jitter Attenuator PLL. Conversely, setting this bit-field to "1" disables the Jitter Attenuator PLL.

D4 – E3/DS3* (Data Rate Select)
This "Read/Write" bit-field along with bit D6 (STS-1) permits the user to configure the XRT71D00 device to operate in either the DS3, E3 or STS-1 Mode.

Setting this bit-field to "1" configures the XRT71D00 device to operate in the E3 Mode. Conversely, setting this bit-field to "0" configures the XRT71D00 device to operate in the "DS3" Mode.

NOTE: The state of this bit-field is ignored if bit D6 (STS-1) is set to "1".

D5 – Set to "Zero"
The user must set this bit-field to "0" in order to insure proper operation of the XRT71D00 device.

D6 – STS-1 (Data Rate Select)
This "Read/Write" bit-field, along with bit D4 (E3/DS3*) permits the user to configure the XRT71D00 device to operate in either the DS3, E3 or STS-1 Mode.

Setting this bit-field to "1" configures the XRT71D00 device to operate in the "STS-1" Mode.

NOTE: In this setting, the state of the "D4" (E3/DS3*) bit-field will be ignored.

Setting this bit-field to "0" configures the XRT71D00 device to operate in either the "DS3" or "E3" Modes. In this setting the state of the "D4" (E3/DS3*) bit-field will dictate whether the chip is operating in the DS3 or E3 Mode.

Command Register CR7 (CR15 or CR23)

Bit D0 – FL

This "Read-Only" bit-field permits the user to determine if the XRT71D00 device is currently declaring a "FIFO Alarm" event. If the FIFO READ and WRITE pointers come within two bit-positions or each other, then the XRT71D00 device will declare a "FIFO Alarm" event. The purpose of this "FIFO Alarm" event is to alert the system that the FIFO (within the XRT71D00 device) is about to "Under-flow" or "Over-flow".

NOTES:

1. This bit-field (and the corresponding output pins) will only be set to "high" whenever the "FIFO READ" and "FIFO WRITE" pointers are CURRENTLY within two bit-positions of each other. This bit-field will be reset to "0" whenever the "FIFO READ" and "FIFO WRITE" pointers move to beyond two bit-positions of each other.
2. This bit-field can be used as an indication that the "Jitter Attenuator" PLL has lost "lock" with the "RCLK" input signal.

APPENDIX C – DESCRIPTION OF MICROPROCESSOR SERIAL INTERFACE PINS

C.0 THE MICROPROCESSOR SERIAL INTERFACE.

The Microprocessor Serial Interface of both the XRT71D00 and the XRT73L00 devices consists of the following pins.

- CS* - Chip Select Input pin
- SCLK – Serial Clock In
- SDI – Serial Data In
- SDO – Serial Data Out
- REG_RESET* or RST* - The Hardware Reset Input pin.

C.1 A BRIEF DESCRIPTION OF THE MICROPROCESSOR SERIAL INTERFACE PINS

A brief description of each of these pins is presented below.

CS* - Chip Select Input pin

The Microprocessor (or the entity responsible for reading data from and writing data to the Command Registers, within the XRT71D00 or the XRT73L00 devices) must assert this input pin (e.g., pull it "LOW") in order to enable communication with the XRT71D00 or the XRT73L00 device, via the Microprocessor Serial Interface.

NOTE: If this input pin is "HIGH", then all data being applied to the SDI input pin will be ignored.

SCLK – Serial Clock Input pin

The Microprocessor (or the entity responsible for reading data from and writing data into the Command Registers, within the XRT71D00 or the XRT73L00 devices) must apply a Clock Signal to this input pin. As the Microprocessor Serial Interface receives this clock signal, it will do the following.

a. It will latch the contents of the data, residing on the SDI input pin, upon the rising edge of this input signal.
b. It will update the contents of SDO output pin (during READ operations), upon the falling edge of this input signal.

SDI – Serial Data Input pin

The Microprocessor (or the entity responsible for reading data from and writing data into the Command Registers, within the XRT71D00 or the XRT73L00 devices) is expected to

apply Address and Data values to this input (in a serial manner) during READ and WRITE operations.

Data that is applied to this input pin will be latched (into the Microprocessor Serial Interface circuitry) upon the rising edge of the SCLK signal. A more definitive description on how to use this particular input pin is presented below.

SDO – Serial Data Output pin

This output pin serial outputs the contents of a specified Command Register, during READ operations. Data, which is output via this pin, is updated upon the falling edge of the SCLK input signal.

This output pin is tri-stated during all other times.

REG_RESET or RST* - Hardware Reset Input pins

This input pin permits the user to command a "Hardware RESET" to either the XRT73L00 or the XRT71D00 devices. In the case of the XRT73L00 and XRT71D00 device, each of the Command Registers will be reset to their default values. Each of these devices will also begin operating in a manner that corresponds with the "default" values of these Command Registers. Further, in the case of the XRT71D00 device, the contents of the FIFO (within the chip) will be flushed. Additionally, the FIFO_READ and FIFO_WRITE pointers, will be reset to their "default" positions.

C.2 USING THE MICROPROCESSOR SERIAL INTERFACE

The following instructions, for using the Microprocessor Serial Interface, are best understood by referring to the diagram in Figure C.1.

In order to use the Microprocessor Serial Interface the user must first provide a clock signal to the SCLK input pin. Afterwards, the user will initiate a "Read" or "Write" operation by asserting the "active-low" Chip Select input pin (CSB). It is important to assert the CSB pin (e.g., toggle it "low") at least 50ns prior to the very first rising edge of the clock signal.

Once the CSB input pin has been asserted the type of operation and the target register address must now be specified by the user. The user provides this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input. Note: each of these bits will be "clocked" into the SDI input, on the rising edge of SCLK. These eight bits are identified and described below.

Bit 1 - "R/W" (Read/Write) Bit

This bit will be clocked into the SDI input, on the first rising edge of SCLK (after CSB has been asserted). This bit indicates whether the current operation is a "Read" or "Write" operation. A "1" in this bit specifies a "Read" operation; whereas, a "0" in this bit specifies a "Write" operation.

Bits 2 through 5: The four (4) bit Address Values (labeled A0, A1, A2 and A3)

The next four rising edges of the SCLK signal will clock in the 4-bit address value for this particular Read (or Write) operation. The address selects the Command Register, within the XRT7300 or XRT71D00 device that the user will either be reading data from, or writing data to. The user must supply the address bits to the SDI input pin, in ascending order with the LSB (least significant bit) first.

Bits 6 and 7:
The next two bits, A4 and A5 must be set to "0", as shown in Figure 23.

Bit 8 - A6
The value of "A6" is a "don't care".

Once these first 8 bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a "Read" or "Write" operation.

Read Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Read" operation will proceed through an idle period, lasting three SCLK periods. On the falling edge of SCLK Cycle #8 (see Figure C.1) the serial data output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed Command Register (at Address [A3, A2, A1, A0]) via the SDO output pin. The Microprocessor Serial Interface will output this five-bit data word (D0 through D4) in ascending order (with the LSB first), on the falling edges of the SCLK pin. As a consequence, the data (on the SDO output pin) will be sufficiently stable for reading (by the Microprocessor), on the very next rising edge of the SCLK pin.

Write Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Write" operation will proceed through an idle period, lasting three SCLK periods. Prior to the rising edge of SCLK Cycle # 9 (see Figure C.1) the user must begin to apply the eight-bit data word, that he/she wishes to write to the Microprocessor Serial Interface, onto the SDI input pin. The Microprocessor Serial Interface will latch the value on the SDI input pin, on the rising edge of SCLK. The user must apply this word (D0 through D7) serially, in ascending order with the LSB first.

Designing the XRT71D00 and the XRT73L00 Devices to operate in the Host Mode, and to be accessed via a single Chip Select pin.

Preliminary

October 19, 2001

Revision 1.05

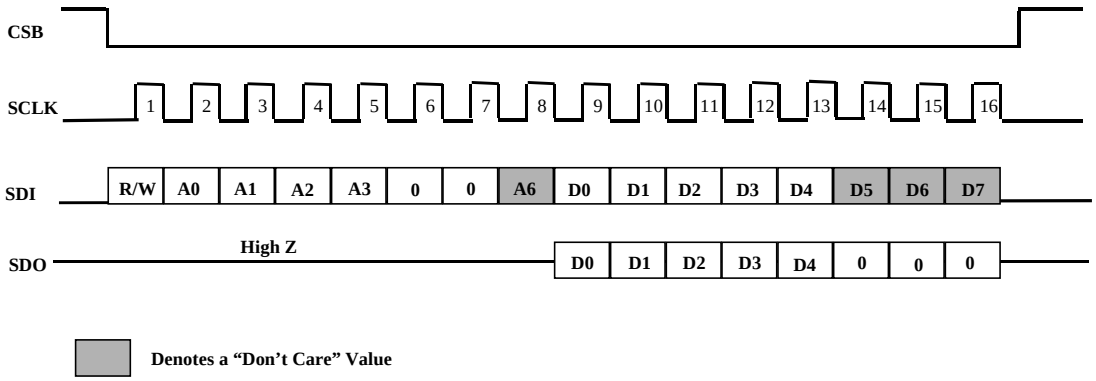


Figure C.1 – Illustration on How to Use the Microprocessor Serial Interface of the XRT71D00 and the XRT73L00 devices

APPENDIX D - CONTACT INFORMATION FOR API-DELEVAN:

Corporate Office
API Delevan
270 Quaker Road
East Aurora, NY 14052
Phone: 716-652-3600
FAX: 716-652-4814

email: apisales@delevan.com

website: www.delevan.com

APPENDIX E – REVISION CHANGE HISTORY

CHANGES FROM REVISION 1.04 TO 1.05

Corrected incorrect references to Figure C.1.

CHANGES FROM REVISION 1.03 TO 1.04

Corrected Figure 2 (on page 8) to reflect the fact that the "FL" bit-field is a READ-ONLY bit-field.
Corrected Figure B1 (on page 40) to reflect the fact that the "FL" bit-field is a READ-ONLY bit-field.

CHANGES FROM REVISION 1.02 TO 1.03

Corrected and added Figure Numbers in the text, where they were previously missing.

CHANGES FROM REVISION 1.01 TO 1.02

Corrected Schematic in Figure 4, in order to have the RxAVDD pins of the XRT73L00 LIU connect to the "RxAVDD" off-page connector of the schematic. Likewise, this schematic change also insured that the "TxAVDD pins of the XRT73L00 LIU connects to the "TxAVDD" off-page connector of the schematic.

CHANGES FROM REVISION 1.00 TO 1.01

1. Included a list of acceptable part numbers for capacitors that can be used to AC couple the BNC Connector shield to Frame GND (Section 6.0).