Clock Application Note

General Application Note for the
ST-49CXXX Clock Family

June 1997-3

INTRODUCTION

The ST49CXXX video/memory clock chips provide 5-130MHz clock outputs which may cause unwanted EMI problems.

To minimize problems with meeting FCC EMI requirements, consideration should be given to the following sections of the board design.

Power Supply Conditioning
Printed Circuit Board Layout
Video/Memory Clock Outputs And Drive Capabilities
External Clock Sources
Reference Clock Sources
Digital Control / Select Inputs
External Loop Filters

Power Supply Considerations

Under normal conditions no external components are required for propper operation of any of the internal circuitry of the ST49CXXX. It is required to have spike free (or minimum) and stable supply source to the chips. To provide stable and clean supply voltage to the clock chips we recommend to use 0.1μF capacitors close to IC's power supply lines (V_{CC}, AV_{CC} and DV_{CC} inputs). Analog and digital supply lines are separated from each other to reduce noise generated due to internal digital switching.

In most of the design cases 5V and 12V supplies are provided. A clean 5V supply can be obtained from the 12V supply by utilizing a 470Ω drop resistor and 5.1V zener diode bypassed by 0.047μF and 2.2μF Tantalum capacitors (or higher) to ground.

Trace width should be maximized from the supply source and good ground planes on top and bottom layers of the printed circuit board are recommended.

Printed Circuit Board (PCB) Layout

We recommend to place all external components as close as possible to the clock chips to reduce trace length between pin and component connections. It is important to keep components not related to clock ICs (DRAM and other memory devices) far and not share the grounds. In applications utilizing a multi-layer board, GND, AGND, and DGND should be directly connected to the ground plane. If possible A full power and ground plane layout should be employed both under and around the IC package.

Video/Memory Clock Outputs And Drive Capabilities

Video clock is usually the highest frequency present in video graphics system board/card and consideration should be given to FCC EMI requirements.

The trace connecting DCLK and MCLK clock output pins to other components should be kept as close as possible (with optional 33 resistor in series) to reduce the possible emitting signals and jitter.

External Clock Sources

When an external clock source is used to bypass the internal VCO to DCLK and MCLK outputs, clock should have fast rise/fall times and minimum jitter. This signal will be connected internally to the clock output pin when it is selected/enabled. The internal VCO circuit will be locked to its internal selected frequency.

Reference Clock Sources

The internal oscillator circuit contains all of the passive components required for the external crystal. An appropriate parallel resonant crystal should be connected between XTAL1 and XTAL2.

The crystal leads and input pins should be maintained as close as possible, and the body of the crystal should be grounded to minimize the noise pickup. For IBM compatible applications, the 14.31818MHz system or crystal clock is used as a reference clock to the chip.

Digital Control/Select Inputs

The ST49CXXX provides TTL compatible address select and latch input pins to interface with CMOS or TTL/LSTTL devices. The A0-A4 and M0-M1 can also be connected to the data bus if required.

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

Notes