

INTRODUCTION TO CALLER ID

The Caller ID feature is an on-hook capability that provides the user information about the caller before actually answering the call. The information displayed is a data message sent from the central office to the CPE using simplex VDI-1 (Voice Band Digital Interface) during the silent interval and after the first 20Hz ringing burst. The data contains the date (month and day), time (hour and minutes), and calling party number information in one of three forms:

- a) 2 to 10 digit extension
- b) privacy indication for those calling parties which do not want their number displayed
- c) out-of-area indication if the calling number can not be recovered for an on-screen display

VDI-1 is specified in terms of three architectural layers (physical, datalink and presentation layers). The XR-2211 is primarily concerned with the physical layer interface requirements, which refers to the electrical and procedural characteristics that the CO uses to physically connect to the CPE. It is concerned solely with transmitting a stream of bits, without regards to meaning or structure. The data link layer provides the procedural characteristics that allow the CO to transfer complete units of information to the CPE and the presentation layer defines the general content and syntax needed to transmit recognizable information.

MESSAGE FORMAT

Caller ID information is sent to the CPE in the silent interval after the first ringing phase. The central office waits half a second after the ringing before starting transmission of the data, and completes the transmission half a second prior to the next ringing signal. FSK data is

sent to the CPE as a single or multiple message format (see *Figure 1* & *Figure 2*). All Caller ID messages are preceded by a 250msec channel seizure sequence (01010101 pattern). This signal is sent at the beginning of each message to alert the CPE of the coming information. This is then followed by a 150msec of ones (1200Hz), intended to aid in "conditioning" the receiver for data. The message begins with the message type in one byte sequence (see *Table 1*). After that, a message length or data word count value of 9 through 18 specifies the number of data words that are going to be transmitted following this word. This number does not include the check sum word which follows the last data word.

Caller ID information bits are grouped into 8-bit characters preceded by a start bit (logical 0) and followed by a stop bit (logical 1) (see *Figure 1*). Data words are sent as ASCII characters without parity. The first eight words of data contain date (month and day) and local time (hour and minutes) two characters each. Word 11 through 20 carries the calling party information. The calling party information can be a 2 to 10 digit number or an ASCII alpha character indicating "P" for privacy or "O" for out of area. The last byte is a check sum word which is used by the CPE to insure the integrity of the received data. The check sum word consists of 2's complement of the module 256 sum of all the words transmitted from the CO including the message type, message length and data words. The CPE then derives the sum and adds this to the check sum. Any result other than zero indicates that the information was not received correctly. (see *Table 1*)

Multiple data message formats include additional parameter information. Each parameter is a series of data words specifying parameter type, parameter length and parameter data as described in *Figure 2*.

Word #	Signification	Binary Contents 7 6 5 4 3 2 1 0	Description	Dec. Value	Hex Value	Mod. 256 in Hex
1	Msg. Type	0 0 0 0 0 1 0 0	CND ¹	04	04	04
2	Length	0 0 0 1 0 0 1 0	18	18	12	16
3	Month	0 0 1 1 0 0 0 0	0	48	30	46
4		0 0 1 1 0 1 0 0	4	52	34	7A
5	Day	0 0 1 1 0 0 1 0	2	50	32	AC
6		0 0 1 1 1 0 0 0	8	56	38	E4
7	Hour	0 0 1 1 0 0 0 1	1	49	31	15
8		0 0 1 1 0 0 1 1	3	51	33	48
9	Minutes	0 0 1 1 0 0 1 0	2	50	32	7A
10		0 0 1 1 0 0 0 0	0	48	30	AA
11	Calling Number	0 0 1 1 0 1 0 0	4	52	34	DE
12		0 0 1 1 0 0 0 0	0	48	30	OE
13		0 0 1 1 1 0 0 0	8	56	38	46
14		0 0 1 1 0 1 0 0	4	52	34	7A
15		0 0 1 1 0 0 1 1	3	51	33	AD
16		0 0 1 1 0 1 0 0	4	52	34	E1
17		0 0 1 1 0 1 1 0	6	54	36	17
18		0 0 1 1 0 1 0 0	4	52	34	4B
19		0 0 1 1 0 0 0 0	0	48	30	7B
20		0 0 1 1 0 0 0 0	0	48	30	AB
21	Checksum	0 1 0 1 0 1 0 1	Checksum ²	85	55	55

Notes

¹ CND = Calling Number Delivery

² Calculated Checksum + Received Checksum = 0 AB + 55 = 0 Mod 256

Table 1. Example of Caller Identification Coding

The demodulation of the FSK signals are done according to Bell 202A specifications which are:

Link Type:	Simplex
Modulation Scheme:	Phase Coherent Frequency Shift Keying
Logical 1 (Mark):	1200+/-12Hz
Logical 0 (Space):	2200+/-22Hz
Transmission rate:	1200 bits per second
Data:	Serial, Binary, Asynchronous
Transmission Level:	-13,5+/-1dBm into 900Ω

Table 2. Bell 202A Specifications

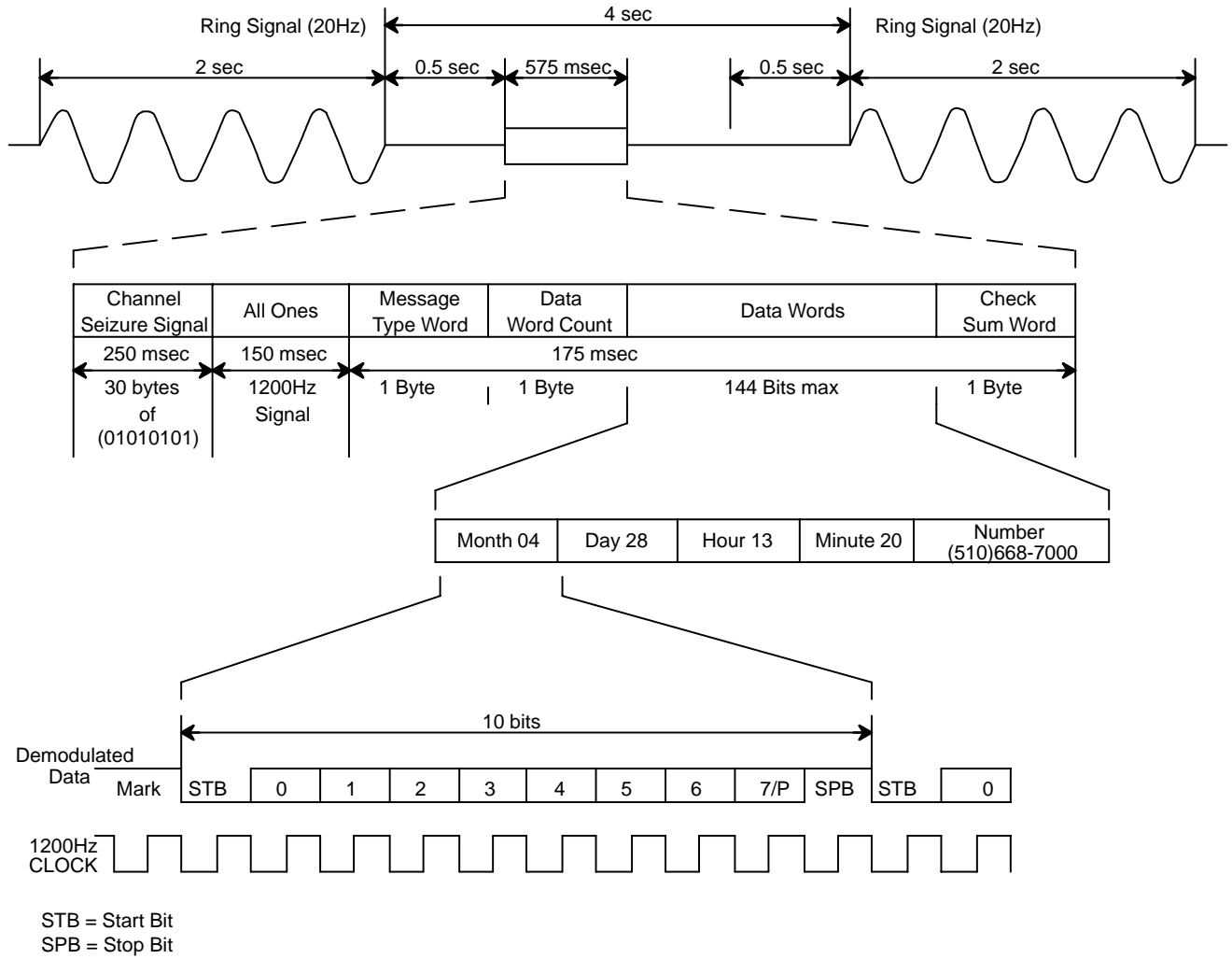


Figure 1. Single Data Message Format

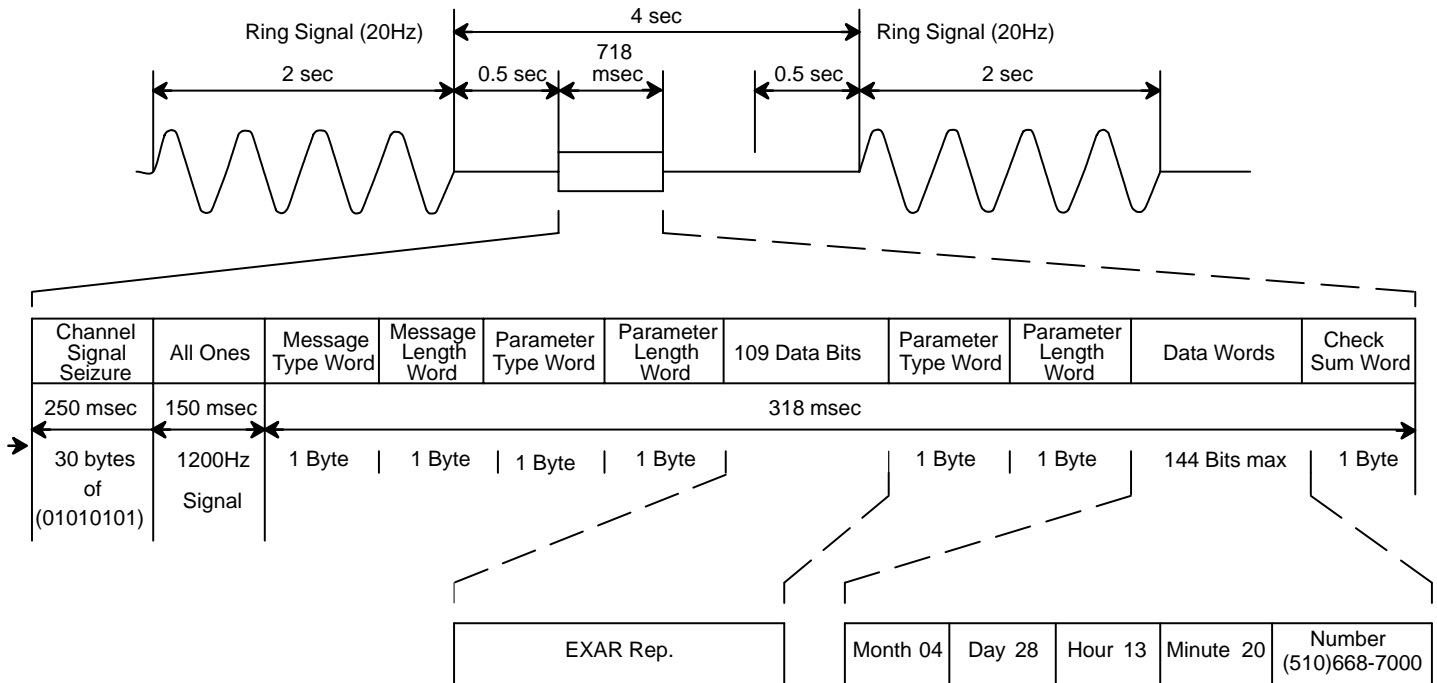


Figure 2. Multiple Data Message Format

DESIGN INSTRUCTIONS

The Caller ID demo board design described herein is a “how to” example on building the basic components required to interface to the telephone line and extract the CO (Central Office) supplied CID (Caller ID) information. The kit includes a set of schematics describing how to interface to the telephone line and extract the CID information. The kit also includes a small executable program that upon receiving the CO provided CID information, converts this information into a form that can be displayed onto a PC’s CRT. The program when used in conjunction with Bellcore TA-NWT-000030 specification is a useful reference when designing your own user interface. The schematics and software discussed herein were built, tested and proven to be functional. For BT specifications, see TAN-009.

EQUIPMENT REQUIRED

The equipment requirement for this user interface is a PC 386 or greater, having an RS-232 port. The executable

program provided with the demo board design runs under a DOS environment.

GENERAL OPERATION

The CID information provided by the CO to the CID demo board is, after being decoded by the demo board, routed directly into the PC via the RS-232 port. The PC is used to control whether or not power is applied to the demo board, as well as display the CID information.

While waiting for a CID signal most of the demo board is powered off. The first event in this sequence to occur is a Ring Indication. This initiates the second event which, by way of the software program powers-up most of the demo board, (this requires that the software program be running). The demo board is now ready to receive the FSK encoded data sent by the CO. Once the data is demodulated, the information is then sent from the demo board via a cable to the PC’s RS-232 port. The program first captures and then displays the data on the PC’s CRT.

After the CID information has been displayed, while still under software control, the demo board is then returned to the powered down state.

POWER SUPPLIES

The demo board design operates on a 6V supply. This supply is broken down into 3 separate sub-supplies, also 6V supplies. The Ring Indicator circuit is connected to one of these supplies. This supply is directly connected to 6V and is always connected.

The balance of the demo board (excluding the RS-232 interface, the MAXIM-235) is powered by a switched supply. The switched supply is activated by the Ring Indication. The MAXIM-235 is powered by the third supply. This scheme allows for easy measurement of the power consumed by each of the 3 blocks in both the powered-down and in the active modes. The total current consumed at the tip and ring inputs to the demo board must be less than 20mA in an off-hook condition, to prevent the CO from sending a dial tone. The on-hook condition must consume less than 5µA which is 1 ringer equivalent.

INPUT STAGE AND DAA

The first stage (see *Figure 4*) of the demo board design is the Input Stage. This stage includes the DAA function and the Ring Indicator detector. The DAA provides the required isolation between the demo board and telephone line while maintaining the ability to extract the data sent by the CO. The DAA optimally terminates the telephone line providing the proper Tip and Ring impedance.

The isolation provided by the DAA is required to prevent the full Ring Indicator voltage (max. 300V peak-to-peak on top of the max. 48V already provided by the CO battery), from damaging the low voltage components of the demo board. At the same time, the DAA must reject any voltage less than the minimum 26V ring voltage as a not valid ring signal. Non-flammable fuse resistors, 10Ω in value, are the first demo board components to come into contact with the phone line, providing a fuse protection in case of over voltage.

In preparing to send CID information, the CO first sends a Ring Signal, which puts the demo board on notice that it is about to receive CID information. The Ring Indicator is used to power up the powered down portions of the demo board.

The input stage also has a RC high pass filter which does not have any appreciable effect on the bandwidth of the filter stage. The demo board has an AC impedance as seen by the CO of more than 7,000Ω. The only DC input resistance is created by the leakage of the input capacitors, which results in less than 5µA, the 1 ringer equivalent specification. Too small of a DC input resistance can potentially result in spurious low frequency noise inadvertently powering up the demo board. The input stage acts in part as a DC blocking stage. Note that devices on the input stage must be able to withstand a maximum potential of 348V.

FILTER STAGE

The second stage (see *Figure 5*) of the demo board design is a filtering stage that consists of a band pass filter and an amplifier. The bandpass function is composed of a 2nd order Low Pass Active Butterworth filter and a 3rd order High Pass Active Butterworth filter. This results in an effective -3dB bandpass frequency range of 960 Hz to 2850 Hz, (see *Figure 8*). While an LM-324 was utilized as the gain element, it should be noted that almost any amplifier with a reasonably large gain (e.g. >10,000), relatively high input impedance and a moderately high bandwidth (e.g. >100,000 Hz) can be used. The Output Drive strength should also be large enough to drive the filter load impedance. The bandpass response and the gain achieved by the filter can be altered by the following equations. In addition, a gain versus frequency plot of the low pass filter and of the high pass filter are provided in *Figure 8*.

The computer program provided in Reference [2], Figure 27 was used to calculate order and component values of the Butterworth filters.

Order of the filter is calculated by:

$$N = INT \left(\text{Log} \frac{10^{(AMAX/10-1)}}{2((10^{0.3})-1)\text{Log}(Wn)} \right) + 1$$

AMAX: Attenuation at the stop band frequency.

Wn = F1 / F2 for low pass filter calculation and

Wn = FC / F1 for a high pass filter.

F1 = Stopband frequency.

FC = Cutoff Frequency

Depending on whether the values of N are even or odd, a different set of equations will be used. The program will

execute a “For...Next” instruction until all the RC values are calculated. Gain at the passband will be unity.

Reference [1], Chapter 8 gives the basic theory about active filters.

Reference [3], explains the basics of circuit theory.

The net result can be viewed as a bandpass filter with a 3 pole rolloff (60dB/decade) on the low frequency side and a 2 pole rolloff (40dB/decade) on the high frequency side. An additional requirement placed on the first and second stages is to filter out the 20Hz ring signal and the 60 or 50 Hz electric line noise. The demo board design achieves this by attenuating a 60Hz signal by at least 70dB. To assure good filter characteristics, 1% resistor and 5% capacitors should be used. If the input stage were to also be utilized for its high pass characteristics it too should have similarly controlled resistor and capacitor values.

GAIN STAGE

The third stage (see *Figure 5*) of the demo board design is a wide band amplifier. The gain is chosen such that with the worst case signal, 3.0mV rms (-48dBm), the PLL FSK decoder will still be working and the system will be able to extract the CID information. This stage also utilizes a LM-324 as the gain element. The controlling equations for the gain stage follow:

$$Gain = \frac{R_{fb}}{R_{in}}$$

R_{fb} : is the resistor connected from the output to the inverting input of the operational amplifier.

R_{in} : is the resistor from the signal source to the inverting input of the amplifier.

PLL, FSK DECODER

The fourth stage (see *Figure 6*) of the demo board design is the FSK Decoder and Carrier detect stage. This stage tracks the phone line signal that passes through the bandpass filter stage. This stage performs two tasks. First it simply detects if a frequency exists in a specific band. If so, the Energy Detect signal becomes active. Second it demodulates the 1200 baud FSK modulation of a frequency in the band from 1200Hz to 2200Hz. This demodulated data constitutes the CID information modulated by the CO. Note that Energy Detect must be valid before any CID information can be considered valid.

This stage utilizes the XR-2211 PLL to perform this function. The XR-2211 center VCO frequency should be adjusted by use of a potentiometer to a geometric mean frequency of 1625Hz to guarantee a 50% duty cycle at pin 7 of the XR-2211.

A note, while it was not done in this demo board design it may be possible to eliminate the amplifier in the filter stage and utilize the XR-2211 as the principal gain stage. This may require extracting more gain from the filter stages or running the risk of not having enough sensitivity to process low level, -48dBm, signals. Equations for PLL calculations follow:

$$C0 = \frac{1}{f0 * R0} \quad f0 = \frac{f1 + f2}{2}$$

$f1, f2$: are the mark and space frequencies.

$R0$: is the frequency control resistor connected at pin 12 of XR-2211.

$$R1 = \frac{f0 * R0 * 2}{f2 - f1}$$

$R1$: is the resistor connected from pin 12 to pin 11.

$$\zeta = \sqrt{\frac{1.25 * C0}{R1 * C1}}$$

ζ : is the Damping Factor. $R1$ in k Ω .

$$V_{REF} = \frac{V_{CC}}{2} - .650$$

V_{REF} : is the reference voltage at pin 10.

$$K0 = \left| \frac{2 * \pi}{V_{REF} * C0 * R1} \right|$$

$K0$: VCO Conversion Factor in Radians per second per volt.

$$Kd = \frac{V_{REF} * R1}{10 * \pi}$$

K_d: Phase Detector Gain in Volts per Radian. R1 in kΩ. For more information on choosing components for use with the XR-2211 in a FSK application, contact EXAR and request the XR-2211 Application Program and Application Note.

RS-232 ENCODER

The fifth stage of the demo board consists of a MAXIM-235. The 235 takes the decoded data provided by the XR-2211 and converts the voltage level provided by the XR-2211 to a level that is required by the RS-232 port of the PC.

To ensure proper operation, the RS-232 registers contained within the PC must be available in a timely

manner to be able to begin downloading the CID information stream.

Once the board detects a Ring signal the Carrier Detect signal becomes active and sends information to the PC through the RS-232 interface, then the PC program responds by turning on the unpowered part of the board, again using the RS-232 interface. Then the system is ready to process the information sent by CO.

After receiving the data the program will perform the checksum test. It will turn off the originally unpowered section of the demo board and will show on the screen the CID data or a message if the transmission was unsuccessful.

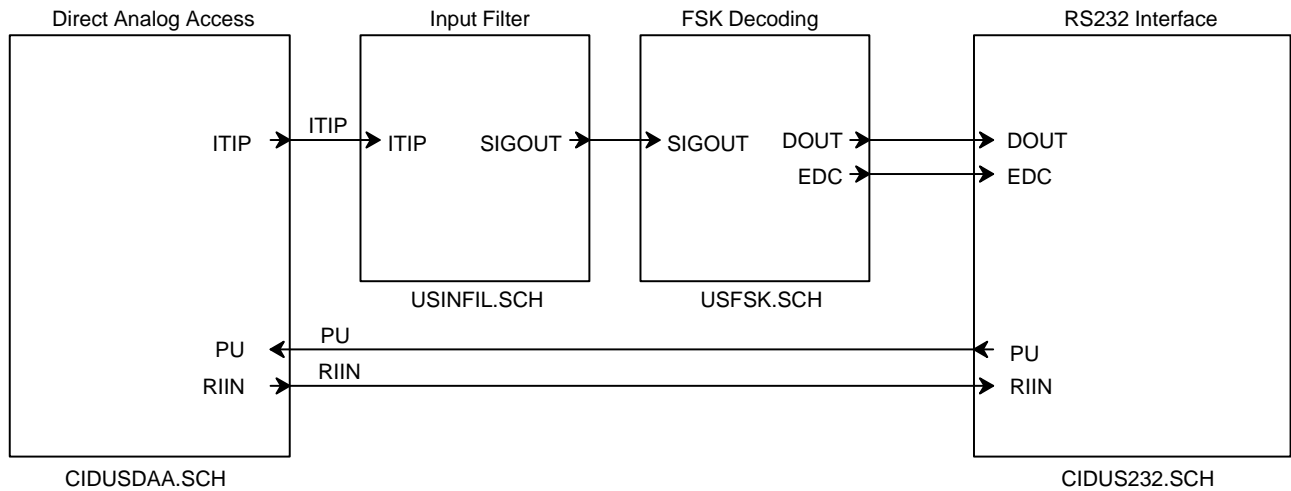


Figure 3. CID for the US Using XR-2211

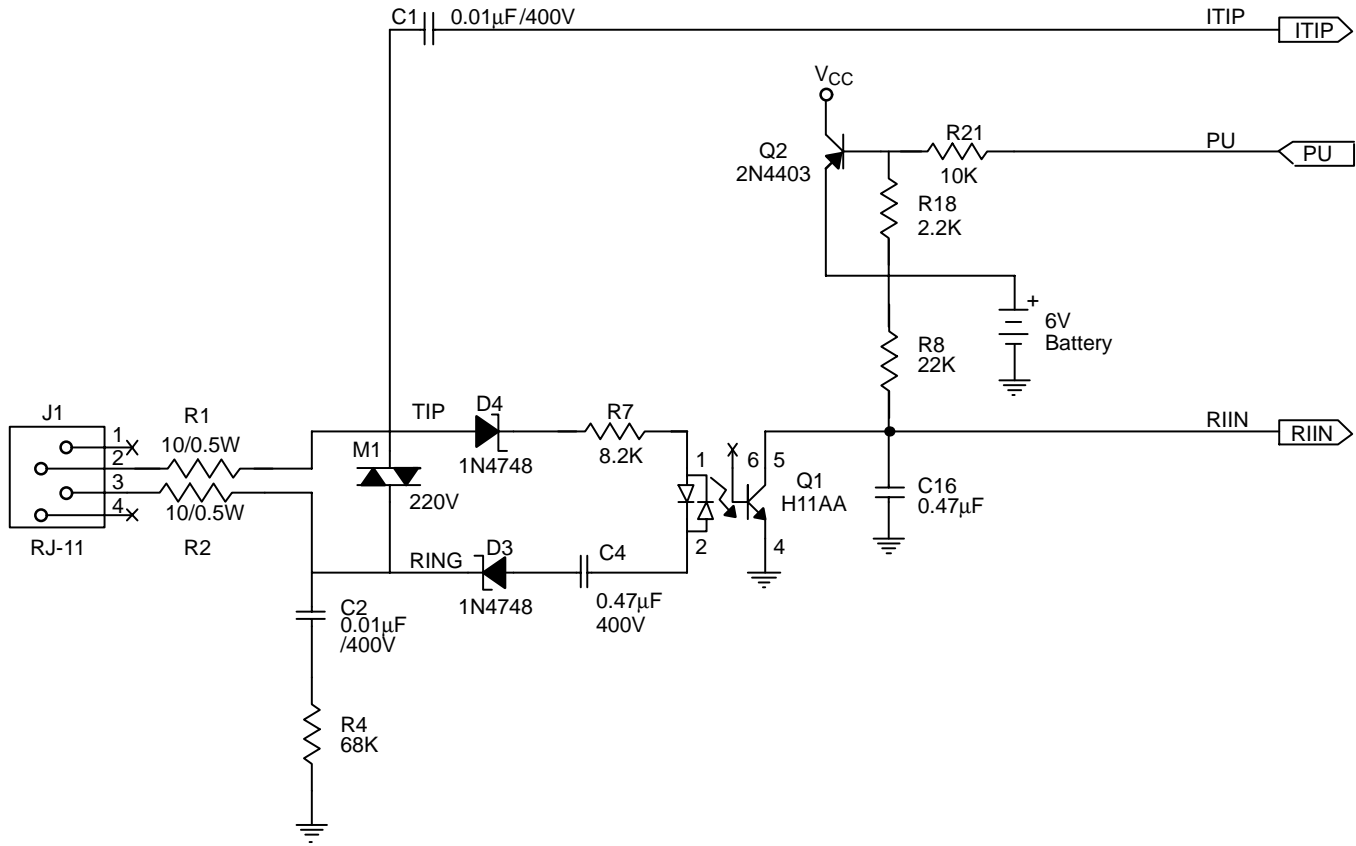


Figure 4. Direct Analog Access

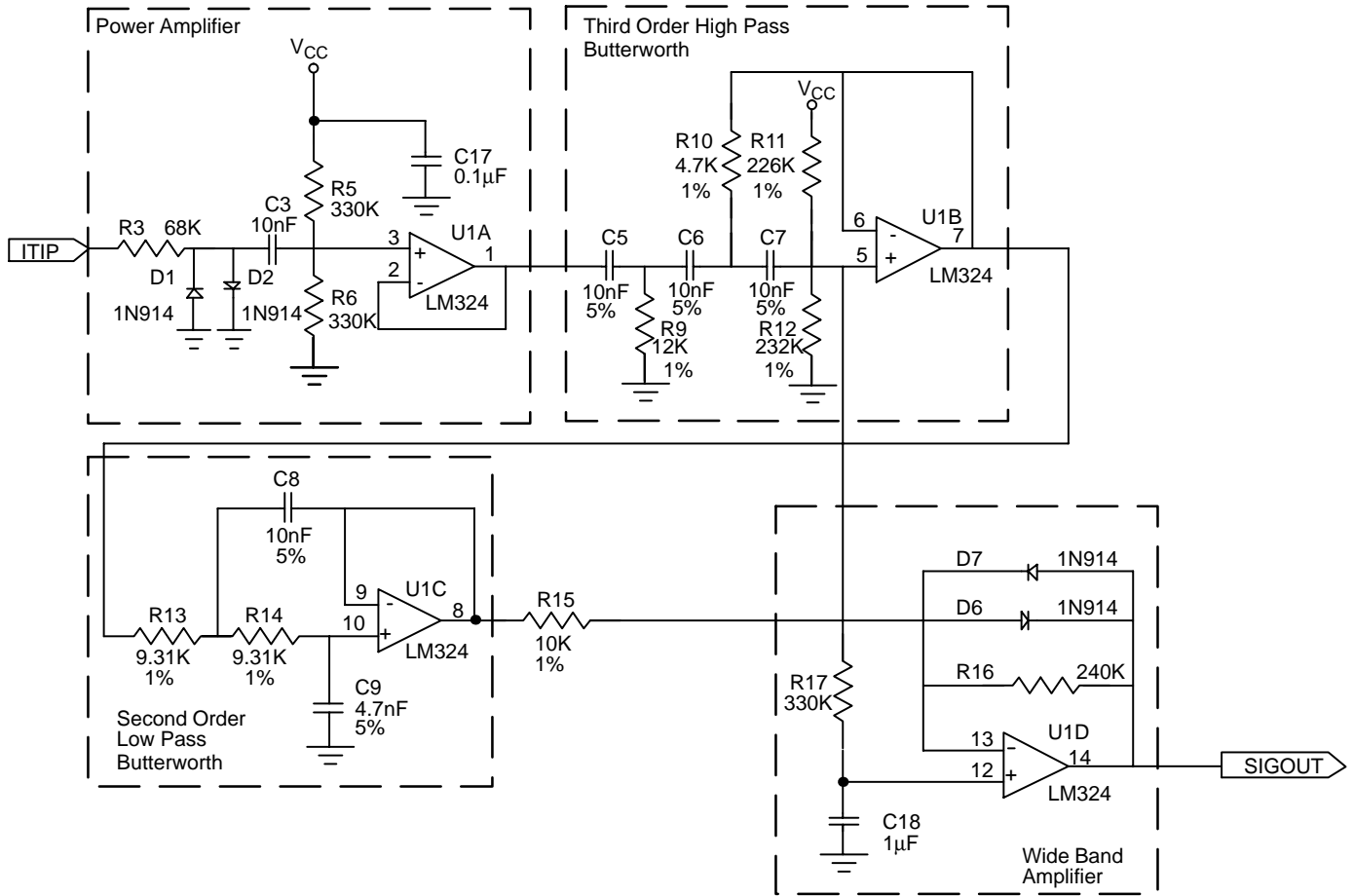


Figure 5. Input Filter for U.S. Implementation

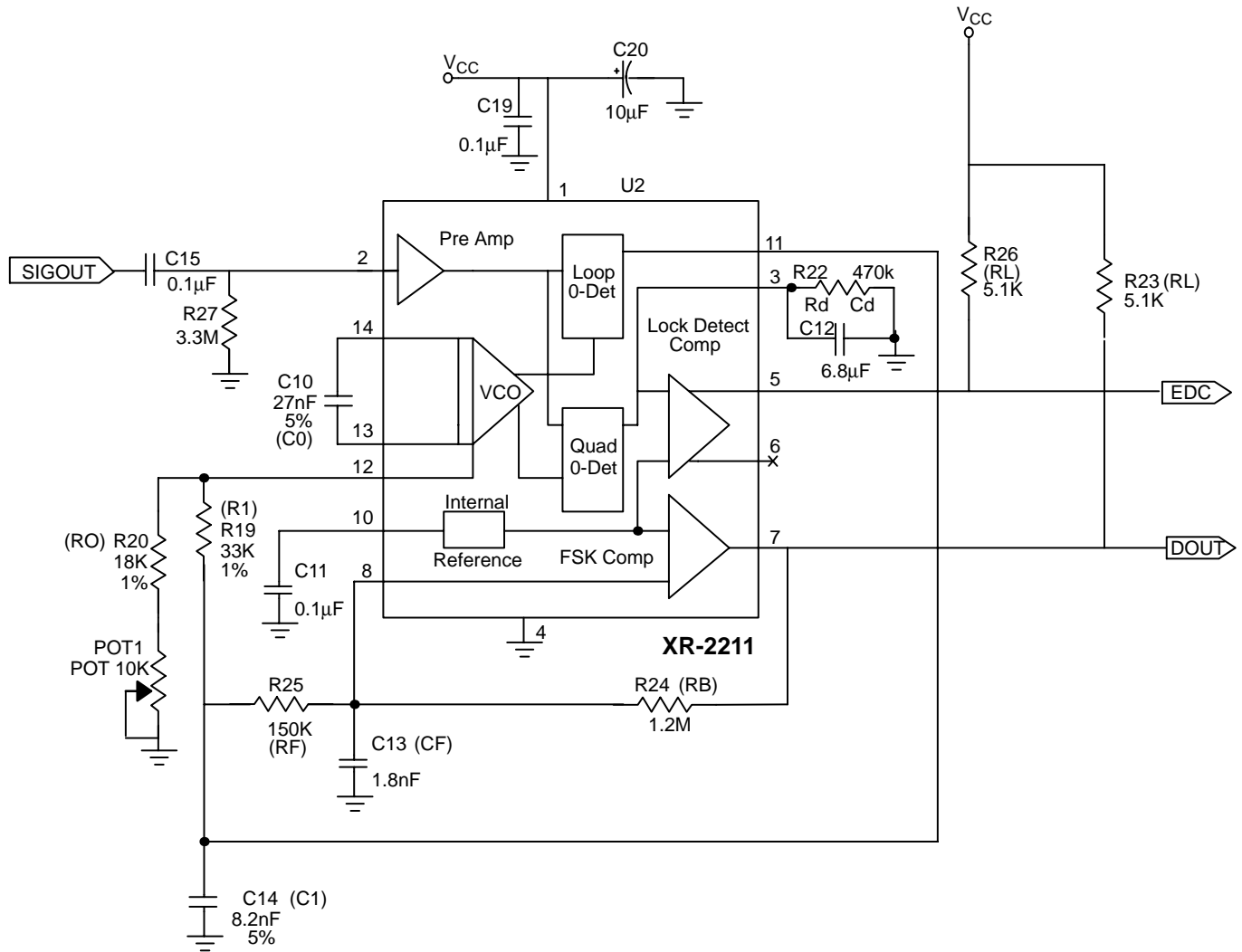


Figure 6. FSK Decoding U.S. Implementation

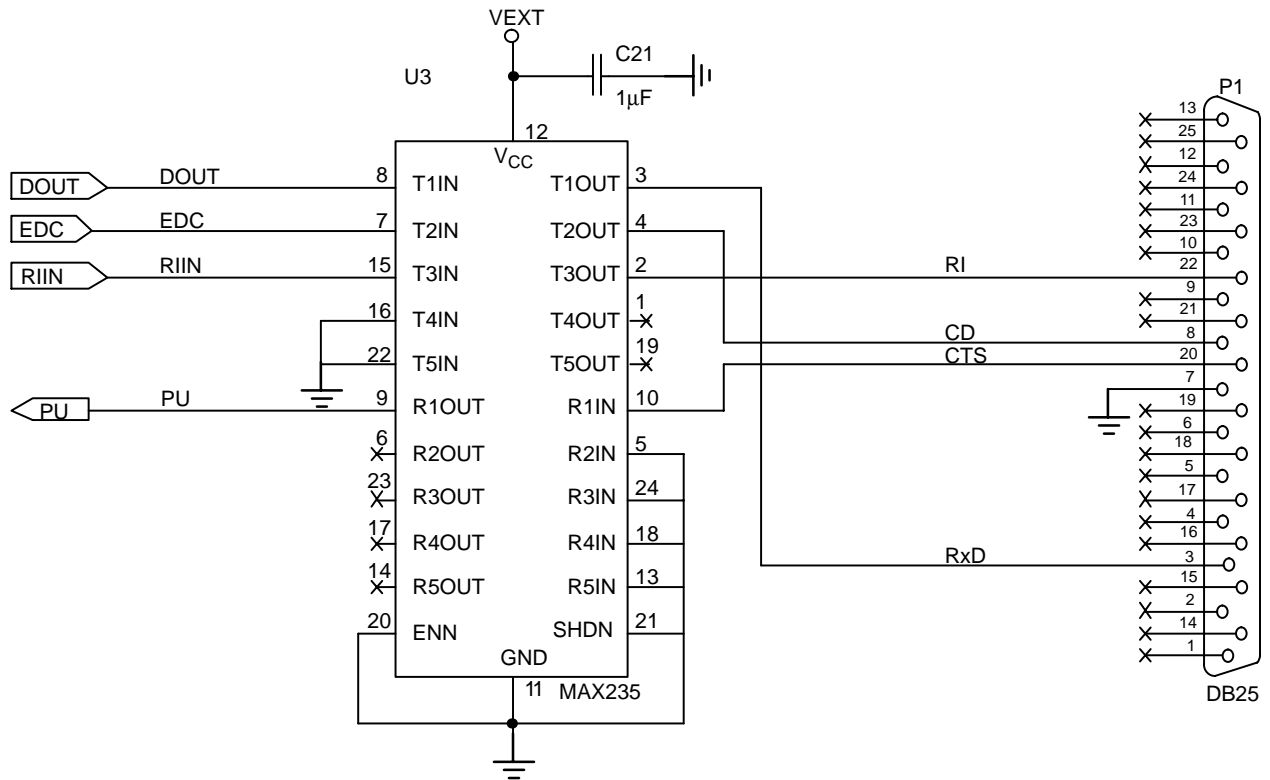


Figure 7. RS232 Interface

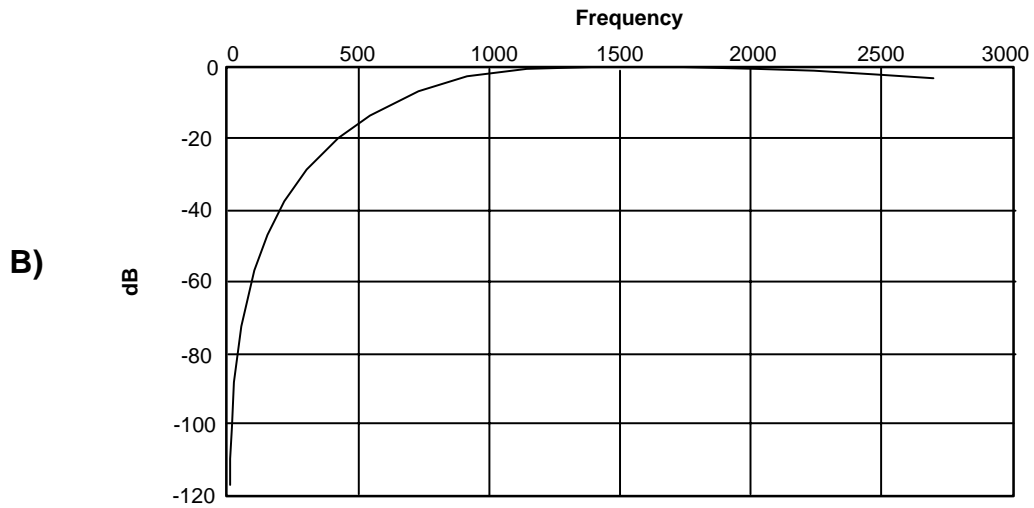
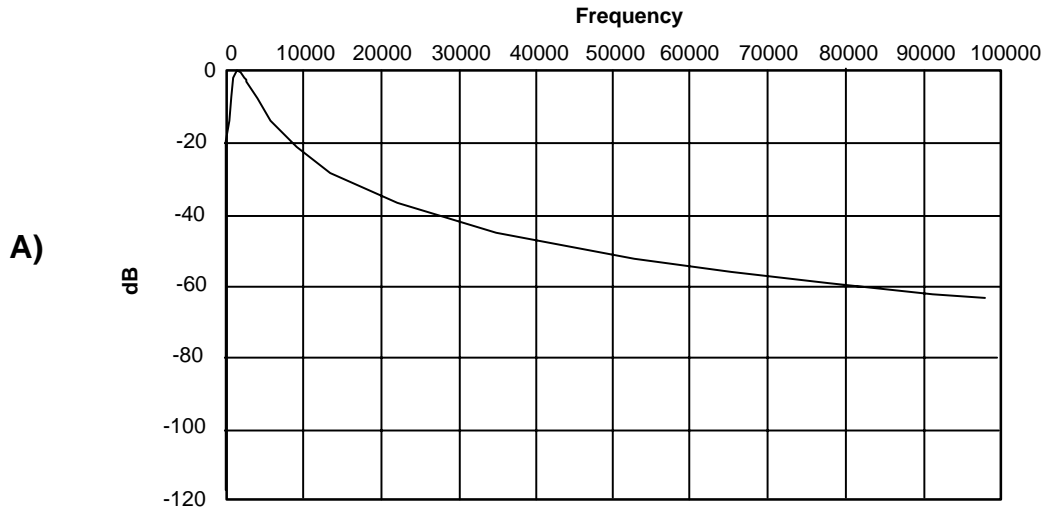


Figure 8. Frequency Response of Input Filter

BILL OF MATERIALS

Direct Analog Access

Item	Quantity	Reference	Part	Tolerance
1	2	C1,C2	0.01 μ F	400V
2	1	C4	0.47 μ F	400V
3	1	C16	0.47 μ F	
4	2	D4,D3	1N4748	
5	1	J1	RJ-11	
6	1	M1	220V	
8	1	Q2	2N4403	
9	2	R1,R2	10	0.5W
10	1	R4	68K	
11	1	R7	8.2K	
12	1	R8	22K	
13	1	R18	2.2K	
14	1	R21	10K	
15	1	6V	BATTERY	

Input Filter for US Implements

Item	Quantity	Reference	Part	Tolerance
1	1	C3	10nF	
2	4	C5,C6,C7, C8	10nF	5%
3	1	C9	4.7nF	5%
4	1	C17	0.1 μ F	
5	1	C18	1 μ F	
6	4	D2,D1,D6, D7	1N914	
7	1	R3	68K	
8	3	R5,R6,R17	330K	
9	1	R9	12K	1%
10	1	R10	4.7K	1%
11	1	R11	226K	1%
12	1	R12	232K	1%
13	2	R13,R14	9.31K	1%
14	1	R15	10K	1%
15	1	R16	240K	
16	1	U1	LM324	

FSK Decoding US Implementation

Item	Quantity	Reference	Part	Tolerance
1	1	C10	27nF	5%
2	3	C11,C15, C19	0.1μF	
3	1	C12	6.8nF	
4	1	C13	1.8nF	
5	1	C14	8.2nF	5%
6	1	C20	10μF	
7	1	POT1	POT	10K
8	1	R19	33K	1%
9	1	R20	18K	1%
10	1	R2	470K	
11	2	R23,R26	5.1K	
12	1	R24	1.2M	
13	1	R25	150K	
14	1	R27	3.3M	
15	1	U2	XR-2211	

RS232 Interface

Item	Quantity	Reference	Part
1	1	C21	1μF
2	1	P1	DB25
3	1	U3	MAX235

NET LIST OF DEMOBOARD

/N00001	R10(2) U1(6) U1(7) R13(1);
/N00002	R10(1) C6(2) C7(1);
/N00003	R5(2) C3(2) U1(3) R6(1);
/N00004	R3(2) D1(CATHODE) D2(ANODE) C3(1);
/N00005	R11(2) C7(2) R17(1) R12(1) U1(5);
/N00006	U1(1) U1(2) C5(1);
/N00007	C5(2) R9(1) C6(1);
/N00008	C8(1) R13(2) R14(1);
/N00009	C8(2) U1(9) U1(8) R15(1);
/N00010	D7(CATHODE) R15(2) D6(ANODE) R16(1) U1(13);
/N00011	R14(2) C9(1) U1(10);
/N00012	R17(2) U1(12) C18(1);
/N00013	R19(2) R25(1) U2(11) C14(1);
/N00014	C15(2) R27(1) U2(2);
/N00015	U2(3) C12(1) R22(1);
/N00016	U2(14) C10(2);
/N00017	C10(1) U2(13);
/N00018	R20(1) R19(1) U2(12);
/N00019	U2(10) C11(1);
/N00020	R20(2) POT1(B);
/N00021	U2(8) R25(2) R24(1) C13(1);
/RXD-5	U3(3) P1(3);
/CD-5	U3(4) P1(8);
/RI-5	U3(2) P1(22);
/CTS-5	U3(10) P1(20);
/TIP-2	C1(2) R1(2) D4(ANODE);
/N00027	Q2(BASE) R18(1) R21(1);
/BAT-2	R18(2) Q2(EMITTER) 6V(+) R8(1);
/N00029	D4(CATHODE) R7(1);
/N00030	R7(2) Q1(1);
/N00031	J1(2) R1(1);
/N000320	J1(3) R2(1);
/RING-2	R2(2) C2(1) D3(CATHODE);
/N000340	Q1(2) C4(2);
/N00035	D3(ANODE) C4(1);
/N000360	C2(2) R4(1);
/ITIP-1	R3(1) C1(1);
/PU-1	U3(9) R21(2);
/RIIN-1	U3(15) R8(2) Q1(5) C16(1);
/N00040	D7(ANODE) D6(CATHODE) R16(2) U1(14) C15(1);
/N00041	R26(2) U2(5) U3(7);
/N00042	U2(7) R24(2) R23(2) U3(8);
/VCC	U1(4) R11(1) C17(2) R5(1) C19(1) U2(1) C20(1) R23(1) R26(1) Q2(COLLECTOR);
/GND	C18(2) C9(2) R12(2) R9(2) R6(2) D2(CATHODE) D1(ANODE) U1(11), C17(1) C14(2) C13(2) POT1(A) POT1(WIPER) U2(4) C11(2) R27(2), R22(2) C12(2) C19(2) C20(2) U3(11) U3(20) U3(5) U3(24), U3(18) U3(13) U3(21) P1(7) U3(16) U3(22) C21(2) R4(2), Q1(4) C16(2) 6V(-);
/VEXT	C21(1) U3(12)

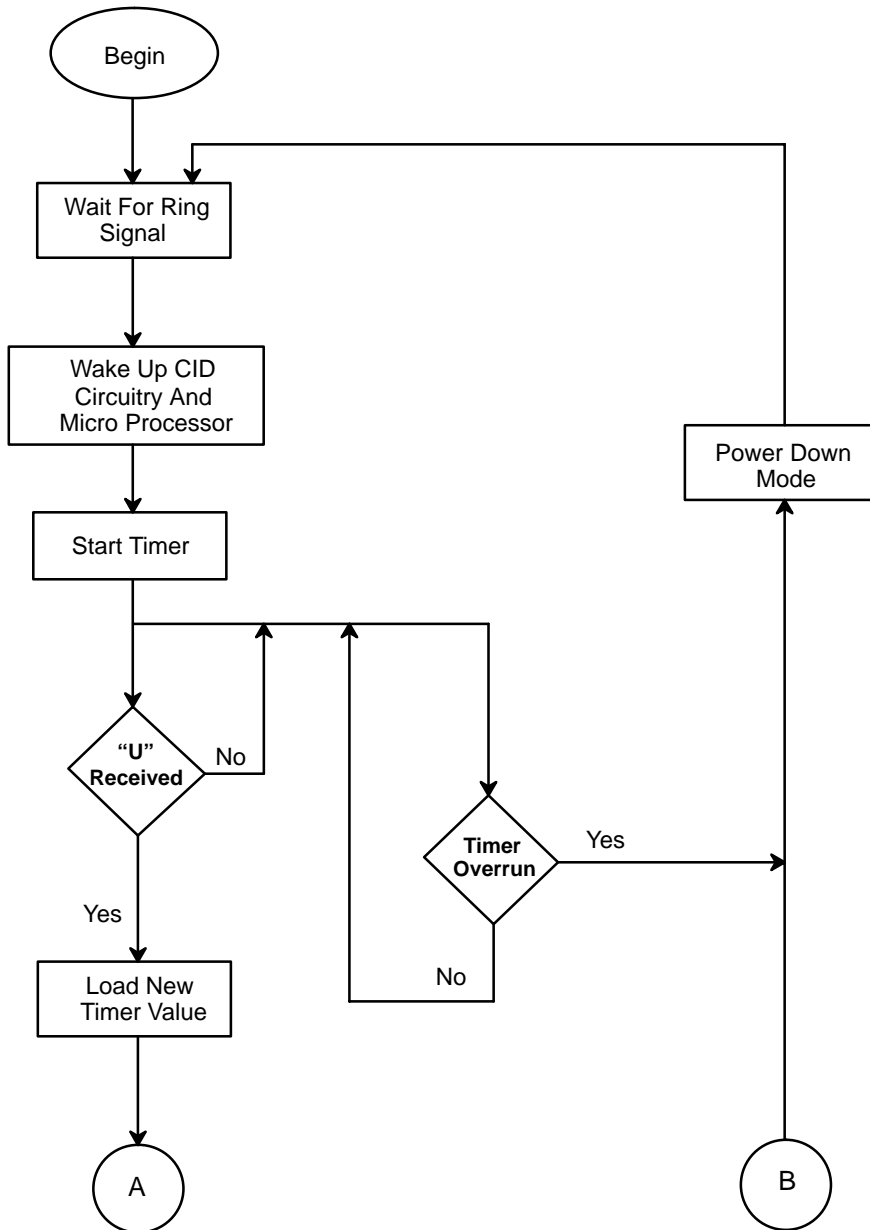


Figure 9. Micro Controller Firmware Flow Chart

The following pages are a description in the form of a flow chart, of a typical program that handles a Caller Identification Delivery Recovery.

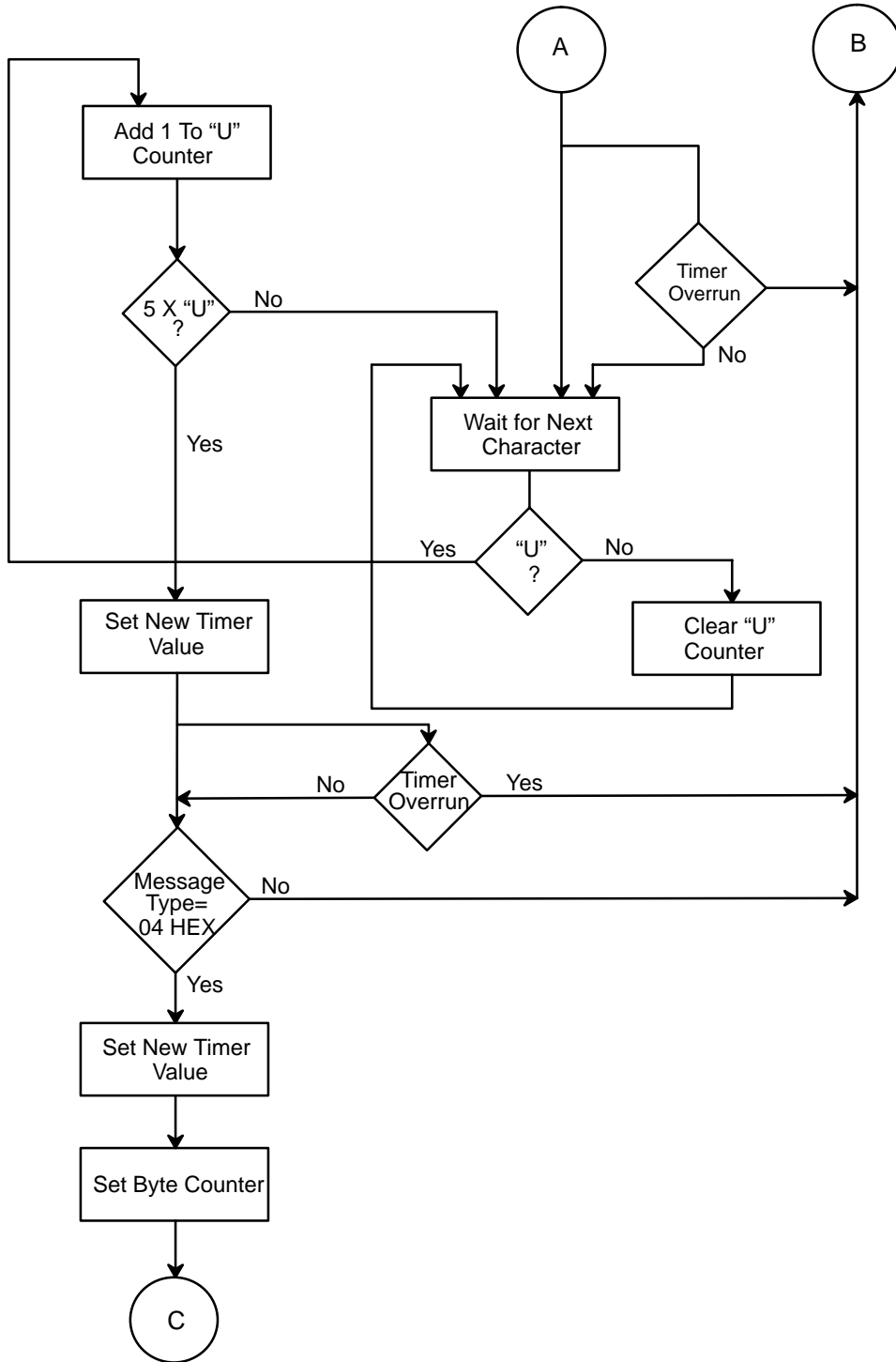


Figure 10. Flow Chart for Caller ID Processing

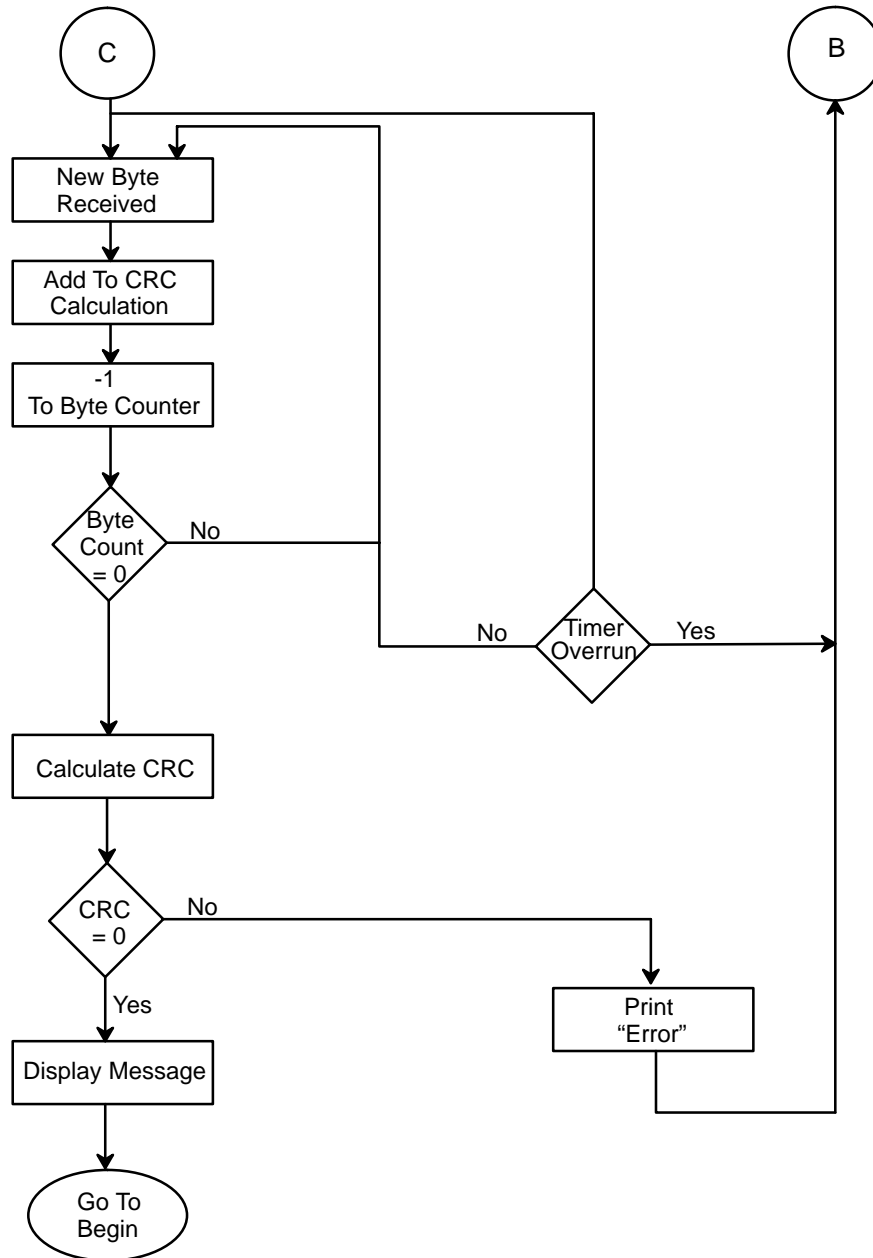


Figure 11. Flow Chart for Caller ID Processing (Cont'd)

REFERENCES:

- [1] Michael G. Ellis. Sr., *Electronic Filter Analysis and Synthesis*, Artech House, Inc. 1994.
- [2] Jack Middlehurst, *Practical Filter Design*, PrenticeHall, 1993.
- [3] Sundaram Seshu and Norman Balabanian, *Linear Network Analysis*, John Wiley & Sons, Inc., 1959.
- [4] Bellcore, *Technical Advisory TA-NWT-000030*. April 1992.

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