DATA SHEET

Communications

XRT8001

WAN Clock

Features
- Clock adaptation for most popular telecommunication frequencies
- Wide input frequency range
- Programmable output frequencies
- Less than 0.05UI wide band output jitter
- Low power operation (5V and 3.3V)
- Maximum lock time of 45ms

Applications
- DSU/CSU
- Frame Relay Access Devices (FRADs)
- Basic Rate (BRI) and Primary Rate (PRI) ISDN terminals
- Concentrators and multiplexers

The XRT8001 is a single-chip, dual phase-locked loop clock adapter for WAN and ISDN applications. This product accommodates the most popular frequencies encountered in T1/E1 access equipment, T1/E1 multiplexers and concentrators, sub-rate switches, routers, Frame Relay Access Devices (FRADs), Remote Access Servers (RASs) and both PRI and BRI ISDN equipment.

Using a serial processor interface the designer can fully control the operational modes of the device by modifying the content of the internal registers. Designed with two internal phase locked loops, the XRT8001 generates two output clocks from a single input reference clock. Each of the two outputs can be independently programmed to generate frequency multiples of 64kHz and 56kHz from T1 and E1 rates.

The extremely impressive jitter performance of the XRT8001 makes it ideal for any equipment deployed in public or private networks with strict regulatory requirements. The device synthesizes two low-jitter clocks with user-selected, industry-standard frequencies, phased-locked to the system reference timing, making it capable of generating less than 0.05UI of wideband.

This chip has several modes of operation to provide designers with greatest flexibility. In the forward master mode, XRT8001 accepts up to 16th harmonic of either 1.544MHz (T1) or 2.048MHz (E1) as input reference, and generates multiples of 56kHz or 64kHz. In the reverse master mode, an input clock of 56kHz or 64kHz is used to generate 1.544MHz (T1) or 2.048MHz (E1) output clocks. In the fractional T1/E1 reverse master mode, the XRT8001 accepts up to the 32nd harmonic of 56kHz or 64kHz as input reference, and generates either 1.544MHz (T1) or 2.048MHz (E1). In the E1 to T1 master mode, the device acccepts up tp the 16th harmonic of 2.048MHz (E1) as input reference and generates 1.544MHz (T1). In the high speed reverse mode, the XRT8001 accepts 64kHz as input reference and generates multiples (1, 2, 4 or 8) of 2.048MHz (E1).

The forward and reverse modes can also be operated in slave configuration where the device generates the same output frequencies as master configuration while being phase locked to an 8kHz input reference.