DATA SHEET

Communications

XRT84L38

Octal T1/E1/J1 Framer

Features
- Programmable Output Clocks for Fractional T1/E1/J1
- Supports CAS and CCS
- Includes Wide Range of T1 Framing Formats: D4, ESF, SLC®96, TIDM and N-Framing
- Supports Programmed I/O Burst and DMA modes of Read-Write access

Applications
- Digital Cross Connect Systems
- Frame Relay Switches and Access Devices
- ATM Equipment with Integrated DS1 Interfaces
- Add/Drop Multiplexers
- Routers
- Voice Over Packet gateways

The XRT84L38 is an eight-channel 1.544 Mbits or 2.048 Mbits T1/E1/J1 CMOS framing controller. Ideal for high-density T1/E1/J1 interfaces for multiplexers, switches, routers and modems. When linked to its complementary T1/E1/J1 Line Interface Unit (LIU), the XRT83L38, the two-chip combination offers customers a complete octal solution.

The XRT84L38 provides framing, error detection and performance monitoring in accordance with ANSI/ITU_T specifications. The XRT84L38 supports Direct Memory Access (DMA) for path maintenance data supplied through the LAP-D channel – this enables the framer to quickly move data to/from the system memory by processing the data in 96 byte blocks. The device supports a wide range of backplane standards including ones with clock rates of up to 16.384 MHz. This allows the system to process T1/E1 data rapidly (8.192 Mbit/sec) and affords minimal connections (trace lines) between the framer and system-side circuitry.

Each framer has its own framer synchronizer and transmit-receive slip buffers, and can independently be configured to common DS1/E1/J1 signal formats. The framer also contains a transmit and overhead data input port which permits data link terminal equipment direct access to the outbound T1/E1/J1 frames. Conversely, the receive overhead output data port allows data link equipment direct access to the data link its of the inbound frames.

The XRT84L38 supports extensive test and diagnostic and test functions including loop-backs, boundary scan, Psuedo Random Bit Sequence (PRBS) test pattern generation, performance monitoring, and BIT ERROR RATE (BER) counter.