GENERAL DESCRIPTION

The XRT73L00A DS3/E3/STS-1 Line Interface Unit is an improved version of the XRT73L00 and consists of a line transmitter and receiver integrated on a single chip and is designed for DS3, E3 or SONET STS-1 applications.

XRT73L00A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates.

In the transmit direction, the XRT73L00A encodes input data to either B3ZS (for DS3/STS-1 applications) or HDB3 (for E3 applications) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction the XRT73L00A performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of line code violations.

The XRT73L00A also contains a 4-Wire Microprocessor Serial Interface for accessing the on-chip Command registers.

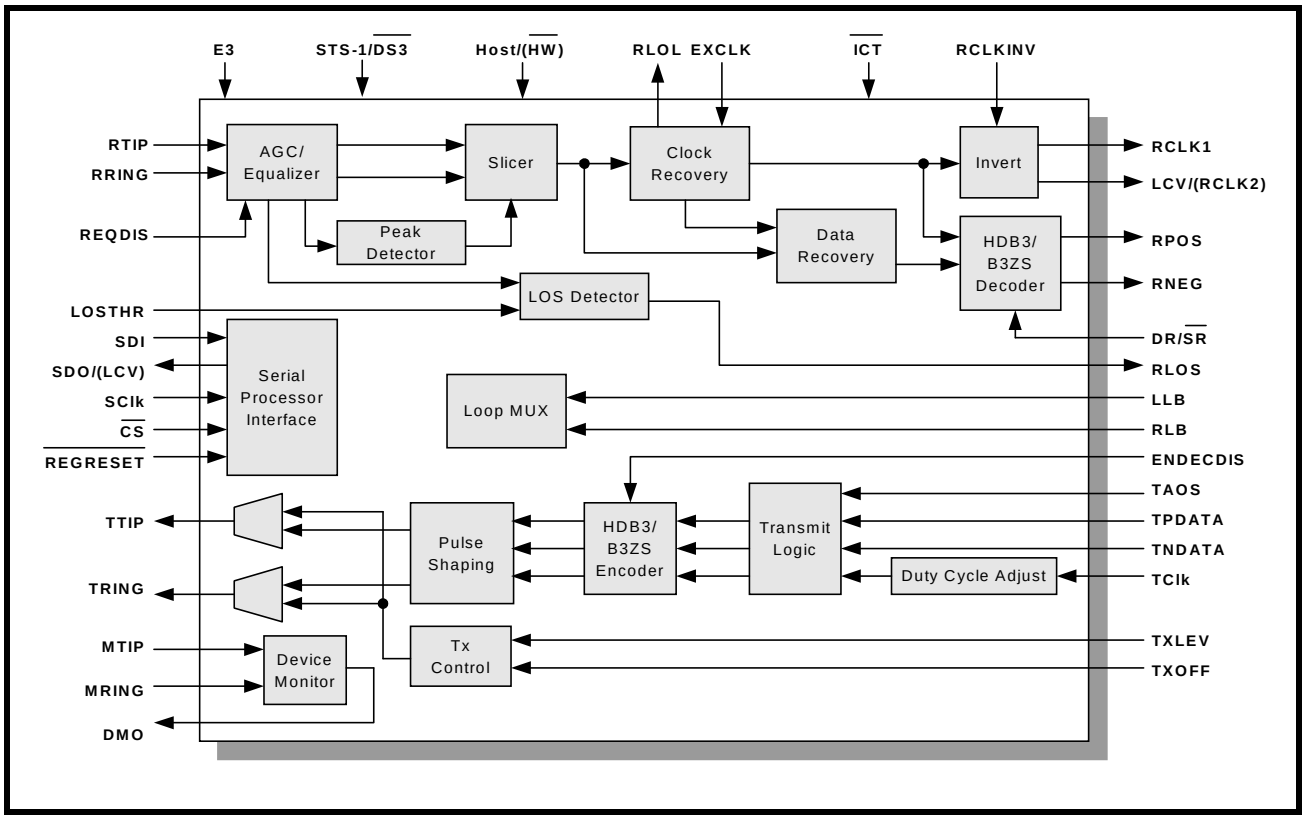
FEATURES

- Incorporates an improved Timing Recovery circuit and is pin and functional compatible to XRT73L00
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Contains a 4-Wire Microprocessor Serial Interface
- Uses Minimum External components
- Single +3.3V Power Supply
- 5 V Tolerant pins
- -40°C to +85°C Operating Temperature Range
- Available in a 44 pin TQFP package

APPLICATIONS

- Interfaces to E3, DS3 or SONET STS-1 Networks
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals
- Multiplexers

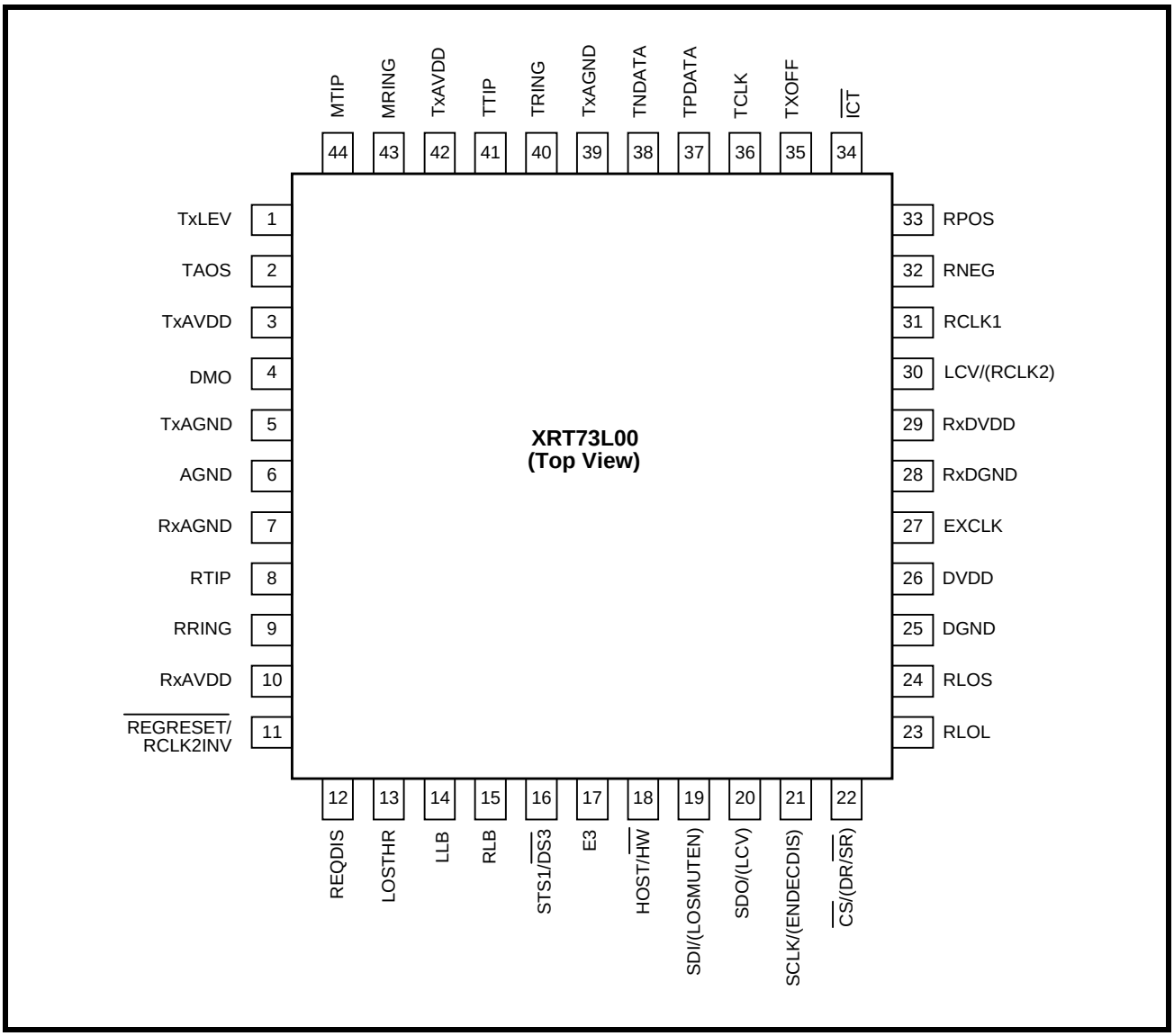
FIGURE 1. BLOCK DIAGRAM OF THE XRT73L00



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT73L00AIV	44 Pin TQFP (10mm x 10mm)	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT73L00A IN THE 44 PIN TQFP



PIN DESCRIPTION

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
1	TXLEV	I	**Transmit Line Build-Out Enable/Disable Select:** This input pin is used to enable or disable the Transmit Line Build-Out circuit in the XRT73L00. Setting this pin to “High” disables the Line Build-Out circuit. In this mode, the XRT73L00A outputs partially shaped pulses onto the line via the TTIP and TRING output pins. Setting this pin to “Low” enables the Line Build-Out circuit. In this mode, the XRT73L00A outputs partially-shaped pulses onto the line via the TTIP and TRING output pins. To comply with the isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-Core or Bellcore GR-253-Core: 1. Set this input pin to a "1" if the cable length between the Cross-Connect and the transmit output of the XRT73L00A is greater than 225 feet. 2. Set this input pin to a "0" if the cable length between the Cross-Connect and the transmit output of the XRT73L00A is less than 225 feet. This pin is active only if both of the following are true: (a) The XRT73L00A is configured to operate in either the DS3 or SONET STS-1 modes and (b) The XRT73L00A is configured to operate in the Hardware Mode. ***NOTE:*** *This pin should be tied to GND if the XRT73L00A is to be operated in the HOST mode.*
2	TAOS	I	**Transmit All Ones Select:** A “High” on this pin causes a continuous AMI all “1’s” pattern to be transmitted onto the line. The frequency of this “1’s” pattern is determined by TCLK. ***NOTES:*** *1. This input pin is ignored if the XRT73L00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73L00A is going to be operating in the HOST Mode.*
3	TxAVDD	****	**Transmit Analog Power Supply**
4	DMO	O	**Drive Monitor Output:** If no bipolar line signal is detected on the TTIP/TRING output pins via the MTIP and MRING input pins for 128±32 TCLK periods, then the DMO output pin toggles and remains “High” until the next bipolar pulse is detected.
5	TxAGND	****	**Transmit Analog Ground**
6	AGND	****	**Analog Ground (Substrate)**
7	RxAGND	****	**Receive Analog Ground**
8	RTIP	I	**Receive TIP Input:** This input pin along with RRING is used to receive the line signal from the Remote DS3/E3/STS-1 Terminal.
9	RRING	I	**Receive RING Input:** This input pin along with RTIP is used to receive the line signal from the Remote DS3/E3/STS-1 Terminal.

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
10	RxAVDD	****	**Receive Analog Power Supply**
11	$\overline{\text{REGRESET}}$/ (RCLK2INV)	I	**Register Reset Input pin (Invert RCLK2 Output - Select):** The function of this pin depends upon whether the XRT73L00A is operating in the HOST Mode or in the Hardware Mode. **HOST Mode - Register Reset Input pin:** Setting this input pin "Low" causes the XRT73L00A to reset the contents of the Command Registers to their default settings and operating configuration. This pin is internally pulled "High". **Hardware Mode - Invert RCLK2 Output Select:** Setting this input pin "Low" configures the Receive Section of the XRT73L00A to output the recovered data via the RPOS and RNEG output pins on the rising edge of the RCLK2 output signal. Setting this input pin "High" configures the Receive Section to output the recovered data on the falling edge of the RCLK2 output signal.
12	REQDIS	I	**Receive Equalization Disable Input:** Setting this input pin "High" disables the Internal Receive Equalizer in the XRT73L00. Setting this pin "Low" enables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2. ***NOTES:*** *1. This input pin is ignored if the XRT73L00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73L00A is going to be operating in the HOST Mode.*
13	LOSTHR	I	**Loss of Signal Threshold Control:** This input pin is used to select the LOS (Loss of Signal) Declaration and Clearance thresholds for the Analog LOS Detector circuit. Two settings are provided by forcing this signal to either GND or VDD. ***NOTE:*** *This pin is only applicable during DS3 or STS-1 operations.*
14	LLB	I	**Local Loop-Back Select:** This input pin along with RLB dictates which Loop-Back mode the XRT73L00A is operating in. A "High" on this pin with RLB being set to "Low" configures the XRT73L00A to operate in the Analog Local Loop-Back Mode. A "High" on this pin with RLB also being set to "High" configures the XRT73L00A to operate in the Digital Local Loop-Back Mode. ***NOTES:*** *1. This input pin is ignored if the XRT73L00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73L00A is going to be operating in the HOST Mode.*

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
15	RLB	I	**Remote Loop-Back Select:** This input pin along with LLB dictates which Loop-Back mode the XRT73L00A is be operating in. A "High" on this pin with LLB being set to "Low" configures the XRT73L00A to operate in the Remote Loop-Back Mode. A "High" on this pin with LLB also being set to "High" configures the XRT73L00A to operate in the Digital Local Loop-Back Mode. ***NOTES:*** *1. This input pin is ignored if the XRT73L00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73L00A is going to be operating in the HOST Mode.*
16	STS-1/$\overline{DS3}$	I	**STS-1/$\overline{DS3}$ Select Input:** A "High" on this pin configures the Clock Recovery Phase Locked Loop to set its VCO Center frequency to around 51.84 MHz for SONET STS-1 operations. A "Low" on this pin configures the Clock Recovery Phase Locked Loop to set its VCO Center frequency to around 44.736 MHz for DS3 operations. ***NOTES:*** *1. The XRT73L00A ignores this pin if the E3 pin (pin 17) is set to "1".* *2. This input pin is ignored if the XRT73L00A is operating in the HOST Mode.* *3. Tie this pin to GND if the XRT73L00A is going to be operating in the HOST Mode.*
17	E3	I	**E3 Select Input:** A "High" on this pin configures the XRT73L00A to operate in the E3 Mode. A "Low" on this pin configures the XRT73L00A to check the state of the STS-1/ $\overline{DS3}$ input pin. ***NOTES:*** *1. This input pin is ignored if the XRT73L00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73L00A is going to be operating in the HOST Mode.*
18	HOST/$\overline{HW}$	I	**HOST/$\overline{HW}$ Mode Select:** This input pin is used to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SCLK, $\overline{CS}$ and $\overline{REGRESET}$ pins). Setting this input pin "High" enables the Microprocessor Serial Interface (e.g. configures the XRT73L00A to operate in the HOST Mode). In this mode, the XRT73L00A is configured by writing data into the on-chip Command Registers via the Microprocessor Serial Interface. When the XRT73L00A is operating in the HOST Mode, it ignores the states of many of the discrete input pins. Setting this input pin "Low" disables the Microprocessor Serial Interface (e.g., configures the XRT73L00A to operate in the Hardware Mode). In this mode, many of the external input control pins are functional.

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
19	SDI/ (LOSMUTEN)	I	**Serial Data Input for the Microprocessor Serial Interface (HOST Mode) or MUTE-upon-LOS Enable Input (Hardware Mode):** The function of this input pin depends upon whether the XRT73L00A is operating in the HOST or the Hardware Mode. **Serial Data Input for the Microprocessor Serial Interface (HOST Mode):** This pin is used to read or write data into the Command Registers of the Microprocessor Serial Interface. The Read/Write bit, the Address Values of the Command Registers and Data Value to be written during Write Operations are applied to this pin. This input is sampled on the rising edge of the SCLK pin (pin 21). **MUTE-upon-LOS Enable Input (Hardware Mode):** In the Hardware Mode this input pin is used to configure the XRT73L00A to MUTE the recovered data via the RPOS and RNEG output pins whenever it declares an LOS condition. Setting this input pin "High" configures the XRT73L00A to automatically pull the RPOS and RNEG output pins to GND whenever it is declaring an LOS condition, thereby MUTing the data being output to the Terminal Equipment. Setting this input pin "Low" configures the XRT73L00A to NOT automatically MUTE the recovered data whenever an LOS condition is declared.
20	SDO/(LCV)	O	**Serial Data Output from the Controller Port/(Line Code Violation Output (LCV) Indicator.):** The function of this input pin depends upon whether the XRT73L00A is operating in the HOST or the Hardware Mode. **HOST Mode - Microprocessor Serial Interface - Serial Data Output.** This pin serially outputs the contents of the specified Command Register during Read Operations. The data on this pin is updated on the falling edge of the SCLK input signal. This pin is tri-stated upon completion of data transfer. **Hardware Mode - Line Code Violation Output Indicator.** This pin pulses "High" for one bit period any time the Receive Section of the XRT73L00A detects a Line Code Violation in the incoming E3, DS3 or STS-1 Data Stream.
21	SCLK/ (ENDECDIS)	I	**Microprocessor Serial Interface Clock Signal/Encoder Disable:** **HOST Mode - Microprocessor Serial Interface Clock Signal** This signal is used to sample the data on the SDI pin on the rising edge of this signal. During Read operations, the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. **Hardware Mode - B3ZS/HDB3 Encoder/Decoder Disable** Setting this input pin "High" disables both the B3ZS/HDB3 Encoder and Decoder. This setting configures the Transmit Section of the XRT73L00A to transmit data to the remote terminal equipment via the AMI Line Code. This setting also configures the Receive Section to receive a line signal via the AMI Line Code. Setting this input pin "Low" enables both the B3ZS/HDB3 Encoder and Decoder. This setting configures the Transmit Section of the XRT73L00A to transmit data in the B3ZS format for DS3/STS-1 applications or the HDB3 format for E3 applications. This setting configures the Receive Section to receive a line signal that has been encoded into the B3ZS or HDB3 line code.

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
22	$\overline{CS}$/(DR/$\overline{SR}$)	I	**Microprocessor Serial Interface - Chip Select/Encoder and Decoder Disable** The function of this input pin depends upon whether the XRT73L00A is operating in the HOST or the Hardware Mode. **HOST Mode - Chip Select Input:** The Local Microprocessor must assert this pin (e.g., set it to "0") in order to enable communication with the XRT73L00A via the Microprocessor Serial Interface. **Hardware Mode - Dual-Rail/Single-Rail Select Input:** Setting this input pin "High" configures the XRT73L00A to operate in the Dual-Rail Mode. When the XRT73L00A is operating in this mode, then the Receive Section of the LIU IC outputs the Recovered Data via both RPOS and RNEG output pins. Setting this input pin "Low" configures the XRT73L00A to operate in the Single-Rail Mode. When the XRT73L00A is operating in this mode, the Receive Section of the LIU IC outputs the Recovered Data via the RPOS output pin in a binary data stream. No data will output via the RNEG output pin.
23	RLOL	O	**Receive Loss of Lock Output Indicator** This output pin toggles "High" if the XRT73L00A has detected a Loss of Lock Condition. The XRT73L00A declares an LOL (Loss of Lock) Condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the EXCLK input pin) by more than 0.5%. ***NOTE:*** *The RCLK1/2 output pins are sourced by the signal applied at the EXCLK input pin anytime the XRT73L00A declares an LOL condition.*
24	RLOS	O	**Receive Loss of Signal Output Indicator** This output pin toggles "High" if the XRT73L00A has detected a Loss of Signal Condition in the incoming line signal. The criteria the XRT73L00A uses to declare an LOS Condition depends upon whether the device is operating in the E3 or DS3/STS-1 Mode.
25	DGND	****	**Digital Ground**
26	DVDD	****	**Digital Power Supply**
27	EXCLK	I	**External Reference Clock Input:** Apply a line-rate clock signal to this input pin. This signal is a 34.368MHz clock signal for E3 applications, a 44.736 MHz clock signal for DS3 applications or a 51.84 MHz clock signal for SONET STS-1 applications. ***NOTE:*** *This input pin functions as the source of the RxCLK output clock signal any time the XRT73L00A declares an LOL condition.*
28	RxDGND	****	**Receiver Digital Ground**
29	RxDVDD	****	**Receiver Digital Power Supply**

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
30	LCV/(RCLK2)	O	**Line Code Violation Indicator/Receive Clock Output pin 2:** The function of this pin depends upon whether the XRT73L00A is operating in the HOST Mode, the Hardware Mode or User selection. **HOST Mode - Line Code Violation Indicator Output:** If the XRT73L00A is configured to operate in the HOST Mode, then this pin functions as the LCV output pin by default. However, by using the on-chip Command Registers, this pin can be configured to function as the second Receive Clock signal output pin RCLK2. **Hardware Mode - Receive Clock Output pin 2:** This output pin is the Recovered Clock signal from the incoming line signal. The receive section of the XRT73L00A outputs data via the RPOS and RNEG output pins on the rising edge of this clock signal. ***NOTE:*** *If the XRT73L00A is operating in the HOST Mode and this pin is configured to function as the additional Receive Clock signal output pin, then the XRT73L00A can be configured to update the data on the RPOS and RNEG output pins on the falling edge of this clock signal.*
31	RCLK1	O	**Receive Clock Output pin 1:** This output pin is the Recovered Clock signal from the incoming line signal. The receive section of the XRT73L00A outputs data via the RPOS and RNEG output pins on the rising edge of this clock signal. ***NOTE:*** *If the XRT73L00A is operating in the HOST Mode, the device can be configured to update the data on the RPOS and RNEG output pins on the falling edge of this clock signal.*
32	RNEG	O	**Receive Negative Pulse Output:** This output pin pulses “High” whenever the XRT73L00A has received a Negative Polarity pulse in the incoming line signal at the RTIP/RRING inputs. ***NOTES:*** 1. *If the B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.* 2. *This output pin is inactive if the XRT73L00A has been configured to operate in the Single-Rail Mode.*
33	RPOS	O	**Receive Positive Pulse Output:** This output pin pulses “High” whenever the XRT73L00A has received a Positive Polarity pulse in the incoming line signal at the RTIP/RRING inputs. ***NOTE:*** *If the B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
34	$\overline{\text{ICT}}$	I	**In-Circuit Test Input:** Setting this input pin “Low” causes all digital and analog outputs to go into a high-impedance state in order to permit in-circuit testing. Set this pin “High” for normal operation. ***NOTE:*** *This pin is internally pulled “High”.*

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
35	TXOFF	I	**Transmitter OFF Input:** Setting this input pin "High" configures the XRT73L00A to turn off the Transmitter in the device. When the Transmitter is shut-off, the TTIP and TRING output pins will be tri-stated in the XRT73L00. ***NOTES:*** *1. This input pin is NOT ignored if the XRT73L00A is operating in the HOST Mode.* *2. Tie this pin to GND if the XRT73L00A is going to be operating in the HOST Mode.*
36	TCLK	I	**Transmit Clock Input for TPDATA and TNDATA:** This input pin must be driven at 34.368 MHz for E3 applications, 44.736MHz for DS3 applications, or 51.84MHz for SONET STS-1 applications. The XRT73L00A uses this signal to sample the TPDATA and TNDATA input pins. The XRT73L00A is configured to sample these two pins on the falling edge of this signal. If the XRT73L00A is operating in the HOST Mode, then the device can be configured to sample the TPDATA and TNDATA input pins on the rising edge of TCLK.
37	TPDATA	I	**Transmit Positive Data Input:** The XRT73L00A samples this pin on the falling edge of TCLK. If the device samples a "1" at this input pin, then it generates and transmits a positive polarity pulse to the line. ***NOTES:*** *1. The data should be applied to this input pin if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* *2. If the XRT73L00A is operating in the HOST Mode, then the XRT73L00A can be configured to sample the TPDATA pin on either the rising or falling edge of TCLK.*
38	TNDATA	I	**Transmit Negative Data Input:** The XRT73L00A samples this pin on the falling edge of TCLK. If the device samples a "1" at this input pin, then it generates and transmits a negative polarity pulse to the line. ***NOTES:*** *1. This input pin is ignored and should be tied to GND if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* *2. If the XRT73L00A is operating in the HOST Mode, then the XRT73L00A can be configured to sample the TNDATA pin on either the rising or falling edge of TCLK.*
39	TxAGND	-	**Transmit Analog Ground**
40	TRING	O	**Transmit TIP Output:** The XRT73L00A uses this pin along with TTIP to transmit a bipolar line signal via a 1:1 transformer. ***NOTE:*** *This output pin along with TTIP is tri-stated anytime the TxOFF input pin or bit-field is set "high".*

PIN DESCRIPTION

PIN #	SYMBOL	TYPE	DESCRIPTION
41	TTIP	O	**Transmit RING Output:** The XRT73L00A uses this pin along with TRING to transmit a bipolar line signal via a 1:1 transformer. ***NOTE:*** *This output pin along with TRING is tri-stated anytime the TxOFF input pin or bit-field is set "high".*
42	TxAVDD	-	**Transmit Analog Power Supply**
43	MRING	I	**Monitor Ring Input:** This input pin along with the MTIP pin function as the input pins for the Transmit Drive Monitor. These two input pins are used to determine whether or not a bipolar line signal is being output via the TTIP and TRING output pins. The Transmit Drive Monitor circuit will toggle the DMO output pin "high" denoting a Transmit Line Fault condition if no bipolar pulses are detected via the TTIP/ TRING output pins for 128 bit-periods. Connect this input pin to the TRING output pin via a 270 ohm resistor. ***NOTE:*** *Tie this input pin to GND if you do not intend to use the Transmit Drive Monitor.*
44	MTIP	I	**Monitor Tip Input:** This input pin along with the MRING pin function as the input pins for the Transmit Drive Monitor. These two input pins are to be used to determine whether or not a bipolar line signal is being output via the TTIP and TRING output pins. The Transmit Drive Monitor circuit will toggle the DMO output pin "high" denoting a Transmit Line Fault condition if no bipolar pulses are detected via the TTIP/ TRING output pins for 128 bit periods. Connect this input pin to the TTIP output pin via a 270 ohm resistor. ***NOTE:*** *Tie this input pin to GND if you do not intend to use the Transmit Drive Monitor.*

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

POWER SUPPLY	**-0.5 TO +3.465V**
STORAGE TEMPERATURE	**-65°C TO 150°C**
INPUT VOLTAGE AT ANY PIN	**-0.5V TO 5.0V**
POWER DISSIPATION TQFP PACKAGE	**1.2W**
INPUT CURRENT AT ANY PIN	**+100MA**
ESD RATING (MIL-STD-883, M-3015)	**1500V**

DC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DDD}	DC Supply Voltage	3.135	3.3	3.465	V
V_{DDA}	DC Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply Current (Measured while Transmitting and Receiving all “1’s”)			180	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.0	V
V_{OL}	Output Low Voltage, IOUT = -4.0mA			0.4	V
V_{OH}	Output High Voltage, IOUT = 4.0mA	2.8			V
I_L	Input Leakage Current*			±10	mA

** Not applicable to pins with pull-up/pull-down resistors.*

AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Terminal Side Timing Parameters (See Figure 3 & Figure 4)					
	TCLK Clock Duty Cycle (DS3/STS-1)	30	50	70	%
	TCLK Clock Duty Cycle (E3)	30	50	70	%
	TCLK Frequency (SONET STS-1)		51.84		MHz
	TCLK Frequency (DS3)		44.736		MHz
	TCLK Frequency (E3)		34.368		MHz
t_{RTX}	TCLK Clock Rise Time (10% to 90%)			4	ns
t_{FTX}	TCLK Clock Fall Time (90% to 10%)			4	ns
t_{TSU}	TPDATA/TNDATA to TCLK Falling Set up time	3			ns
t_{THO}	TPDATA/TNDATA to TCLK Falling Hold time	3			ns
t_{LCVO}	RCLK to rising edge of LCV output delay		2.5		ns
t_{TDY}	TTIP/TRING to TCLK Rising Propagation Delay time	0.6		14	ns
	RCLK Clock Duty Cycle	45	50	55	%
	RCLK Frequency (SONET STS-1)		51.84		MHz
	RCLK Frequency (DS3)		44.736		MHz
	RCLK Frequency (E3)		34.368		MHz
t_{CO}	RCLK to RPOS/RNEG Delay Time			4	ns
t_{RRX}	RCLK Clock Rise Time (10% to 90%)		2	4	ns
t_{FRX}	RCLK Clock Fall Time (10% to 90%)		1.5	3	ns
C_i	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

FIGURE 3. TIMING DIAGRAM OF THE TRANSMIT TERMINAL INPUT INTERFACE

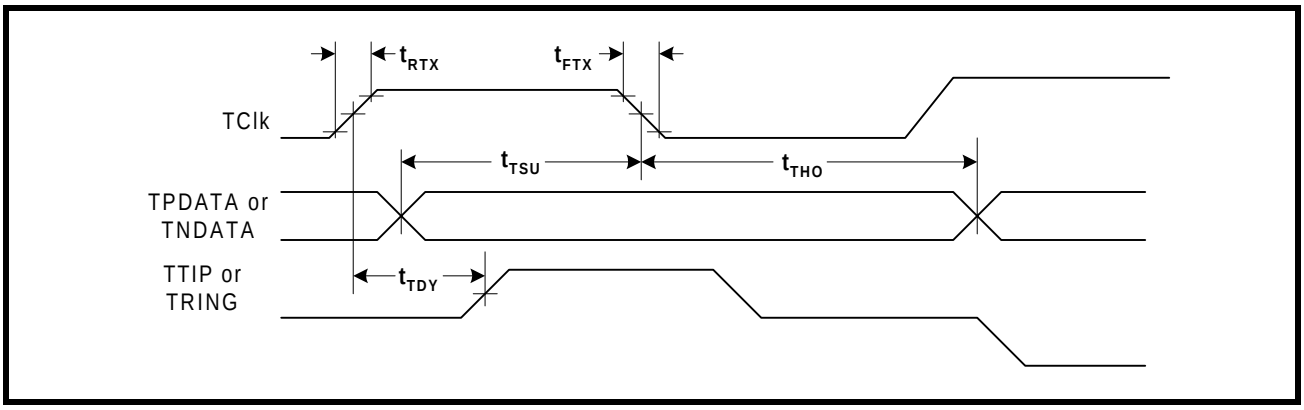


FIGURE 4. TIMING DIAGRAM OF THE RECEIVE TERMINAL OUTPUT INTERFACE

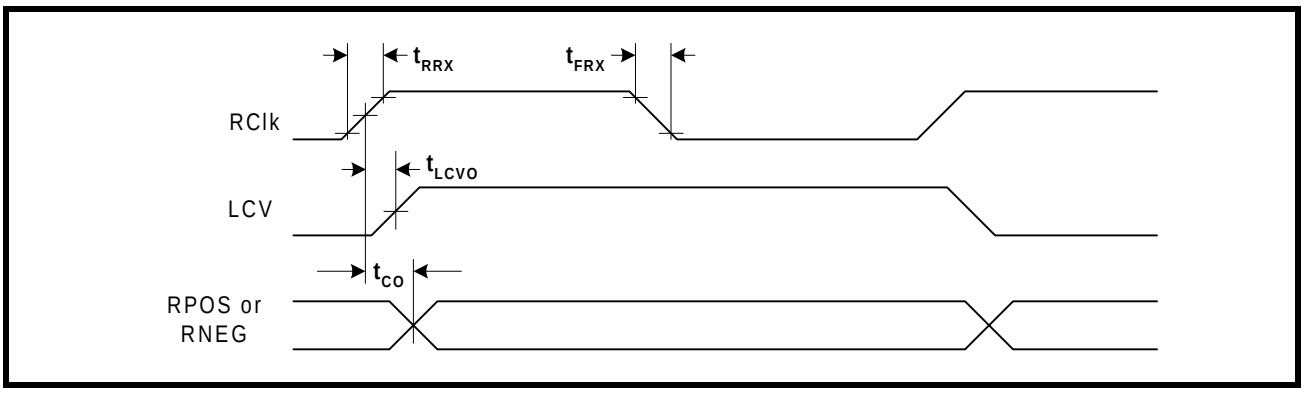
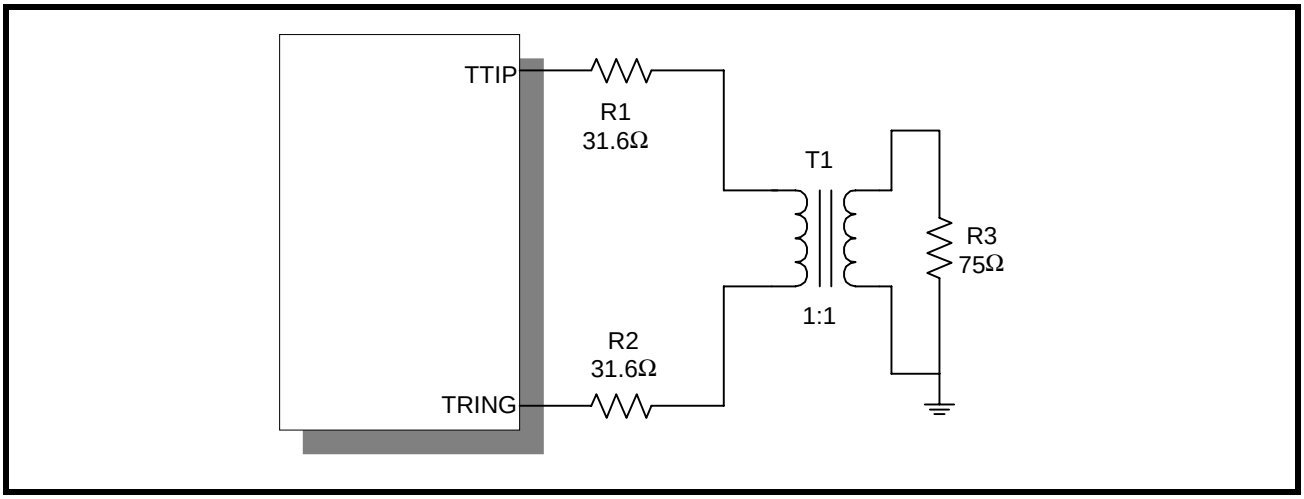


FIGURE 5. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR DS3, E3 AND STS-1 RATES



AC ELECTRICAL CHARACTERISTICS (CONT'D) Line Side Parameters

(T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
E3 Application Parameters Transmit Line Characteristics (See Figure 5)					
	Transmit Output Pulse Amplitude (Measured at Secondary Output of Transformer)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
	Transmit Output Pulse Width	12.5	14.55	16.5	ns
	Transmit Output Pulse Width Ratio	0.95	1.00	1.05	
	Transmit Output Jitter with jitter-free input clock at TCLK		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	1200	1400		feet
	Interference Margin	-20	-17		dB
	Signal Level to Declare Loss of Signal			-35	dB
	Signal Level to Clear Loss of Signal	-15			dB
	Occurrence of LOS to LOS Declaration Time	10	100	255	UI
	Termination of LOS to LOS Clearance Time	10	100	255	UI
	Intrinsic Jitter (all "1's" Pattern)		0.01		UI
	Max Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 1KHz	30			UI
	Max Jitter Tolerance @ Jitter Frequency = 10KHz	4			UI
	Max Jitter Tolerance @ Jitter Frequency = 800KHz	0.15	0.20		UI

AC ELECTRICAL CHARACTERISTICS (CONT'D) Line Side Parameters

(T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
SONET STS-1 Application Parameters Transmit Line Characteristics (See Figure 5)					
	Transmit Output Pulse Amplitude (Measured with TXLEV = 0)	0.65	0.75	0.90	Vpk
	Transmit Output Pulse Amplitude (Measured with TXLEV = 1)	0.93	0.98	1.08	Vpk
	Transmit Output Pulse Width	8.6	9.65	10.6	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free clock input at TCLK		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	900	1100		feet
	Signal Level to Declare or Clear Loss of Signal (see Table 4)				mV
	Intrinsic Jitter (all "1's" Pattern)		0.03		UI
	Max Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 1KHz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 10KHz	5			UI
	Max Jitter Tolerance @ Jitter Frequency = 400KHz	0.15	0.35		UI

AC ELECTRICAL CHARACTERISTICS (CONT'D) LINE SIDE PARAMETERS

(T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DS3 Application Parameters **Transmit Line Characteristics (See Figure 5)**					
	Transmit Output Pulse Amplitude (Measured at 0 feet, TXLEV = 0)	0.65	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured at 0 feet, TXLEV = 1)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Width	10.10	11.18	12.28	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input clock at TCLK		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of Cable)	900	1100		feet
	Intrinsic Jitter (All One's Pattern)		0.01		UI
LOS Level With Equalizer Enabled (Table 4)					
	Signal Level to Declare Loss of Signal (LOSTHR = 0)			55	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 0)	220			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 1)			22	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 1)	90			mV
LOS Level With Equalizer Disabled (Table 4)					
	Signal Level to Declare Loss of Signal (LOSTHR = 0)			35	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 0)	155			mV
	Signal Level to Declare Loss of Signal (LOSTHR = 1)			17	mV
	Signal Level to Clear Loss of Signal (LOSTHR = 1)	70			mV
	Max Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 1KHz	64			UI
	Max Jitter Tolerance @ Jitter Frequency = 10KHz	5			UI
	Max Jitter Tolerance @ Jitter Frequency = 300KHz -- (Cat II)	0.35	0.45		UI

Figure 6, Figure 7 and Figure 8 present the Pulse Template requirements for the E3, DS3 and STS-1 Rates.

FIGURE 6. ITU-T G.703 TRANSMIT OUTPUT PULSE TEMPLATE FOR E3 APPLICATIONS

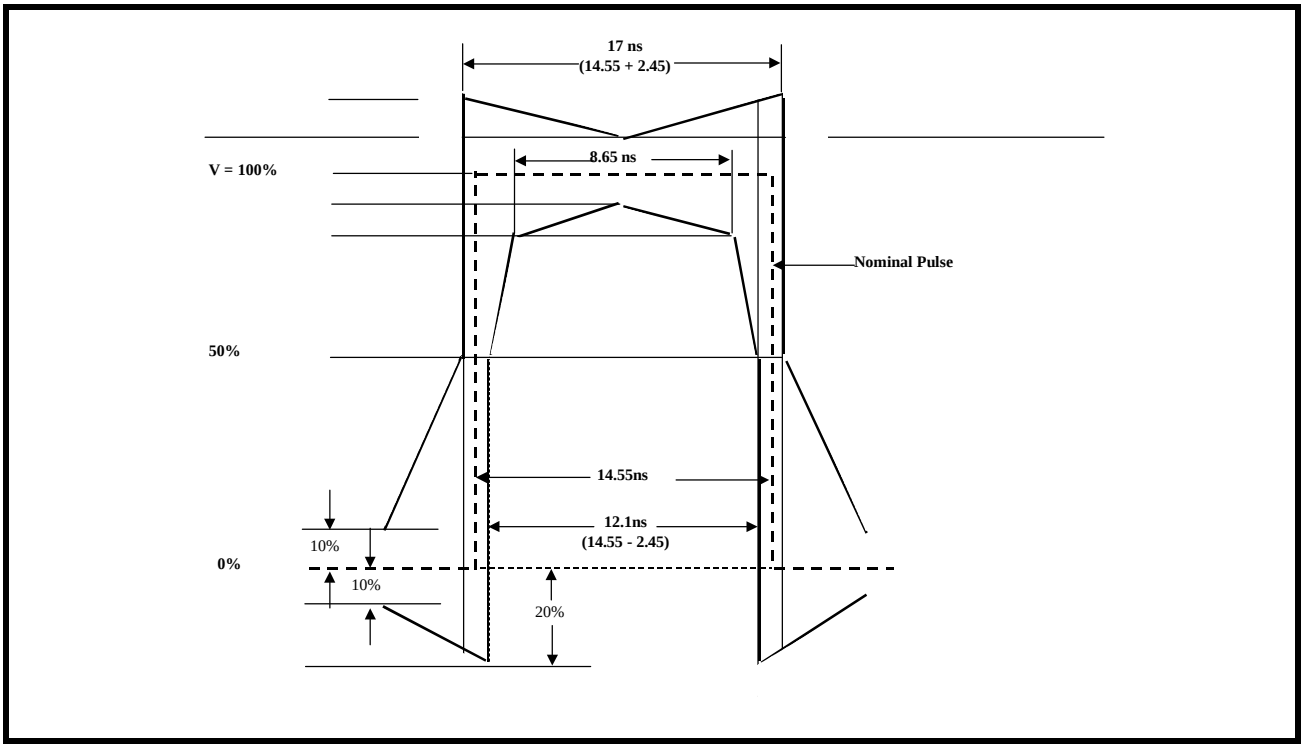


FIGURE 7. BELLCORE GR-499-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS

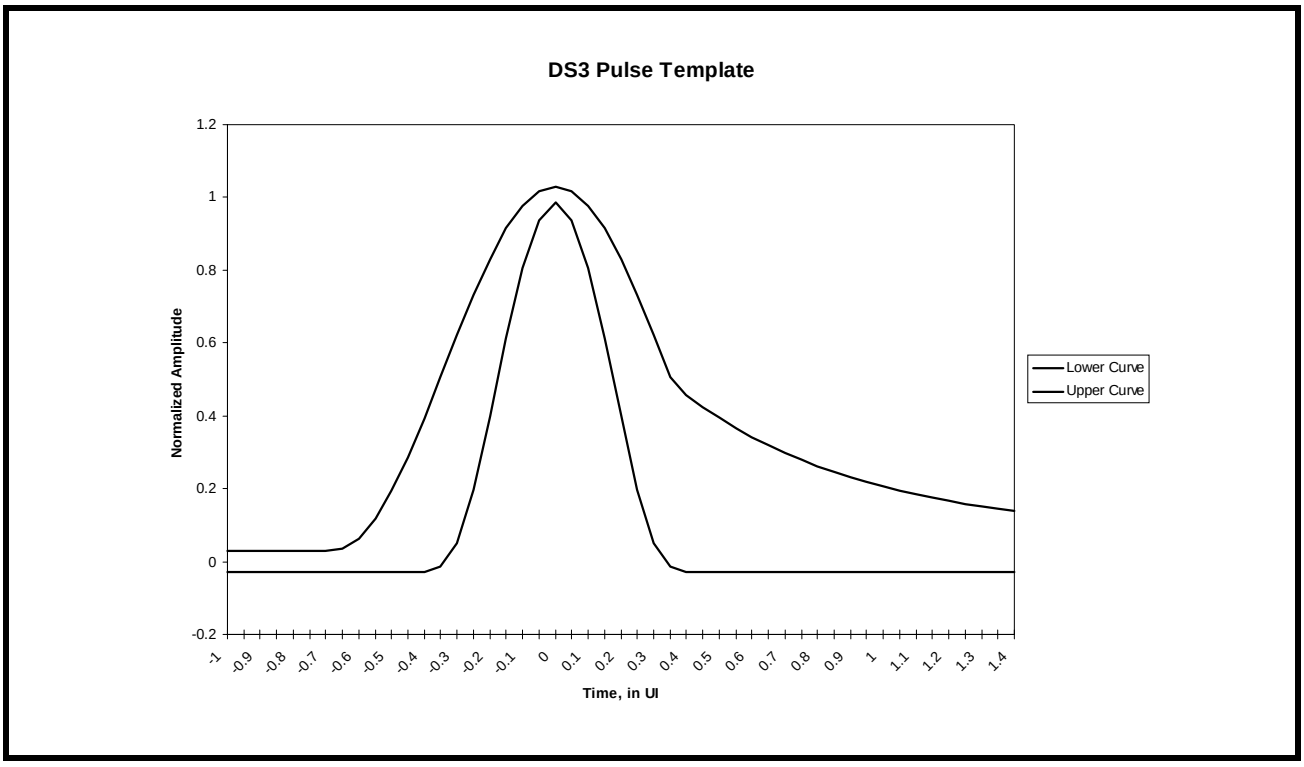


FIGURE 8. BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

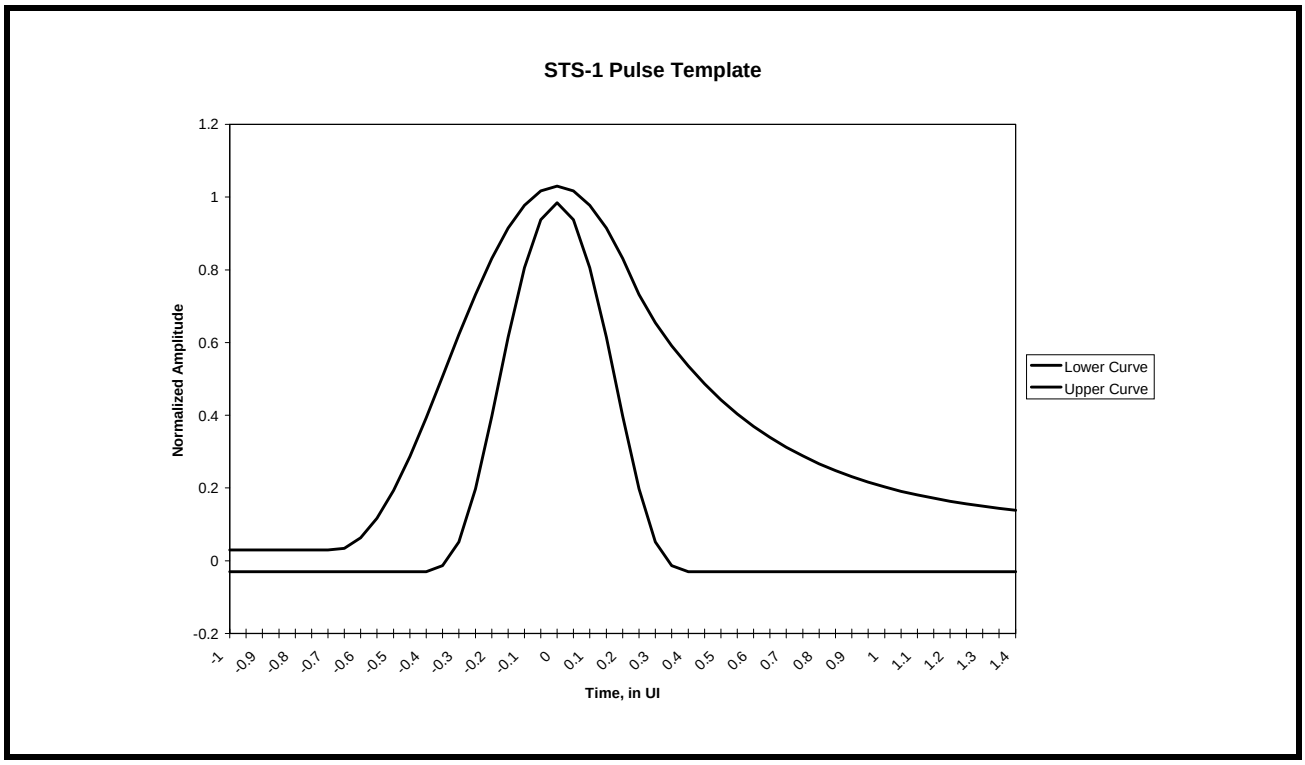
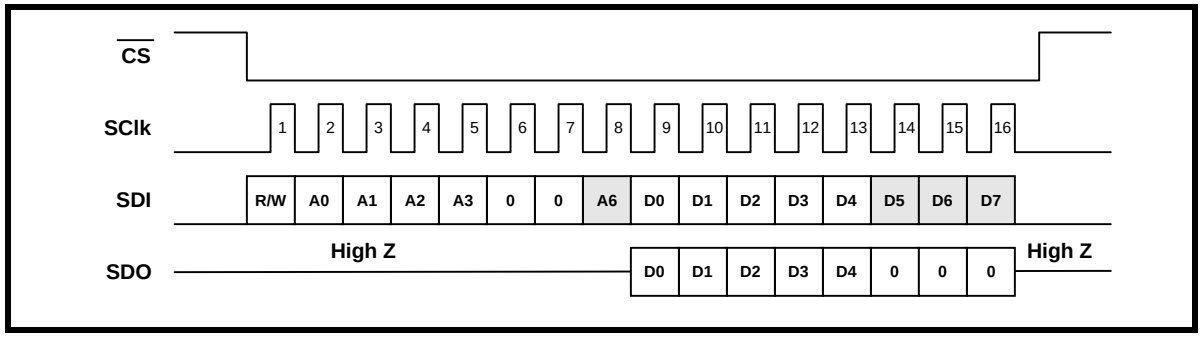


FIGURE 9. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



NOTES:

1. *A4 and A5 are always "0".*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*

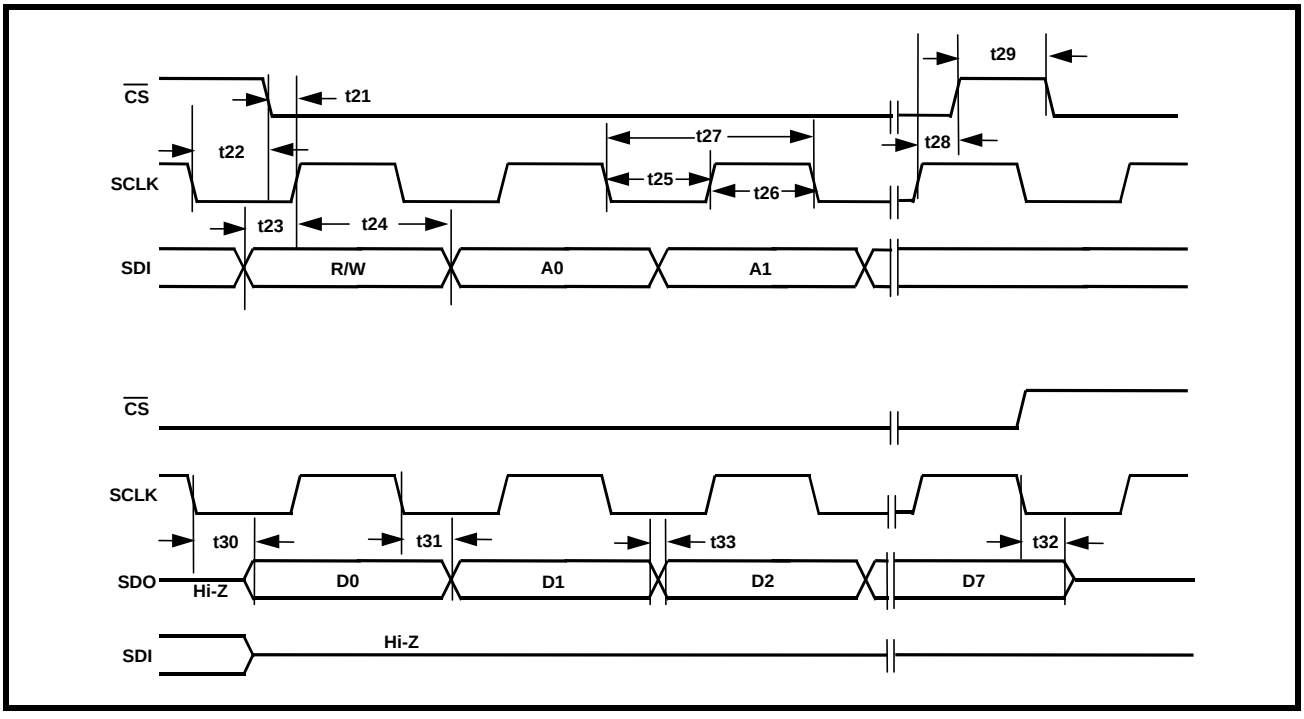
A shaded pulse, denotes a “don’t care” value.

AC ELECTRICAL CHARACTERISTICS (CONT.)

(T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Microprocessor Serial Interface Timing (see Figure 10)					
t_{21}	$\overline{CS}$ Low to Rising Edge of SCLK Setup Time	50			ns
t_{22}	$\overline{CS}$ High to Rising Edge of SCLK Hold Time	20			ns
t_{23}	SDI to Rising Edge of SCLK Setup Time	50			ns
t_{24}	SDI to Rising Edge of SCLK Hold Time	50			ns
t_{25}	SCLK “Low” Time	240			ns
t_{26}	SCLK “High” Time	240			ns
t_{27}	SCLK Period	500			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SCLK Hold Time	50			ns
t_{29}	$\overline{CS}$ Inactive Time	250			ns
t_{30}	Falling Edge of SCLK to SDO Valid Time			200	ns
t_{31}	Falling Edge of SCLK to SDO Invalid Time			100	ns
t_{32}	Falling Edge of SCLK or Rising Edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			40	ns

FIGURE 10. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



SYSTEM DESCRIPTION

A functional block diagram of the XRT73L00A E3/DS3/STS-1 Transceiver IC (see Figure 1) shows that the device contains three distinct sections:

- The Transmit Section
- The Receive Section
- The Microprocessor Serial Interface

THE TRANSMIT SECTION

The Transmit Section accepts TTL/CMOS level signals from the Terminal Equipment in either a Single-Rail or Dual-Rail format. The Transmit Section then takes this data and does the following:

- Encodes the data into the B3ZS format if the DS3 or SONET STS-1 Modes have been selected or into the HDB3 format if the E3 Mode has been selected.
- Converts the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements.
- Drives these pulses onto the line via the TTIP and TRING output pins across a 1:1 Transformer.

NOTE: *The Transmit Section drives a "1" (or a Mark) on the line by driving either a positive or negative polarity pulse across the 1:1 Transformer within a given bit period. The Transmit Section drives a "0" (or a Space) onto the line by driving no pulse onto the line.*

THE RECEIVE SECTION

The Receive Section receives a bipolar signal from the line either via a 1:1 Transformer or a 0.01mF Capacitor. As the Receive Section receives this line signal it does the following:

- Adjusts the signal level through an AGC circuit.
- Optionally equalizes this signal for cable loss.
- Attempts to quantify a bit-interval within the line signal as either a “1”, “-1” or a “0” by slicing this data. This sliced data is used by the Clock Recovery PLL to recover the timing element within the line signal.
- The sliced data is routed to the HDB3/B3ZS Decoder, during which the original data content as transmitted by the Remote Terminal Equipment is restored to its original content.
- Outputs the recovered clock and data to the Local Terminal Equipment in the form of CMOS level signals via the RPOS, RNEG, RCLK1 and RCLK2 output pins.

THE MICROPROCESSOR SERIAL INTERFACE

The XRT73L00A can be configured to operate in either the Hardware Mode or the HOST Mode.

The Hardware Mode

Connect the HOST/$\overline{HW}$ input pin (pin 18) to GND to configure the XRT73L00A to operate in the Hardware Mode.

When the XRT73L00A is operating in the Hardware Mode, the following is true:

1. The Microprocessor Serial Interface block is disabled.
2. The XRT73L00A is configured via input pin settings.

Each of the pins associated with the Microprocessor Serial Interface takes on their alternative role as defined in Table 1.

3. All of the remaining input pins become active.

TABLE 1: ROLE OF MICROPROCESSOR SERIAL INTERFACE PINS WHEN THE XRT73L00A IS OPERATING IN THE HARDWARE MODE

PIN #	PIN NAME	FUNCTION WHILE IN THE HARDWARE MODE
11	$\overline{REGRESET}$/(RCLK2INV)	RCLK2INV
19	SDI/(LOSMUTEN)	LOSMUTEN
20	SDO/(LCV)	LCV
21	SCLK/(ENDECDIS)	ENDECDIS
22	$\overline{CS}$/(DR/$\overline{SR}$)	DR/$\overline{SR}$
30	LCV/(RCLK2)	RCLK2

The HOST Mode

To configure the XRT73L00A to operate in the HOST Mode, connect the HOST/$\overline{HW}$ input pin (pin 18) to VDD.

When the XRT73L00A is operating in the HOST Mode, the following is true:

1. The Microprocessor Serial Interface block is enabled. Many configuration selections are made by writing the appropriate data into the on-chip Command Registers via the Microprocessor Serial Interface.
2. All of the following input pins are disabled:
   - Pin 1 - TXLEV
   - Pin 2 - TAOS
   - Pin 12 - REQDIS
   - Pin 14 - LLB
   - Pin 15 - RLB
   - Pin 16 - STS-1/$\overline{DS3}$
   - Pin 17 - E3
   - Pin 35 - TXOFF

Tie each of these pins to GND if the XRT73L00A IC is to be operated in the HOST Mode.

Please see Section 5.0 for a detailed description on operating the Microprocessor Serial Interface or the on-chip Command Registers.

1.0 SELECTING THE DATA RATE

The XRT73L00A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Selection of the data rate is dependent on whether the XRT73L00A is operating in the Hardware or HOST Mode.

TABLE 2: SELECTING THE DATA RATE FOR THE XRT73L00A VIA THE E3 AND STS-1/$\overline{DS3}$ INPUT PINS (HARDWARE MODE)

DATA RATE	STATE OF E3 PIN (PIN 17)	STATE OF STS-1/$\overline{DS3}$ PIN (PIN 16)	MODE OF B3ZS/HDB3 ENCODER/ DECODER BLOCKS
E3 (34.368 Mbps)	VDD	X (Don't Care)	HDB3
DS3 (44.736 Mbps)	0	0	B3ZS
STS-1 (51.84 Mbps)	0	VDD	B3ZS

A. When operating in the Hardware Mode.

To configure the XRT73L00A for the desired data rate, the E3 and the STS-1/$\overline{DS3}$ pins must be set to the appropriate logic states shown in Table 2.

B. When operating in the HOST Mode.

To configure the XRT73L00A for the desired data rate, appropriate values need to be written into the STS-1/$\overline{DS3}$ and E3 bit-fields in Command Register CR4.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$	E3	LLB	RLB
X	X	X	X	X

Table 3 relates the values of these two bit-fields with respect to the selected data rates.

TABLE 3: SELECTING THE DATA RATE FOR THE XRT73L00A VIA THE STS-1/$\overline{DS3}$ AND THE E3 BIT-FIELDS WITHIN COMMAND REGISTER CR4 (HOST MODE)

SELECTED DATA RATE	STS-1/$\overline{DS3}$	E3
E3	Don't Care	1
DS3	0	0
STS-1	1	0

The results of making these selections are:

1. The VCO Center Frequency of the Clock Recovery Phase-Locked-Loop is configured to match the selected data rate.
2. The B3ZS/HDB3 Encoder and Decoder blocks are configured to support B3ZS Encoding/Decoding if the DS3 or STS-1 data rates were selected or,
3. The B3ZS/HDB3 Encoder and Decoder blocks are configured to support HDB3 Encoding/ Decoding if the E3 data rate was selected.

4. The on-chip Pulse-Shaping circuitry is configured to generate Transmit Output pulses of the correct shape and width to meet the applicable pulse template requirement.
5. The LOS Declaration/Clearance Criteria is established.

2.0 THE TRANSMIT SECTION

Figure 1 indicates that the Transmit Section of the XRT73L00A consists of the following blocks:

- Transmit Logic Block
- Duty Cycle Adjust Block
- HDB3/B3ZS Encoder
- Pulse Shaping Block

The purpose of the Transmit Section in the XRT73L00A is to take TTL/CMOS level data from the terminal equipment and encode it into a format that can:

1. be efficiently transmitted over coaxial cable at E3, DS3 or STS-1 data rates.
2. be reliably received by the Remote Terminal at the other end of the E3, DS3 or STS-1 data link.
3. comply with the applicable pulse template requirements.

2.1 THE TRANSMIT LOGIC BLOCK

The purpose of the Transmit Logic Block is to accept either Dual-Rail or Single-Rail (a binary data stream) TTL/CMOS level data and timing information from the Terminal Equipment.

Accepting Dual-Rail Data from the Terminal Equipment

The XRT73L00A accepts Dual-Rail data from the Terminal Equipment via the following input signals:

- TPDATA
- TNDATA
- TCLK

Figure 11 illustrates the typical interface for the transmission of data in a Dual-Rail Format between the Terminal Equipment and the Transmit Section of the XRT73L00.

FIGURE 11. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL-RAIL FORMAT FROM THE TRANSMITTING TERMINAL EQUIPMENT TO THE TRANSMIT SECTION OF THE XRT73L00

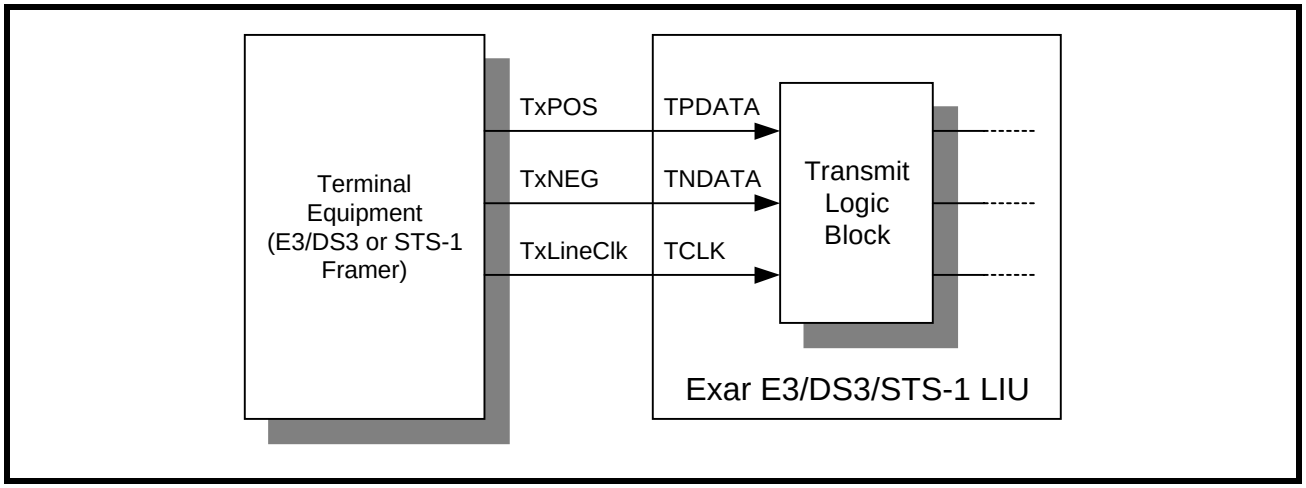
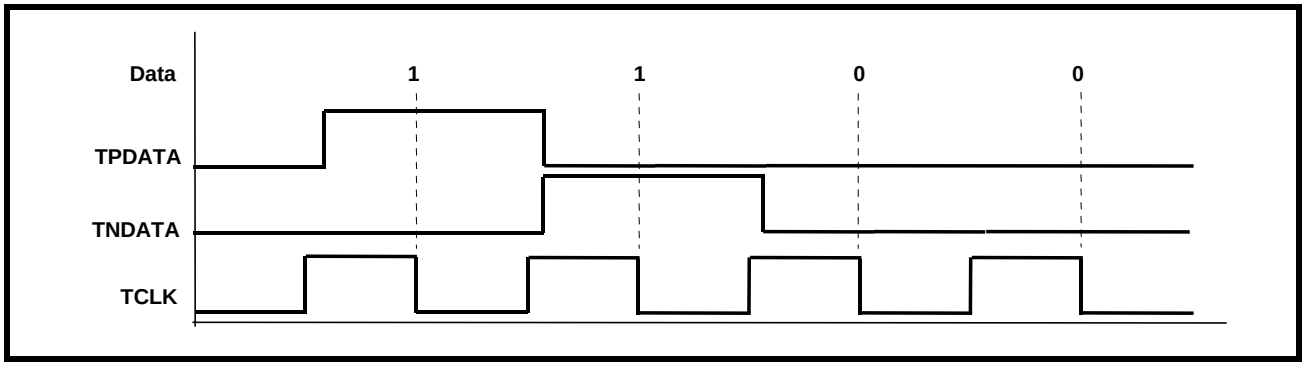


FIGURE 12. HOW THE XRT73L00A SAMPLES THE DATA ON THE TPDATA AND TNDATA INPUT PINS



The manner that the LIU handles Dual-Rail data is described below and illustrated in Figure 12. The XRT73L00A typically samples the data on the TPDATA and TNDATA input pins on the falling edge of TCLK.

TCLK is typically a clock signal that is of the selected data rate frequency. For the E3 data rate, TCLK is 34.368 MHz. For the DS3 data rate, TCLK is 44.736 MHz and for the SONET STS-1 rate, TCLK is 51.84 MHz. In general, if the XRT73L00A samples a "1" on the TPDATA input pin, the Transmit Section of the device ultimately generates a positive polarity pulse via the TTIP and TRING output pins across a 1:1 transformer. If the XRT73L00A samples a "1" on the TNDATA input pin, the Transmit Section of the device ultimately generates a negative polarity pulse via the TTIP and TRING output pins across a 1:1 transformer.

2.1.1 Accepting Single-Rail Data from the Terminal Equipment

Do the following if data is to be transmited from the Terminal Equipment to the XRT73L00A in Single-Rail format (a binary data stream) without having to convert it into a Dual-Rail format.

A. Configure the XRT73L00A to operate in the HOST Mode or,

B. access the Microprocessor Serial Interface and write a "1" into the TXBIN (TRANSMIT BINary) bit-field in Command Register 1.

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
X	X	X	X	1

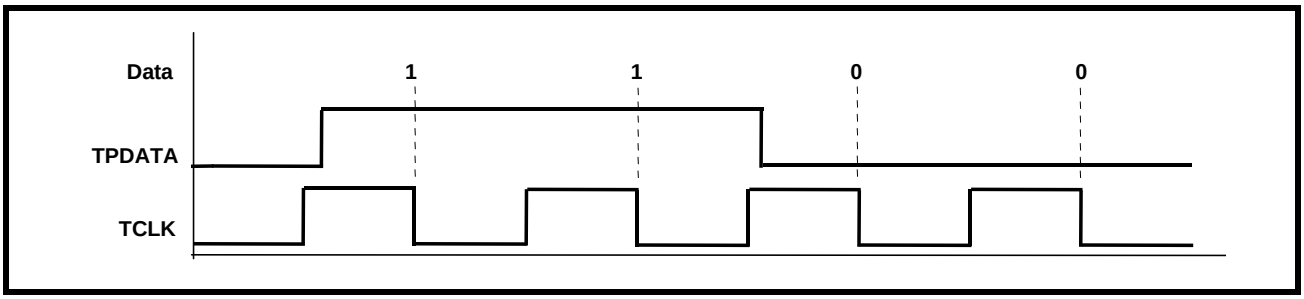
After taking these steps, the Transmit Logic Block accepts Single-Rail data via the TPDATA input pin. The XRT73L00A samples this input pin on the falling edge of the TCLK clock signal and encodes it into the appropriate bipolar line signal across the TTIP and TRING output pins.

NOTES:

1. *In this mode the Transmit Logic Block ignores the TNDATA input pin.*
2. *If the Transmit Section of the XRT73L00A is configured to accept Single-Rail data from the Terminal Equipment, the B3ZS/HDB3 Encoder must be enabled.*

Figure 13 illustrates the behavior of the TPDATA and TCLK signals when the Transmit Logic Block has been configured to accept Single-Rail data from the Terminal Equipment.

FIGURE 13. THE BEHAVIOR OF THE TPDATA AND TCLK INPUT SIGNALS WHILE THE TRANSMIT LOGIC BLOCK IS ACCEPTING SINGLE-RAIL DATA FROM THE TERMINAL EQUIPMENT



2.2 THE TRANSMIT CLOCK DUTY CYCLE ADJUST CIRCUITRY

The on-chip Pulse-Shaping circuitry in the Transmit Section of the XRT73L00A has the responsibility for generating pulses of the shape and width to comply with the applicable pulse template requirement. The widths of these output pulses are defined by the width of the half-period pulses in the TCLK signal.

Allowing the widths of the pulses in the TCLK clock signal to vary significantly could jeopardize the chip's ability to generate Transmit Output pulses of the appropriate width, thereby failing the applicable Pulse Template Requirement Specification. The chips ability to generate compliant pulses could depend upon the duty cycle of the clock signal applied to the TCLK input pin.

In order to combat this phenomenon, the Transmit Clock Duty Cycle Adjust circuit was designed into the XRT73L00. The Transmit Clock Duty Cycle Adjust Circuitry is a PLL that was designed to accept clock pulses via the TCLK input pin at duty cycles ranging from 30% to 70% and to regenerate these signals with a 50% duty cycle.

The XRT73L00A Transmit Clock Duty Cycle Adjust circuit alleviates the need to supply a signal with a 50% duty cycle to the TCLK input pin.

2.3 THE HDB3/B3ZS ENCODER BLOCK

The purpose of the HDB3/B3ZS Encoder Block is to aid in the Clock Recovery process at the Remote Terminal Equipment by ensuring an upper limit on the number of consecutive zeros that can exist in the line signal.

2.3.1 B3ZS Encoding

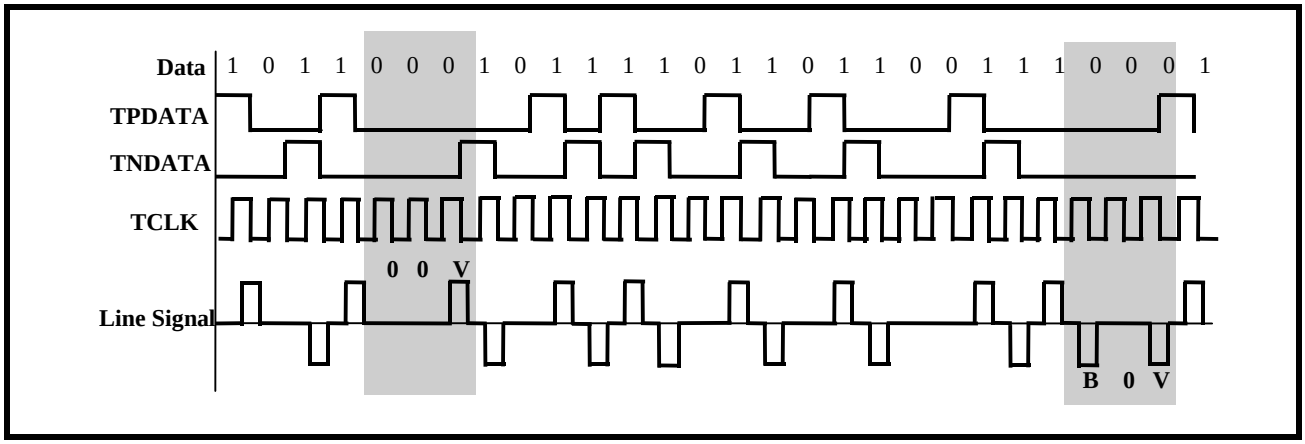
If the XRT73L00A is configured to operate in the DS3 or SONET STS-1 Modes, then the HDB3/B3ZS Encoder block operates in the B3ZS Mode. When the Encoder is operating in this mode, it parses through and searches the Transmit Binary Data Stream from the Transmit Logic Block for the occurrence of three (3) consecutive zeros (“000”). If the B3ZS Encoder finds an occurrence of three consecutive zeros, it substitutes these three “0’s” with either a "00V" or a "B0V" pattern.

“B” represents a Bipolar pulse that is compliant with the Alternating Polarity requirements of the AMI (Alternate Mark Inversion) line code and “V” represents a bipolar Violation (e.g., a bipolar pulse that violates the Alternating Polarity requirements of the AMI line code).

The B3ZS Encoder decides whether to substitute with either a "00V" or a "B0V" pattern to insure that an odd number of bipolar pulses exist between any two consecutive violation pulses.

Figure 14 illustrates the B3ZS Encoder at work with two separate strings of three (or more) consecutive zeros.

FIGURE 14. AN EXAMPLE OF B3ZS ENCODING

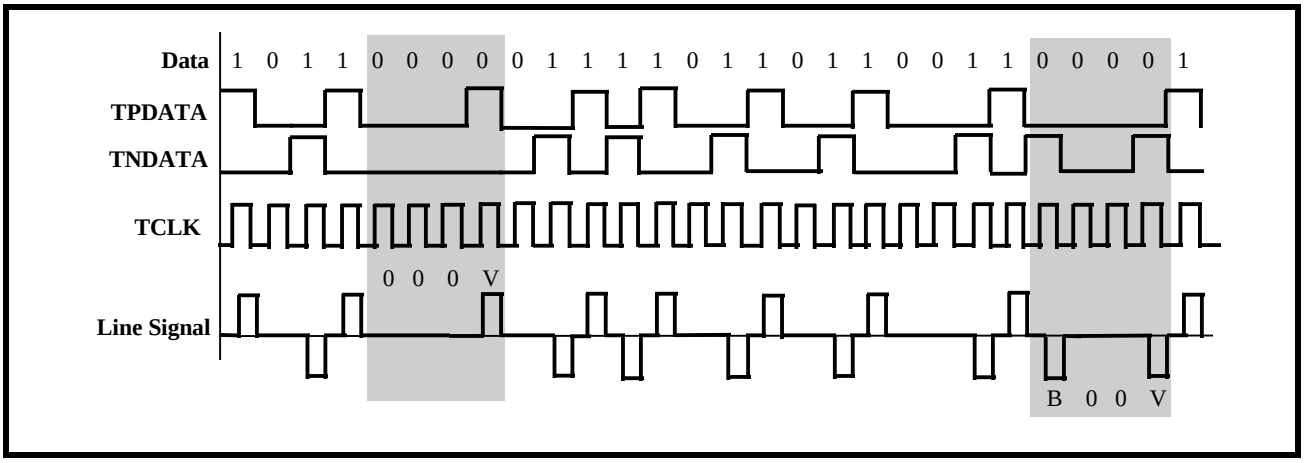


2.3.2 HDB3 Encoding

If the XRT73L00A is configured to operate in the E3 Mode, then the HDB3/B3ZS Encoder block operates in the HDB3 Mode. When the Encoder is operating in this mode, it parses through and searches the Transmit Data Stream from the Transmit Logic Block for the occurrence of four (4) consecutive zeros (“0000”). If the HDB3 Encoder finds an occurrence of four consecutive zeros, then it substitutes these four “0’s” with either a “000V” or a “B00V” pattern to insure that an odd number of bipolar pulses exist between any two consecutive violation pulses.

Figure 15 illustrates the HDB3 Encoder at work with two separate strings of four (or more) consecutive zeros.

FIGURE 15. AN EXAMPLE OF HDB3 ENCODING



2.3.3 Enabling/Disabling the HDB3/B3ZS Encoder

The XRT73L00A allows two methods to enable or disable the HDB3/B3ZS Encoder.

If the XRT73L00A is operating in the Hardware Mode.

To enable the HDB3/B3ZS Encoder, set the ENDECDIS input pin (pin 21) to “0”. To disable the HDB3/B3ZS Encoder, set the ENDECDIS input pin (pin 21) to “1”.

If the XRT73L00A is operating in the HOST Mode.

To enable the HDB3/B3ZS Encoder, set the ENDECDIS bit-field in Command Register (CR2) to “0”.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
X	0	X	X	X

To disable the HDB3/B3ZS Encoder, set the ENDECDIS bit-field in Command Register (CR2) to “1”.

If either of these two methods is employed to disable the HDB3/B3ZS Encoder, the LIU transmits the data onto the line as it is received via the TPDATA and TNDATA input pins.

2.4 THE TRANSMIT PULSE SHAPER CIRCUITRY

The Transmit Pulse Shaper Circuitry consists of a Transmit Line Build-Out circuit which can be enabled or disabled by setting the TXLEV input pin or bit-field to “High” or “Low”. The purpose of the Transmit Line Build-Out circuit is to permit configuring of the XRT73L00A to transmit an output pulse which is compliant to either of the following Bellcore pulse template requirements when measured at the Digital Cross Connect System. Each of these Bellcore specifications further state that the cable length between the Transmit Output and the Digital Cross Connect system can range anywhere from 0 to 450 feet.

The Isolated DSX-3 Pulse Template Requirement per Bellcore GR-499-CORE is illustrated in Figure 7.

The Isolated STSX-1 Pulse Template Requirement per Bellcore GR-253-CORE is illustrated in Figure 8.

2.4.1 Enabling the Transmit Line Build-Out Circuit

If the Transmit Line Build-Out Circuit is enabled, the XRT73L00A outputs shaped pulses onto the line via the TTIP and TRING output pins.

Do the following to enable the Transmit Line Build-Out circuit in the XRT73L00:

- If the XRT73L00A is operating in the Hardware Mode, set theTXLEV input pin (pin 1) to “Low”
- If the XRT73L00A is operating in the HOST Mode, set the TXLEV bit-field to “0” as illustrated below.

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
0	X	X	0	X

2.4.2 Disabling the Transmit Line Build-Out Circuit

If the Transmit Line Build-Out circuit is disabled, then the XRT73L00A outputs partially-shaped pulses onto the line via the TTIP and TRING output pins.

Disable the Transmit Line Build-Out circuit in the XRT73L00A by doing the following:

- If the XRT73L00A is operating in the Hardware Mode, set the TXLEV input pin (pin 1) to “High”
- If the XRT73L00A is operating in the HOST Mode, set the TXLEV bit-field to “1” as illustrated below.

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
0	X	X	1	X

2.4.3 Design Guideline for Setting the Transmit Line Build-Out Circuit

The setting ofTXLEV input pin or bit-field should be based upon the overall cable length between the Transmitting Terminal and the Digital Cross Connect system where the pulse template measurements are made.

If the cable length between the Transmitting Terminal and the DSX-3 or STSX-1 is less than 225 feet, it is advisable to enable the Transmit Line Build-Out circuit by setting the TXLEV input pin or bit-field to "0".

NOTE: *In this case the XRT73L00A outputs shaped (e.g., not square-wave) pulses onto the line via the TTIP and TRING output pins. The shape of this output pulse is such that it complies with the pulse template requirements even when subjected to cable loss ranging from 0 to 225 feet.*

If the cable length between the Transmitting Terminal and the DSX-3 or STSX-1 is greater than 225 feet, it is advisable to disable the Transmit Line Build-Out circuit by setting the TXLEV input pin or bit-field to "1".

NOTE: *In this case the XRT73L00A outputs partially-shaped pulses onto the line via the TTIP and TRING output pins. The cable loss that these pulses experience over long cable lengths (e.g., greater than 225 feet) causes these pulses to be properly shaped and comply with the appropriate pulse template requirement.*

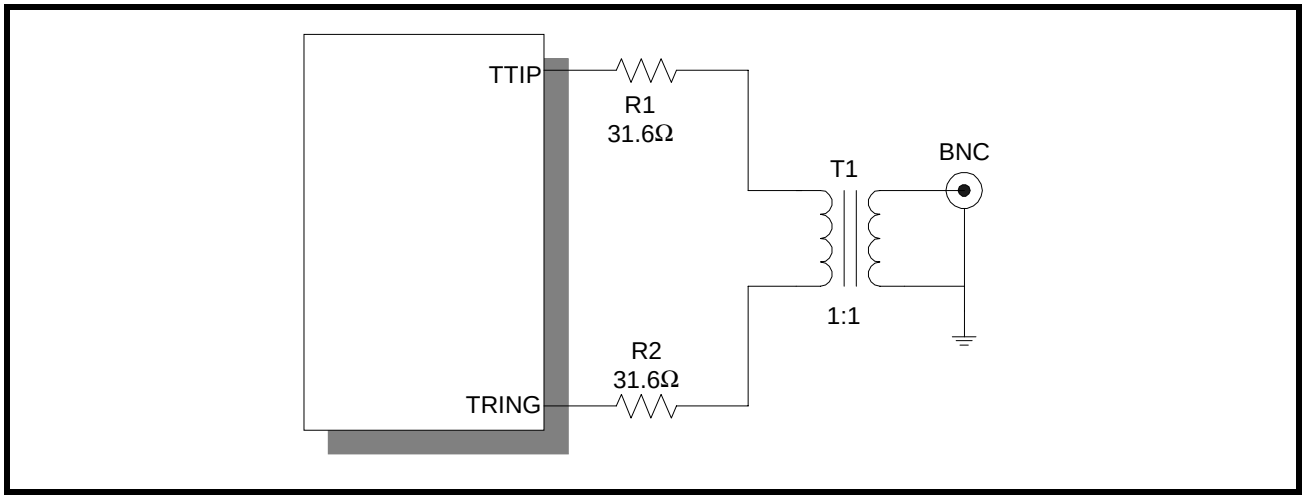
2.4.4 The Transmit Line Build-Out Circuit and E3 Applications

The ITU-T G.703 Pulse Template Requirements for E3 states that the E3 transmit output pulse should be measured at the Secondary Side of the Transmit Output Transformer for Pulse Template compliance. There is no Digital Cross Connect System pulse template requirement for E3 and the Transmit Line Build-Out circuit in the XRT73L00A is disabled whenever it is operating in the E3 Mode.

2.5 INTERFACING THE TRANSMIT SECTION OF THE XRT73L00A TO THE LINE

The E3, DS3 and SONET STS-1 specification documents all state that line signals transmitted over coaxial cable are to be terminated with 75 Ohms. Therefore, interface the Transmit Section of the XRT73L00, as illustrated in Figure 16 which shows two 31.6 Ohm resistors in series with the primary side of the transformer. These two 31.6Ohm resistors closely match the 75Ohm load termination resistor thereby minimizing Transmit Return Loss.

FIGURE 16. RECOMMENDED SCHEMATIC FOR INTERFACING THE TRANSMIT SECTION OF THE XRT73L00A TO THE LINE



TRANSFORMER RECOMMENDATIONS

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	40µH
Isolation Voltage	1500Vrms
Leakage Inductance	0.6µH

PART NUMBER	VENDOR	INSULATION	PACKAGE TYPE
PE-68629	Pulse	3000V	Large Thru-Hole
PE-65966	Pulse	1500V	Small Thru-Hole
PE-65967	Pulse	1500V	Small SMT
T3001	Pulse	1500V	Small SMT
TG01-0406NS	Halo	1500V	Small SMT
TTI 7601-SM	Trans-Power	1500V	Small SMT

TRANSFORMER VENDOR INFORMATION

Pulse

Corporate Office

12220 World Trade Drive
San Diego, CA 92128
Tel: (858)-674-8100
FAX: (858)-674-8262

Europe

1 & 2 Huxley Road
The Surrey Research Park
Guildford, Surrey GU2 5RE
United Kingdom
Tel: 44-1483-401700
FAX: 44-1483-401701

Asia

150 Kampong Ampat
#07-01/02
KA Centre
Singapore 368324
Tel: 65-287-8998
FAX: 65-280-0080

Website: http://www.pulseeng.com

Halo Electronics

Corporate Office

P.O. Box 5826
Redwood City, CA 94063
Tel: (650)568-5800
FAX: (650)568-6165

Email: info@haloelectronics.com

Website: http://www.haloelectronics.com

Transpower Technologies, Inc.

Corporate Office

Park Center West Building
9805 Double R Blvd, Suite # 100
Reno, NV 89511
(800)500-5930 or (775)852-0140

Email: info@trans-power.com

Website: http://www.trans-power.com

3.0 THE RECEIVE SECTION

Figure 1 indicates that the XRT73L00A Receive Section consists of the following blocks:

- AGC/Equalizer
- Peak Detector
- Slicer
- Clock Recovery PLL
- Data Recovery
- HDB3/B3ZS Decoder

The purpose of the XRT73L00A Receive Section is to take an incoming attenuated/distorted bipolar signal from the line and encode it back into the TTL/CMOS format where it can be received and processed by digital circuitry in the Terminal Equipment.

3.1 INTERFACING THE RECEIVE SECTION OF THE XRT73L00A TO THE LINE

By design, the Receive Section of the XRT73L00A can be transformer-coupled or capacitive-coupled to the line. The specification documents for E3, DS3 and STS-1 all specify 75Ohm termination loads when transmitting over coaxial cable. It is recommended to interface the Receive Section of the XRT73L00A to the line as shown in Figure 17 or Figure 18.

FIGURE 17. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTION OF THE XRT73L00A TO THE LINE (TRANSFORMER-COUPLING)

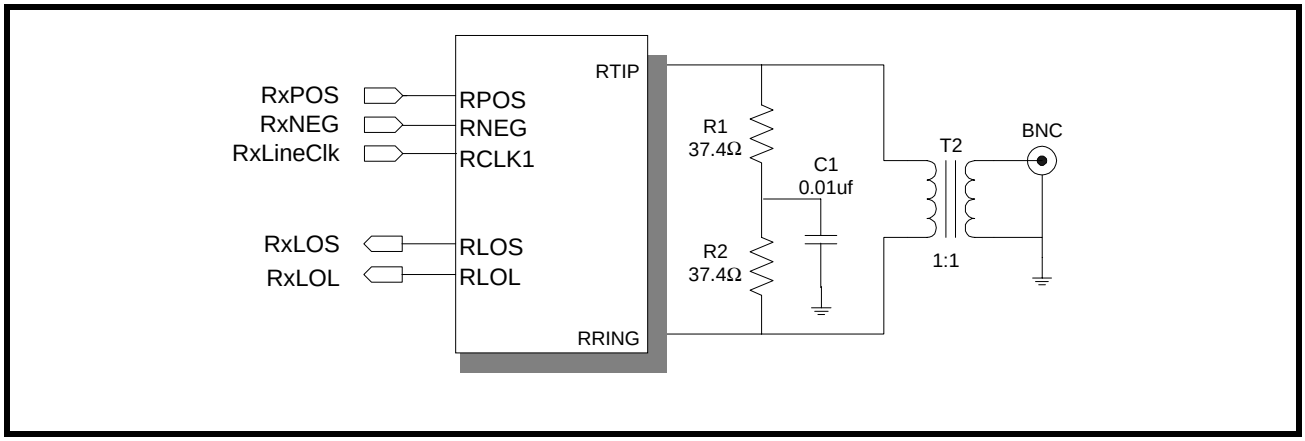
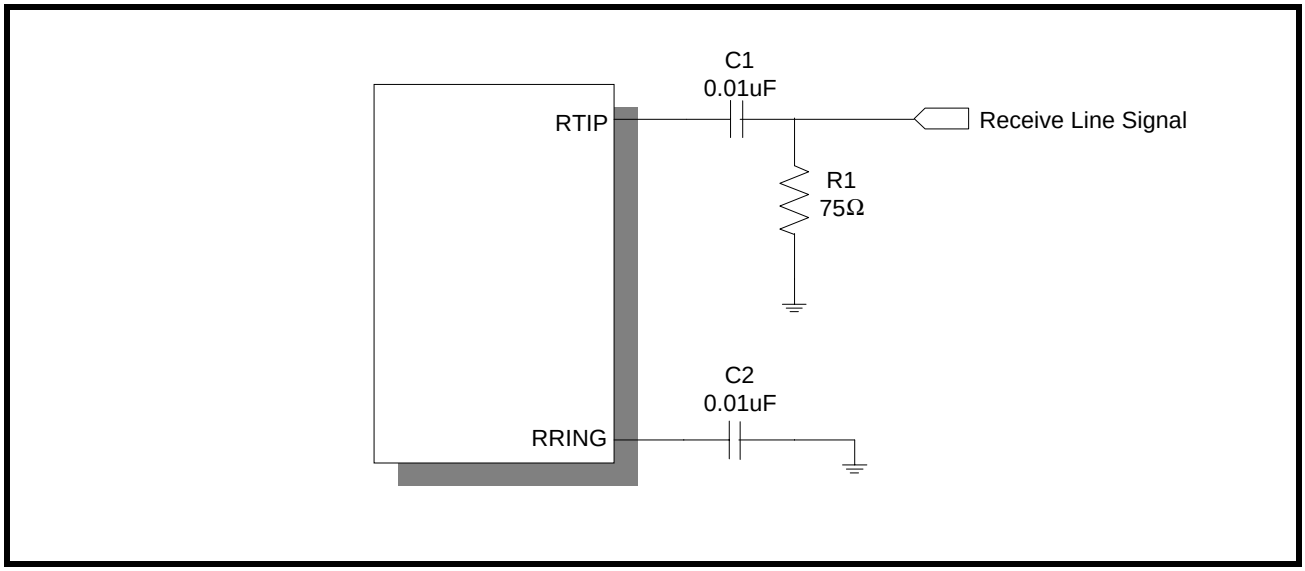


FIGURE 18. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTION OF THE XRT73L00A TO THE LINE (CAPACITIVE-COUPLING)



3.2 THE RECEIVE EQUALIZER BLOCK

After the XRT73L00A has received the incoming line signal via the RTIP and RRING input pins, the first block that this signal passes through is the AGC (Automatic Gain Control) circuit followed by the Receive Equalizer.

As the line signal is transmitted from a given transmitting terminal, the pulse shapes at that location are basically square. These pulses consist of a combination of “Low” and “High” frequency Fourier components. As this line signal travels from the transmitting terminal via the coaxial cable to the receiving terminal, it is subjected to frequency-dependent loss. The higher-frequency components of the signal is subjected to a greater amount of attenuation than the lower-frequency components. If this line signal travels over reasonably long cable lengths (e.g., greater than 450 feet), then the shape of the pulses which were originally square is distorted and inter-symbol interference increases.

The purpose of the Receive Equalizer is to equalize the distortion of the incoming signal due to cable loss. The Receive Equalizer accomplishes this by subjecting the received line signal to frequency-dependent amplification which attempts to counter the frequency dependent loss that the line signal has experienced and to restore the shape of the line signal so that the transmitted data and clock can be recovered reliably.

3.2.1 Guidelines for Setting the Receive Equalizer

This data sheet presents guidelines for setting the Receive Equalizer, for the following conditions.

1. If the overall cable length from the local Receiving Terminal to the remote Transmitting Terminal is NOT known.
2. If the overall cable length from the local Receiving Terminal to the remote Transmitting Terminal is known.

3.2.1.1 If the Overall Cable Length is NOT Known

This section presents recommendations on what state to set the Receive Equalizer when the overall cable-length from the local Receiving Terminal to the remote Transmitting Terminal is NOT known. For DS3, STS-1 and E3 applications, enable the Receive Equalizer by setting either the REQDIS input pin “low” or the REQDIS bit-field to “0”. The remainder of this section provides an explanation why we recommend enabling the Receive Equalizer for these applications.

3.2.1.1.1 The Use of the Receive Equalizer in a Typical DS3 or STS-1 Application

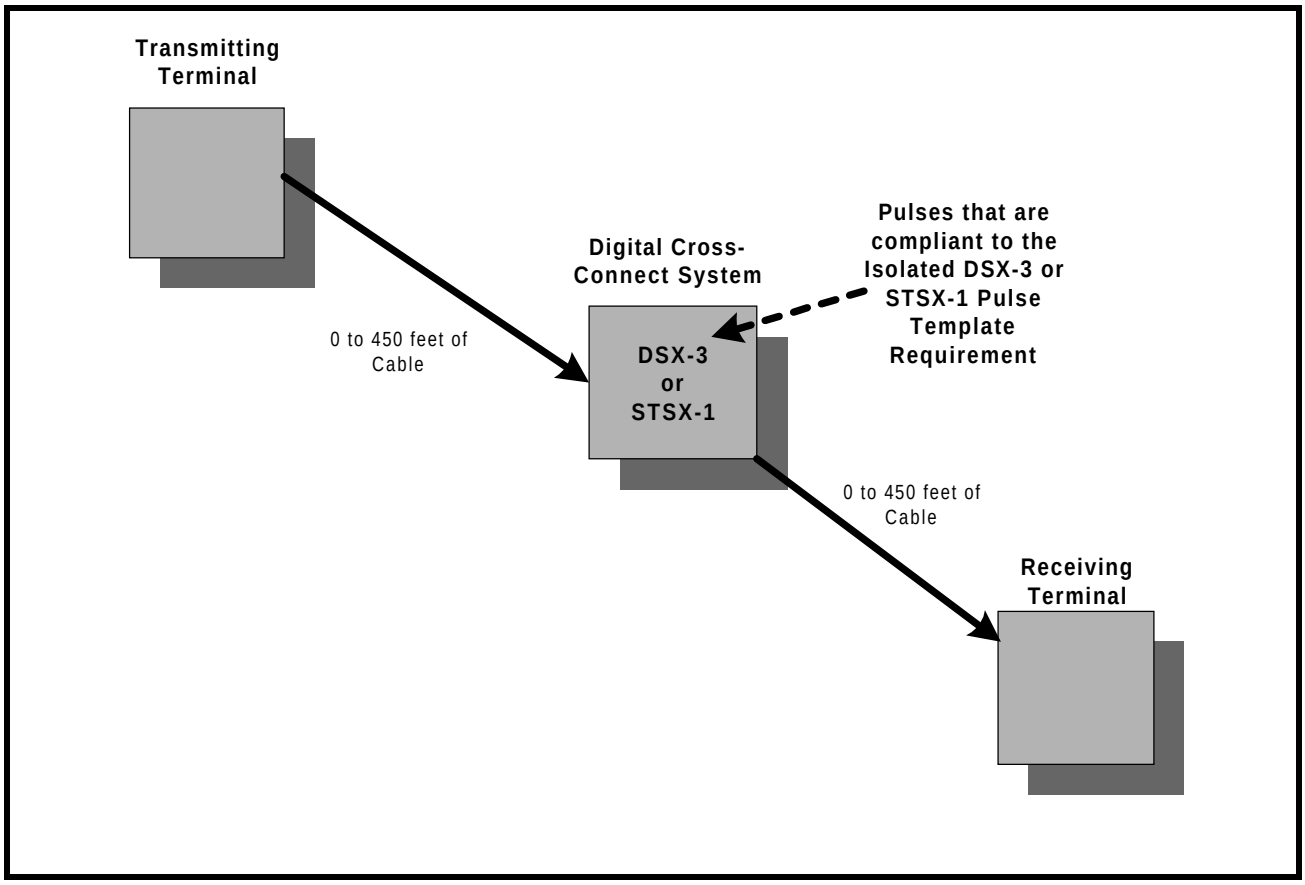
Most System Manufacturers of equipment supporting DS3 and STS-1 lines interface their equipment to either a DSX-3 or STSX-1 Cross-Connect. While installing their equipment the Transmit Line Build-Out circuit is set to the proper setting that makes the transmit output pulse compliant with the Isolated DSX-3 or STSX-1 Pulse Template requirements. For the XRT73L00A this is achieved by setting the TXLEV input pin or bit-field to the appropriate level.

When the System Manufacturer is interfacing the Receive Section of the XRT73L00A to the Cross-Connect, they should keep aware of the following facts:

1. All DS3 or STS-1 line signals that are present at either the DSX-3 or the STSX-1 Cross-Connect are required to meet the Isolated Pulse Template Requirements per Bellcore GR-499-CORE for DS3 applications or Bellcore GR-253-CORE for STS-1 applications.
2. Bellcore documents state that the amplitude of these pulses at the DSX-3 or STSX-1 can range in amplitude from 360mVpk to 850mVpk.
3. Bellcore documents stipulate that the Receiving Terminal must be able to receive this pulse-template compliant line signal over a cable length of 0 to 450 feet from the DSX-3 or the STSX-1 Cross Connect.

These facts are reflected in Figure 19.

FIGURE 19. THE TYPICAL APPLICATION FOR THE SYSTEM INSTALLER



Design Considerations for DS3 and STS-1 Applications

When installing equipment into environments as depicted in Figure 18, the system installation personnel may be able to determine the cable length between the local terminal equipment and the DSX-3/STSX-1 Cross-Connect Patch-Panel. The cable length between the local terminal equipment and the DSX-3/ STSX-1 Cross-Connect Patch Panel ranges between 0 and 450 feet.

It is extremely unlikely that the system installation personnel will know the cable length between the DSX-3/STSX-1 Cross-Connect Patch-Panel and the remote terminal equipment. We recommend that the Receive Equalizer be enabled by setting the REQDIS input pin or bit-field to "0".

The only time the Receive Equalizer should be disabled is when there is an off-chip equalizer in the Receive path between the DSX-3/STSX-1 Cross-Connect and the RTIP/RRING input pins or, in applications where the Receiver is monitoring the transmit output signal directly.

3.2.1.1.2 Design Considerations for E3 Applications

In E3 system installation, it is recommended that the Receive Equalizer of the XRT73L00A be enabled by pulling the REQDIS input pin to GND or by setting the REQDIS bit-field to “0”.

NOTE: *The results of extensive testing indicates that when the Receive Equalizer is enabled, the XRT73L00A is capable of receiving an E3 line signal with anywhere from 0 to 12dB of cable loss over the Industrial Temperature range.*

Design Considerations if the Overall Cable Length is known

If during system installation the overall cable length is known, then in order to optimize the performance of the XRT73L00A in terms of receive intrinsic jitter, etc., the Receive Equalizer should be enabled or disabled based upon the following recommendations:

The Receive Equalizer should be turned ON if the Receive Section is going to receive a line signal with an overall cable length of 300 feet or greater. The Receive Equalizer should be turned OFF if the Receive Section is going to receive a line signal over a cable length of less than 300 feet.

NOTES:

1. *If the Receive Equalizer block is turned ON in a given Receive Section that is receiving a line signal over short cable length, there is the risk of over-equalizing the received line signal which could degrade performance by increasing the amount of jitter that exists in the recovered data and clock signals or by creating bit-errors.*
2. *The Receive Equalizer has been designed to counter the frequency-dependent cable loss that a line signal experiences as it travels from the Transmitting Terminal to the Receiving Terminal. However, Receive Equalizer was not designed to counter flat loss where all of the Fourier frequency components in the line signal are subject to the same amount of attenuation. Flat loss is handled by the AGC block.*

The Receive Equalizer block can be disabled setting the REQDIS input pin "High" when operating in the Hardware Mode or writing a "1" to the REQDIS bit-field in Command Register CR2 when operating the XRT73L00A in the HOST Mode.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
X	X	X	X	1

3.3 PEAK DETECTOR AND SLICER

After the incoming line signal has passed through the Receive Equalizer, it is routed to the Slicer block. The purpose of the Slicer is to quantify a given bit-period or symbol within the incoming line signal as either a "1" or a "0".

3.4 CLOCK RECOVERY PLL

The output of the Slicer, which is now Dual-Rail digital pulses, is routed to the Clock Recovery PLL. The purpose of the Clock Recovery PLL is to track the incoming Dual-Rail data stream and to derive and generate a recovered clock signal.

It is important to note that the Clock Recovery PLL requires a line rate clock signal at the EXCLK input pin.

The Clock Recovery PLL operates in one of two modes:

- The Training Mode.
- The Data/Clock Recovery Mode

1. The Training Mode

If the XRT73L00A is not receiving a line signal via the RTIP and RRING input pins or if the frequency difference between the line signal and that applied via the EXCLK input pin exceeds 0.5%, then the XRT73L00A LIU IC is operating in the Training Mode. When the LIU is operating in the Training Mode it does the following:

A. declares a Loss of Lock indication by toggling the RLOL output pin "High" and

B. outputs a clock signal via the RCLK1 and RCLK2 output pins which is derived from the signal applied to the EXCLK input pin.

2. The Data/Clock Recovery Mode

If the frequency difference between the line signal and that applied via the EXCLK input pin is less than 0.5%, the XRT73L00A LIU IC is operating in the Data/Clock Recovery Mode. In this mode, the Clock Recovery PLL is locked onto the line signal via the RTIP and RRING input pins.

3.5 THE HDB3/B3ZS DECODER

The Remote Transmitting Terminal typically encodes the line signal into some sort of Zero Suppression Line Code (e.g., HDB3 for E3 and B3ZS for DS3 and STS-1). The purpose of this encoding activity was to aid in the Clock Recovery process of this data in the Near-End Receiving Terminal. Once the data has made it across the E3, DS3 or STS-1 Transport Medium and has been recovered by the Clock Recovery PLL, it is now necessary to restore the original content of the data. The purpose of the HDB3/B3ZS Decoding block is to restore the data transmitted over the E3, DS3 or STS-1 line to its original content prior to Zero Suppression encoding.

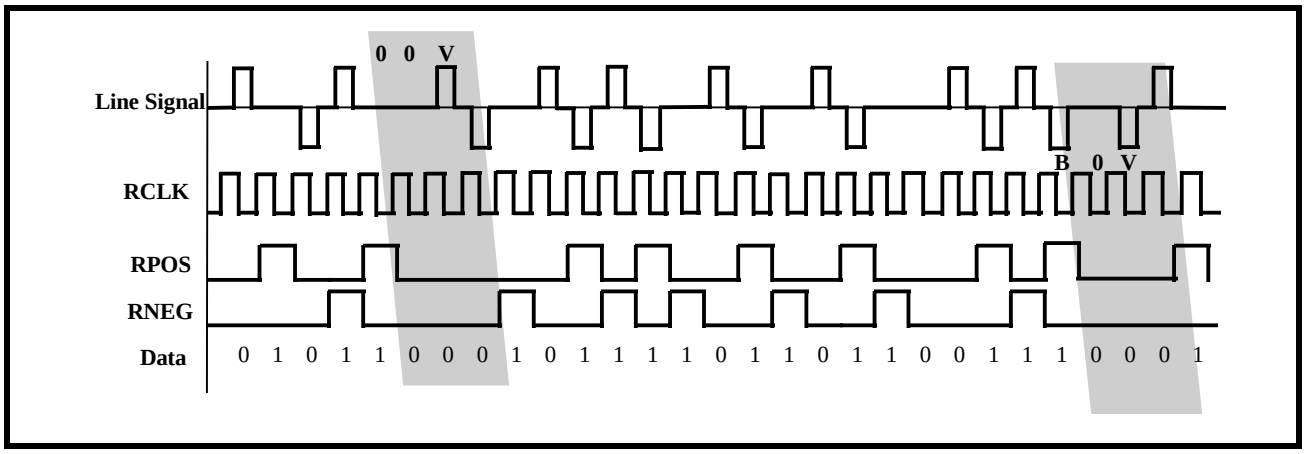
3.5.1 B3ZS Decoding DS3/STS-1 Applications

If the XRT73L00A is configured to operate in the DS3 or STS-1 Modes, then the HDB3/B3ZS Decoding Block performs B3ZS Decoding. When the Decoder is operating in this mode it parses through the incoming Dual-Rail data and checks for the occurrence of either a "00V" or a "B0V" pattern. If the B3ZS Decoder detects this particular pattern it substitutes these bits with a "000" pattern.

NOTE: *If the B3ZS Decoder detects any bipolar violations that is not in accordance with the"B3ZS Line Code" format, or if the B3ZS Decoder detects a string of 3 (or more) consecutive "0's" in the incoming line signal, then the B3ZS Decoder flags this event as a Line Code Violation by pulsing the LCV output pin "High".*

Figure 20 illustrates the B3ZS Decoder at work with two separate Zero Suppression patterns in the incoming Dual-Rail Data Stream.

FIGURE 20. AN EXAMPLE OF B3ZS DECODING

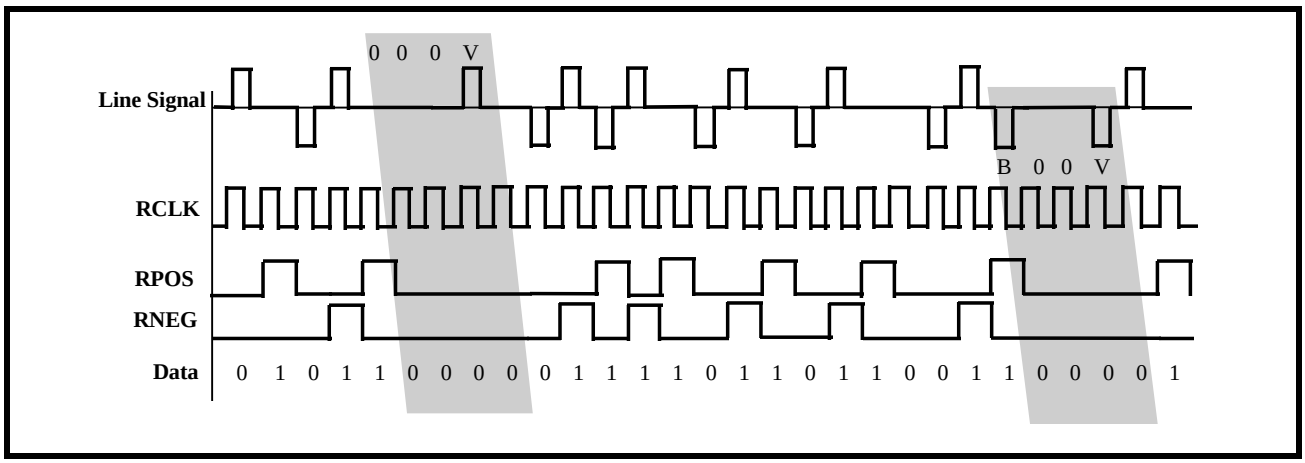


3.5.2 HDB3 Decoding E3 Applications

If the XRT73L00A is configured to operate in the E3 Mode, the HDB3/B3ZS Decoding Block performs HDB3 Decoding. When the Decoder is operating in this mode it parses through the incoming Dual-Rail data and checks for the occurrence of either a "000V" or a "B00V" pattern. If the HDB3 Decoder detects this particular pattern, it substitutes these bits with a "0000" pattern.

Figure 21 illustrates the HDB3 Decoder at work with two separate Zero Suppression patterns in the incoming Dual-Rail Data Stream.

FIGURE 21. AN EXAMPLE OF HDB3 DECODING



NOTE: If the HDB3 Decoder detects any bipolar violation (e.g., "V") pulses that is not in accordance with the HDB3 Line Code format, or if the HDB3 Decoder detects a string of 4 (or more) "0's" in the incoming line signal, then the HDB3 Decoder flags this event as a Line Code Violation by pulsing the LCV output pin "High".

3.5.3 Enabling/Disabling the HDB3/B3ZS Decoder

The HDB3/B3ZS Decoder of the XRT73L00A can be enabled or disabled by either of the following means:

If the XRT73L00A is operating in the Hardware Mode:

Encoder/Decoder, write a "1" into the ENDECDIS bit-Enable the HDB3/B3ZS Encoder/Decoder by pulling the ENDECDIS input pin (pin 21) to GND. To disable the HDB3/B3ZS Encoder/Decoder, pull the ENDECDIS input pin to VDD.

If the XRT73L00A is operating in the HOST Mode:

Enable the XRT73L00A HDB3/B3ZS Encoder/Decoder by writing a "0" into the ENDECDIS bit-field in Command Register CR2. To disable the HDB3/B3ZS

field.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
X	0	X	X	X

3.6 LOS Declaration/Clearance

The XRT73L00A contains circuitry that monitors the following two parameters associated with the incoming line signals.

1. The amplitude of the incoming line signal via the RTIP and RRING inputs; and
2. The number of pulses detected in the incoming line signal within a certain amount of time.

If the XRT73L00A determines that the incoming line signal is missing due to insufficient amplitude or a lack of pulses in the incoming line signal) then it declares a Loss of Signal (LOS) condition. The XRT73L00A declares the LOS condition by toggling the RLOS output pin "High" and by setting the RLOS bit field in Command Register 0 to "1".

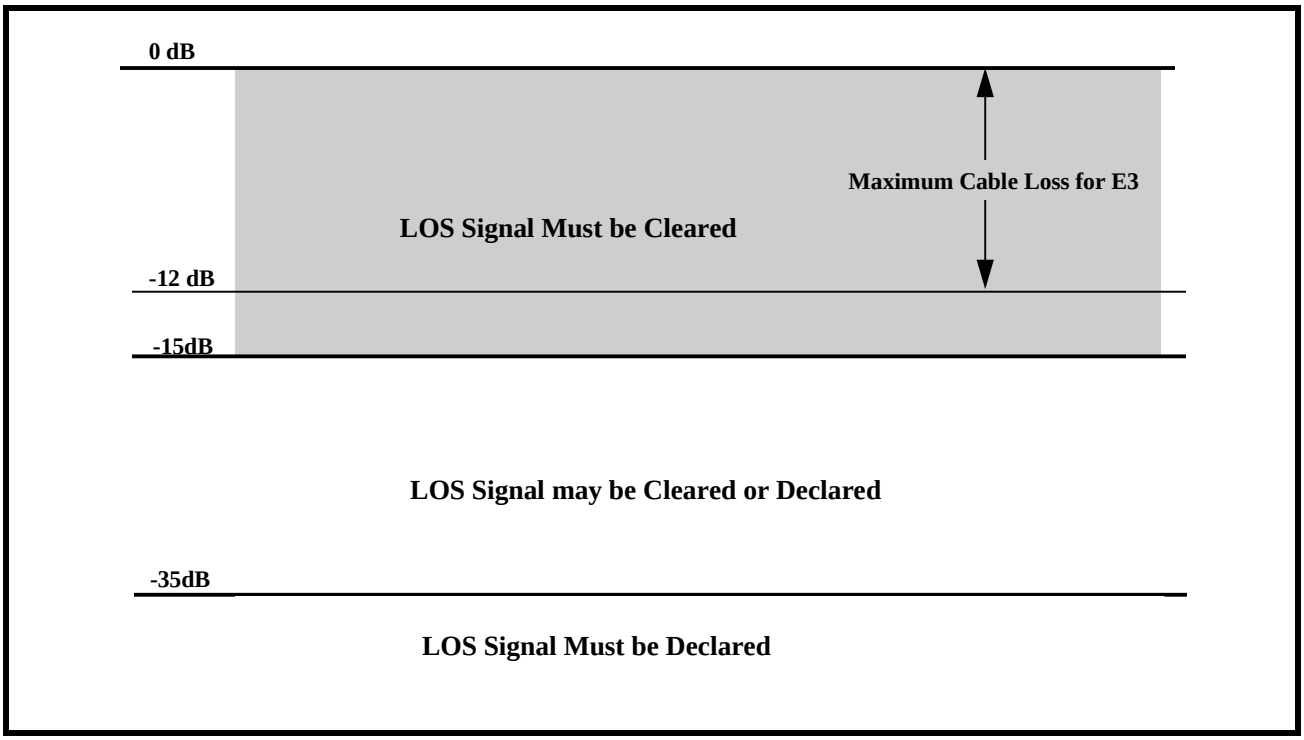
If the XRT73L00A determines that the incoming line signal has been restored (e.g., there is sufficient amplitude and pulses in the incoming line signal) then it clears the LOS condition by toggling the RLOS output pin "Low" and setting the RLOS bit-field to "0".

The LOS Declaration/Clearance scheme that is employed in the XRT73L00A is based upon ITU-T Recommendation G.775 for both E3 and DS3 applications. The LOS Declaration and Clearance criteria that the XRT73L00A uses for each of these modes (e.g., E3 and DS3) are presented below.

3.6.1 The LOS Declaration/Clearance Criteria for E3 Applications

When the XRT73L00A is operating in the E3 Mode, it declares an LOS Condition if the signal amplitude drops to -35dB or below. The XRT73L00A clears the LOS Condition if the signal amplitude rises back up to -15dB or above. Figure 22 illustrates the signal levels at which the XRT73L00A asserts and clears LOS.

FIGURE 22. THE SIGNAL LEVELS THAT THE XRT73L00A DECLARES AND CLEARS LOS (E3 MODE ONLY)

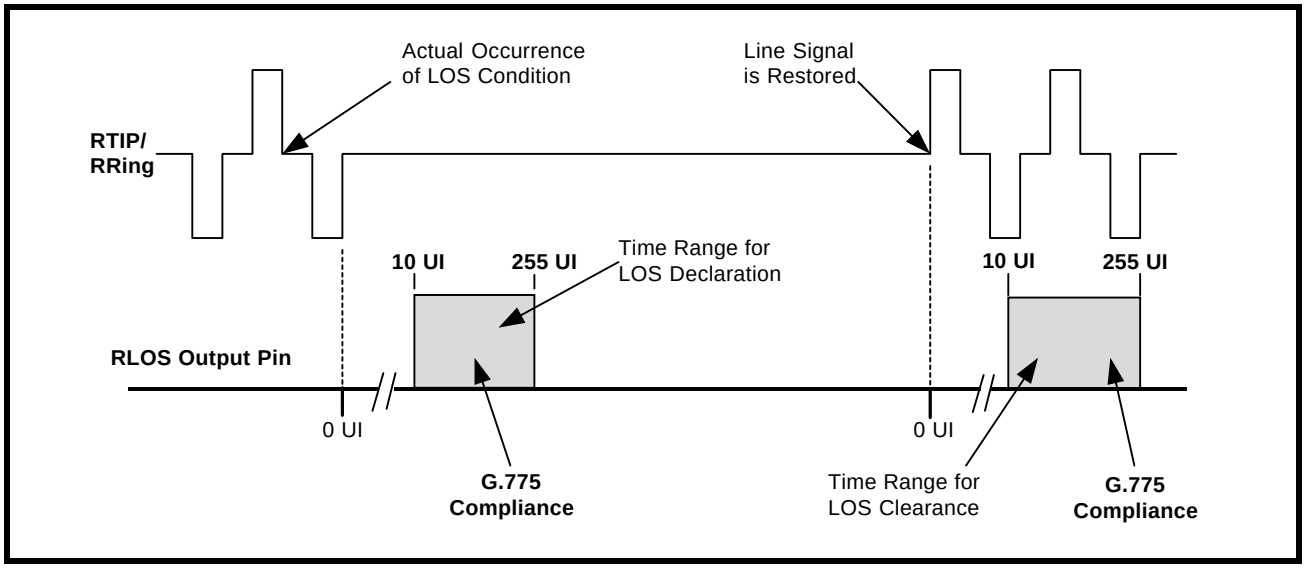


Timing Requirements associated with Declaring and Clearing the LOS Indicator for E3 Applications

The XRT73L00A was designed to meet the ITU-T G.775 specification timing requirements for declaring and clearing the LOS indicator. The XRT73L00A declares an LOS between 10 and 255 UI or E3 bit-periods after the actual time the LOS condition occurred. The XRT73L00A clears the LOS indicator within 10 to 255 UI after restoration of the incoming line signal. Figure 23 illustrates the LOS Declaration and Clearance behavior in response to the first loss

of signal event and then afterwards to the restoration of the signal.

FIGURE 23. THE BEHAVIOR THE LOS OUTPUT INDICATOR IN RESPONSE TO THE LOSS OF SIGNAL AND THE RESTORATION OF SIGNAL



3.6.2 The LOS Declaration/Clearance Criteria for DS3 and STS-1 Applications

When the XRT73L00A is operating in the DS3 or STS-1 Modes it declares and clears LOS based on either:

- Analog LOS (ALOS) Declaration/Clearance Criteria or,
- Digital LOS (DLOS) Declaration/Clearance Criteria

In the DS3 or STS-1 Modes the LOS output (RLOS) is simply the logical OR of the ALOS and DLOS states.

1. The Analog LOS (ALOS) Declaration/Clearance Criteria

The XRT73L00A declares an Analog LOS (ALOS) Condition if the amplitude of the incoming line signal drops below a specific amplitude as defined by the state of the LOSTHR input pin.

TABLE 4: THE ALOS DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR (DS3 AND STS-1 APPLICATIONS) FOR EQUALIZER ENABLED OR DISABLED

APPLICATION	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS	SIGNAL LEVEL TO CLEAR ALOS
LOS LEVEL WITH EQUALIZER ENABLED			
DS3	0	≤ 55mV	≥ 220mV
	1	≤ 22mV	≥ 70mV
Sonet STS-1	0	≤ 75mV	≥ 270mV
	1	≤ 25mV	≥ 110mV
LOS LEVEL WITH EQUALIZER DISABLED			
DS3	0	≤ 35mV	≥ 155mV
	1	≤ 17mV	≥ 70mV
Sonet STS-1	0	≤ 55mV	≥ 210mV
	1	≤ 20mV	≥ 90mV

Declaring ALOS

The XRT73L00A declares an ALOS (Analog LOS) condition whenever the amplitude of the input signal falls below the Signal Level to Declare ALOS levels specified in Table 4.

Clearing ALOS

The XRT73L00A clears ALOS whenever the amplitude of the input signal rises above the Signal Level to Clear ALOS levels specified in Table 4.

NOTE: *There is approximately a 2dB hysteresis in the received signal level that exists between declaring and clearing ALOS in order to prevent chattering in the RLOS output signal.*

Monitoring the State of ALOS

If the XRT73L00A is operating in the HOST Mode, the state of ALOS can be polled or monitored by reading in the contents of Command Register 0. The bit-format of Command Register 0 is presented below.

COMMAND REGISTER CR0 (ADDRESS = 0X00)

D4	D3	D2	D1	D0
RLOL	RLOS	ALOS	DLOS	DMO
Read Only	Read Only	Read Only	Read Only	Read Only

If the ALOS bit-field contains a “1”, the XRT73L00A is currently declaring an ALOS condition. If the ALOS bit-field contains a “0”, the device is NOT currently declaring an ALOS condition.

Disabling the ALOS Detector

It is useful to disable the ALOS Detector in the XRT73L00A for debugging purposes. If the XRT73L00A is operating in the HOST Mode, the ALOS Detector can be disabled by writing a “1” into the ALOSDIS bit-field in Command Register 2 as depicted below.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
X	X	1	X	X

NOTE: *Setting both the ALOSDIS and DLOSDIS bit-fields to “1” disables LOS Declaration in the XRT73L00.*

2. The Digital LOS (DLOS) Declaration/Clearance Criteria

The XRT73L00A declare a Digital LOS (DLOS) condition if the XRT73L00A detects 160±32 or more consecutive “0’s” in the incoming data.

The XRT73L00A clears DLOS if it detects four consecutive sets of 32 bit-periods each of which contains at least 10 “1’s” (e.g., average pulse density of greater than 33%).

Monitoring the State of DLOS

If the XRT73L00A is operating in the HOST Mode, the state of DLOS can be polled or monitored by reading in the contents of Command Register 0 as shown.

COMMAND REGISTER CR0 (ADDRESS = 0X00)

D4	D3	D2	D1	D0
RLOL	RLOS	ALOS	DLOS	DMO
Read Only	Read Only	Read Only	Read Only	Read Only

If the DLOS bit-field contains a “1”, the XRT73L00A is currently declaring a DLOS condition. If the DLOS bit-field contains a “0”, the device is NOT currently declaring the DLOS condition.

Disabling the DLOS Detector

It is useful to disable the DLOS Detector in the XRT73L00A for debugging purposes. If the XRT73L00A is operating in the HOST Mode, the DLOS Detector can be disabled by writing a “1” into the DLOSDIS bit-field in Command Register 2.

COMMAND REGISTER CR2 (ADDRESS = 0X02)

D4	D3	D2	D1	D0
Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
X	X	X	1	X

NOTE: *Setting both the ALOSDIS and DLOSDIS bit-fields to a “1” disables LOS Declaration in the XRT73L00.*

3.6.3 Muting the Recovered Data while the LOS is being Declared

In some applications it is not desirable for the XRT73L00A E3/DS3/STS-1 LIU to recover data and route it to the Receiving Terminal while the LIU is declaring an LOS condition. The LOS Muting feature, if enabled, causes the XRT73L00A to halt transmission of the recovered data to the Receiving Terminal while the LOS condition is True. In this case, the RPOS and RNEG output pins are forced to “0”. Once the LOS condition has been cleared, the XRT73L00A resumes the transmission of the recovered data to the Receiving Terminal. The XRT73L00A allows enabling of the Muting Upon LOS feature by either of the following means.

If the XRT73L00A is Operating in the Hardware Mode:

The Muting Upon LOS feature is enabled by pulling the LOSMUTEN input pin (pin 19) to VDD.

If the XRT73L00A is Operating in the HOST Mode:

To enable this feature, access the Microprocessor Serial Interface and write a “1” into the LOSMUT bit-field in Command Register 3.

COMMAND REGISTER CR3 (ADDRESS = 0X03)

D4	D3	D2	D1	D0
RNRZ	LOSMUT	CLK2DIS	RCLK2INV	CLK1INV
X	1	X	X	X

NOTE: *The XRT73L00A automatically declares an LOS Condition any time it has been configured to operate in either the Analog Local Loop-Back or Digital Local Loop-Back Modes. MUTing -upon -LOS must be disabled prior to configuring the device to operate in either of these local Loop-Back modes.*

3.7 Routing the Recovered Timing and Data Information to the Receiving Terminal Equipment

The XRT73L00A ultimately takes the Recovered Timing and Data information, converts it into CMOS levels and routes it to the Receiving Terminal Equipment via the RPOS, RNEG, RCLK1 and RCLK2 output pins.

The XRT73L00A can deliver the recovered data and clock information to the Receiving Terminal in either a Single-Rail or Dual-Rail format.

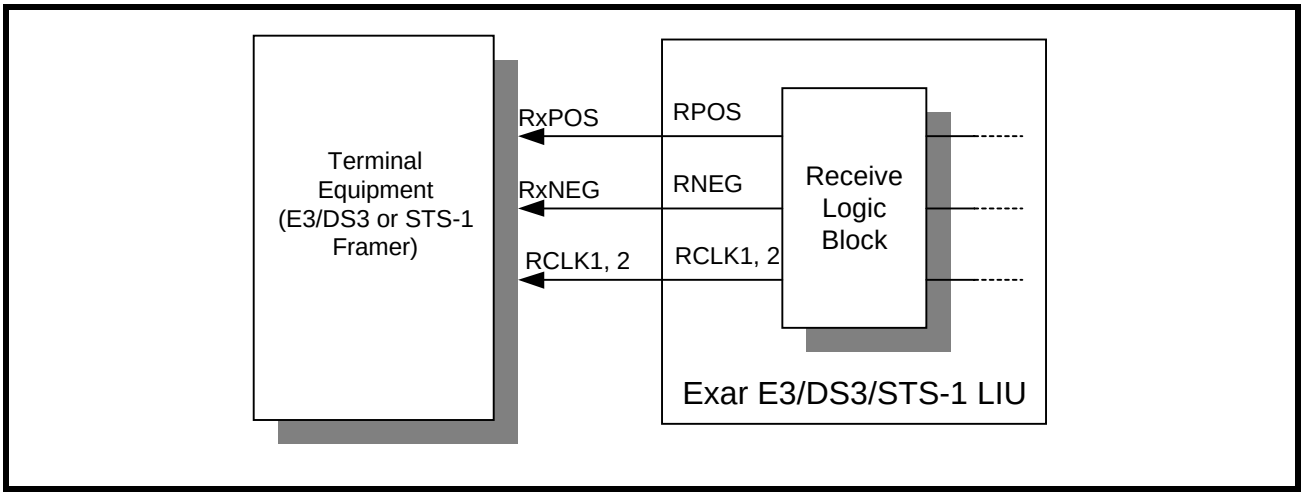
Routing Dual-Rail Format Data to the Receiving Terminal Equipment

Whenever the XRT73L00A delivers Dual-Rail format to the Terminal Equipment it does so via the following output signals.

- RPOS
- RNEG
- RCLK1
- RCLK2

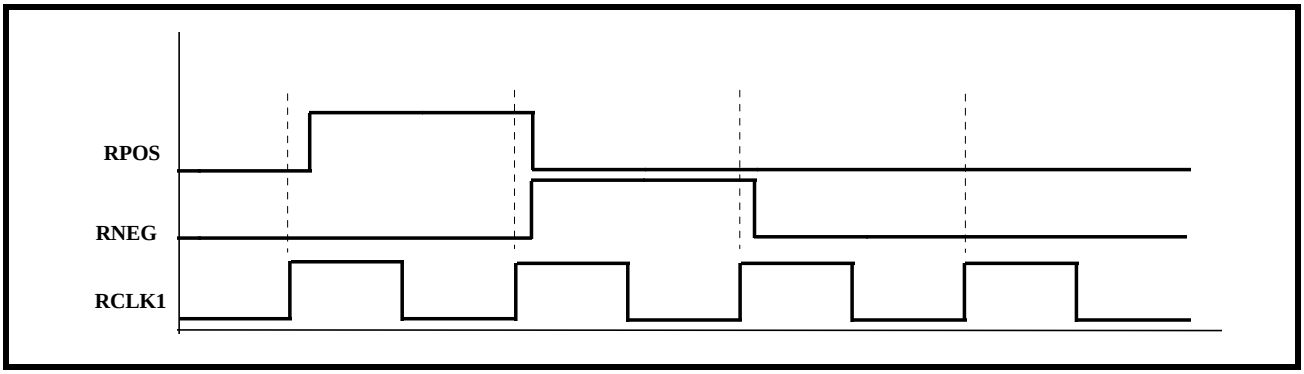
Figure 24 illustrates the typical interface for the transmission of data in a Dual-Rail Format from the Receive Section of the XRT73L00A to the Receiving Terminal Equipment.

FIGURE 24. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL-RAIL FORMAT FROM THE RECEIVE SECTION OF THE XRT73L00A TO THE RECEIVING TERMINAL EQUIPMENT



The manner that the LIU transmits Dual-Rail data to the Receiving Terminal Equipment is described below and illustrated in Figure 25. The XRT73L00A typically updates the data on the RPOS and RNEG output pins on the rising edge RCLK1 (or RCLK2).

FIGURE 25. HOW THE XRT73L00A OUTPUTS DATA ON THE RPOS AND RNEG OUTPUT PINS



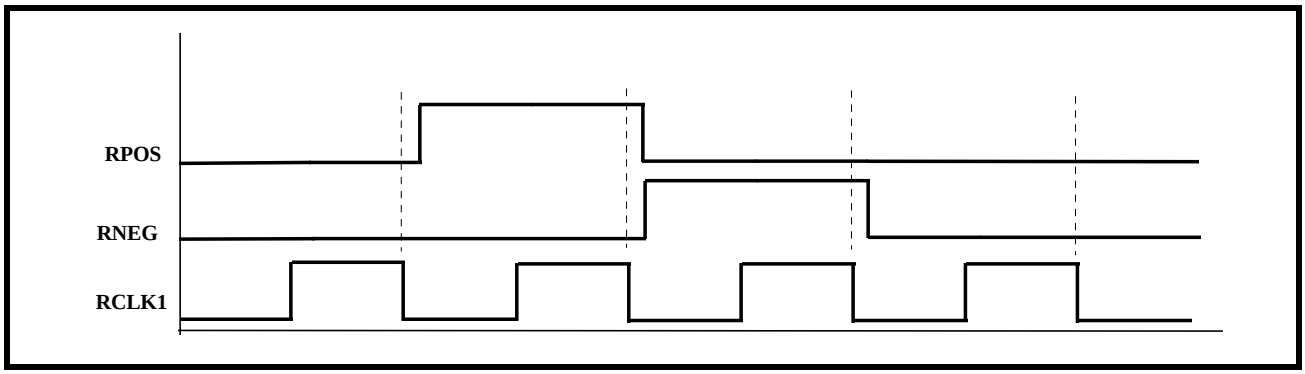
RCLK1 (or RCLK2) is the Recovered Clock signal from the incoming Received line signal. These clock signals are typically 34.368 MHz for E3 applications, 44.736 MHz for DS3 applications and 51.84 MHz for SONET STS-1 applications.

If the XRT73L00A received a positive-polarity pulse in the incoming line signal via the RTIP and RRING input pins, then the XRT73L00A pulses the RPOS output pin “High”. If the XRT73L00A received a negative-polarity pulse in the incoming line signal via the RTIP and RRING input pins, then the XRT73L00A pulses the RNEG output pin “High”.

Inverting the RCLK1 or RCLK2 outputs

When using the XRT73L00, either of the RCLK1 or RCLK2 signals can be inverted with respect to the delivery of the RPOS and RNEG output signals to the Receiving Terminal Equipment. This feature may be useful for those customers whose Receiving Terminal Equipment logic design is such that the RPOS and RNEG data must be sampled on the rising edge of RCLK1 or RCLK2. Figure 26 illustrates the behavior of the RPOS, RNEG and RCLK signals when the RCLK signal has been inverted.

FIGURE 26. THE BEHAVIOR OF THE RPOS, RNEG AND RCLK1 SIGNALS WHEN RCLK1 IS INVERTED



To configure the XRT73L00A to invert the RCLK1 output signal, the XRT73L00A must be operating in the HOST Mode. This configuration can be implemented by accessing the Microprocessor Serial Interface block and writing a “1” into the RCLK1INV bit-field in Command Register CR3 to invert RCLK1.

COMMAND REGISTER CR3 (ADDRESS = 0X03)

D4	D3	D2	D1	D0
RNRZ	LOSMUT	CLK2DIS	RCLK2INV	RCLK1INV
X	X	X	1	1

The RCLK2 output signal can also be inverted when the XRT73L00A is operating in the Hardware Mode by setting the RCLK2INV input pin “High”.

3.7.1 Routing Single-Rail Format data (Binary Data Stream) to the Receive Terminal Equipment

To route Single-Rail format data (e.g., a binary data stream) from the Receive Section of the XRT73L00A to the Receiving Terminal Equipment, do the following:

A. configure the XRT73L00A to operate in the HOST Mode and

B. access the Microprocessor Serial Interface and write a “1” into the RNRZ bit-field in Command Register CR3.

COMMAND REGISTER CR3 (ADDRESS = 0X03)

D4	D3	D2	D1	D0
RNRZ	LOSMUT	CLK2DIS	RCLK2INV	RCLK1INV
1	X	X	X	X

After these steps are taken, the XRT73L00A outputs Single-Rail data to the Receiving Terminal Equipment via the RPOS and RCLK1 (or RCLK2) output pins as illustrated in Figure 27 and Figure 28.

NOTE: *The RNEG output pin is internally tied to GND whenever this feature is enabled.*

FIGURE 27. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A SINGLE-RAIL FORMAT FROM THE RECEIVE SECTION OF THE XRT73L00A TO THE RECEIVING TERMINAL EQUIPMENT

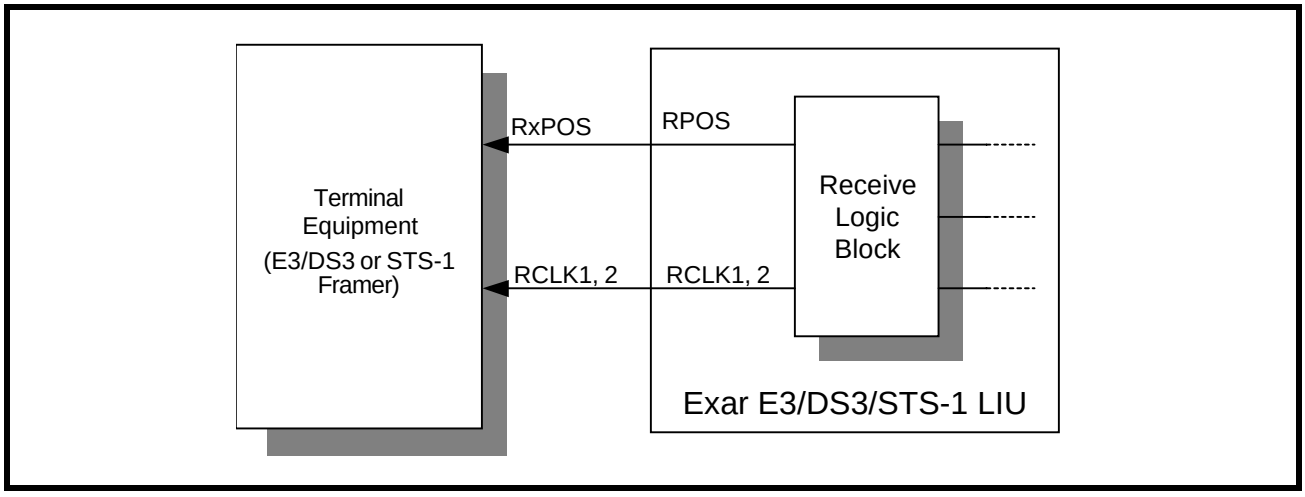
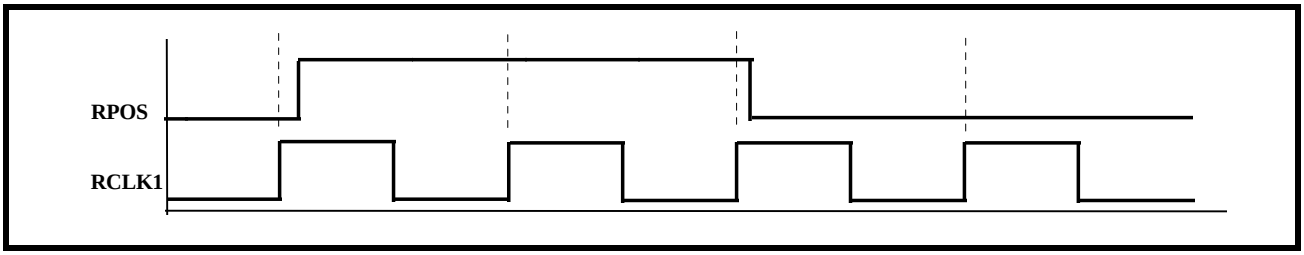


FIGURE 28. THE BEHAVIOR OF THE RPOS AND RCLK1 OUTPUT SIGNALS WHILE THE XRT73L00A IS TRANSMITTING SINGLE-RAIL DATA TO THE RECEIVING TERMINAL EQUIPMENT



4.0 DIAGNOSTIC FEATURES OF THE XRT73L00

The XRT73L00A supports equipment diagnostic activities by supporting the following Loop-Back modes in the chip:

- Analog Local Loop-Back
- Digital Local Loop-Back
- Remote Loop-Back.

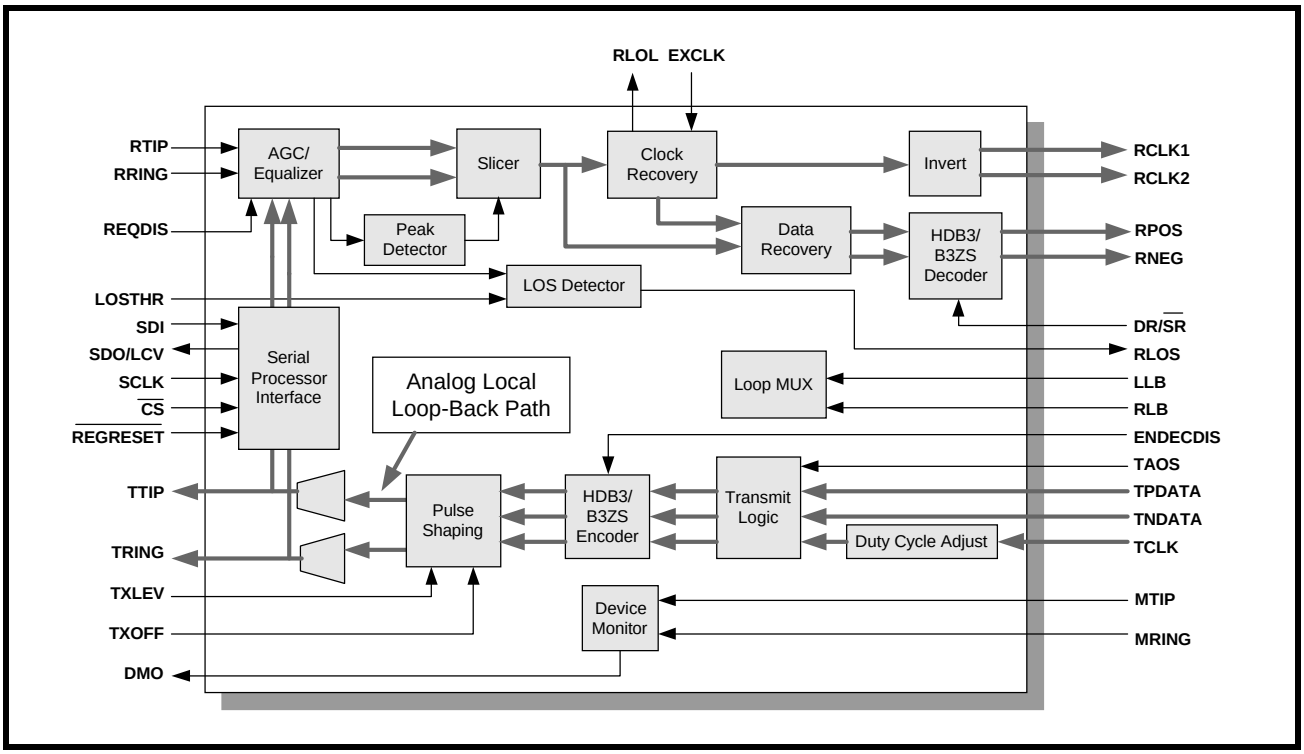
4.1 THE ANALOG LOCAL LOOP-BACK MODE

When the XRT73L00A is configured to operate in the Analog Local Loop-Back Mode, the XRT73L00A ignores any signals that are input to the RTIP and RRING input pins. The Transmitting Terminal Equipment transmits clock and data into the XRT73L00A via the TPDATA, TNDATA and TCLK input pins. This data is processed through the Transmit Clock Duty Cycle Adjust PLL and the HDB3/B3ZS Encoder. Finally, this data outputs to the line via the TTIP and TRING output pins and is looped back into the AGC/Receive Equalizer Block. Consequently, this data is also processed through the Receive Section of the XRT73L00. After this post-loop-back data has been processed through the Receive Section it outputs to the Near-End Receiving Terminal Equipment via the RPOS, RNEG, RCLK1 and RCLK2 output pins.

Figure 29 illustrates the path that the data takes when the chip is configured to operate in the Analog Local Loop-Back Mode.

The XRT73L00A can be configured to operate in the Analog Local Loop-Back Mode by employing either one of the following two steps:

FIGURE 29. THE ANALOG LOCAL LOOP-BACK IN THE XRT73L00



If the XRT73L00A is operating in the HOST Mode:

Access the Microprocessor Serial Interface and write a “1” into the LLB bit-field and a “0” into the RLB bit-field in Command Register 4.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$	E3	LLB	RLB
X	X	X	1	0

If the XRT73L00A is operating in the Hardware Mode:

The LLB input pin (pin 14) must be set to “High” and the RLB input pin (pin 15) must be set to “Low”.

NOTES:

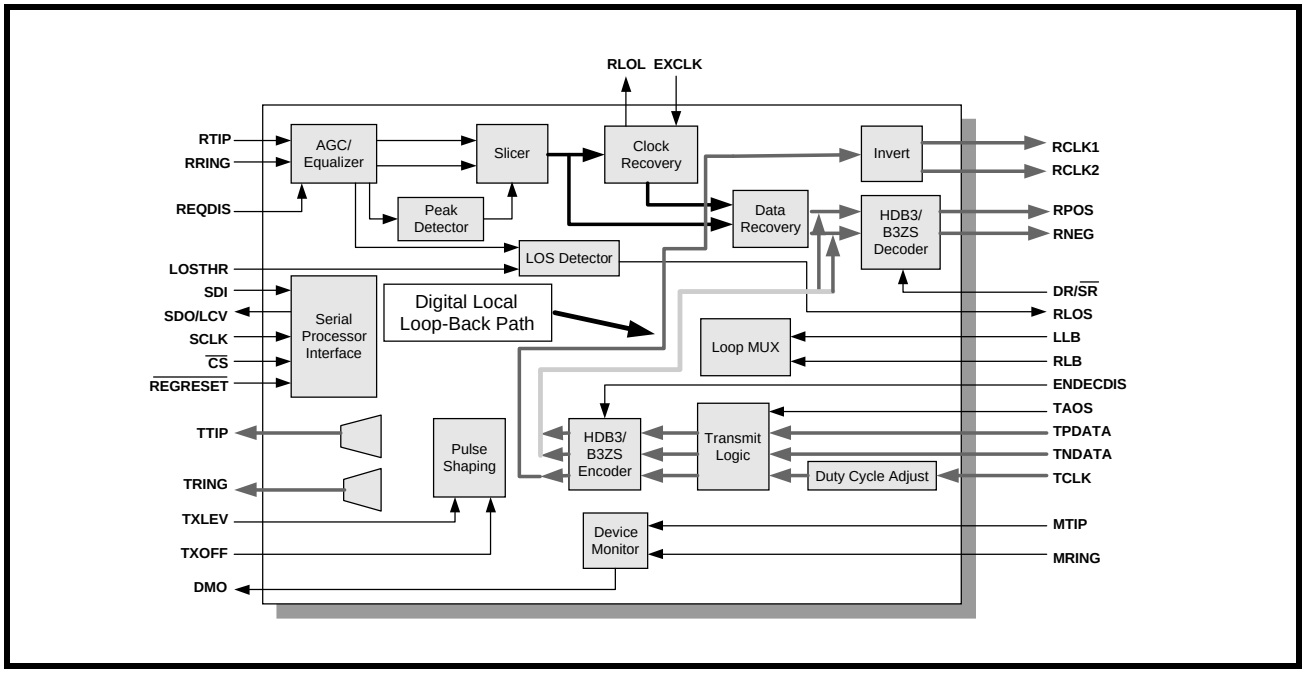
1. *The Analog Local Loop-Back Mode does not work if the transmitter is turned off via the TXOFF feature.*
2. *The XRT73L00A automatically Declares an LOS Condition anytime it has been configured to operate in either the Analog Local Loop-Back or Digital Local Loop-Back Modes. Consequently, the MUTing -upon -LOS must be disabled prior to configuring the device to operate in either of these local Loop-Back modes.*

4.2 THE DIGITAL LOCAL LOOP-BACK MODE

When the XRT73L00A is configured to operate in the Digital Local Loop-Back Mode, it ignores any signals that are input to the RTIP and RRING input pins. The Transmitting Terminal Equipment transmits clock and data into the XRT73L00A via the TPDATA, TNDATA and TCLK input pins. This data is processed through the Transmit Clock Duty Cycle Adjust PLL and the HDB3/B3ZS Encoder block and then looped back to the HDB3/B3ZS Decoder block.

Figure 30 illustrates the path that the data takes when the chip is configured to operate in the Digital Local Loop-Back Mode.

FIGURE 30. THE DIGITAL LOCAL LOOP-BACK PATH IN THE XRT73L00



The Digital Local Loop-Back Mode, along with the Tx-OFF feature, is useful in Redundancy System Design. These two features permit the system to execute some diagnostic tests in the Back-up Line Card without transmitting data onto the line and interfering with the DS3/E3/STS-1 traffic from the Primary Line Card.

The XRT73L00A can be configured to operate in the Digital Local Loop-Back Mode by employing either one of the following two-steps.

A. If the XRT73L00A is operating in the HOST Mode

Access the Microprocessor Serial Interface and write a “1” into both the LLB and RLB bit-fields in Command Register 4.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$	E3	LLB	RLB
X	X	X	1	1

B. If the XRT73L00A is operating in the Hardware Mode

Set both the LLB input pin (pin 14) and the RLB input pin (pin 15) to “High”.

NOTES:

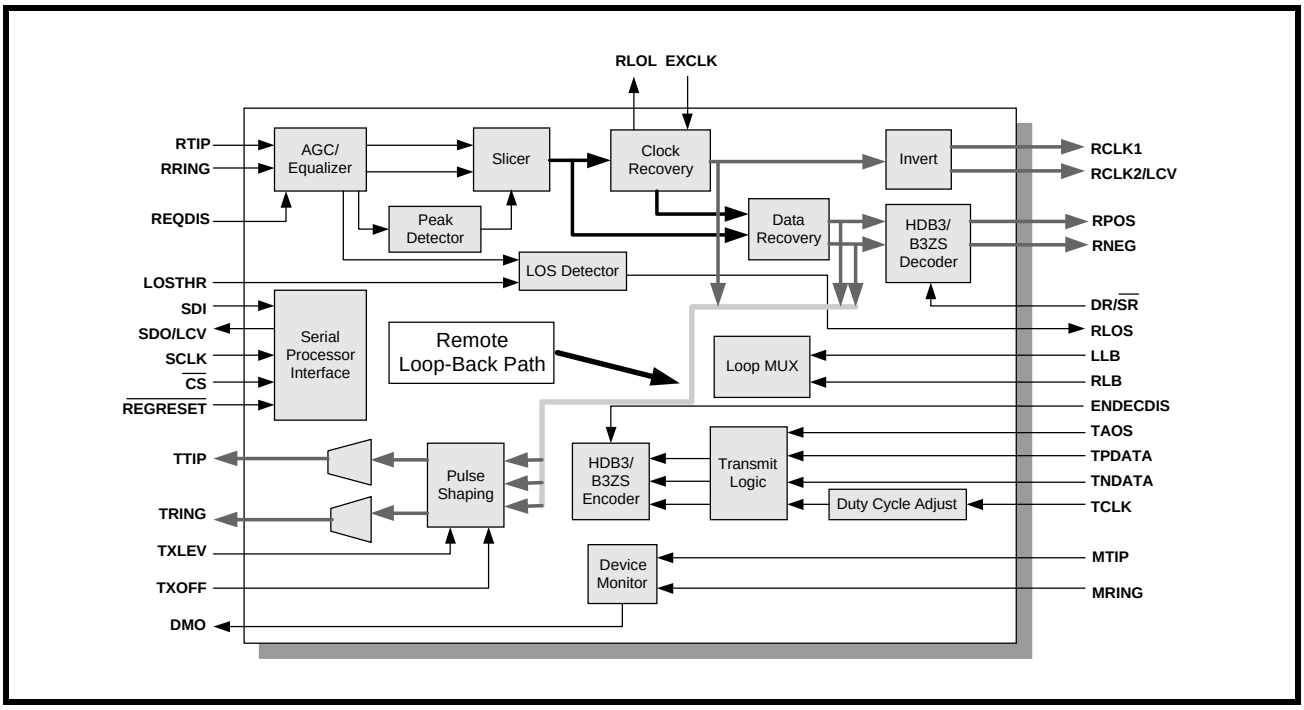
1. *The Digital Local Loop-Back Mode feature works even if the transmitter is turned off via the TXOFF feature.*
2. *The XRT73L00A automatically declares an LOS Condition any time it has been configured to operate in either the Analog Local Loop-Back or Digital Local Loop-Back Modes. Consequently, the MUTing -upon -LOS must be disabled prior to configuring the device to operate in either of these local Loop-Back modes.*

4.3 THE REMOTE LOOP-BACK MODE

When the XRT73L00A is configured to operate in the Remote Loop-Back Mode, it ignores any signals that are input to the TPDATA and TNDATA input pins. The XRT73L00A receives the incoming line signal via the RTIP and RRING input pins. This data is processed through the Receive Section of the XRT73L00A and outputs to the Receive Terminal Equipment via the RPOS, RNEG, RCLK1 and RCLK2 output pins. Additionally, this data is internally looped back into the Pulse-Shaping block in the Transmit Section. At this point, this data is routed through the remainder of the Transmit Section of the XRT73L00A and transmitted out onto the line via the TTIP and TRING output pins.

Figure 31 illustrates the path that the data takes in the XRT73L00A when the chip is configured to operate in the Remote Loop-Back Mode.

FIGURE 31. THE REMOTE LOOP-BACK PATH IN THE XRT73L00



During Remote Loop-Back operation, any data which is inputted via the RTIP and RRING input pins is also outputted to the Terminal Equipment via the RPOS, RNEG and RCLK output pins.

The XRT73L00A can be configured to operate in the Remote Loop-Back Mode by employing either one of the following two steps

If the XRT73L00A is operating in the HOST Mode:

Access the Microprocessor Serial Interface and write a “1” into the RLB bit-field and a “0” in the LLB bit-field in Command Register CR4.

COMMAND REGISTER CR4 (ADDRESS = 0X04)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$	E3	LLB	RLB
X	X	X	0	1

If the XRT73L00A is operating in the Hardware Mode:

Set the RLB input pin (pin 15) to "High" and the LLB input pin (pin 16) to "Low".

4.4 TXOFF Features

The XRT73L00A allows the Transmit Driver in the Transmit Section of the chip to be shut off. This feature can be advantageous for system redundancy conditions or during diagnostic testing. This feature can be activated by either of the following ways.

When the XRT73L00A is operating in the Hardware Mode

Shut off the Transmit Driver by toggling the TXOFF input pin (pin 35) "High". Turn on the Transmit Driver by toggling the TXOFF input pin "Low".

When the XRT73L00A is operating in the HOST Mode

If the XRT73L00A is operating in the HOST Mode, the TXOFF input pin is disabled. Consequently, the Transmit Driver is turned off by writing to Command Register CR1 and setting the TXOFF bit-field (bit D4) to "1".

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
1	X	X	X	X

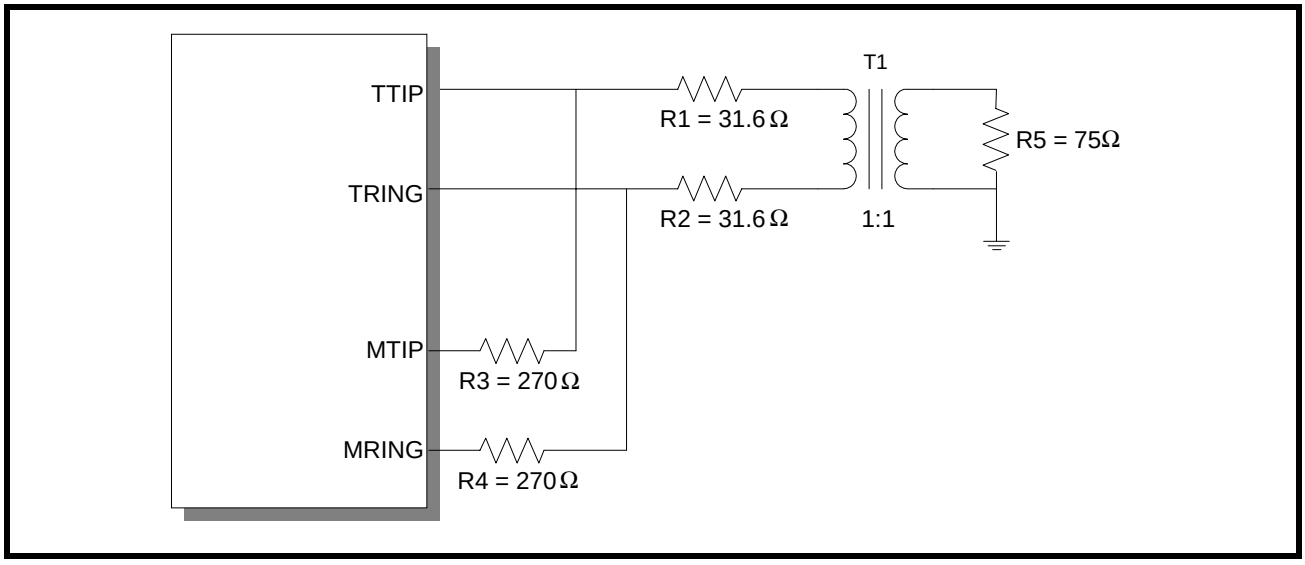
NOTE: *If the Transmitter is shut off via the TXOFF feature, the XRT73L00A can NOT be configured to operate in the Analog Local Loop-Back Mode. To perform diagnostics on the chip and still invoke the TXOFF feature as in System Redundancy Applications, use the Digital Local Loop-Back feature instead.*

4.5 The Transmit Drive Monitor Features

The Transmit Drive Monitor feature performs monitoring of the line in the Transmit Direction for the occurrence of fault conditions such as a short circuit on the line or a defective Transmit Drive in the XRT73L00.

The Transmit Drive Monitor is activated by connecting the MTIP pin (pin 44) to the TTIP line through a 270 Ω resistor connected in series and by connecting the MRING pin (pin 43) to the TRING line through a 270 Ω resistor connected in series, as illustrated in Figure 32.

FIGURE 32. THE XRT73L00A EMPLOYING THE TRANSMIT DRIVE MONITOR FEATURES

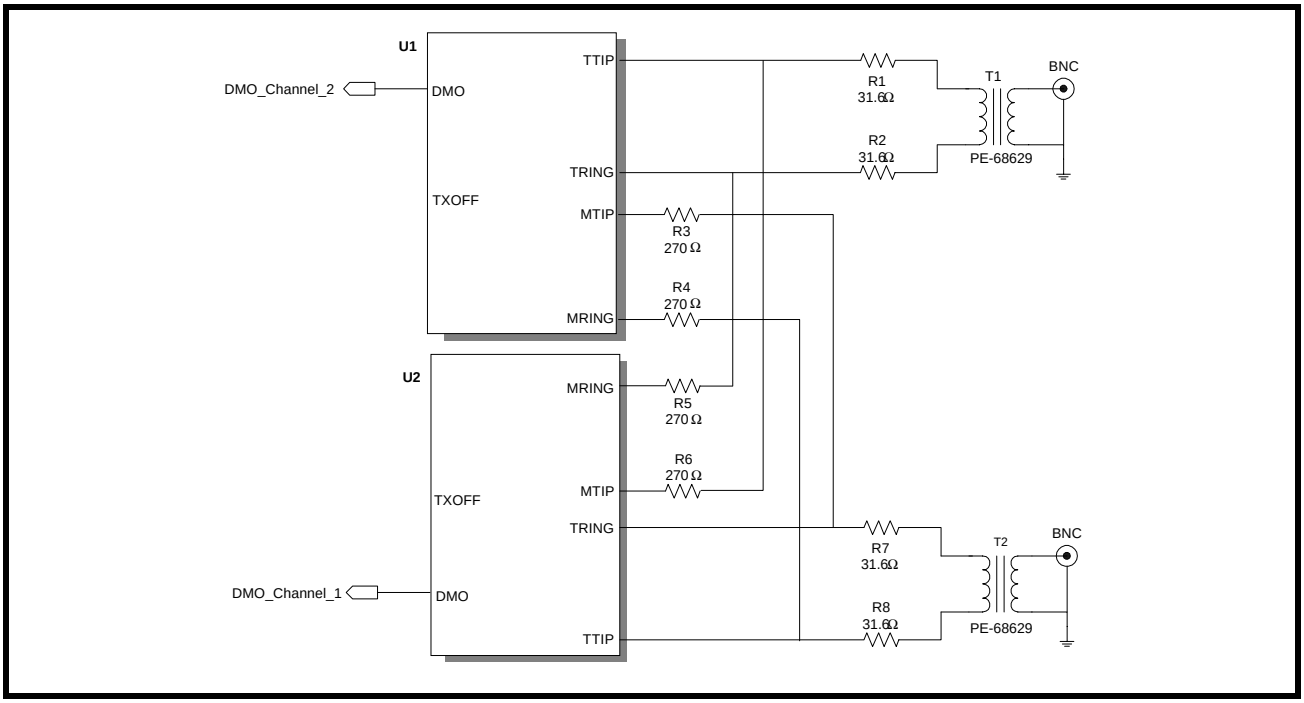


When the Transmit Drive Monitor circuitry is connected to the line as illustrated in Figure 26, then it monitors the line for transitions. As long as the Transmit Drive Monitor circuitry detects transitions on the line via the MTIP and MRING pins, it keeps the DMO (Drive Monitor Output) signal "Low". However, if the Transmit Drive Monitor circuit detects no transitions on the line for 128±32 TCLK periods, then the DMO signal toggles "High".

NOTES:

1. *The Transmit Drive Monitor circuit does not have to be used to operate the Transmit Section of the XRT73L00. This is purely a diagnostic feature.*
2. *The Transmit Drive Monitor feature can also be used to monitor the Transmit Output Line Signal of another LIU IC as illustrated in Figure 33.*

FIGURE 33. TWO LIU'S, EACH MONITORING THE TRANSMIT OUTPUT SIGNAL OF THE OTHER LIU IC



Presented in Figure 33, if LIU # 1 (U1) fails, then LIU # 2 (U2) drives its DMO output pin "High". Likewise, if LIU # 2 (U2) fails, then LIU # 1 (U1) drives its DMO output pin "High".

The scheme presented in Figure 33 is a better design approach. It overcomes situations in which a LIU monitoring its own signal (Figure 32) may experience a failure mode such that it cannot drive a bipolar signal onto the line. That same failure mode may prevent the LIU from driving the DMO output pin "High".

4.6 THE TAOS (TRANSMIT ALL ONES) FEATURE

The XRT73L00A can transmit an all "1's" pattern onto the line by toggling a single input pin or by setting a single bit-field in one of the Command Registers to "1".

NOTE: *When this feature is activated, the Transmit Section of the XRT73L00A overwrites the Terminal Equipment data with this all "1's" pattern.*

This feature can be activated by either of the following methods.

When the XRT73L00A is operating in the Hardware Mode:

Configure the device to transmit an all "1's" pattern by toggling the TAOS input pin (pin 2) "High". Terminate the all "1's" pattern by toggling the TAOS input pin "Low".

When the XRT73L00A is operating in the HOST Mode:

If the XRT73L00A is operating in the HOST Mode, the TAOS input pin is disabled. Consequently, the XRT73L00A can be configured to transmit an all "1's" pattern by writing to Command Register CR1 and setting the TAOS bit-field (bit D3) to "1".

COMMAND REGISTER CR1 (ADDRESS = 0X01)

D4	D3	D2	D1	D0
TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
0	1	X	X	X

The all "1's" pattern can be terminated by writing to Command Register CR1 and setting the TAOS bit-field (D3) to "0".

5.0 THE MICROPROCESSOR SERIAL INTERFACE

The on-chip Command Registers of the XRT73L00A DS3/E3/STS-1 Line Interface Unit IC are accessed to configure the XRT73L00A into a variety of modes.

This section describes the Command Registers and how to use the Microprocessor Serial Interface.

5.1 DESCRIPTION OF THE COMMAND REGISTERS

A listing of these Command Registers, their Addresses and their Bit-Formats are listed in Table 5.

TABLE 5: ADDRESSES AND BIT FORMATS OF XRT73L00A COMMAND REGISTERS

ADDRESS	COMMAND REGISTER	TYPE	REGISTER BIT-FORMAT				
			D4	D3	D2	D1	D0
0x00	CR0	RO	RLOL	RLOS	ALOS	DLOS	DMO
0x01	CR1	R/W	TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN
0x02	CR2	R/W	Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQDIS
0x03	CR3	R/W	RNRZ	LOSMUT	RCLK2/$\overline{\text{LCV}}$	RCLK2INV	RCLK1INV
0x04	CR4	R/W	Reserved	STS-1/$\overline{\text{DS3}}$	E3	LLB	RLB
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x08	CR8	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x09	CR9	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x10	CR10	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x11	CR11	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x12	CR12	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x13	CR13	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x14	CR14	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x15	CR15	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Address:

The register addresses are in **Hexadecimal** format.

Type:

The Command Registers are either Read-Only (RO) or Read/Write (R/W) registers.

NOTES:

1. *The default value for each of the bit-fields in these registers is "0".*
2. *If the $\overline{\text{REGRESET}}$ input pin is asserted, then the contents of the command registers is reset to all "0's" resulting in the XRT73L00A operating in the mode corresponding to the default values of the Command Registers.*

DESCRIPTION OF BIT-FIELDS FOR EACH COMMAND REGISTER

5.1.1 Command Register - CR0

Bit D4 - RLOL (Receive Loss of Lock Status)

This Read-Only bit-field reflects the lock status of the Clock Recovery Phase-Locked-Loop in the XRT73L00.

This bit-field is set to "0" if the Clock Recovery PLL is in lock with the incoming line signal. This bit-field is set to "1" if the Clock Recovery PLL is out of lock with the incoming line signal.

Bit D3 - RLOS (Receive Loss of Signal Status)

This Read-Only bit-field indicates whether or not the Receiver in the XRT73L00A is currently declaring an LOS (Loss of Signal) Condition.

This bit-field is set to "0" if the XRT73L00A is not currently declaring the LOS Condition. This bit-field is set to "1" if the XRT73L00A is declaring an LOS Condition.

Bit D2 - ALOS (Analog Loss of Signal Status)

This Read-Only bit-field indicates whether or not the Analog LOS Detector in the XRT73L00A is currently declaring an LOS condition.

This bit-field is set to “0” if the Analog LOS Detector in the XRT73L00A is NOT currently declaring an LOS condition. Conversely, this bit-field is set to “1” if the Analog LOS Detector is currently declaring an LOS condition.

The purpose of this feature is to isolate either the Analog LOS or the Digital LOS detector that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.

Bit D1 - DLOS (Digital Loss of Signal Status)

This Read-Only bit-field indicates whether or not the Digital LOS Detector in the XRT73L00A is currently declaring an LOS condition.

This bit-field is set to “0” if the Digital LOS Detector in the XRT73L00A is NOT currently declaring an LOS condition. Conversely, this bit-field is set to “1” if the Digital LOS Detector is currently declaring an LOS condition.

NOTE: *The purpose of this feature is to isolate the Detector (e.g., either the Analog LOS or the Digital LOS detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.*

Bit D0 - DMO (Drive Monitor Output Status)

This Read-Only bit-field reflects the status of the DMO output pin.

5.1.2 Command Register - CR1

Bit D4 - TXOFF (Transmitter OFF)

This Read/Write bit-field is used to turn off the Transmitter in the XRT73L00.

Writing a “1” to this bit-field turns off the Transmitter and tri-states the Transmit Output. Writing a “0” to this bit-field turns on the Transmitter.

Bit D3 - TAOS (Transmit All OneS)

This Read/Write bit-field is used to command the XRT73L00A Transmitter to generate and transmit an all “1’s” pattern onto the line.

Writing a “1” to this bit-field commands the Transmitter to transmit an all “1’s” pattern onto the line. Writing a “0” to this bit-field commands normal operation.

Bit D2 - TXCLKINV (Transmit Clock Invert)

This Read/Write bit-field is used to configure the XRT73L00A Transmitter to sample the signal at the TPDATA and TNDATA pins on the rising or falling edge of TCLK (the Transmit Line Clock signal).

Writing a “1” to this bit-field configures the Transmitter to sample the TPDATA and TNDATA input pins on the rising edge of TCLK. Writing a “0” to this bit-field configures the Transmitter to sample the TPDATA and TNDATA input pins on the falling edge of TCLK.

Bit D1 - TXLEV (Transmit Level Select)

This Read/Write bit-field is used to enable or disable the XRT73L00A Transmit Line Build-Out circuit.

Setting this bit-field "High" disables the Line Build-Out circuit of the XRT73L00. In this mode, the XRT73L00A outputs partially-shaped pulses onto the line via the TTIP and TRING output pins. Setting this bit-field "Low" enables the Line Build-Out circuit of the XRT73L00. In this mode the XRT73L00A outputs shaped pulses onto the line via the TTIP and TRING output pins.

To comply with the Isolated DSX/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or GR-253-CORE, either:

1. set this input pin to "1" if the cable length between the Cross-Connect and the transmit output of the XRT73L00A is greater than 225 feet or
2. set this input pin to "0" if the cable length between the Cross-Connect and the transmit output of the XRT73L00A is less than 225 feet.

NOTE: *This option is only available when the XRT73L00A is operating in the DS3 or STS-1 Mode.*

Bit D0 - TXBIN (Transmit Binary Data)

This Read/Write bit-field permits configuring of the Transmitter in the XRT73L00A to accept an un-encoded binary data stream via the TPDATA input and converts this data into the appropriate bipolar signal to the line.

Writing a “1” configures the Transmitter to accept a binary data stream via the TPDATA input.

NOTE: *The TNDATA input is ignored.*

This form of data acceptance is sometimes referred to as Single-Rail mode operation. The Transmitter then encodes this data into the appropriate line code (e.g., B3ZS or HDB3) prior to its transmission over the line.

Writing a “0” configures the Transmitter to accept data in a Dual-Rail manner (e.g., via both the TPDATA and TNDATA inputs).

5.1.3 Command Register - CR2

Bit D4 - Reserved

This bit-field has no defined functionality

Bit D3 - ENDECDIS (B3ZS/HDB3 Encoder/Decoder-Disable)

This Read/Write bit-field is used to enable or disable the B3ZS/HDB3 Encoder/Decoder in the XRT73L00.

Writing a “1” to this bit-field disables the B3ZS/HDB3 Encoder. Writing a “0” to this bit-field enables the B3ZS/HDB3 Encoder.

NOTE: *This Encoder performs HDB3 Encoding if the XRT73L00A is operating in the E3 Mode. Otherwise, it performs B3ZS Encoding.*

Bit D2 - ALOSDIS (Analog LOS Disable)

This Read/Write bit-field is used to disable the Analog LOS Detector.

Writing a “0” to this bit-field enables the Analog LOS Detector. Writing a “1” to this bit-field disables the Analog LOS Detector.

NOTE: *If the Analog LOS Detector is disabled, then the RLOS input pin is only asserted by the DLOS (Digital LOS Detector).*

Bit D1 - DLOSDIS (Digital LOS Disable)

This Read/Write bit-field is used to disable the Digital LOS Detector.

Writing a “0” to this bit-field enables the Digital LOS Detector. Writing a “1” to this bit-field disables the Digital LOS Detector.

NOTE: *If the Digital LOS Detector is disabled, then the RLOS input pin is only asserted by the ALOS (Analog LOS Detector).*

Bit D0 - REQDIS (Receive Equalization Disable)

This Read/Write bit-field is used to either enable or disable the internal Receive Equalizer in the XRT73L00.

Writing a “0” to this bit-field enables the Internal Equalizer. Writing a “1” to this bit-field disables the Internal Equalizer.

5.1.4 Command Register - CR3

Bit D4 - RNRZ (Receive Binary Data)

This Read/Write bit-field is used to configure the XRT73L00A to output the received data from the Remote Terminal in a binary or Dual-Rail format.

Writing a “1” to this bit-field configures the XRT73L00A to output data to the Terminal Equipment in a Single-Rail (binary) format via the RPOS output pin. The RNEG is grounded. A “0” to this bit-field configures the XRT73L00A to output data to the Terminal Equipment in a Dual-Rail format via both the RPOS and RNEG output pins.

Bit D3 - LOSMUT (Recovered Data MUTing during LOS Condition)

This Read/Write bit-field is used to configure the XRT73L00A to NOT output any recovered data while it is declaring an LOS condition to the terminal equipment.

Writing a “0” to this bit-field configures the chip to output recovered data even while the XRT73L00A is declaring an LOS condition. Writing a “1” to this bit-field configures the chip to NOT output the recovered data while an LOS condition is being declared.

NOTE: *In this mode, RPOS and RNEG is set to “0” asynchronously.*

Bit D2 - RCLK2/$\overline{\text{LCV}}$ (Receive Clock Output 2/Line Code Violation)

This Read/Write bit-field is used to select the function of pin 30 (RCLK2/LCV). Pin 30 can be configured to function as the Line Code Violation output indicator or as the additional Receive Clock Output (RCLK2).

Writing a “0” to this bit-field configures the pin to function as the Line Code Violation output pin. Writing a “1” to this bit-field configures this pin to function as the RCLK2 output pin.

Bit D1 - RCLK2INV (Invert RCLK2)

This Read/Write bit-field is used to configure the Receiver in the XRT73L00A to output the recovered data on either the rising edge or the falling edge of the RCLK2 clock signal.

Writing a “0” to this bit-field configures the Receiver to output the recovered data on the rising edge of the RCLK2 output signal. Writing a “1” to this bit-field configures the Receiver to output the recovered data on the falling edge of the RCLK2 output signal.

Bit D0 - RCLK1INV (Invert RCLK1)

This Read/Write bit-field is used to configure the Receiver in the XRT73L00A to output the recovered data on either the rising edge or the falling edge of the RCLK1 clock signal.

Writing a “0” to this bit-field configures the Receiver to output the recovered data on the rising edge of the RCLK1 output signal. Writing a “1” to this bit-field configures the Receiver to output the recovered data on the falling edge of the RCLK1 output signal.

5.1.5 Command Register - CR4

Bit D4 - Reserved

This bit-field has no defined functionality

Bit D3 - STS-1/DS3 Mode Select

This Read/Write bit-field is used to configure the XRT73L00A to operate in either the SONET STS-1 Mode or the DS3 Mode.

Writing a "0" into this bit-field configures the XRT73L00A to operate in the DS3 Mode. Writing a "1" into this bit-field configures the XRT73L00A to operate in the SONET STS-1 Mode.

NOTE: *This bit-field is ignored if the E3 bit-field (D2 in this Command Register) is set to "1".*

Bit D2 - E3 Mode Select

This Read/Write bit-field is used to configure the XRT73L00A to operate in the E3 Mode.

Writing a "0" into this bit-field configures the XRT73L00A to operate in either the DS3 or SONET STS-1 Mode specified by the setting of the DS3 bit-field in this Command Register. Writing a "1" into this bit-field configures the XRT73L00A to operate in the E3 Mode.

Bit D1 - LLB (Local Loop-Back)

This Read/Write bit-field along with RLB (bit D0 in this Command Register) is used to select which Loop-Back mode the XRT73L00A operates in. Table 6 relates the state of the LLB and RLB to the selected Loop-Back mode.

Bit D0 - RLB (Remote Loop-Back)

This Read/Write bit-field along with LLB (bit D1 in this Command Register) is used to select which Loop-Back mode the XRT73L00A operate in. Table 6 relates the state of the LLB and RLB bits to the selected Loop-Back mode.

TABLE 6: LOOP-BACK MODES

LLB (BIT D1)	RLB (BIT D0)	LOOP-BACK MODE
0	0	No Loop-Back Mode (Normal Operation)
0	1	Remote Loop-Back Mode
1	0	Analog Loop-Back Mode
1	1	Digital Loop-Back Mode

5.2 OPERATING THE MICROPROCESSOR SERIAL INTERFACE.

The XRT73L00A Serial Interface is a simple four wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

$\overline{CS}$	-	Chip Select (Active Low)
SCLK	-	Serial Clock
SDI	-	Serial Data Input
SDO	-	Serial Data Output

Using the Microprocessor Serial Interface

The following instructions for using the Microprocessor Serial Interface are best understood by referring to the diagram in Figure 34.

In order to use the Microprocessor Serial Interface, a clock signal must be supplied to the SCLK input pin. A Read or Write operation can then be initiated by asserting the active-low Chip Select input pin ($\overline{CS}$). It is important to assert the $\overline{CS}$ pin (e.g., toggle it "Low") at least 50ns prior to the very first rising edge of the clock signal.

Once the $\overline{CS}$ input pin has been asserted, the type of operation and the target register address must now be specified. This information is supplied to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input.

NOTE: *Each of these bits is clocked into the SDI input on the rising edge of SCLK. These eight bits are identified and described below.*

Bit 1 - R/W (Read/Write) Bit

This bit is clocked into the SDI input on the first rising edge of SCLK after $\overline{CS}$ has been asserted. This bit indicates whether the current operation is a Read or Write operation. A "1" in this bit specifies a Read operation, a "0" in this bit specifies a Write operation.

Bits 2 through 5: The four (4) bit Address Values (labeled A0, A1, A2 and A3)

The next four rising edges of the SCLK signal clock in the 4-bit address value for this particular Read (or Write) operation. The address selects the Command Register in the XRT73L00A that the user is either reading data from or writing data to. The address bits must be supplied to the SDI input pin in ascending order with the LSB (least significant bit) first.

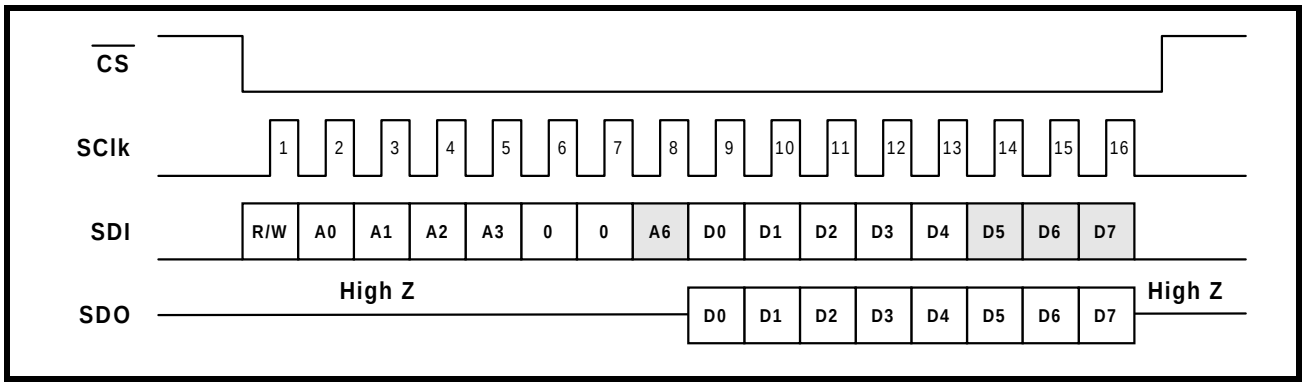
Bits 6 and 7:

The next two bits, A4 and A5 must be set to "0" as shown in Figure 34.

Bit 8:

The value of A6 is a "don't care".

FIGURE 34. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



Notes:

- Denotes a "don't care" value

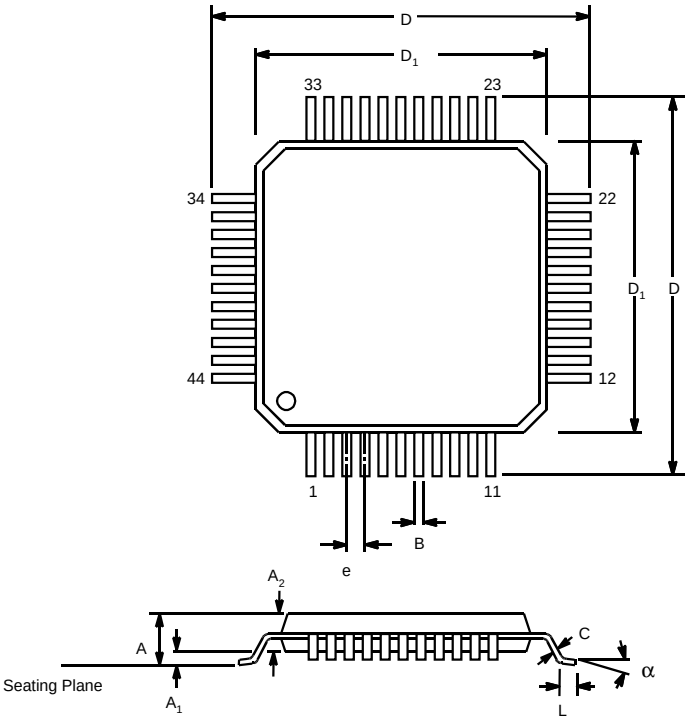
A4 and A5 are always "0".
R/W = "1" for "Read" Operations
R/W = "0" for "Write" Operations

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73L00AIV	44 Pin TQFP (10mm x 10mm)	-40°C to +85°C

PACKAGE DIMENSIONS

44 LEAD THIN QUAD FLAT PACK
(10 x 10 x 1.4 mm TQFP)
rev. 1.00



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.055	0.063	1.4	1.6
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.3	0.45
C	0.004	0.008	0.09	0.2
D	0.465	0.48	11.8	12.2
D1	0.39	0.398	9.9	10.1
e	0.0315 BSC		0.80 BSC	
L	0.018	0.03	0.45	0.75
α	0°	7°	0°	7°

Note: *The control dimension is the millimeter column*

REVISION HISTORY

Rev.P1.0.0 original

Rev. P1.0.1 Removed figures 34 &35, modified figures 3 & 4 to show timing more adequately

Rev. P1.0.2 modified figure 4 LCV signal

Rev. P1.0.3 added Device Monitor section to block diagram. Changed RxIN to RTIP/RRING in fig. 22.

Rev. P1.0.4 Transmit Digital Power Supply/Ground changed to Analog Power Supply/Ground

Rev. P1.0.5

Rev. P1.0.6 Figures 5,15,31,32 changed resistor values from 36 Ω to 31.6 Ω. Figure 16 changed resistor value 37.5 Ω to 37.4 Ω. Changed the pin names in the pinout diagram and the pin descriptions to include (A)nalog, (D)igital, (Rx)Receive, (Tx)Transmit on VDD and GND pins. Modified some of the pin descriptions. Section 2.5 changed the resistor value from 36 Ω to 31.6 Ω. Revised Transformer Vendor Information.

Rev 1.1.0 - Changed from preliminary to final

Rev 1.2.0 - Changed electrical characteristics tables for Transmit Output Pulse Amplitude (TxLev=0). STS-1 min 0.65V from 0.68V, max 0.90V from 0.85V. DS3 min 0.65V from 0.68V.

Rev. 1.3.0 - Redesigned 73L00A with improved performance and added timing recovery circuit. Added typical Jitter tolerance @800kHz. Receiver Sensitivity (cable length) increased. Part Number changed to XRT73L00A, ordering information changed to XRT73L00AIV.

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