XRT74L74

4 CHANNEL, ATM UNI/PPP DS3/E3 FRAMING CONTROLLER

AUGUST 2001 REV. P1.1.0

GENERAL DESCRIPTION

The XRT74L74 4 Channel, ATM UNI/PPP Physical Layer Processor with integrated DS3/E3 framing controller is designed to support ATM direct mapping and cell delineation as well as PPP mapping and Frame processing. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3/E3 rates. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT74L74 DS3 ATM UNI/Clear-Channel Framer incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive functional sections.

FEATURES

- Compliant with 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface Specifications and supports UTOPIA Bus operating at 25, 33 or 50 MHz
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports ATM cell or PPP Packet Mapping
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola, PowerPC, and Mips µPs
- HDLC controller per channel for Tx and Rx
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 388 pin PBGA Package

APPLICATIONS

- Digital Access and Cross Connect Systems
- Digital, ATM, WAN and LAN Switches
- Network Interface Service Units

FIGURE 1. BLOCK DIAGRAM OF THE XRT74L74 ATM UNI/PPP DS3/E3 FRAMING CONTROLLER

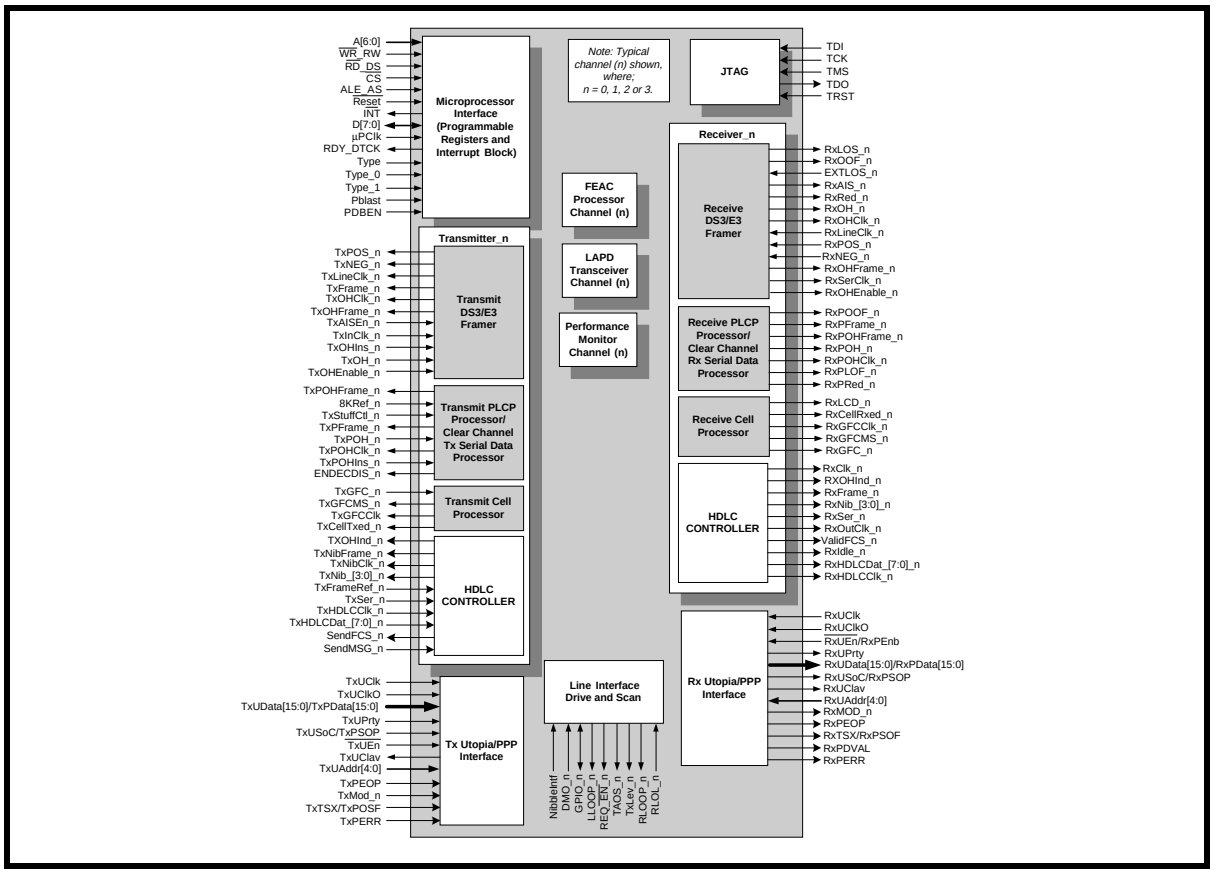
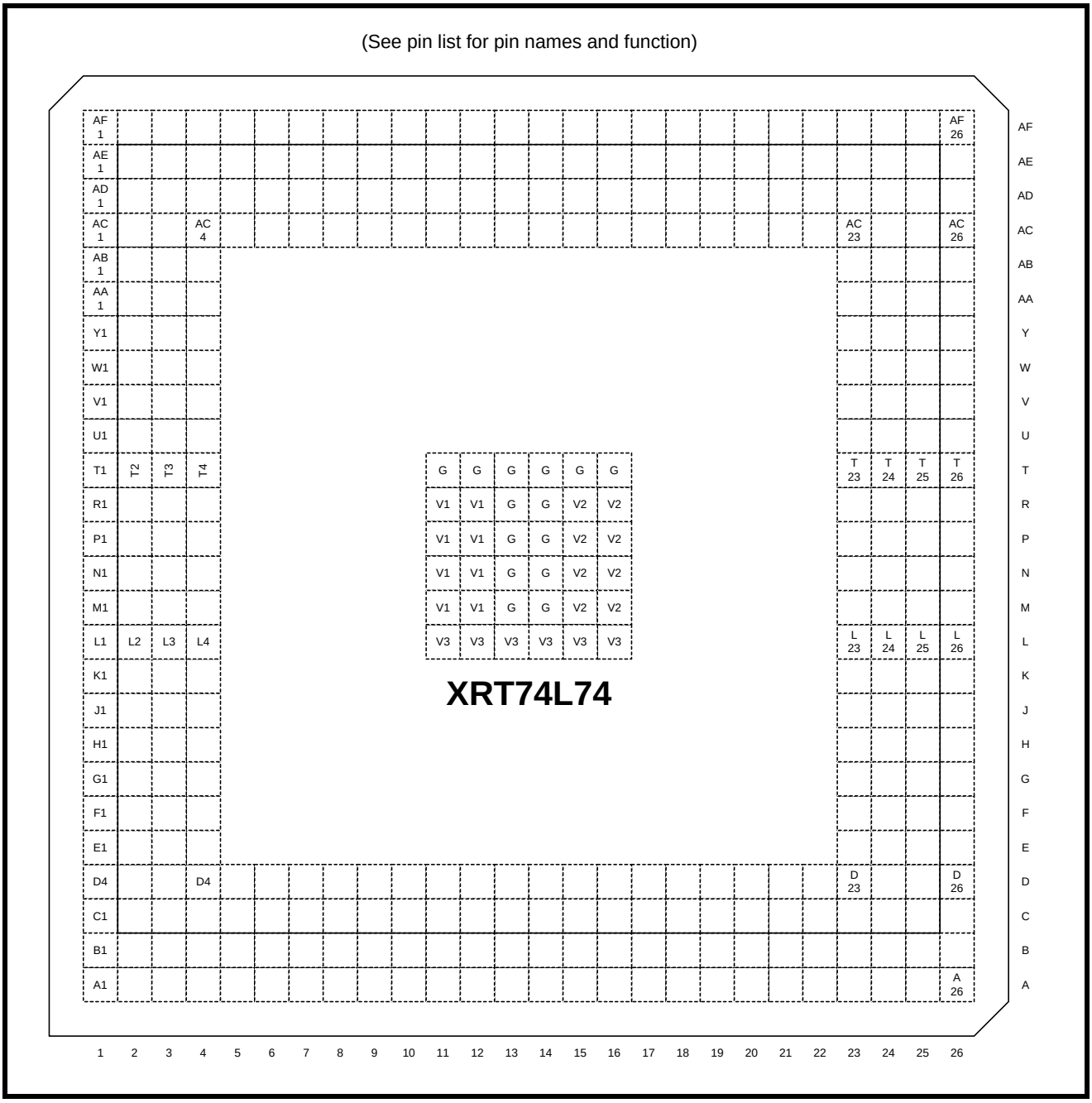


FIGURE 2. PIN OUT OF THE XRT74L74 DS3/E3 ATM UNI/PPP (388 BALL PBGA)



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT74L74IB	35 x 35 mm, 388 Plastic Ball Grid Array	-40°C to +85°C

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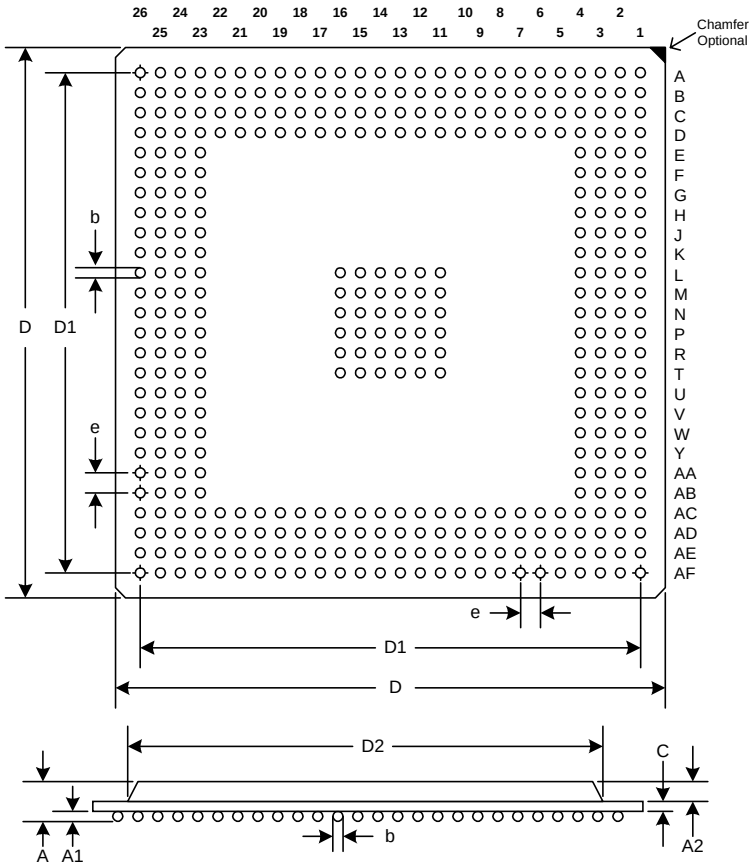
XRT74L74IB	35 x 35 mm, 388 Plastic Ball Grid Array	-40^{0}C to +85^{0}C

PACKAGE DIMENSIONS

388 Ball Plastic Ball Grid Array
(35 x 35 mm PBGA)
Rev. 1.0



Symbol	Inches MIN	Inches MAX	Millimeters MIN	Millimeters MAX
A	0.075	0.106	1.90	2.70
A1	0.020	0.028	0.50	0.70
A2	0.039	0.051	1.00	1.30
b	0.024	0.035	0.60	0.90
C	0.016	0.028	0.40	0.70
D	1.370	1.386	34.80	35.20
D1	1.250BSC		31.75BSC	
D2	1.177	1.185	29.90	30.10
e	0.050BSC		1.27BSC	

Note: The control dimension is the millimeter column

REVISION HISTORY

NOTICE