SIX-CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH SONET DESYNCHRONIZER

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GENERAL DESCRIPTION

The XRT75L06D is a four-channel fully integrated Line Interface Unit (LIU) with Jitter Attenuator for E3/DS3/STS-1 applications. It incorporates six independent Receivers, Transmitters and Jitter Attenuators in a single 208-lead QFP package.

Each channel of the XRT75L06D can be independently configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz) rates. Each transmitter can be turned off and tri-stated for redundancy support and for conserving power.

The XRT75L06D's differential receivers provide high noise interference margin and are able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75L06D incorporates an advanced crystal-less jitter attenuator that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications. Also the jitter attenuator can be used for clock smoothing in SONET STS-1 to DS3 de-mapping.

The XRT75L06D provides Parallel Microprocessor Interface for programming and control.

The XRT75L06D supports local, remote and digital loop-backs. The XRT75L06D also contains an on-board Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error.

FEATURES

Receiver:

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip Clock Synthesizer generates the appropriate rate clock from a single frequency Crystal
- Provides low jitter clock outputs for either E3, DS3 or STS-1 rates
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications

Transmitter:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Transmitter can be turned on or off

Jitter Attenuator:

- On chip advanced crystal-less Jitter Attenuators
- Jitter Attenuators can be selected in Receive or Transmit paths
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755, GR-253 and GR-499-CORE,1995 standards
- Meets ETSI TBR 24 Jitter Transfer Requirements
- 16, 32 or 128 bits selectable FIFO size
- De-Synchronizer for SONET STS-1 to DS3 de-mapping
- Meets the Jitter and Wander specifications described in the ANSI T1.105.03b
- Jitter Attenuators can be disabled

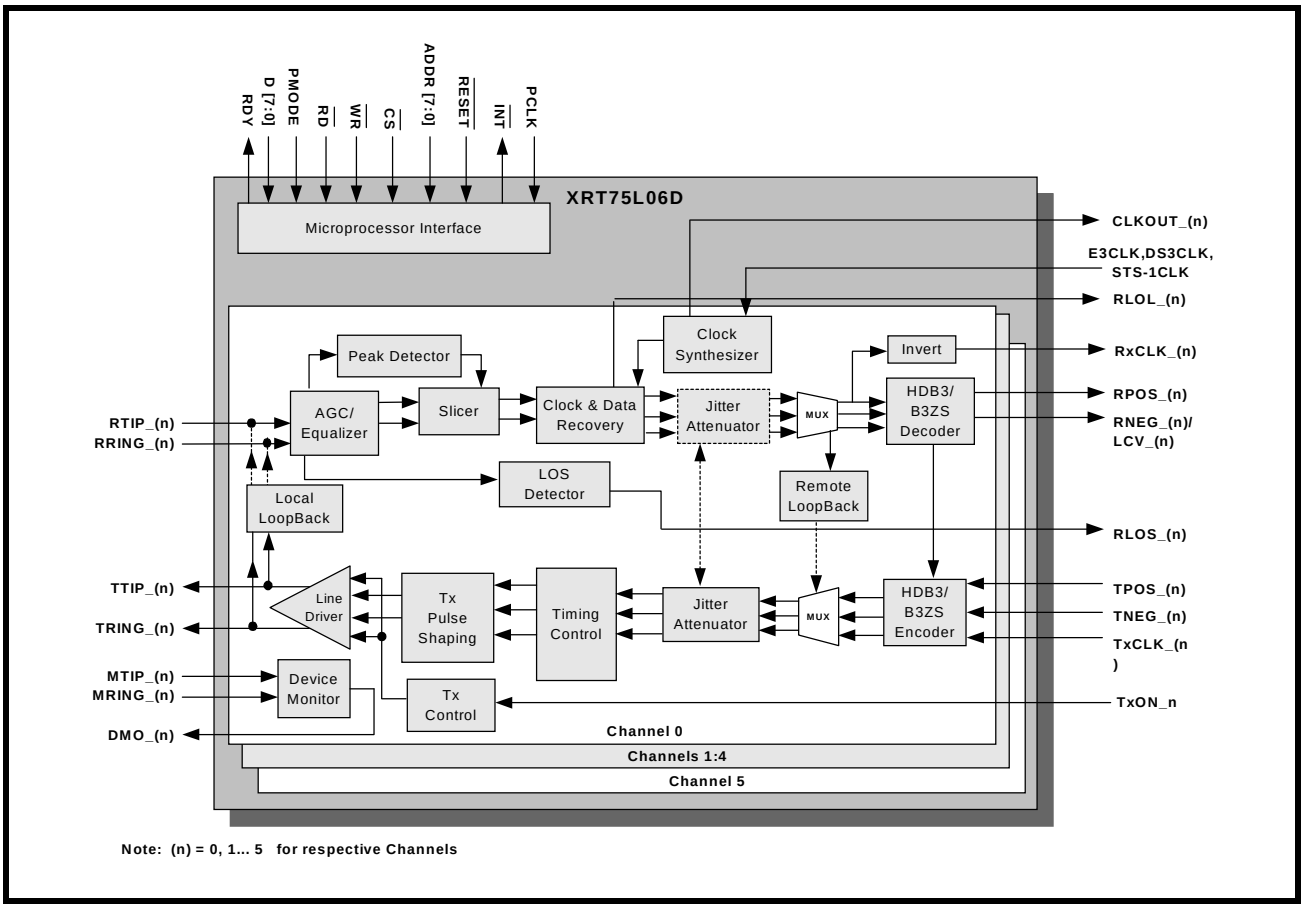
Control and Diagnostics:

- 5 wire Serial Microprocessor Interface for control and configuration
- Supports optional internal Transmit Driver Monitoring
- PRBS Error Counter Register to accumulate errors
- Supports Local, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant I/O
- Available in 208 pin QFP package
- -40°C to 85°C Industrial Temperature Range

APPLICATIONS

- E3/DS3 Access Equipment
- STS1-SPE to DS3 Mapper
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT75L06D



Transmit Interface Characteristics

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

Receive Interface Characteristics

- Integrated Adaptive Receive Equalization for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L06DIQ	208 lead Plastic Quad Flat Pack (28 x 28mm)	-40°C to +85°C