DATA SHEET

APPNOTE TAN-042

Communications

XRT71D00

Single-Chip Jitter Attenuator for High-Speed DS3/E3 WANs

Features
- Accepts "jittery" clock and data from an LIU IC
- Internally reduces clock and data signal jitter
- Outputs "smooth" data to the terminal equipment
- Selectable buffer size of 16- and 32-bits
- Jitter attenuator can be disabled
- Available in 24-pin SOIC, or 32-pin TQFP package
- Single 3.3V, or 5.0V supply

Applications
- ETSI TBR-24 34Mbits/s D34U, and D34S systems
- DS3/E3 Digital multiplex and de-multiplex equipment
- DSLAM
- ATM equipment
- PCM Test equipment
- E3/DS3 Access equipment

Communications systems require maintenance of correct data signals to ensure transmission accuracy. Errors in pulse arrival times, or phase noise can constitute line jitter.

Jitter is caused by many factors: cross-talk noise, imperfect timing recovery circuit or line interface/signal distortion. Typical WAN environments contain many pieces of equipment (nodes). At each point of connection (node), jitter can increase, and as a result, new errors can be introduced into transmitted data. To ensure reliable data reception, jitter must be reduced from the transmitted signal.

Exar's XRT71D00 jitter attenuator circuit provides a fresh approach which promises to match, or outperform other methods, and is considerably easier to deploy at a lower cost. The XRT71D00 meets the European Telecommunication Standards Institute (ETSI), technical committee draft standards TBR24 (34.368 Mbits/sec digital unstructured and structured leased lines. Both TBR24, and Bellcore GR-499 require that terminal equipment, which derives its timing from the received signal at the input port, must not exceed specified output jitter levels. The XRT71D00 performs the jitter attenuation for both E3 (34.368 Mbits/sec) and DS3 (44.736 Mbits/sec)rates enabling development of full standards compliant E3/DS3 products.

The XRT71D00 is targeted at E3/DS3 applications including DSLAM, digital Multiplex and de-Multiplex equipment, ATM equipment, fiber optics and microwave radio terminals, and Pulse Code Modulation (PCM) test equipment.

The XRT71D00 is a fully integrated single-chip jitter attenuator for E3/DS3 applications designed to attenuate the jitter from the incoming clock and data signals. The device is compliant with ETSI TBR-24, ITU-T G.751,752 and 755 as well as the Bellcore GR-499CORE Category I and Category II equipment. It supports both hardware and software modes for configuration control.