DATA SHEET

Communications

XRT72L71

Single-Chip, Single-Channel ATM UNIs for DS3 ATM

Features
- Low-power 3.3V, 5V tolerant inputs
- Supports UTOPIA Level 1 and 2
- Supports DS-3 to Sonet rates
- Seamless interface with Exar's XRT7300 transceiver product family

Applications
- ATM Switch
- ATM Multiplxer
- ATM Routers and Bridges
- SONET/SDH Concentrators
- PDH Mux Line Interface
- Digital Cross Connects
- DS3 Frame Relay Equipment
- Multiservice Platforms

Further cementing its position as an industry-leading provider of innovative User Network Interfaces (UNIs), the XRT72L71/73/74 series is ideal for WANs, the dominant networking infrastructure. In single-, dual-, and quad-channel configurations, this DS3-based product series adds another capability level to Exar's already robust ATM UNI product family.

At DS3-level speeds (44.736 MBPS) and compliance with UTOPIA Level 2 interface specifications, the new devices support not only ATM data cells, but can also transport clear channel data throughout the network. All devices can easily interface with leading processors, and support burst mode operation. In addition, all three parts interface seamlessly with Exar's industry leading portfolio of DS3 LIUs and jitter attenuators providing the most complete line up of DS3 physical layer products in the industry.

This multi-channel ATM UNI family supports DS3 applications and equipment running at Sonet rates. They perform all the Transmission Coverage (TC) sublayer functions: cell rate decoupling, cell header processing, cell delineation and transmission frame adaptation/recover. Distinctive of the new devices are an extensive diagnostic capability. Specifically the multi-channel ATM UNIs support Organization, Management and Administration (OAM) at the network management level. There are a series of tests that can be conducted including: test cell generation, cell and PLCP frame loopbacks, as well as tracking errors, line code violations and idle/valid cell statistics.

The family performs parity checking of ATM cells, contains on-chip 16-cell FIFO (configurable in depths of 4-, 8-, 12-, 16-cells) ion moth transmit and receive directions. Additionally, the devices have an on-chip 54-byte transmit and receive OAM cell buffer, and support M13, or C-bit parity framing formats.

All devices are low-power, 3.3V with 5V tolerant inputs, and support both 8- and 16-bit Intel, or Motorola microprocessor/microcontroller buses.