DATA SHEET

Communications

XRT75L00D

Single-Chip Desynchronizer and Jitter Attenuator for Mapping/Demapping between SONET/SDH and DS3/E3 Environments

Features:
Receiver:
- On-Chip Clock and Data Recovery Circuit for High-Input Jitter Tolerance On-Chip B3ZS/HDB3 Encoder/Decoder Can be Disabled or Enabled Transmitter: Tri-state Transmit Output Capability for Redundancy Applications Transmitter Can be Turned On or Off

Jitter Attenuator:
- Jitter Attenuator Can be Selected in Receive or Transmit Paths Selectable FIFO Size of 16 or 32 Bits

Control and Diagnostics:
- Five Wire Serial Microprocessor for Control and Configuration Supports Optional Internal Transmit Driver Monitoring

Applications:
- E3/DS3 Access Equipment
- STS-1-SPE to DS# Mapper
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSC Equipment
- Routers
- Fiber Optic Terminals

Recognized for an already robust series of physical layer, access and metro products, Exar extends its capabilities by releasing the industry's first monolithic desynchronization solution for mapping/demaping from SONET/SDH (synchronous) to DS3/E3 (asynchronous). The XRT75L00D is a single-channel DS3/E3/STS-1 Line Interface Unit (LIU). Using an innovative combination of analog and digital signal processing technologies this new approach will be embedded in Exar's physical interface and data aggregation devices.

The XRT75L00 is the next generation solution for the design challenges presented by jitter. Previously, Exar launched the XRT71D00, the industry's first standards compliant jitter attenuator for DS3/E3 applications. It was soon followed by the industry's first multi-channel jitter attenuators (XRT71D03 and XRT71D04).

What is Clock Desynchronization?
The process of mapping and subsequent de-mapping of DS3/E3 signals into SONET introduces excessive jitter and timing irregularities. Examples of jitter sources include mapping jitter, caused by bit justification, or stuffing, and pointer jitter, the outcome of frequency mismatches between networks that causes pointer movement. Current desynchronizing solutions use both a very narrow-bandwidth crystal oscillator based Phase Locked Loop (PLL) referred to as a Voltage Control Oscillator (VCXO), and a deep FIFO for each data rate and channel. For multi-channel/multi-rate applications, chip requirements can rise at exponential levels driven by the number of supported rates and channels. Enter Exar's solution; it uses only one highly integrated programmable PLL, now each channel can support multi-rate (DS3, E3 or STS-1) operations. Here jitter/timing irregularities are removed, and then desynchronized to provide a smooth GR-253-CORE specification-compliant clock signal. Once this operation is complete the signal is suitable for retransmission and returned to the data stream.

Product Highlights
The XRT75L00D has an independent receiver, transmitter and jitter attenuator in a single 52-pin TQFP package. It supports E3 (34.368.Mbps), DS3 (44.736Mbps) and STS-1 (51.84 Mbps) operations, has a differential receiver which provides a high noise interference margins — capable of receiving data from cables of over 1,000 feet, or up to 12dB of cable attenuation. The device has an onboard Pseudo Random Binary Sequence (PRBS) generator and detector that can insert and detect single bit errors. This function is often used for diagnostic purposes. The XRT75L00D provides both serial microprocessor interface as well as hardware mode for additional programming and control. It also supports local, remote and digital loop-backs.

Standard's Compliance
The receiver, transmitter, and jitter attenuator all meet Bellcore GR-499 CORE requirements. Also, the transmitter meets the GR-253 CORE and ANSI T1.102 specifications and it includes a duty cycle correction PLL. The device meets jitter and wander specifications described in the T1.105.03b, and ETSI TBR-24, and is compliant with jitter transfer templates outlined in ITU G.751, G.752 and G.755.