

**FEATURES**

- Wide Frequency Range, 0.01Hz to 300kHz
- Wide Supply Voltage Range, 4.5V to 20V
- HCMOS/TTL/Logic Compatibility
- FSK Demodulation, with Carrier Detection
- Wide Dynamic Range, 10mV to 3V rms
- Adjustable Tracking Range ( $\pm 1\%$  to 80%)
- Excellent Temp. Stability, 100 ppm/ $^{\circ}\text{C}$ , typ.

**APPLICATIONS**

- Caller Identification Delivery
- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

**GENERAL DESCRIPTION**

The XR-2211A is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 10mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a

quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply is provided at an output pin.

The XR-2211A is available in 14 pin packages specified for commercial temperature ranges.

**ORDERING INFORMATION**

Part No.	Package	Operating Temperature Range
XR-2211ACP	14 Lead PDIP (0.300")	0 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$
XR-2211ACD	14 Lead SOIC (Jedec, 0.150")	0 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$

## BLOCK DIAGRAM

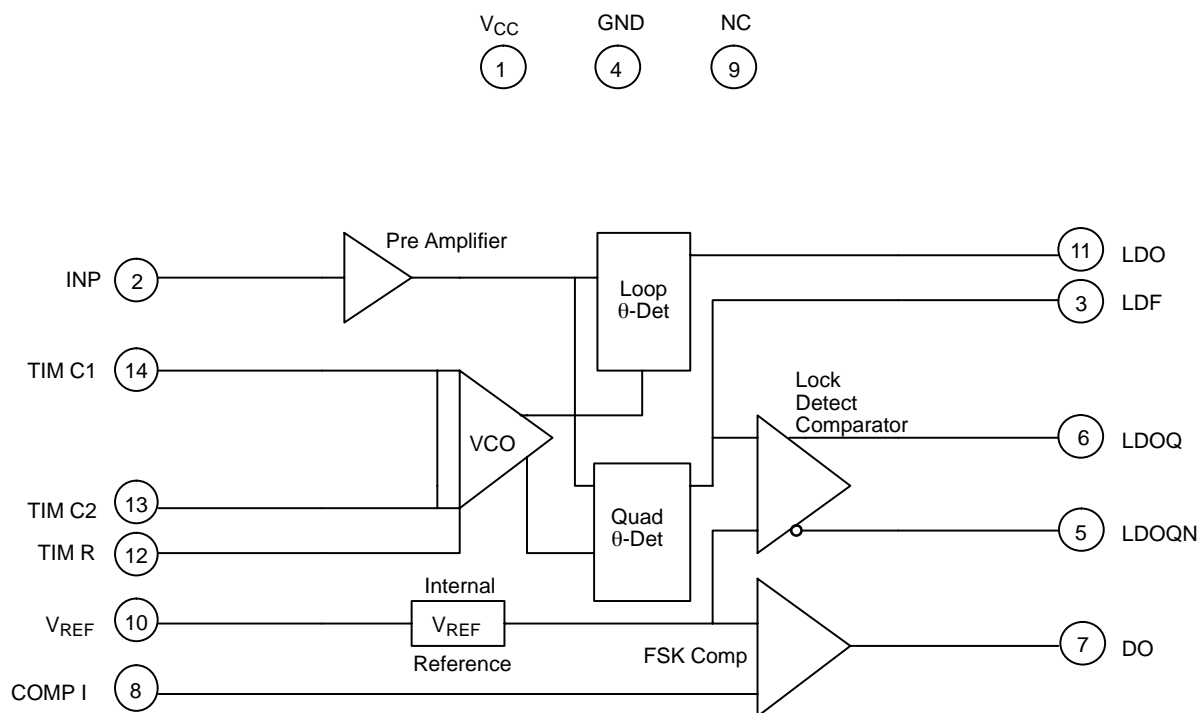
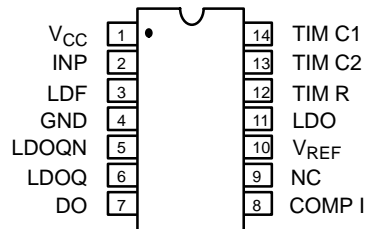
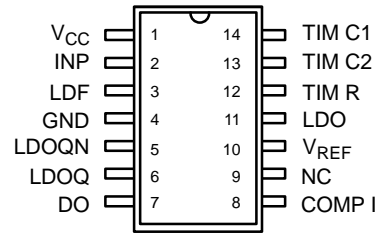


Figure 1. XR-2211A Block Diagram

## PIN CONFIGURATION



14 Lead PDIP (0.300")



14 Lead SOIC (Jedec, 0.150")

## PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	V <sub>CC</sub>		<b>Positive Power Supply.</b>
2	INP	I	<b>Receive Analog Input.</b>
3	LDF	O	<b>Lock Detect Filter.</b>
4	GND		<b>Ground Pin.</b>
5	LDOQN	O	<b>Lock Detect Output Not.</b> This output will be low if the VCO is in the capture range.
6	LDOQ	O	<b>Lock Detect Output.</b> This output will be high if the VCO is in the capture range.
7	DO	O	<b>Data Output.</b> Decoded FSK output.
8	COMP I	I	<b>FSK Comparator Input.</b>
9	NC		<b>Not Connected.</b>
10	V <sub>REF</sub>	O	<b>Internal Voltage Reference.</b> The value of V <sub>REF</sub> is V <sub>CC</sub> /2 - 650mV.
11	LDO	O	<b>Loop Detect Output.</b> This output provides the result of the quadrature phase detection.
12	TIM R	I	<b>Timing Resistor Input.</b> This pin connects to the timing resistor of the VCO.
13	TIM C2	I	<b>Timing Capacitor Input.</b> The timing capacitor connects between this pin and pin 14.
14	TIM C1	I	<b>Timing Capacitor Input.</b> The timing capacitor connects between this pin and pin 13.

## PDC ELECTRICAL CHARACTERISTICS

Test Conditions:  $V_{CC} = 12V$ ,  $T_A = +25^\circ C$ ,  $R_O = 30K\Omega$ ,  $C_O = 0.033\mu F$ , unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
<b>General</b>					
Supply Voltage	<b>4.5</b>		<b>20</b>	V	
Supply Current		5	<b>9</b>	mA	$R_O \geq 10K\Omega$ . See <i>Figure 4</i> .
<b>Oscillator Section</b>					
Frequency Accuracy		$\pm 3$		%	Deviation from $f_O = 1/R_O C_O$
Frequency Stability					
Temperature		$\pm 100$		ppm/ $^\circ C$	See <i>Figure 8</i>
Power Supply		0.25		%/V	$V_{CC} = 12 \pm 1V$ . See <i>Figure 7</i> .
		0.2		%/V	$V_{CC} = \pm 5.0V$ . See <i>Figure 7</i> .
Upper Frequency Limit		300		kHz	$R_O = 8.2K\Omega$ , $C_O = 400pF$
Lowest Practical					
Operating Frequency		0.01		Hz	$R_O = 2M\Omega$ , $C_O = 50\mu F$
Timing Resistor, $R_O$ - See <i>Figure 5</i>					
Operating Range	<b>5</b>		2000	K $\Omega$	
Recommended Range	5		100	K $\Omega$	See <i>Figure 7</i> and <i>Figure 8</i> .
<b>Loop Phase Detector Section</b>					
Peak Output Current	<b><math>\pm 100</math></b>	$\pm 200$	<b><math>\pm 300</math></b>	$\mu A$	Measured at Pin 11
Output Offset Current		$\pm 2$		$\mu A$	
Output Impedance		1		M $\Omega$	
Maximum Swing	<b><math>\pm 4</math></b>	$\pm 5$		V	Referenced to Pin 10
<b>Quadrature Phase Detector</b>					Measured at Pin 3
Peak Output Current		300		$\mu A$	
Output Impedance		1		M $\Omega$	
Maximum Swing		11		V <sub>PP</sub>	
<b>Input Preampt Section</b>					Measured at Pin 2
Input Impedance		20		K $\Omega$	
Input Signal					
Voltage Required to Cause Limiting		2		mV rms	

**Notes**

Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.

**Bold face parameters** are covered by production test and guaranteed over operating temperature range.

## DC ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions:  $V_{CC} = 12V$ ,  $T_A = +25^{\circ}C$ ,  $R_O = 30K\Omega$ ,  $C_O = 0.033\mu F$ , unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
<b>Voltage Comparator Section</b>					
Input Impedance		2		M $\Omega$	Measured at Pins 3 and 8
Input Bias Current		100		nA	
Voltage Gain	55	70		dB	$R_L = 5.1K\Omega$
Output Voltage Low		300	<b>500</b>	mV	$I_C = 3mA$
Output Leakage Current		0.01	<b>10</b>	$\mu A$	$V_O = 20V$
<b>Internal Reference</b>					
Voltage Level	<b>4.75</b>	5.3	<b>5.85</b>	V	Measured at Pin 10
Output Impedance		100		$\Omega$	AC Small Signal
Maximum Source Current		80		$\mu A$	

### Notes

Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.

**Bold face parameters** are covered by production test and guaranteed over operating temperature range.

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS

Power Supply ..... 20V  
 Input Signal Level ..... 3V rms  
 Power Dissipation ..... 900mW

Plastic Package ..... 800mW  
 Derate Above  $T_A = 25^{\circ}C$  ..... 6mW/ $^{\circ}C$   
 JEDEC SOIC ..... 390mW  
 Derate Above  $T_A = 25^{\circ}C$  ..... 5mW/ $^{\circ}C$

## SYSTEM DESCRIPTION

The main PLL within the XR-2211A is constructed from an input preamplifier, analog multiplier used as a phase detector and a precision voltage controlled oscillator (VCO). The preamplifier is used as a limiter such that input signals above typically 10mV rms are amplified to a constant high level signal. The multiplying-type phase detector acts as a digital exclusive or gate. Its output (unfiltered) produces sum and difference frequencies of the input and the VCO output. The VCO is actually a current controlled oscillator with its normal input current ( $f_O$ ) set by a resistor ( $R_O$ ) to ground and its driving current with a resistor ( $R_1$ ) from the phase detector.

The output of the phase detector produces sum and difference of the input and the VCO frequencies

(internally connected). When in lock, these frequencies are  $f_{IN} + f_{VCO}$  (2 times  $f_{IN}$  when in lock) and  $f_{IN} - f_{VCO}$  (0Hz when lock). By adding a capacitor to the phase detector output, the 2 times  $f_{IN}$  component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The FSK comparator is used to determine if the VCO is driven above or below the center frequency (FSK comparator). This will produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

## PRINCIPLES OF OPERATION

**Signal Input (Pin 2):** Signal is AC coupled to this terminal. The internal impedance at pin 2 is 20K $\Omega$ . Recommended input signal level is in the range of 10mV rms to 3V rms.

**Quadrature Phase Detector Output (Pin 3):** This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of  $R_D$  and  $C_D$  (see *Figure 3*) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, pin 3 can be left open.

**Lock Detect Output, Q (Pin 6):** The output at pin 6 is at "low" state when the PLL is out of lock and goes to "high" state when the PLL is locked. It is an open collector type output and requires a pull-up resistor,  $R_L$ , to  $V_{CC}$  for proper operation. At "low" state, it can sink up to 5mA of load current.

**Lock Detect Complement, (Pin 5):** The output at pin 5 is the logic complement of the lock detect output at pin 6. This output is also an open collector type stage which can sink 5mA of load current at low or "on" state.

**FSK Data Output (Pin 7):** This output is an open collector logic stage which requires a pull-up resistor,  $R_L$ , to  $V_{CC}$  for proper operation. It can sink 5mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

**FSK Comparator Input (Pin 8):** This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by  $R_F$  and  $C_F$  (see *Figure 3*). The threshold voltage of the comparator is set by the internal reference voltage,  $V_{REF}$ , available at pin 10.

**Reference Voltage,  $V_{REF}$  (Pin 10):** This pin is internally biased at the reference voltage level,  $V_{REF}$ :  $V_{REF} = V_{CC}/2 - 650mV$ . The DC voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin

10 must be bypassed to ground with a 0.1 $\mu F$  capacitor for proper operation of the circuit.

**Loop Phase Detector Output (Pin 11):** This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by  $R_1$  and  $C_1$  connected to pin 11 (see *Figure 3*). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to  $V_{REF}$ . The peak to peak voltage swing available at the phase detector output is equal to  $2 \times V_{REF}$ .

**VCO Control Input (Pin 12):** VCO free-running frequency is determined by external timing resistor,  $R_0$ , connected from this terminal to ground. The VCO free-running frequency,  $f_O$ , is:

$$f_O = \frac{1}{R_0 \cdot C_0} \text{ Hz}$$

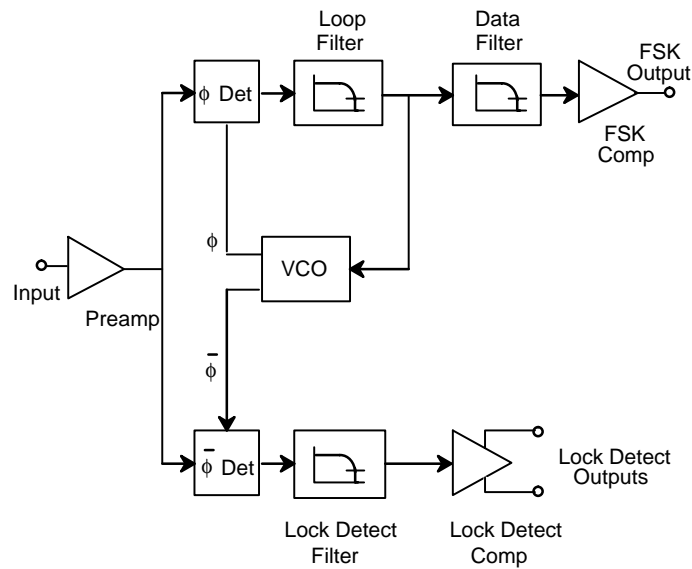
where  $C_0$  is the timing capacitor across pins 13 and 14. For optimum temperature stability,  $R_0$  must be in the range of 10K $\Omega$  to 100K $\Omega$  (see *Figure 9*).

This terminal is a low impedance point, and is internally biased at a DC level equal to  $V_{REF}$ . The maximum timing current drawn from pin 12 must be limited to  $\leq 3mA$  for proper operation of the circuit.

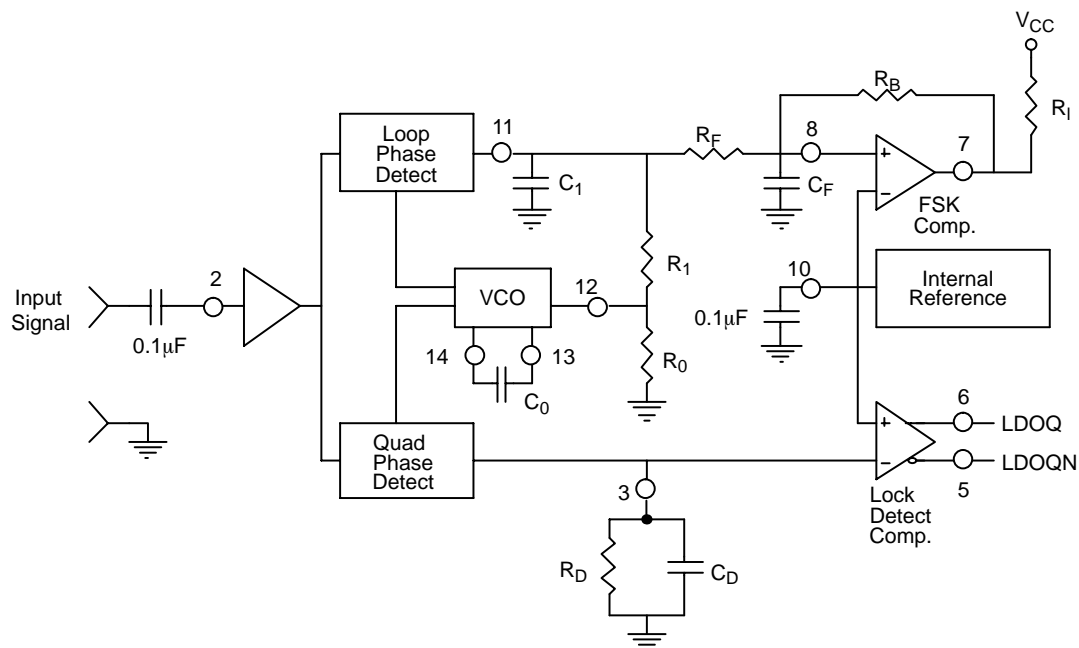
**VCO Timing Capacitor (Pins 13 and 14):** VCO frequency is inversely proportional to the external timing capacitor,  $C_0$ , connected across these terminals (see *Figure 6*).  $C_0$  must be non-polar, and in the range of 200pF to 10 $\mu F$ .

**VCO Frequency Adjustment:** VCO can be fine-tuned by connecting a potentiometer,  $R_X$ , in series with  $R_0$  at pin 12 (see *Figure 10*).

**VCO Free-Running Frequency,  $f_O$ :** XR-2211A does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment purposes, the VCO free-running frequency can be tuned by using the generalized circuit in *Figure 3*, and applying an alternating bit pattern of 0's and 1's at the known mark and space frequencies. By adjusting  $R_0$ , the VCO can then be tuned to obtain a 50% duty cycle on the FSK output (pin 7). This will ensure that the VCO  $f_O$  value is accurately referenced to the mark and space frequencies.



**Figure 2. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211A**



**Figure 3. Generalized Circuit Connection for FSK and Tone Detection**

## DESIGN EQUATIONS

(All resistance in  $\Omega$ , all frequency in Hz and all capacitance in farads, unless otherwise specified)

(See *Figure 3* for definition of components)

1. VCO Center Frequency,  $f_O$ :

$$f_O = \frac{1}{R_0 \cdot C_0}$$

2. Internal Reference Voltage,  $V_{REF}$  (measured at pin 10):

$$V_{REF} = \left( \frac{V_{CC}}{2} \right) - 650mV \text{ in volts}$$

3. Loop Low-Pass Filter Time Constant,  $\tau$ :

$$\tau = C_1 \cdot R_{PP} \text{ (seconds)}$$

where:

$$R_{PP} = \left( \frac{R_1 \cdot R_F}{R_1 + R_F} \right)$$

if  $R_F$  is  $\infty$  or  $C_F$  reactance is  $\infty$ , then  $R_{PP} = R_1$

4. Loop Damping,  $\zeta$ :

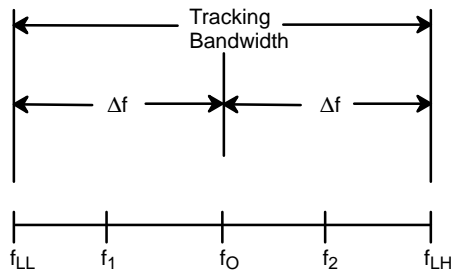
$$\zeta = \sqrt{\left( \frac{1250 \cdot C_0}{R_1 \cdot C_1} \right)}$$

**Note:** For derivation/explanation of this equation, please see TAN-011.

5. Loop-tracking

bandwidth,  $\pm = \frac{\Delta f}{f_0}$

$$\frac{\Delta f}{f_0} = \frac{R_0}{R_1}$$





6. FSK Data filter time constant,  $t_F$ :

$$\tau_F = \frac{R_B \cdot R_F}{(R_B + R_F)} \cdot C_F \text{ (seconds)}$$

7. Loop phase detector conversion gain,  $K_d$ : ( $K_d$  is the differential DC voltage across pin 10 and pin11, per unit of phase error at phase detector input):

$$K_d = \frac{V_{REF} \cdot R_1}{10,000 \cdot \pi} \left[ \frac{\text{volt}}{\text{radian}} \right]$$

**Note:** For derivation/explanation of this equation, please see TAN-011.

8. VCO conversion gain,  $K_o$ : ( $K_o$  is the amount of change in VCO frequency, per unit of DC voltage change at pin 11):

$$K_o = \frac{-2\pi}{V_{REF} \cdot C_0 \cdot R_1} = \left( \frac{\text{radian/second}}{\text{volt}} \right)$$

9. The filter transfer function:

$$F(s) = \frac{1}{1 + sR_1 \cdot C_1} \text{ at } 0 \text{ Hz.} \quad S = j\omega \text{ and } \omega = 0$$

10. Total loop gain.  $K_T$ :

$$K_T = K_o \cdot K_d \cdot F(s) = \left( \frac{R_F}{5,000 \cdot C_0 \cdot (R_1 + R_F)} \right) \left[ \frac{1}{\text{seconds}} \right]$$

11. Peak detector current  $I_A$ :

$$I_A = \frac{V_{REF}}{20,000} \text{ (} V_{REF} \text{ in volts and } I_A \text{ in amps)}$$

**Note:** For derivation/explanation of this equation, please see TAN-011.

## APPLICATIONS INFORMATION

### FSK Decoding

Figure 10 shows the basic circuit connection for FSK decoding. With reference to Figure 3 and Figure 10, the functions of external components are defined as follows:  $R_0$  and  $C_0$  set the PLL center frequency,  $R_1$  sets the system bandwidth, and  $C_1$  sets the loop filter time constant and the loop damping factor.  $C_F$  and  $R_F$  form a one-pole post-detection filter for the FSK data output. The resistor  $R_B$  from pin 7 to pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

### Design Instructions:

The circuit of Figure 10 can be tailored for any FSK decoding application by the choice of five key circuit components:  $R_0$ ,  $R_1$ ,  $C_0$ ,  $C_1$  and  $C_F$ . For a given set of FSK mark and space frequencies,  $f_0$  and  $f_1$ , these parameters can be calculated as follows:

(All resistance in  $\Omega$ 's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

- a) Calculate PLL center frequency,  $f_0$ :

$$f_0 = \sqrt{F_1 \cdot F_2}$$

- b) Choose value of timing resistor  $R_0$ , to be in the range of 10K $\Omega$  to 100K $\Omega$ . This choice is arbitrary. The recommended value is  $R_0 = 20K\Omega$ . The final value of  $R_0$  is normally fine-tuned with the series potentiometer,  $R_X$ .

$$R_o = R_o + \frac{R_X}{2}$$

- c) Calculate value of  $C_0$  from design equation (1) or from Figure 7:

$$C_o = \frac{1}{R_o \cdot f_0}$$

- d) Calculate  $R_1$  to give the desired tracking bandwidth (See design equation 5).

$$R_1 = \frac{R_o \cdot f_0}{(f_1 - f_2)} \cdot 2$$

- e) Calculate  $C_1$  to set loop damping. (See design equation 4):

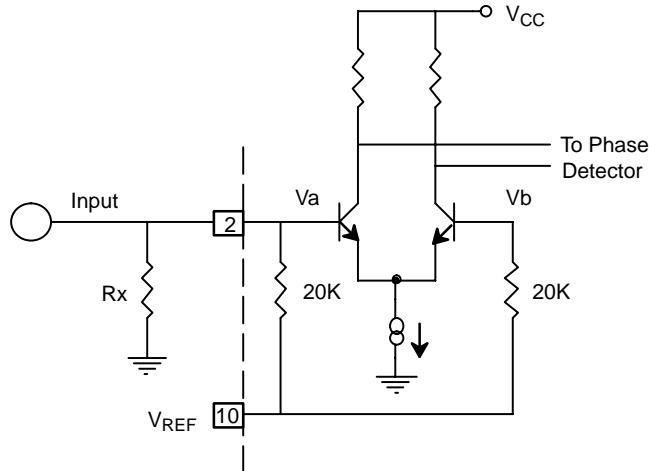
Normally,  $\zeta = 0.5$  is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \zeta^2}$$

- f) The input to the XR-2211A may sometimes be too sensitive to noise conditions on the input line. *Figure 4* illustrates a method of de-sensitizing the XR-2211A from such noisy line conditions by the use of a resistor,  $R_x$ , connected from pin 2 to ground. The value of  $R_x$  is chosen by the equation and the desired minimum signal threshold level.

$$V_{IN} \text{ minimum (peak)} = V_a - V_b = \Delta V \pm 2.8mV \text{ offset} = V_{REF} \frac{20,000}{(20,000 + R_x)} \text{ or } R_x = 20,000 \left( \frac{V_{REF}}{\Delta V} - 1 \right)$$

$V_{IN}$  minimum (peak) input voltage must exceed this value to be detected (equivalent to adjusting V threshold)



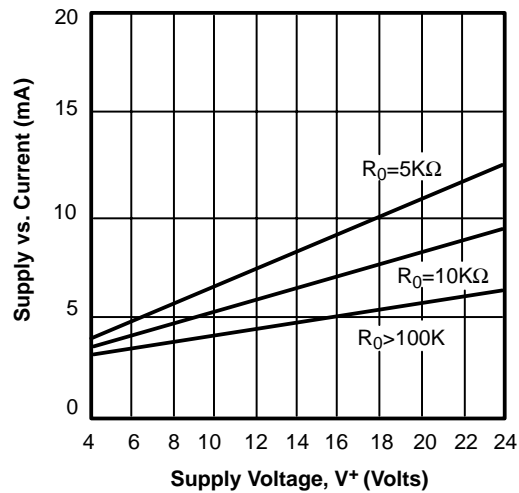
**Figure 4. Desensitizing Input Stage**

- g) Calculate Data Filter Capacitance,  $C_F$ :

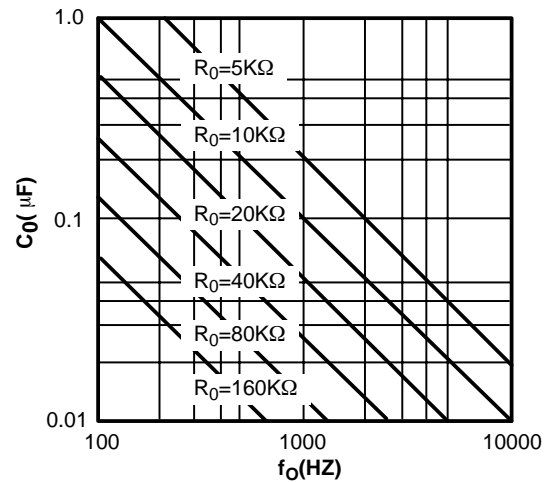
$$R_{sum} = \frac{(R_F + R_1) \cdot R_B}{(R_1 + R_F + R_B)}$$

$$C_F = \frac{0.25}{(R_{sum} \cdot \text{Baud Rate})} \quad \text{Baud rate in } \frac{1}{\text{seconds}}$$

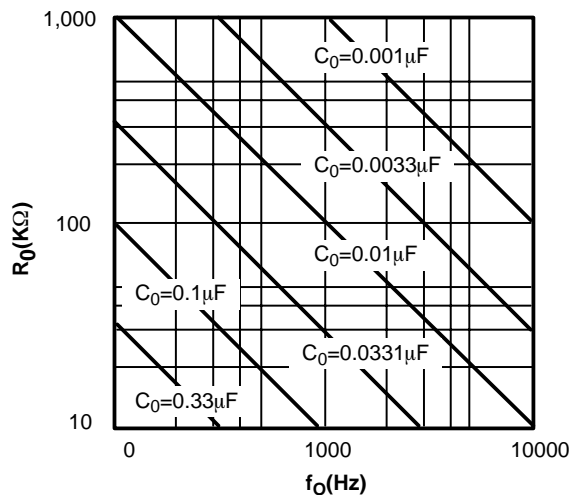
**Note:** All values except  $R_0$  can be rounded to nearest standard value.



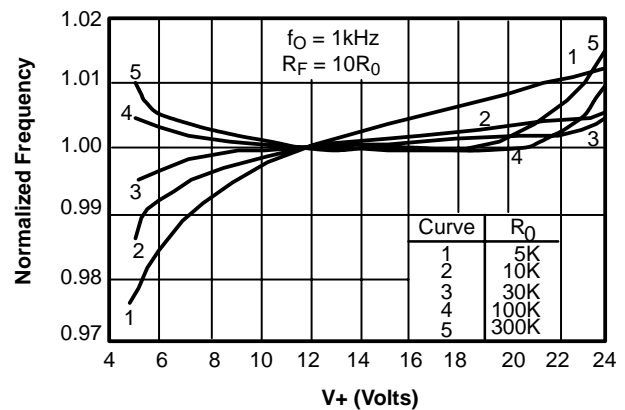
**Figure 5. Typical Supply Current vs. V+ (Logic Outputs Open Circuited)**



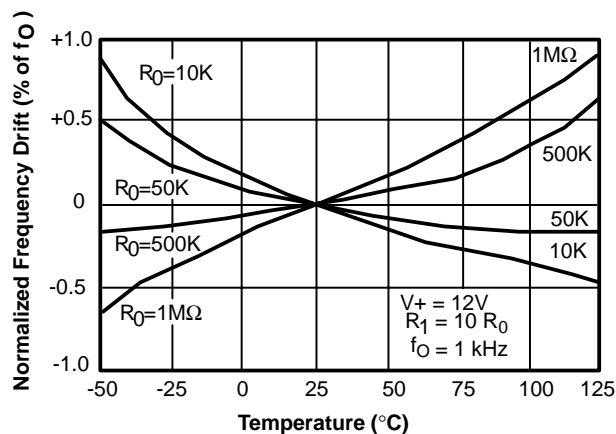
**Figure 6. VCO Frequency vs. Timing Resistor**



**Figure 7. VCO Frequency vs. Timing Capacitor**



**Figure 8. Typical  $f_0$  vs. Power Supply Characteristics**



**Figure 9. Typical Center Frequency Drift vs. Temperature**

**Design Example:****1200 Baud FSK demodulator with mark and space frequencies of 1200/2200.**Step 1: Calculate  $f_O$ : from design instructions

$$(a) \quad f_O = \sqrt{1200 \cdot 2200} = 1624$$

Step 2: Calculate  $R_0$ :  $R_0 = 10K$  with a potentiometer of 10K. (See design instructions (b))

$$(b) \quad R_T = 10 + \left(\frac{10}{2}\right) = 15K$$

Step 3: Calculate  $C_0$  from design instructions

$$(c) \quad C_O = \frac{1}{15000 \cdot 1624} = 39nF$$

Step 4: Calculate  $R_1$ : from design instructions

$$(d) \quad R_1 = \frac{20000 \cdot 1624 \cdot 2}{(2200 - 1200)} = 51,000$$

Step 5: Calculate  $C_1$ : from design instructions

$$(e) \quad C_1 = \frac{1250 \cdot 39nF}{51000 \cdot 0.5^2} = 3.9nF$$

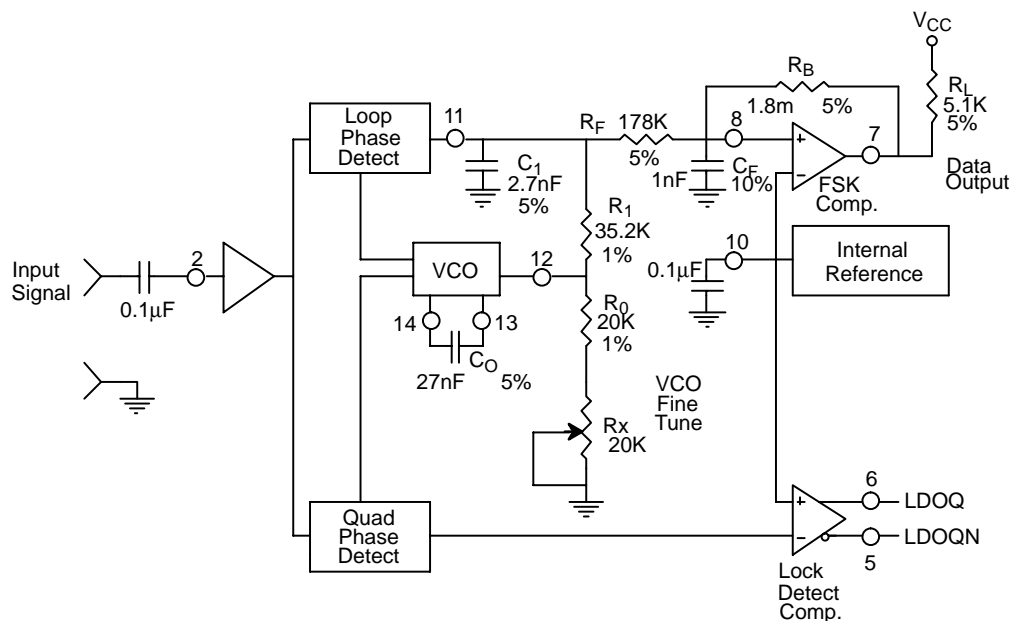
Step 6: Calculate  $R_F$ :  $R_F$  should be at least five times  $R_1$ ,  $R_F = 51,000 \cdot 5 = 255 K\Omega$ Step 7: Calculate  $R_B$ :  $R_B$  should be at least five times  $R_F$ ,  $R_B = 255,000 \cdot 5 = 1.2 M\Omega$ Step 8: Calculate  $R_{SUM}$ :

$$R_{SUM} = \frac{(R_F + R_1) \cdot R_B}{(R_F + R_1 + R_B)} = 240K\Omega$$

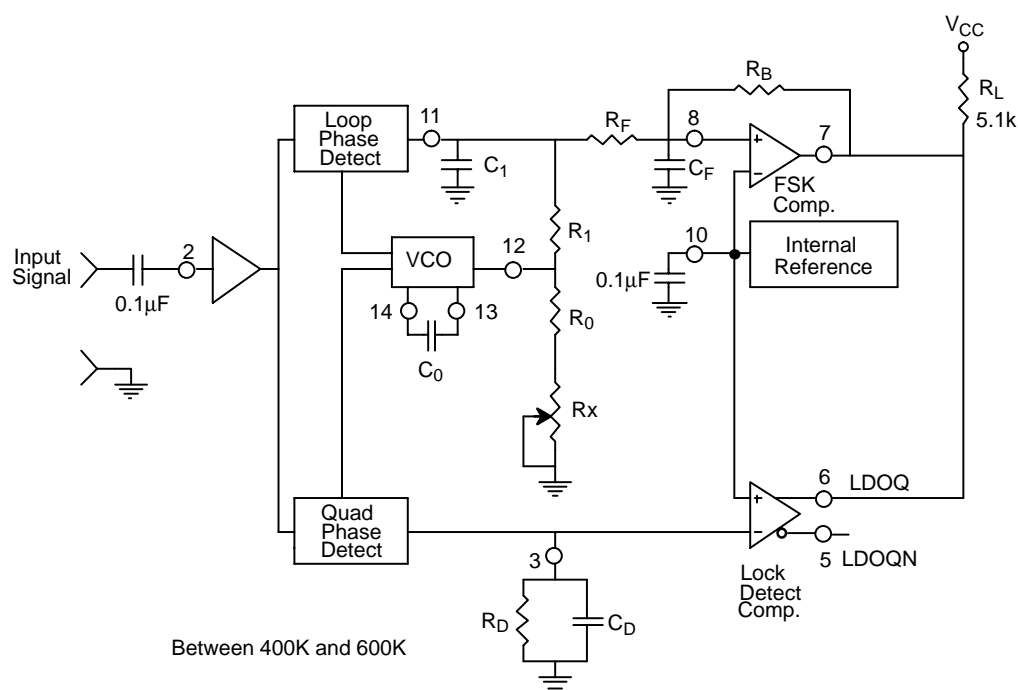
Step 9: Calculate  $C_F$ :

$$C_F = \frac{0.25}{(R_{SUM} \text{ Baud Rate})} = 1nF$$

**Note:** All values except  $R_0$  can be rounded to nearest standard value.



**Figure 10. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)**



**Figure 11. External Connectors for FSK Demodulation with Carrier Detect Capability**

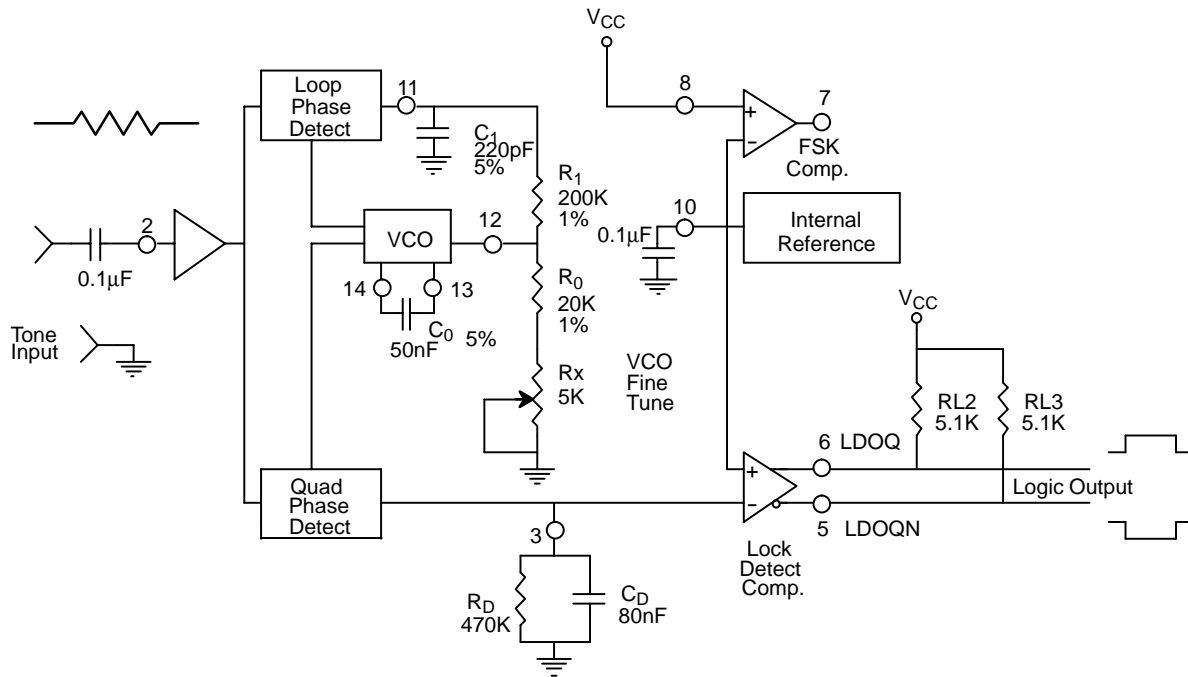


Figure 12. Circuit Connection for Tone Detection

### FSK Decoding with Carrier Detect

The lock detect section of XR-2211A can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 11. The open collector lock detect output, pin 6, is shorted to data output (pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL and the pin 6 output goes "high" to enable the data output.

**Note:** Data Output is "Low" When No Carrier is Present.

The minimum value of the lock detect filter capacitance  $C_D$  is inversely proportional to the capture range,  $\pm\Delta f_c$ . This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by  $C_1$ . For most applications,  $\Delta f_c > \Delta f/2$ . For  $R_D = 470K\Omega$ , the approximate minimum value of  $C_D$  can be determined by:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F \text{ and } f \text{ in Hz.}$$

$C$  in  $\mu F$  and  $f$  in Hz.

With values of  $C_D$  that are too small, chatter can be observed on the lock detect output as an incoming signal

frequency approaches the capture bandwidth. Excessively large values of  $C_D$  will slow the response time of the lock detect output. For Caller I.D. applications choose  $C_D = 0.1\mu F$ .

### Tone Detection

Figure 12 shows the generalized circuit connection for tone detection. The logic outputs, LDOQN and LDOQ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both outputs at pins 5 and 6 are open collector type stages, and require external pull-up resistors  $R_{L2}$  and  $R_{L3}$ , as shown in Figure 12.

With reference to Figure 3 and Figure 12, the functions of the external circuit components can be explained as follows:  $R_0$  and  $C_0$  set VCO center frequency;  $R_1$  sets the detection bandwidth;  $C_1$  sets the low pass-loop filter time constant and the loop damping factor.

## Design Instructions:

The circuit of *Figure 12* can be optimized for any tone detection application by the choice of the 5 key circuit components:  $R_0$ ,  $R_1$ ,  $C_0$ ,  $C_1$  and  $C_D$ . For a given input, the tone frequency,  $f_S$ , these parameters are calculated as follows:

(All resistance in  $\Omega$ 's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

- Choose value of timing resistor  $R_0$  to be in the range of 10K $\Omega$  to 50K $\Omega$ . This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is  $R_0 = 20K\Omega$ . The final value of  $R_0$  is normally fine-tuned with the series potentiometer,  $R_X$ .
- Calculate value of  $C_0$  from design equation (1) or from *Figure 7*  $f_S = f_O$ :

$$C_0 = \frac{1}{R_0 \cdot f_S}$$

- Calculate  $R_1$  to set the bandwidth  $\pm \Delta f$  (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0 \cdot 2}{\Delta f}$$

**Note:** The total detection bandwidth covers the frequency range of  $f_O \pm \Delta f$

- Calculate value of  $C_1$  for a given loop damping factor:

Normally,  $\zeta = 0.5$  is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \zeta^2}$$

Increasing  $C_1$  improves the out-of-band signal rejection, but increases the PLL capture time.

- Calculate value of the filter capacitor  $C_D$ . To avoid chatter at the logic output, with  $R_D = 470K\Omega$ ,  $C_D$  must be:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F$$

Increasing  $C_D$  slows down the logic output response time.

## Design Examples:

Tone detector with a detection band of  $\pm 100\text{Hz}$ :

- Choose value of timing resistor  $R_0$  to be in the range of 10K $\Omega$  to 50K $\Omega$ . This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is  $R_0 = 20K\Omega$ . The final value of  $R_0$  is normally fine-tuned with the series potentiometer,  $R_X$ .
- Calculate value of  $C_0$  from design equation (1) or from *Figure 6*  $f_S = f_O$ :

$$C_0 = \frac{1}{R_0 \cdot f_S} = \frac{1}{20,000 \cdot 1,000} = 50nF$$



- c) Calculate  $R_1$  to set the bandwidth  $\pm\Delta f$  (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0 \cdot 2}{\Delta f} = \frac{20,000 \cdot 1,000 \cdot 2}{100} = 400K$$

**Note:** The total detection bandwidth covers the frequency range of  $f_0 \pm \Delta f$

- d) Calculate value of  $C_0$  for a given loop damping factor:

Normally,  $\zeta = 0.5$  is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \zeta^2} = \frac{1250 \cdot 50 \cdot 10^{-9}}{400,000 \cdot 0.5^2} = 6.25pF$$

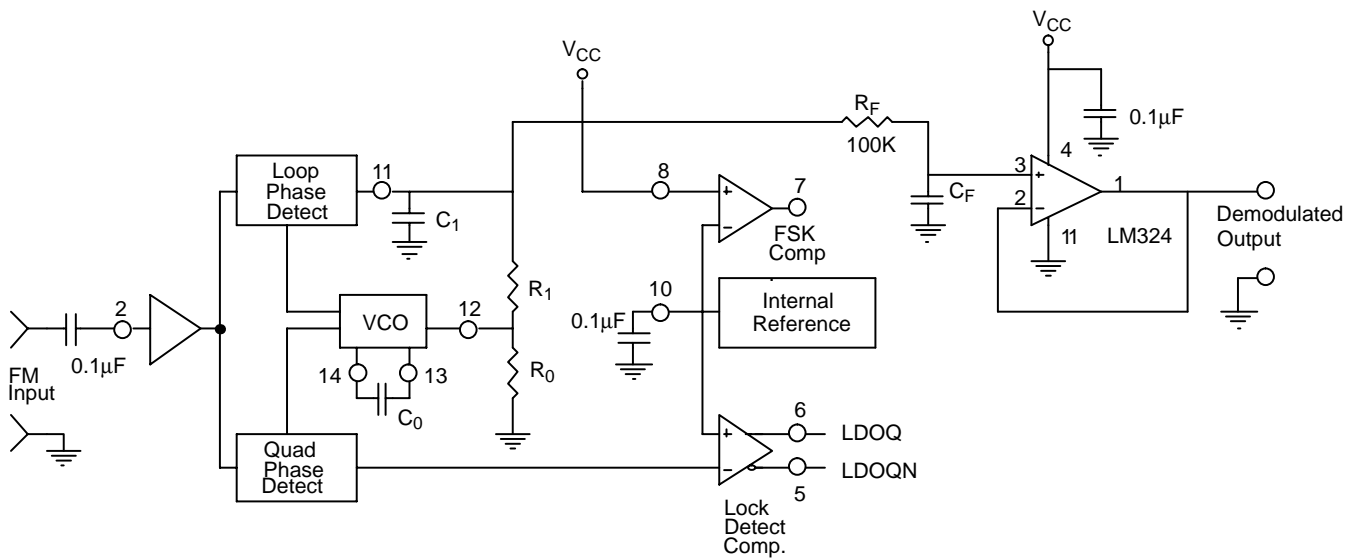
Increasing  $C_1$  improves the out-of-band signal rejection, but increases the PLL capture time.

- e) Calculate value of the filter capacitor  $C_D$ . To avoid chatter at the logic output, with  $R_D = 470K\Omega$ ,  $C_D$  must be:

$$C_D = \frac{16}{\Delta f} \geq \frac{16}{200} \geq 80nF$$

Increasing  $C_D$  slows down the logic output response time.

- f) Fine tune center frequency with  $5K\Omega$  potentiometer,  $R_X$ .



**Figure 13. Linear FM Detector Using XR-2211A and an External Op Amp.**  
(See Section on Design Equation for Component Values.)

## Linear FM Detection

XR-2211A can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in *Figure 13*. The demodulated output is taken from the loop phase detector output (pin 11), through a post-detection filter made up of  $R_F$  and  $C_F$ , and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in *Figure 13*.

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{OUT} = \frac{R_1 \cdot V_{REF}}{100 \cdot R_0}$$

where  $V_R$  is the internal reference voltage ( $V_{REF} = V_{CC}/2 - 650\text{mV}$ ). For the choice of external components  $R_1$ ,  $R_0$ ,  $C_D$ ,  $C_1$  and  $C_F$ , see the section on design equations.

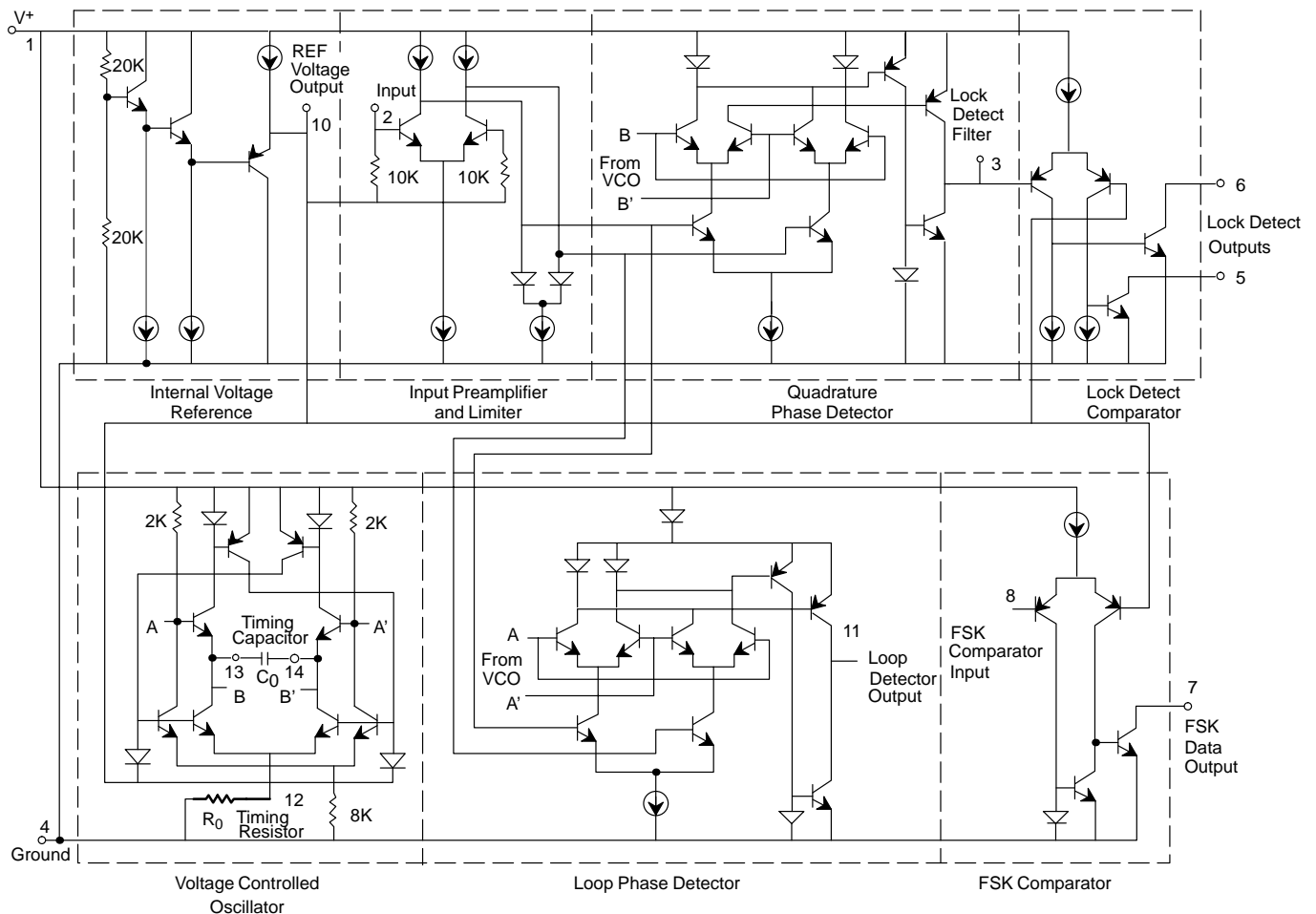
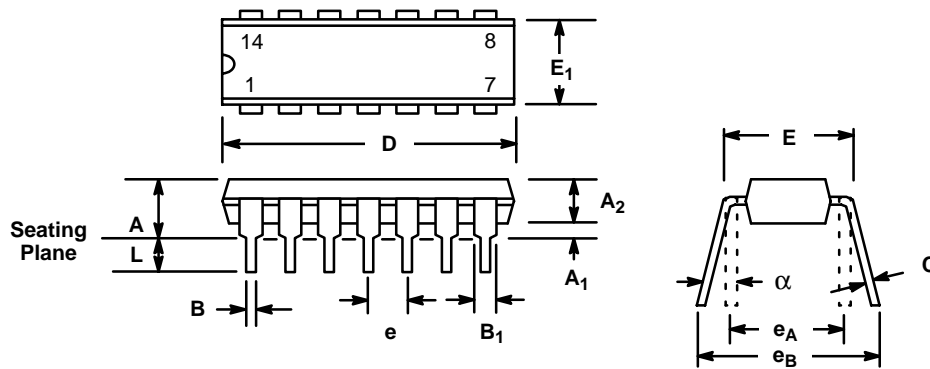


Figure 14. Equivalent Schematic Diagram

**14 LEAD PLASTIC DUAL-IN-LINE  
(300 MIL PDIP)**

*Rev. 1.00*

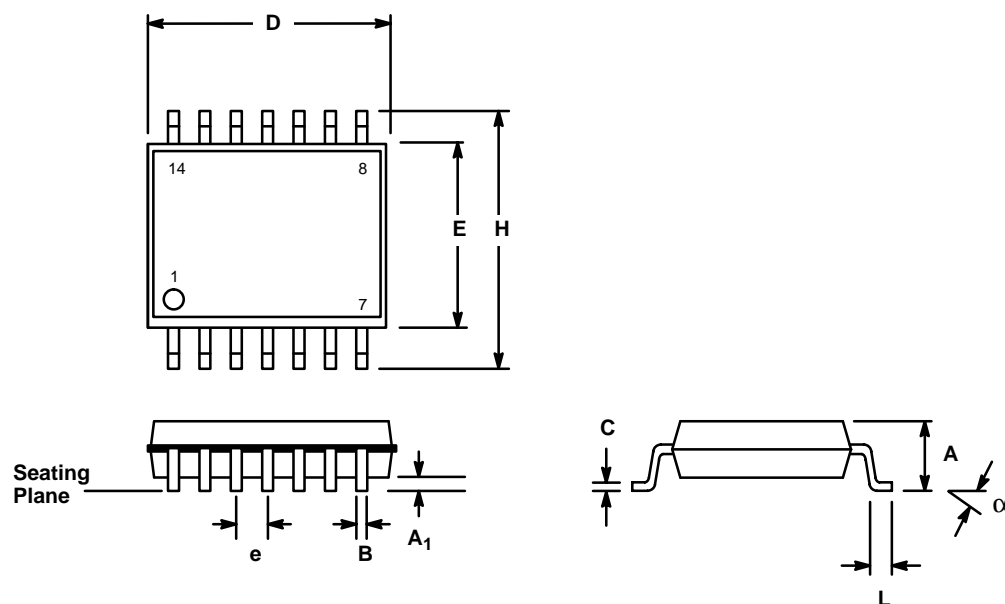


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A <sub>1</sub>	0.015	0.070	0.38	1.78
A <sub>2</sub>	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B <sub>1</sub>	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E <sub>1</sub>	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e <sub>A</sub>	0.300 BSC		7.62 BSC	
e <sub>B</sub>	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

*Note: The control dimension is the inch column*

## 14 LEAD SMALL OUTLINE (150 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A <sub>1</sub>	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0° 8°		0° 8°	

Note: The control dimension is the millimeter column

## Notes

## Notes

## Notes

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