

Communications

XRT6166

Codirectional Digital Data Processor

Features

- Low Power CMOS Technology
- All Receiver and Transmitter Inputs and Outputs are TTL-Compatible
- Transmitter Inhibits Bipolar Violation Insertion for Transmission of Alarm Conditions
- Alarm Output Indicates Loss of Received Bipolar Violations
- Tolerance of 125ms Variance of Data Transfer Timing in Both Transmit and Receive Paths Allows Operation in Plesiochronous Networks
- Both Receiver and Transmitter Perform Byte Insertion or Deletion in Response to Local Clock Slips and Provide Outputs Indicating Slip Logic Activity

Applications

- CCITT G.703 Compliant 64kbps Codirectional Interface
- Performs the Digital and Analog Functions for a Complete 64kbps Data Adaption Unit (DAU) When Used With the XRT6164

The XRT6166 is a CMOS device which contains the digital circuitry necessary to interface both directions of a 64kbps data stream to 2.048Mbps transmit and receive PCM time-slots. The XRT6166 and the companion XRT6164 line interface chip together form a CCITT G.703 compliant 64kbps codirectional interface.

The XRT6166 contains separate transmit and receive sections. The transmitter transforms 8-bit serial data from a 2.048Mbps time-slot into an encoded 64kbps data stream. The receiver, which performs the reverse operation, decodes the 64kbps data, extracts a clock signal, and then outputs the data to a 2.048Mbps time-slot. The XRT6166 provides features which allow the repetitions and deletions of both received and transmitted data as clock skews and transients occur. These slip occurrences are indicated by byte insertion and deletion flags. Outputs are also provided for extracted receive clock and clock recovery circuit loss of lock.