650 MHZ CLOCK & CRYSTAL MULTIPLIER WITH LVDS OUTPUTS

MARCH 2002 *REV. P1.0.1*

DESCRIPTION

The XRT8020 is a monolithic analog phase locked loop that provides a high frequency LVDS clock output, using a low frequency crystal or reference clock. It is designed for SONET/SDH and other low jitter applications.The high performance of the IC provides a very low jitter LVDS clock output up to 650 MHz, while operating at 3.3 volts. The XRT8020 has a selectable 8x, 16x or 32x internal multiplier for an external crystal or signal source. The Output Enable pin provides a true disconnect for the LVDS output. The very compact (4 x 4 mm) low inductance package is ideal for high frequency operation.

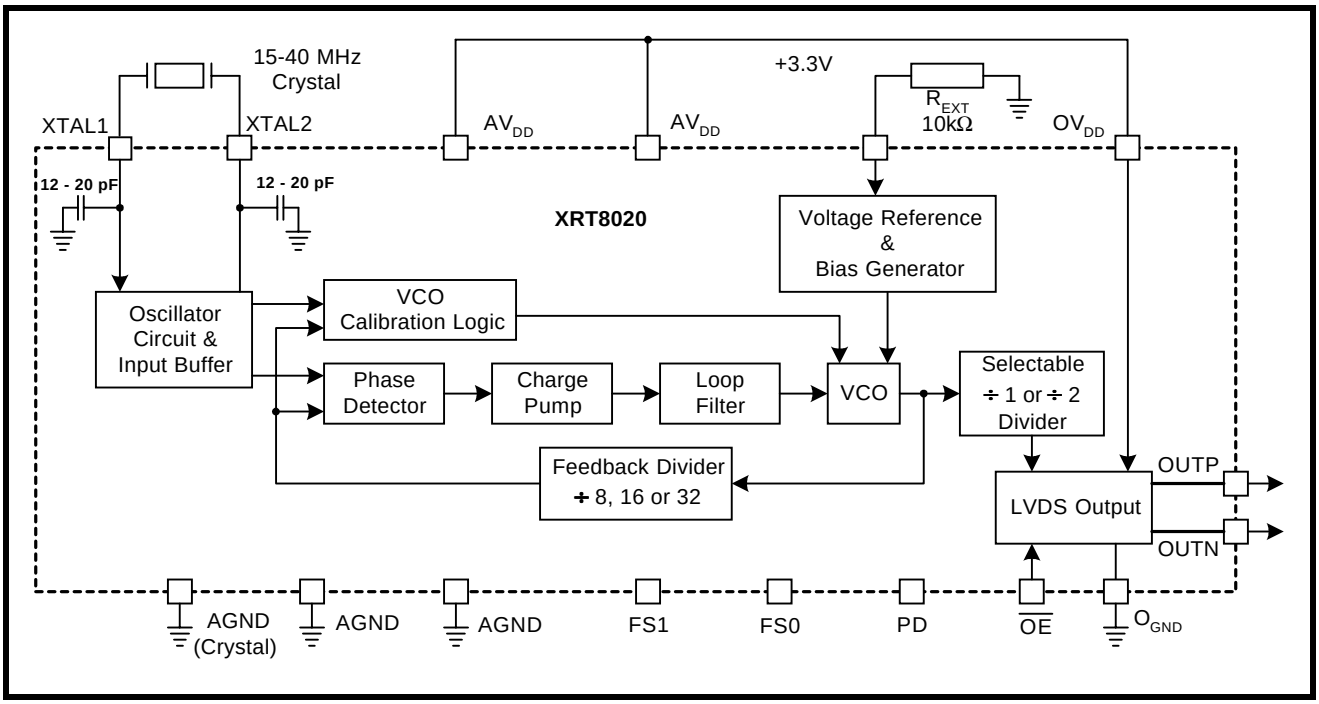
APPLICATIONS

- Gigabit Ethernet
- SONET/SDH
- SPI - 4 Phase 2
- Voltage Controlled Crystal Oscillator (VCXO)
- 8x, 16x or 32x Clock Multiplier for Computer and Telecommunication Systems

FEATURES

- Up to 650 MHz operation
- Low Output Jitter: 10ps rms max at 622 MHz
- On Chip Crystal Oscillator Circuit
  - Optimized for 15 to 40 MHz crystals
  - Uses parallel fundamental mode crystal
- Selectable 8x, 16x or 32x multiplier
- Selectable ÷ 1 or ÷ 2 LVDS output
- LVDS output meets TIA/EIA 644A Specification (2001)
- 3.3V Low power CMOS: 80 mW typical
- -40°C to +85°C operating temperature
- Extremely small 16-lead QLP package

FIGURE 1. BLOCK DIAGRAM OF THE XRT8020



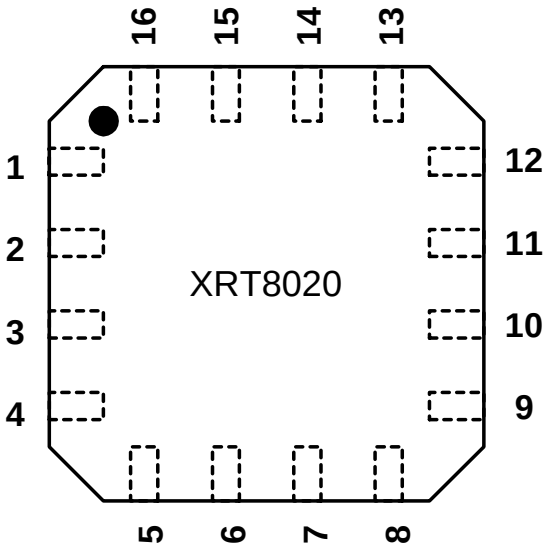
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT8020IL	16 - Pin QLP	-40°C to +85°C

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AVDD		+ 3.3V Analog Supply for Crystal Oscillator
2	AGND		Analog Ground for Crystal Oscillator
3	XTAL1	I	Crystal pin 1 or external clock input
4	XTAL2	O	Crystal pin 2 (output drive for crystal)
5	AGND		Analog Ground
6	REXT	I	External Bias Resistor (10KΩ to ground)
7	$\overline{OE}$	I	Output Enable, Active low (*Internal 50KΩ pull-down to ground*)
8	PD	I	Power Down, Active High *(Internal 50KΩ pull-down to ground)*
9	FS1	I	Frequency select "1" *(Internal 50KΩ pull-down to ground)*
10	FS0	I	Frequency select "0" *(Internal 50KΩ pull-up to VDD)*
11	AGND		Analog Ground
12	OGND		Output Ground for LVDS outputs
13	OUTN	O	LVDS negative output for 50Ω line
14	OUTP	O	LVDS positive output for 50Ω line
15	OVDD		+ 3.3V Digital Supply for LVDS Output buffer
16	AVDD		+ 3.3V Analog Supply

FIGURE 2. XRT8020 PIN LOCATION - (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5 to 6.0 V
V_{IN}	-0.5 to 6.0 V
Storage Temperature	-65°C to + 150°C
Operating Temperature	-40°C to + 85°C
ESD	>2,000 volts

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply current	I_{DD}		25	30	mA	
Input Digital High	V_{INH}	2.0			V	
Input Digital Low	V_{INL}			0.8	V	
Crystal Frequency		15		40	MHz	Crystal Jitter < 1 ps p-p
Power on Calibration time				5	ms	After VDD reaches 2.8V ***NOTE:*** *Calibration time = 16,000 clock cycles*
Max Frequency	F_{OUT}	500		650	MHz	624 MHz nominal F_{OUT}
Max Frequency	F_{OUT}	250		325	MHz	312 MHz nominal F_{OUT}
Rise time	T_R			300	ps	CL = 5pF, RL = 100Ω, (20% - 80%)
Fall Time	T_F			300	ps	CL = 5pF, RL = 100Ω, (20% - 80%)
Duty cycle		45		55	%	LVDS output
Output skew				10	ps	Differential
Output Loading			100		Ω	
Output voltage	V_{OUT}	-400		400	mV	Differential (OUTP-OUTN)
Common Mode Voltage	V_{CM}		1.2		V	
Output Impedance					Ω	
Output short circuit current			-5.7	-8	mA	Current limit to ground, V_{DD} or Vp to Vn
Period Output Jitter				10	ps	rms, at 624 MHz
Period Output Jitter				10	ps	rms, at 312 MHz
Accumulated Output Jitter				20	ps	rms, 1,000 cycles, at 622 MHz
Accumulated Output Jitter				20	ps	rms, 1,000 cycles, at 312 MHz
Input Clock Frequency		0		80	MHz	Pin 3, XTAL1
Crystal Frequency Range		15		40	MHz	Fundamental Mode Crystal

FIGURE 3. LVDS OUTPUT TEST CIRCUITS AND WAVEFORMS

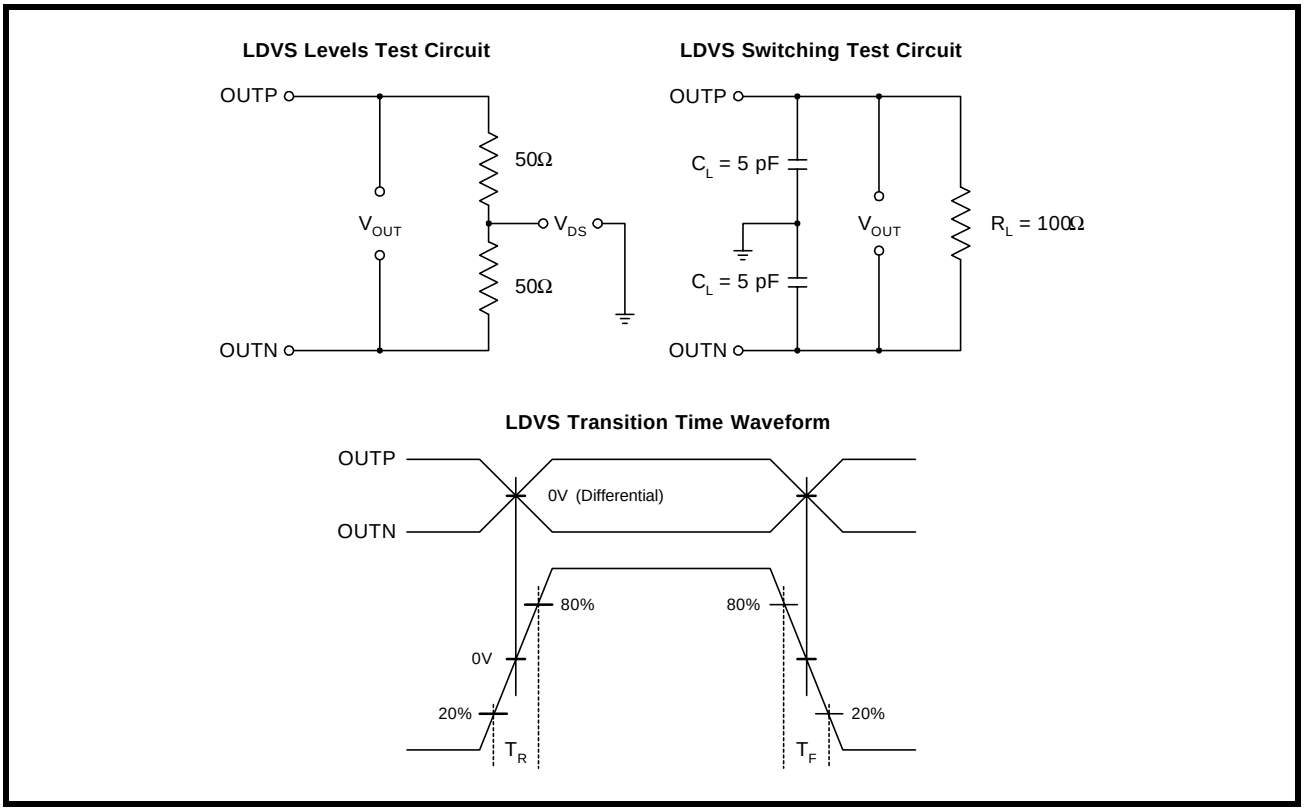


TABLE 1: FREQUENCY SELECTION TABLE

FS0 PIN 10	FS1 PIN 9	CRYSTAL OR CLOCK FREQUENCY	INTERNAL CAPACITOR	MULTIPLY RATIO	OUTPUT DIVIDE	OUTPUT FREQUENCY
1	1	78.0 MHz Clock	NA	8x	1	624 MHz
0	1	39.0 MHz	12 pF	16x	1	624 MHz
1	0	19.5 MHz	20 pF	32x	1	624 MHz
0	0	19.5 MHz	20 pF	32x	2	312 MHz

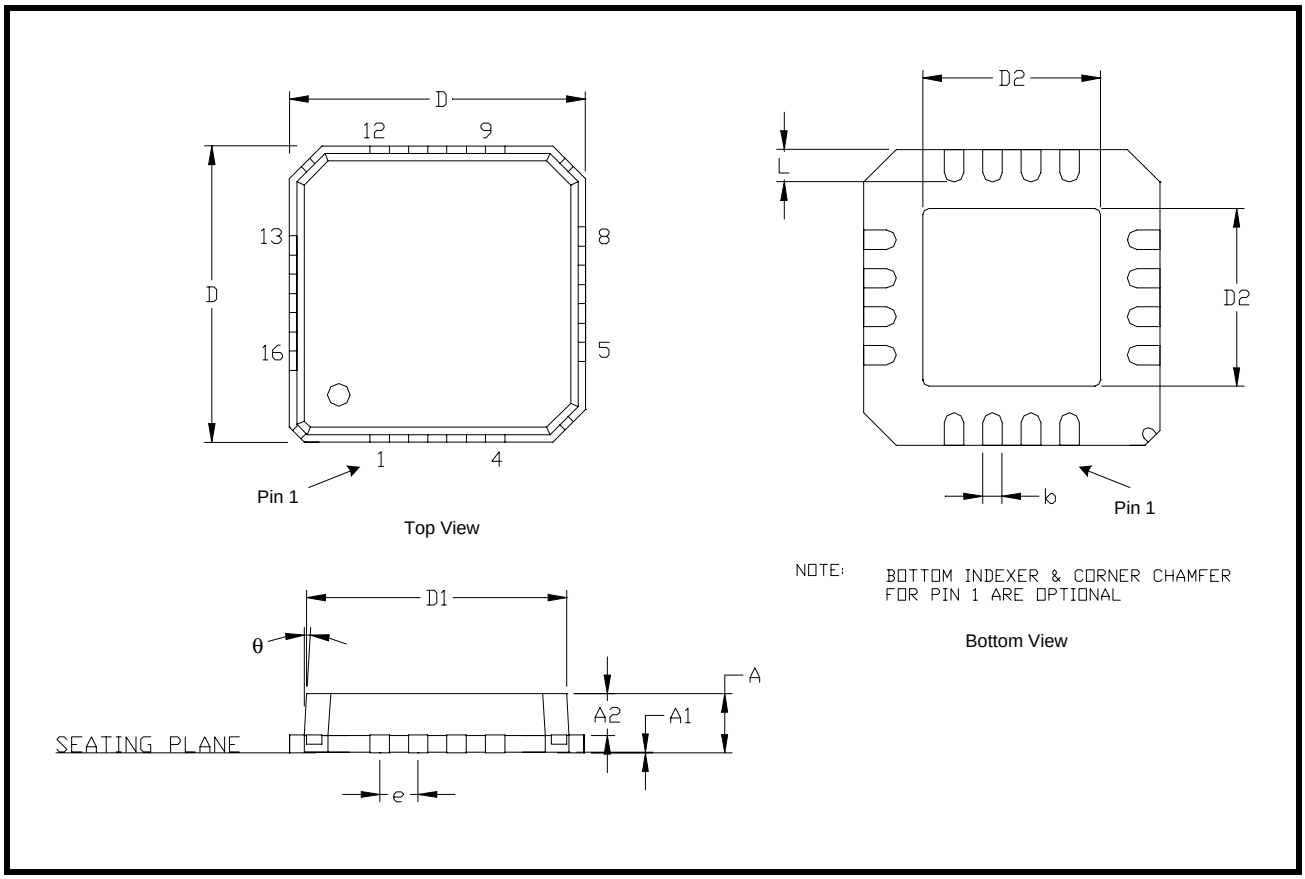
NOTES:

1. *Use Parallel Fundamental mode crystal*
2. *FS0 has an internal 50KΩ pull-up resistor to VDD*
3. *FS1 has an internal 50KΩ pull-down resistor to GND*

TABLE 2: POWER-DOWN AND OUTPUT TRI-STATE SELECTION TABLE

PD PIN 8	$\overline{OE}$ PIN 7	STATUS	*NOTES:*
1	X	Outputs tri-stated and chip Powered-down	1. *"X" = Don't care* 2. *PD and $\overline{OE}$ have an internal 50KΩ pull-down resistor to ground.*
0	1	Output tri-stated	

PACKAGE DIMENSIONS (16-PIN QLP)



Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A2	0.000	0.039	0.00	1.00
D	0.154	0.161	3.90	4.10
D1	0.144	0.152	3.65	3.85
D2	0.030	0.089	0.75	2.25
b	0.007	0.012	0.18	0.30
e	0.020 BSC		0.50 BSC	
L	0.014	0.030	0.35	0.75
θ	0°	12°	0°	12°

REVISIONS

P1.0.1 Accumulated output jitter in electrical specs changed from 25 ps @ 624MHz to 20 @ 622Mhz and TBD to 20 ps @312Mhz. Pin 9 has internal a pull-down resistor instead of pull-up. Table 1 FS0 and FS1 bit pattern changed.