SONET/SDH STS-12/STM-4 TO E3/DS3/STS-1 MAPPER/DEMAPPER

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GENERAL DESCRIPTION

The XRT94L43 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-12 or STM-4 data stream. The XRT94L43 interfaces to either STS-12 or STM-4 signals using a byte wide parallel interface in Telecom Bus format or via serial line interface that operates at 622.08 MHz.

The XRT94L43 processes the section,line and path overhead in the SONET/SDH data stream. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L43 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L43 memory map or from external interface. A1,A2 framing pattern, C1 byte and H1,H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L43 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L43 provides 12 mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general purpose microprocessor interface is included for control, configuration and monitoring.

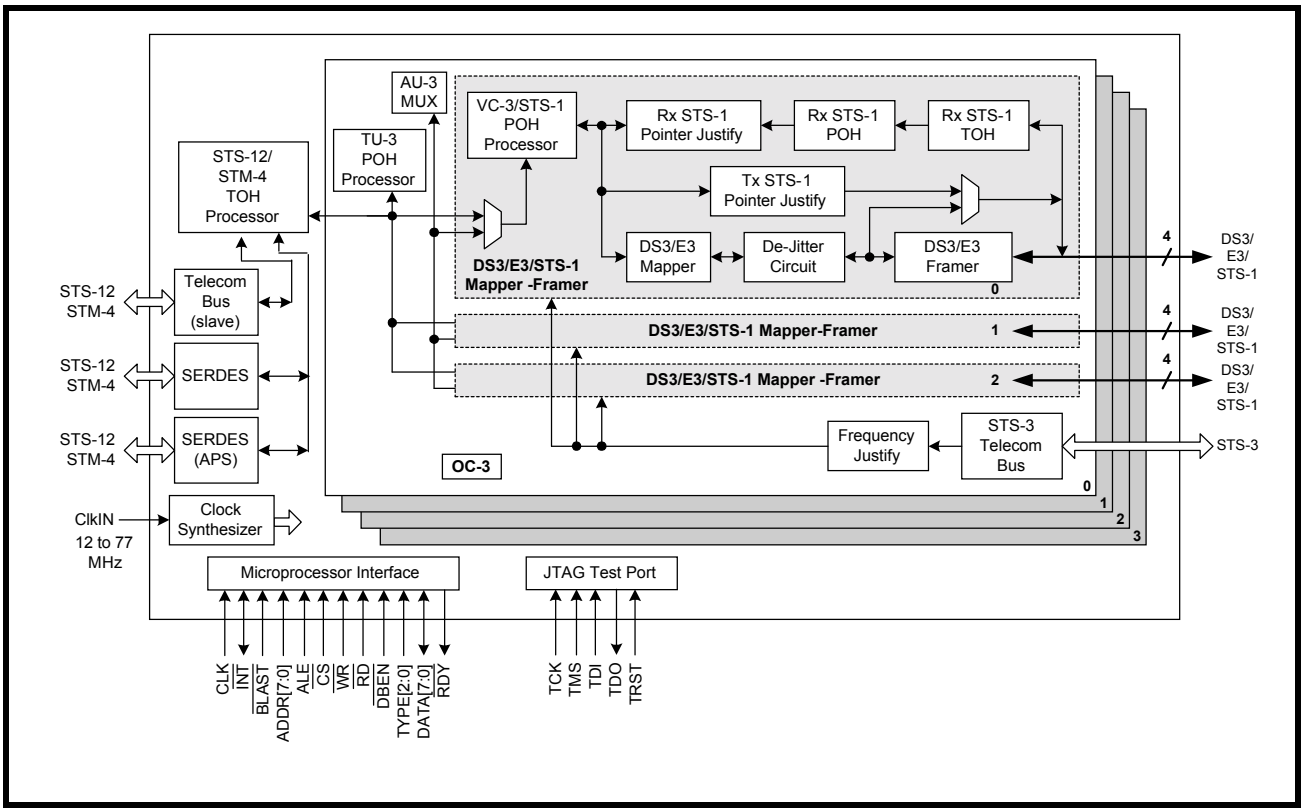
FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 12 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers.
- Generates and terminates SONET/SDH section,line and path layers.
- Integrated SERDES with Clock Recovery Circuit.
- Provides SONET frame scrambling and descrambling.
- Integrated Clock Synthesizer that generates 622.08 MHz and 77.76 MHz clock from an external 12.96/ 19.44/77.76 MHz reference clock.
- Provides STS-1 (EC1) mapping/de-mapping for up to 12 STS-1s.
- Integrated 12 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05UIpp jitter requirements.
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3.
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries.
- Performs STS-3/STM-1 to STS-12/STM-4 Mapping/De-Mapping.
- E3 and DS3 framers for both Transmit and Receive directions.
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards.
- Complete Path Overhead processing and generation for one STS-12 or for 12 STS-1s
- Full line APS support for redundancy applications.
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1.
- Boundary scan capability with JTAG IEEE 1149.1
- 8-bit microprocessor interface
- Power Supply 2.5 V for Core and 3.3 V for I/O
- -40°C to +85°C Operating Temperature Range
- Available in a 516 Ball PBGA package

APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

FIGURE 1. BLOCK DIAGRAM OF THE XRT94L43



PRODUCT FEATURES

SONET TRANSMITTER

- Performs standard STS-12/STM-4 Transmit Processing
- Conforms to ITU-T 1.432, ANSI T1.105 and Bellcore GR-253 Standards
- Provides 155.52 MHz 16-bit parallel interface
- Performs SONET frame insertion and accepts external frame synchronization
- Performs Optional Transmit Data Scrambling
- Performs POH,TOH generation/insertion
- Generates transmit payload pointer (H1,H2) (fixed at 522) with NDF insertion
- Inserts A1/A2 with optional error mask
- Computes and inserts BIP-8 (B1,B2) with optional error mask
- Generates AIS-L, REI-L and RDI-L according to receiver state with option of SW/HW insertion
- Inserts LOS and forces SEF by software
- Generates RDI-P and REI-P automatically with optional SW/HW override
- Inserts fixed-stuff columns, calculates and inserts B3 error code

SONET RECEIVER

- Performs standard STS-12/STM-4 receive processing
- Provides fully programmable threshold detection for SD and SF condition
- Provides section trace buffer with mismatch detection and invalid message detection
- Performs SONET Frame Synchronization
- Supports NDF, positive stuff and negative stuff for pointer processor
- Performs receive data de-scrambling
- Performs POH and TOH interpretation/extraction
- Interprets payload pointer (H1,H2)
- Extracts data communication channels from D1-D3 and D4-D12
- Detects Out of Frame (OOF), Loss of Frame(LOF), Loss of Signal(LOS) AND APS failure
- Detects Line Alarm Indication (L-AIS), Line Remote Defect Indication (L-RDI) and Loss of Pointer
- Detects Path Alarm Indication, Path Remote Defect Indication and Path extended RDI
- Provides Signal Label Monitor with PLM detection
- Supports path trace buffer with TIM-P and invalid message detection
- Computes and compare B3, REI-L and REI-P errors
- Computes and compare BIP-8 (B1,B2) and counts the errors

MAPPER

- Performs standard SONET STS-1 mapping for DS3 conforming with Bellcore GR-253 and GR-499
- Performs SDH VC-3 mapping for DS3 and E3 to conform ITU-T G.707
- Implements AU-3 to VC-3 multiplexing and de-multiplexing
- Provides STS-1 mapping and de-mapping functions
- Accepts data from external STS-1 inputs
- In the transmit direction, provides STS-1 framing, descrambling, performance monitoring and pointer processing functions
- In the receive direction, provides frame generation and scrambling

SONET/SDH INTERFACE

- Supports an 8-bit parallel interface at 77.76 MHz for STS-12/STM-4 in Telecom bus format.
- Supports an 8-bit parallel interface at 19.44 MHz for STS-3/STM-1 in Telecom bus format.
- Serial Interface at 622.08 MHz with SERDES

APS SUPPORT

- Supports both 1+1 and 1:1 configurations
- APS interface consists of two Serial Interface with SERDES.
- Provides both input and output interface for APS

E3/DS3/STS-1 INTERFACE

- Supports up to 12 E3/DS3/STS-1 tributaries
- In the receive direction, generates the single-rail or dual-rail data along with smoothed E3/DS3 clock as well as start of frame indication
- Provides RX serial and single-rail (NRZ) data and clock at 51.84 MHz for STS-1E
- In transmit direction, accepts clear channel E3/DS3 signal and performs framing on incoming signal

DS3 RECEIVE FRAMER

- Offers off-line framing algorithm
- Complies with the standards as: Bellcore TR-NWT-000499 and TR-NWT-000009
- Supports overhead extraction
- Provides line code violation detection and excess zero count
- Reports and counts FEBE

- HDLC controller complies with ITU-T Q.921 LAPD protocol
- Provides Line and Local Loopbacks
- Supports M13 and C-bit parity mode
- Supports B3ZS line decoding which can be user enabled. Replaces valid B0V or 00V with 3 zeros
- Synchronizes to incoming frame based upon 10 valid F bits followed by 3 consecutive valid M frames. Offers optional AIC-bit or parity verification before declaration of sync
- Detects Out of Frame (OOF) upon 3 or 6 F bits out of 15 F bits in error or 1 or more M bits in 3 of 4 consecutive frames in error
- Detects Loss of Signal (LOS) upon encountering 180 consecutive 0's and clears on at least 60 of successive received 1's.Offers optional disable
- Detects idle state by checking C-bit in subframe 3 are all zero, X-bits are one and repeating 11001100 payloads. Declaration occurs when all the above conditions persist for 63 M-frames. Clears the condition when 63 valid M-frames are received
- Detects AIS with different algorithm
- Calculate parity and compare
- Validate FERF bits, sets to one when both X-bits are zero and clears when they are One
- Detects and validates FEAC codes upon 8 out of 10 last identical received codes. Invalidates on 3 in 10 mismatch
- Provides 15-bit PRBS lock

DS3 TRANSMIT FRAMER

- Offers following frame generation mechanism: Asynchronous operation, using receive side clock, external framing
- Supports either C-bit operation or M13 operation: optional all C bits set to "1" or C-bit parity ID bit (C11) toggled in each frame for M13 operation
- Provides start of frame control with external pin
- Inserts frame overhead bits via External serial port or Internal generation
- Generates and checks parity
- Enables FERF insertion by receiver LOS and/or OOF and/or AIS conditions with polarity suitability
- Enables FEBE insertion through register bit. Indicates receiver F-bit errors, M-bit errors and CP-bit parity errors
- Provides FEAC channel processing including generation of valid FEAC patterns and transmissions of all 1's upon programming of idle code
- Inserts path maintenance data link through HDLC transmitter which contains the following features:
  - AM for storage of entire LAPD message
  - Selection of message length to 82 or 76 bytes
  - Optional frame header generation
  - Generation of flag sequences
  - Computation and insertion of CRC
  - Zero stuffing
  - Register bits for communication with microprocessor
  - Interrupt generation upon transmission of message
- LOS Insertion enabled by register bit
- AIS Insertion enabled by register bit or pin
- Idle signal insertion enabled by register bit
- Supports B3ZS encoding
- Generates AIS, Idle and Yellow force alarms
- Inserts errors optionally in the P, F, FEBE and M bits
- Provides 15-bit PRBS generator

E3 RECEIVE FRAMER

- Offers off-line framing algorithm
- Complies with standards ITU-T G.751 and G.832
- Provides line code violation detection and excess zero count
- LAPD controller complies with ITU Q.921 LAPD protocol
- Provides local loop-back
- Supports G.751 and G.832 framing formats
- Supports HDB3 line decoding which can be user enabled. Replaces valid B00V or 000V with 4 zero's
- Synchronizes to incoming frame based upon occurrence of two sets of FA1, FA2 with expected separation -G.832 or detection of three consecutive frame alignment signals (FAS) - G.751
- Detects Out of Frame (OOF) upon 4 consecutive invalid frames
- Detects Loss of Signal (LOS) upon encountering 32 consecutive 0's and clears on occurrence of 32 bits without a string of 4 0s
- Detects AIS if 7 or less 0s detected in each of 2 consecutive frames and clears if more than seven 0's detected in each of 2 consecutive frames
- Calculation and comparison of BIP-8 (G.832) or BIP-4 (G.751). BIP-4 calculation can be disabled
- Supports overhead extraction

- Microprocessor access to TR trail trace message - 16 TTB registers (G.832) or service (Alarm and Nation) bits (G.751)
- Detects MA FERF if 3 or 5 consecutive MA MSBs are 1and clears if 3 or 5 consecutive MA MSBs are 0 (only E3 G.832)
- Indicates last validated FERF value and interrupt upon a change in validated FERF value
- Extracts payload type (MA) bits and stores in a register (Only E3 G.832)
- Extracts Timing Marker bit and checks for consistency over 3 or 5 consecutive frames (only E3 G.832)
- Extracts Synchronous Status Message bits and stores it in register bits when enabled (only G.832)
- Overhead output on synchronous serial interface

E3 TRANSMIT FRAMER

- Offers following frame generation mechanism: Asynchronous operation, using receive side clock, external framing
- Supports either G.751 or G.832 framing format
- Generates and checks parity BIP-8 (G.832), BIP-4 (G.751) BIP-4 computation can be disabled
- Inserts data link message through E3 data line channel which contains the following features:
  - Insertion into NR or GC byte (programmable through register bit) (E3 G.832 only)
  - Insertion into Nation bit in case of E3 G.751 when LAPD is enabled
  - RAM storage of entire LAPD message
  - Selection of message length to 82 or 76 bytes
  - Generation of flag sequences
  - Computation and insertion of CRC-16
  - Zero stuffing
  - Register bits for communication with microprocessor
  - Interrupt generation upon complete transmission of message
- LOS insertion enabled by register bit to force all 0s in the transmit stream
- AIS insertion enabled by register bit and/or pin to force all 1's in the transmit stream
- Supports HDB3 encoding enabled by register bit
- Inserts frame overhead bits via External serial/nibble port (except for FA1,FA2 and EM bytes in case of E3 G.832 and FAS and BIP-4 in case of G.751) or through external overhead interface or from configuration register or internal generation
- Inserts FA1, FA2, EM, TR, MA and GC bytes into G.832 stream or FAS service bits and BIP4 (if enabled) into G.751 stream
- Inserts MA,NR,GC and TR (TTB) from microprocessor accessible registers (service bit for G.751)
- Inserts FEBE in MA upon receipt of EM byte errors. Programmable through register bit (G.832)
- Asserts FERF upon any combination of LOS,OOF or AIS received from receiver (G.832)
- Inserts synchronous status message from microprocessor accessible registers, when enabled (G.832)
- Error masks for framing bytes, and computed parity (BIP-8 in case of G.832 and BIP-4 in case of G.751)
- Optionally accepts overhead bits (except FA bytes for G.832 and FAS bits for G.751) from input interface

E3/DS3/STS-1 DE-JITTERING/DE-SYNC CIRCUIT

- Meets the E3/DS3/STS-1 jitter requirements
- Compliant with jitter transfer template outlined in ITU G.751,G.752,G.755 and GR-499-CORE
- Meets output jitter requirement as specified by ETSI TBR24
- Meets the jitter and wander specifications described in T1.105.03b,GR-253 and GR-499 standards
- Performs the Desynchronizer function and pointer adjustments for STS-1 to DS3 mapping

.PERFORMANCE MONITORING

- Supports line and path performance monitoring
- Provides 32-bit saturating counter of OOF errors
- Provides 32-bit saturating counter LOF errors
- Provides 32-bit saturating counter of LOS errors
- Provides 32-bit saturating counter of SD errors
- Provides 32-bit saturating counter of SF errors
- Provides 32-bit saturating counter B3 errors
- Provides 32-bit saturating counter of the line RDI,path AIS,REI-L errors,REI-P errors and BIP-8(B1,B2),B3 errors and loss of pointer
- Provides 16-bit saturating counter of DS3 framing bit errors, DS3 frame parity errors, line code violations, frame parity (BIP) errors, DS3 frame CP bit errors and DS3 Far-End Block errors
- One second statistics
  1. Bipolar violations

2. Frames with parity errors
3. Frames with CP bit errors
4. Error second indication
5. Severely errored second indication

INTERRUPT, STATUS AND TEST

- Provides individually maskable interrupts
- Provides one second interrupt generations
- Generates interrupts from the following causes:
- DS3 OOF status change, LOS status change, DS3 AIS status, LAPD message received, DS3 parity error,DS3 FEAC validation, DS3 FEAC removal, DS3 IDLE status change, FEBE (E3) change, DS3 FERF change, DS3 format change (AIC), LAPD end of message transmission and DS3 FEAC end of message transmission, DS3 Framing alignment change, SONET OOF status change and COFA
- Provides local and remote line loopback
- Provides SONET remote loopback

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L43IB	35 x 35 516 Lead PBGA	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT94L43