XRT95L34

OC-12/STM-4, QUAD OC-3/STM-1 POS/ATM FRAMER WITH INTEGRATED CDR'S

MARCH 2002 *REV. P1.0.0*

GENERAL DESCRIPTION

The XRT95L34 is an OC-12/STM-4, Quad OC-3/ STM-1 POS/ATM Framer with integrated CDR's. ATM direct mapping and cell delineation are supported, so are packets (PPP) over SONET for POS mapping and frame processing. The XRT95L34 contains an integral SONET framer which provides framing and error accumulation in accordance with ANSI/ITU-T specifications. The configuration of this device is through internal registers accessible via an 8-bit parallel, memory mapped, microprocessor interface.

APPLICATIONS

- Edge and WAN ATM Switches
- IP Routers, Packet Switches and Hubs
- Multi-protocol Switches

FEATURES

- A single chip solution for ATM UNI and packet over SONET
- Provides the highest level of protection switching flexibility for up to 1:14 protected OC-3/STM-1 ports.
- Provides quad serial OC-3/STM-1 interfaces with integrated CDR, compatible with industry standard optical modules.
- Provides serial OC-12/STM-4 interfaces with integrated CDR, compatible with industry standard optical modules.
- Supports the mappings for any standard combination of STS-12c/AU-4c or STS-3c/AU4.
- Provides four 8-bit busses on the line side running at 19.44 MHz to connect OC-12 framers through a parallel interface or aggregate four low speed OC-3 devices into an OC-12 line.
- Supports both SONET and SDH on all interfaces. SONET/SDH is programmable per interface.
- Terminates Section Overhead, Line Overhead and STS-Path Overhead on 4xOC-3, 1xOC-12 interfaces. Supports performance monitoring and alarms required by GR.253, G.707 and ANSI T1.105.
- Provides SONET frame scrambling and de-scrambling.
- Supports 50 msecond APS by monitoring and filtering K1 and K2 bytes as required by the standards.
- Offers differential line interfaces.
- Offers multiple microprocessor compatible interface - Intel, Motorola, PowerPC, Mips.
- Provides 8/16-bit data UTOPIA level II Interface and POS interface.
- Includes ATM cell or PPP packet Mapping.
- Single +3.3V power supply with +5V input tolerance.

SONET TRANSMITTER

- Performs standard OC-3c/STM-1c transmit processing.
- Conforms to ITU-T I.432, ANSI T1.105, and Bellcore-253.

SONET RECEIVER

- Performs standard STS-12/STS-3c/STM-1c receive processing.
- Conforms to ITU-T I.432, ANSI T1.105, and Bellcore-253.

HIGH SPEED INTERFACE

- Quad serial OC-3/STM-1 PECL interfaces with integrated CDR, compatible with industry standard optical modules.
- Single serial OC-12/STM-4 PECL interface with integrated CDR, compatible with industry standard optical modules.

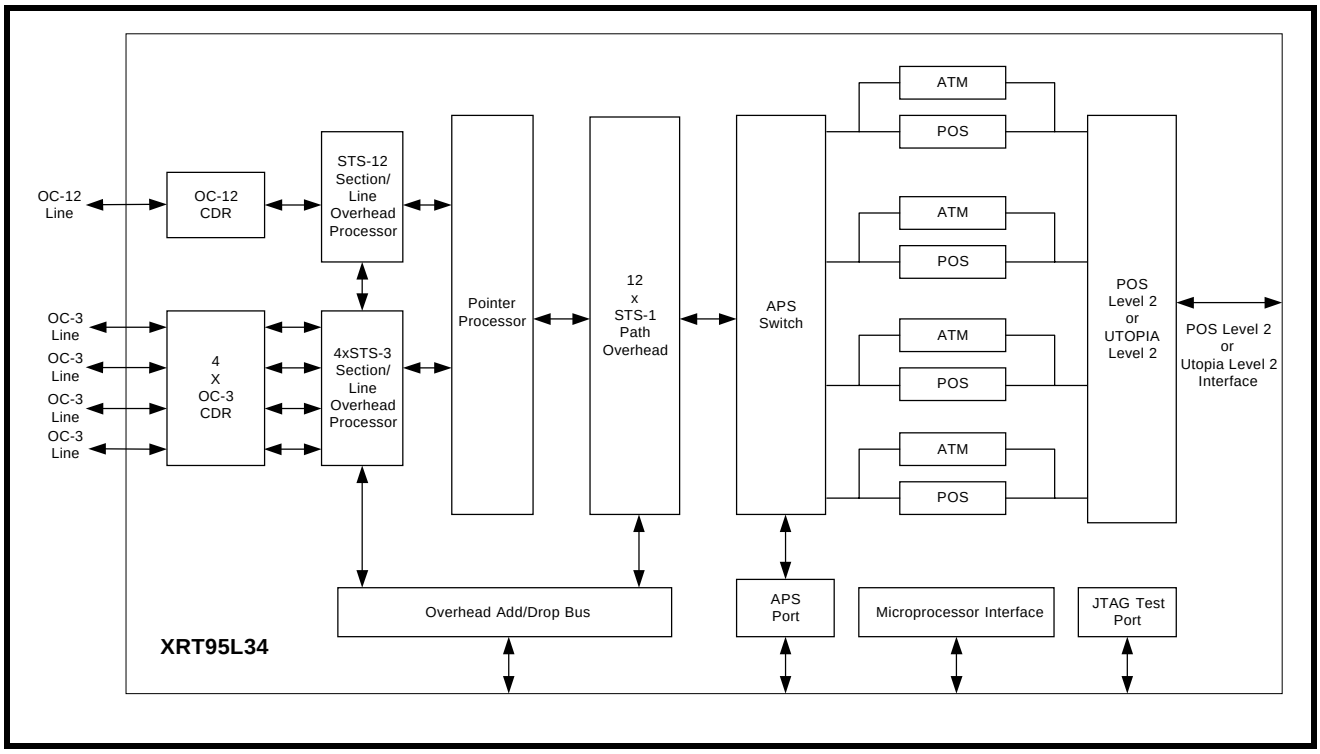
LOW SPEED INTERFACE

- Complies with ATM forum Utopia Level 2 Specification
- Supports 8/16-bit 50MHz transmit and receive interface.
- Provides up to total 16 cell buffers for transmit and receive.

MICROPROCESSOR INTERFACE

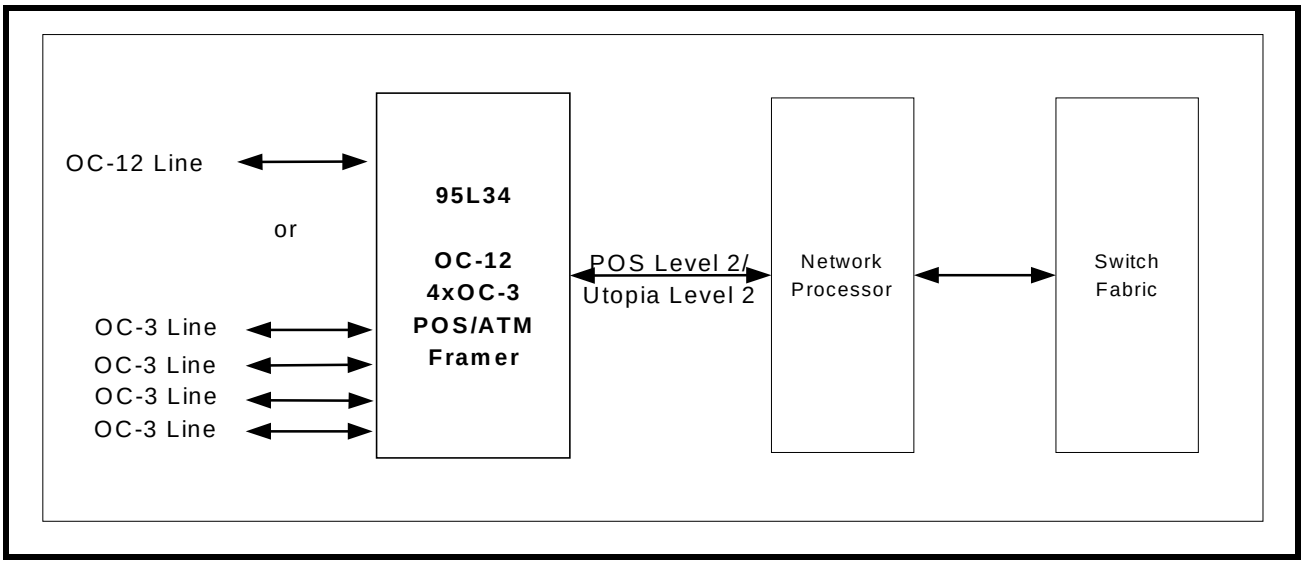
- Supports standard 8-bit micro-controllers with Intel or Motorola style interfaces.
- ·33 MHz read and write access.
- Provides burst bus transfers.
- Provides DMA controller interface for OAM buffer interface.
- Separated and multiplexed data/address bus.
- Both write-clear and reset-upon-read for control of status registers.
- Provides interrupts for alarm processing.

FIGURE 1. BLOCK DIAGRAM OF THE XRT95L34



XRT95L34 POS/ATM APPLICATIONS

FIGURE 2. MULTI-PROTOCOL ROUTER APPLICATION

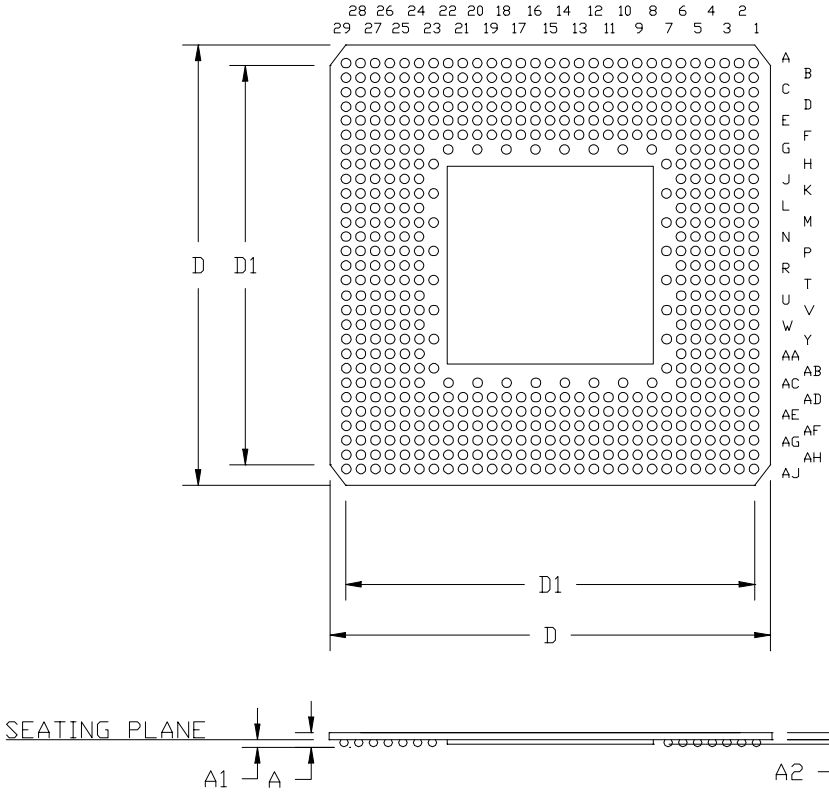


ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT95L34IV	584 Ball TBGA	-40°C to +85°C

PACKAGE OUTLINE DRAWING

584 Tape Ball Grid Array
(37.5 mm x 37.5 mm, TBGA)
Rev. 1.00



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.057	0.065	1.45	1.65
A1	0.024	0.028	0.60	0.70
A2	0.033	0.037	0.85	0.95
D	1.469	1.484	37.30	37.70
D1	1.400 BSC		35.56 BSC	
b	0.026	0.033	0.65	0.85
e	0.050 BSC		1.27 BSC	
P	0.006	0.012	0.15	0.30

REVISIONS

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