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## FUNCTIONAL OVERVIEW

XRT95L51 implements the SONET/SDH framing function with full duplex ATM/POS interface for the STS-48/STM-16 data streams. The XRT95L51 is functionally and architecturally, divided into the following blocks and modules:

### LINE SIDE INTERFACE

- Differential inputs/outputs for high speed chip-to-chip communication using Pseudo ECL logic.
- Programmable parity bit for both incoming and outgoing data paths.
- Monitors the Loss of Optical Carrier.
- The transmit line side provides the direct looped back version of the line clock, framing pulse and parity.
- The reference signal derived from the receive clock input can be programmed to be 77.76 MHz, 38.88 MHz, 19.44 MHz or 8 kHz.
- The reference signal derived from the transmit clock input can be programmed to be 77.76 MHz, 38.88 MHz, 19.44 MHz and 8 kHz.
- 8 kHz reference signal can be phase locked to either incoming or outgoing SONET/SDH frame.
- Supports Local and Remote Line Loopback.
- Provides 155.52 MHz 16-bit parallel interface

### SONET/SDH TRANSMITTER

- Performs standard OC-48c/STM-16c transmit processing
- Conforms to IYU-T I.432, ANSI.105 and Bellcore GR-253
- Performs SONET/SDH frame insertion and accepts external frame synchronization
- Performs optional transmit data scrambling
- Performs POH, TOH generation/insertion
- Generates transmit payload pointer (H1, H2) (fixed at 522) with NDF insertion
- Inserts A1/A2 with optional error mask
- Computes and inserts BIP-8 (B1, B2) with optional error mask
- Generates AIS-L, REI-L and RDI-L according to receiver state with option of SW/HW insertion
- Inserts LOS, forces SEF by software
- Generates RDI-P and REI-P automatically with optional SW/HW override
- Inserts fixed stuff columns, calculates and inserts B3 error code
- Performs payload insertion from cell processor

## SONET/SDH RECEIVER

- Performs standard STS-48c/STM-16c receive processing
- Provides fully programmable threshold detection for SD and SF condition
- Provides 155.52MHz 16-bit parallel interface
- Provides section trace buffer with mis-match detection and invalid message detection
- Performs SONET/SDH frame synchronization
- Supports NDF, positive stuff and negative stuff pointer processor
- Performs receive data de-scrambling
- Performs POH, TOH interpretation/extraction
- Interprets payload pointer (H1, H2)
- Extracts data communication channels from D1-D3 and D4-D12
- Detects out of frame (OOF), loss of frame (LOF), loss of signal (LOS), APS failure
- Detects Line Alarm Indication (L-AIS), Line remote Defect Indication (L-RDI), Loss of Pointer
- Detects Path Alarm Indication, Path remote Defect Indication, Path extended RDI
- Provides signal label monitor with PLM detection
- Supports path travel buffer with TIM-P and invalid message detection
- Computes and compare B3, REI-L and REI-P errors
- Computes and compare BIP-8 (B1, B2) and counts the errors
- Performs payload extraction.

### ATM CELL PROCESSOR

- Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432
- Supports SDH mapping
- Provides selectable on-going HEC insertion and verification
- Provides selectable Coset addition and removal
- Provides single bit error correction and multiple bit error detection for HEC processing
- Provides HEC correctable and uncorrectable indications
- Provides HEC correction selectability
- Supports external cell GFC insertion and extraction
- Provides the functions of cell rate de-coupling; idle cell insertion and detection, 16-cell FIFO cell buffering, programmable idle cell header and payload and idle cell HEC generation

- Offers cell delineation with three states (hunt, pre-sync and sync) synchronization algorithm and provides LCD (Loss of Cell Delineation) indication and interrupt
- Supports multiple programmable VPI/VCI filters on Transmit and Receive
- Provides self-synchronizing SDH cell scrambling/de-scrambling,  $x^{43}+1$
- Supports OAM cell insertion and extraction with dedicated cell store via microprocessor interface. Transmission is enabled through semaphore
- Provides TXCell and TXCell indication signals
- Provides test cell generation and verification

#### **PACKET OVER SONET (POS) PROCESSOR**

- Supports packet based link protocols by using byte synchronous HDLC framing like PPP, HDLC and frame relay
- 32-bit extended Saturn POS-PHY host interface clocked to 100 MHz
- Performs transmit HDLC frame insertion and receive data extraction
- Performs self-synchronous data scrambling and de-scrambling using  $1+X^{43}$  polynomial
- Performs transmit flag sequence insertion and receive synchronization
- Performs byte stuffing and de-stuffing for transparency processing
- Performs optional CRC-CCITT and CRC-32 FCS generation and error checking
- Supports optionally flow-through mode
- Performs abort sequence insertion and detection
- Arbitrary packet length (1 or more octets) and flag sharing (single flag between frames)
- Provide minimum and maximum packet length checking, removing and reporting
- Transparency by octet stuffing of flag (0x7E), control escape (0x7D) and abort sequence
- Automatic transfer halt on receive FIFO host-side at end of packet
- Error detection for Underflow of transmit FIFO, Overflow of receive FIFO, parity error on transmit
- Optional removal of FCS from receive frames

- Optional transmit FCS insertion

#### **UTOPIA / POS-PHY INTERFACE**

- Complies with ATM forum Utopia Level 2 and 3 Specification
- Supports 32-bit 100MHz Transmit and Receive interface
- Provides up to total 16 cell buffers for transmit and receive
- Transmits and receives both 52 and 54 byte cell
- Generates and checks data parity of Utopia interface
- Supports programmable Transmit CLAV (transmit cell available) signal for 0,1,2,3 cell look ahead
- Supports programmable Receive CLAV (receive cell available) signal for 0,1,2,3 byte look ahead
- Provides 32-bit up to 100 MHz industrial standard POS-PHY interface

#### **PERFORMANCE MONITORING**

- Supports line path performance monitoring
- Provides 32-bit saturating counter of idle cells transmitted
- Provides 32-bit saturating counter of assigned cells transmitted
- Provides 32-bit saturating counter of valid cells received
- Provides 32-bit saturating counter of idle cells received
- Provides 32-bit saturating counter of cells received with HEC error
- Provides 32-bit saturating counter of cells discarded
- Provides 32-bit saturating counter of REI-L errors
- Provides 32-bit saturating counter of REI-P errors
- Provides 32-bit saturating counter of BIP-8 (B1, B2 and B3) errors
- Provides 32-bit saturating counter of POS frame check sequence errors
- Provides 32-bit saturating PPP good frame counter
- Provides 32-bit saturating PPP bad FCS counter
- Provides 32-bit saturating PPP aborted frame counter
- Provides 32-bit saturating PPP Runt frame counter

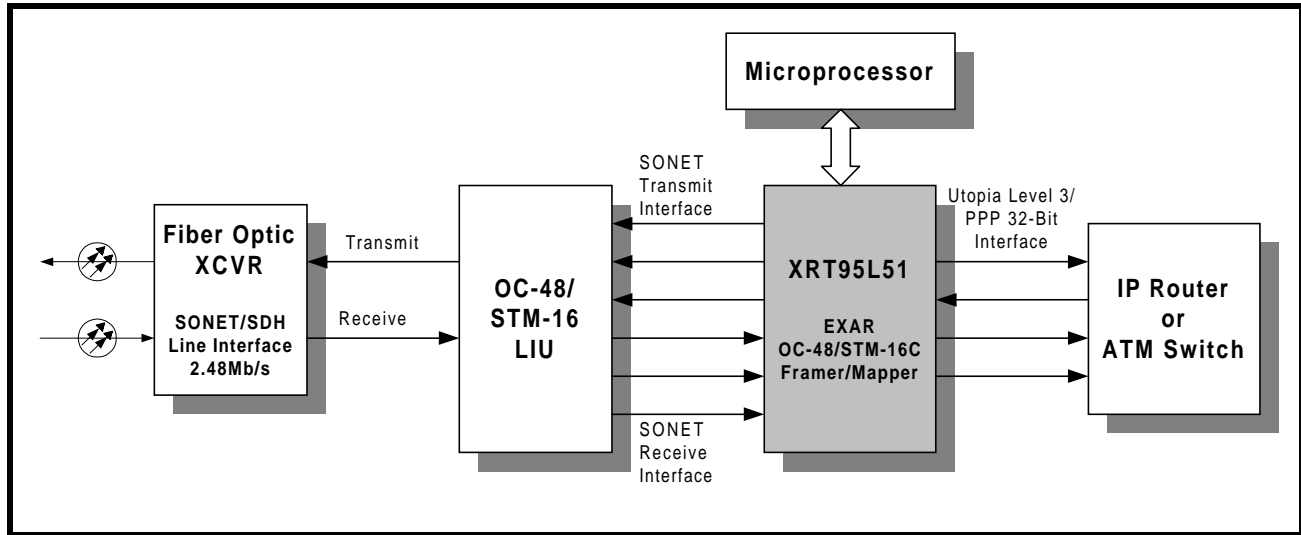
**INTERRUPT, STATUS AND TEST**

- Provides individually maskable interrupts
- Provides one second interrupt generations
- Generates interrupts from the following causes:  
 OOF status change, LOS status change, AIS status change, COFA, Utopia/PPP-PHY parity error, Utopia/PPP-PHY FIFO overrun, Utopia/PPP-PHY

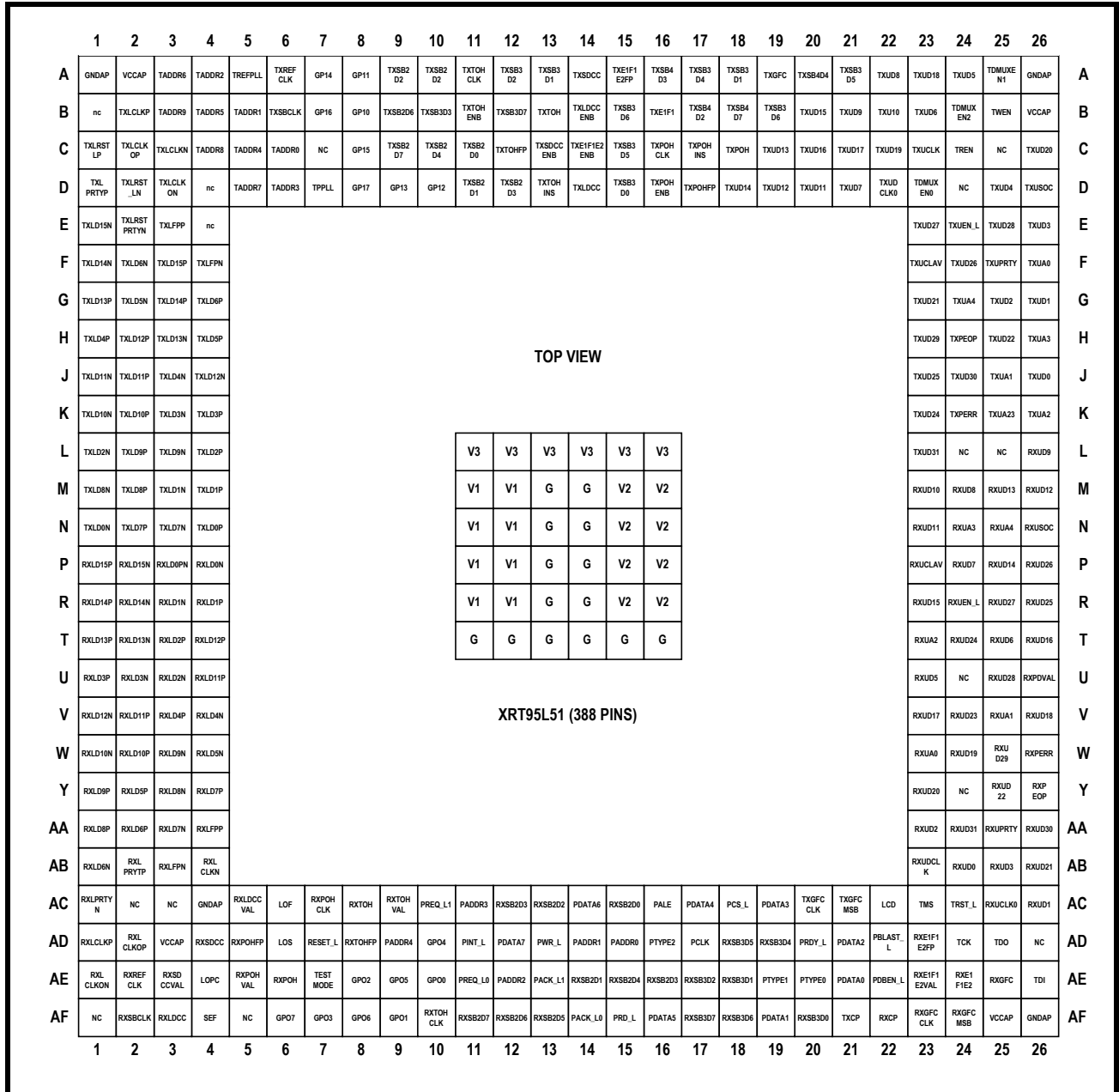
FIFO under-run, change of cell alignment, HEC errors, LCD status change

- Provides Local and Remote Line Loopback
- Provides SONET Remote Loopback
- Provides local ATM/PPP and UTOPIA Loopback
- Supports IEEE 1149.1 JTAG testing

**FIGURE 2. TYPICAL APPLICATION**



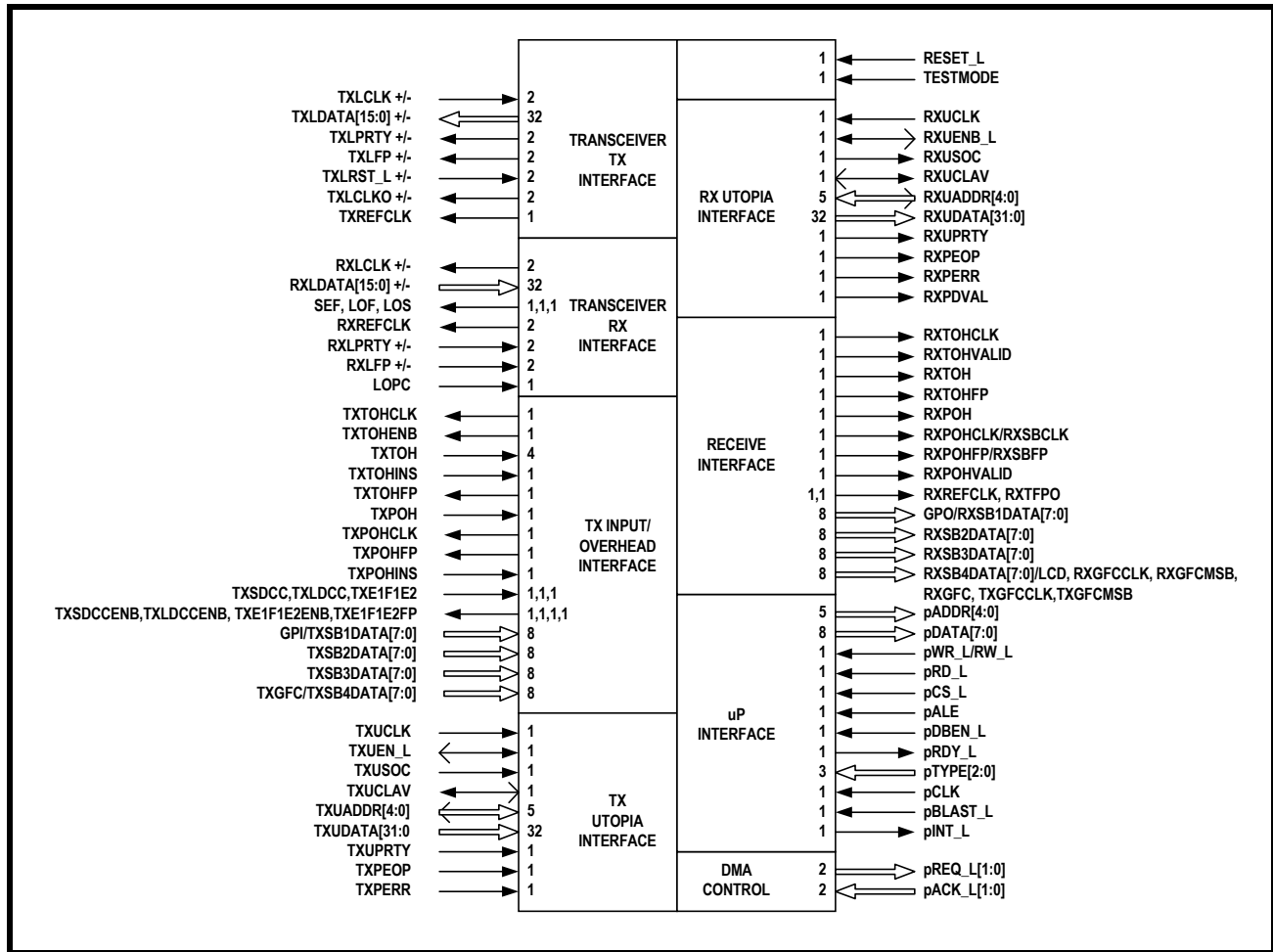
**FIGURE 3. PIN OUT OF THE XRT95L51 IN THE 388 PIN PBGA PACKAGE**



**ORDERING INFORMATION**

<b>PART NUMBER</b>	<b>PACKAGE TYPE</b>	<b>OPERATING TEMPERATURE RANGE</b>
XRT95L51IB	388 Pin PBGA 35x35 mm, 26x26 Ball Matrix	-40°C to +85°C

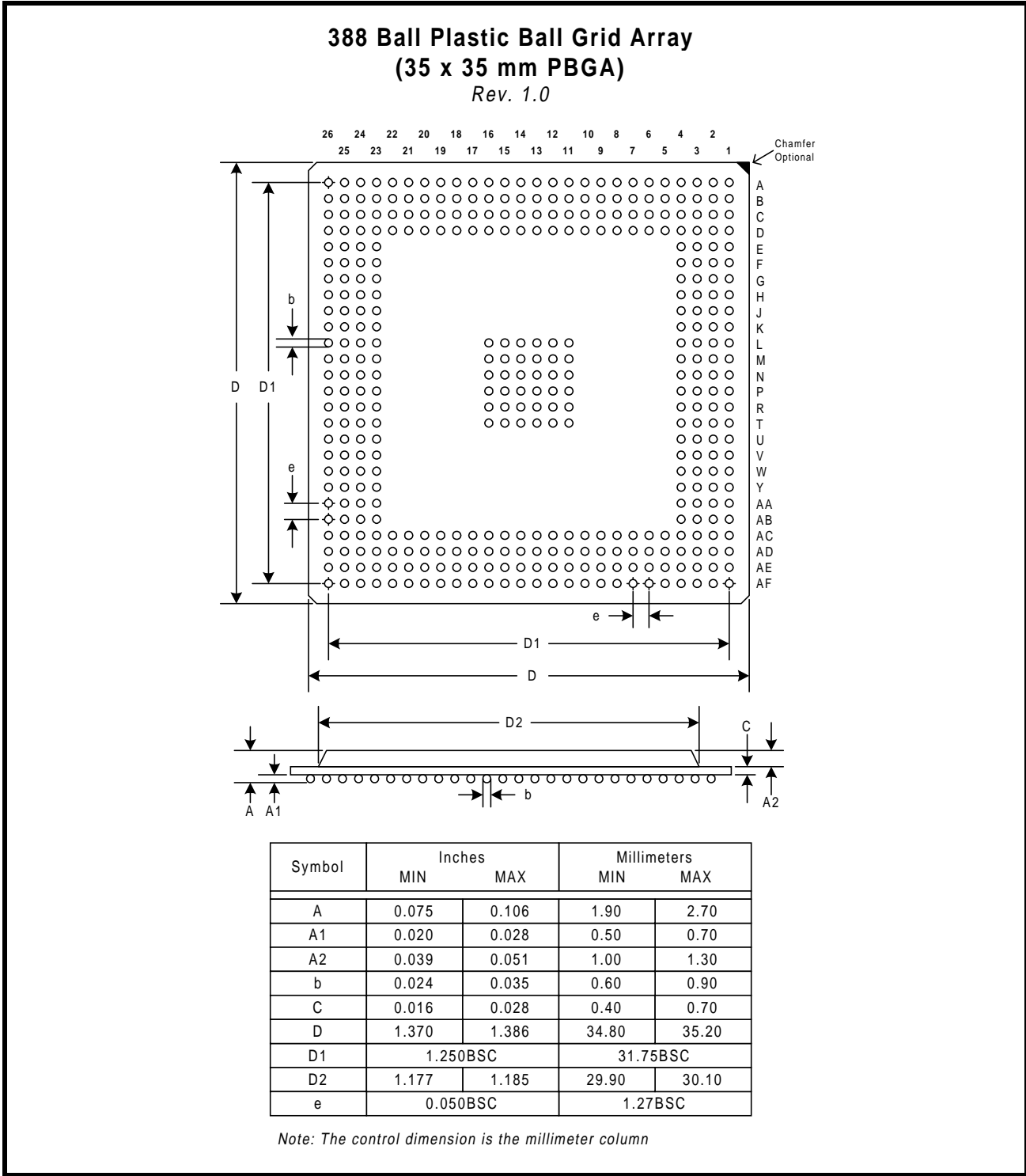
FIGURE 4. SIGNAL DIAGRAM OF XRT95L51



**ORDERING INFORMATION**

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT95L51B	388 Pin PBGA 35x35 mm, 26x26 Ball Matrix	-40°C to +85°C

**PACKAGE DIMENSIONS**



**REVISION HISTORY**

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