DATA SHEET

Communications

XRT94L43

SONET/SDH STS-12/STM-4 to E3/DS3/STS-1 Mapper/Demapper

Features
- Provides SONET frame scrambling and descrambling
- Provides STS-1 (EC1) mapping/demapping for up to 12 STS-1s
- Supports mixing different signal speeds: STS-1 and DSE/E3 and DS3 tributaries
- Full APS support for full redundancy applications
- Lookback support for SONET/SDH and E3/DS3/STS-1

Applications
- Add/Drop multiplexers
- Digital cross connects
- Sonet/SDH multiplexers
- MSPP switches
- Access Equipment

First in a series of pioneering SONET aggregation devices, the XRT94L43 is a framer/mapper/jitter attenuator capable of aggregating 12 DS3/E3/STS-1 data into SONET/SDH STS-12/STM-4. The device offers several new industry functions that distinguish the XRT94L43 in a crowded marketplace. Characteristics including Level 2 performance monitoring, internal clock generation, and simultaneous support for different data rates in the same device illustrate how this product is different than competitive offerings. The XRT94L43 is focused on the growing access and metro area network equipment manufacturers that need to groom or aggregate lower power signals to OC-12.

The XRT93L43 supports the mapping and demapping of 12 channels of T3, E3, or STS-1 rate signals to and from STS-12/STM-4. It has a fully synthesized clocking approach that generates all clock speeds (622 MHz, 77.6 MHz, 19.44 MHz) from a single 6.48, 12.96, 19.44, or 77.76MHz clock signal. This eliminates the need for Telecom Bus/Serial Port Interfaces and additional clocks for jitter attenuator de-synchronization at DS3, E3, and STS-1 data rates, offering designers reduced costs, and more development flexibility. The XRT94L43 can also multiplex and groom four channels of STS-3/STM-1 onto a single STS-12/STM-4 signal. The STS-12 input can be configured either as a 622MHz serial interface or as a 77.76MHz Telecom Bus interface. Both interfaces support 1:1 and 1+1 automatic protection switching.

Desynchronization from the SONET frame to DS3/E3 is provided through 12 independent jitter attenuators. The jitter attenuators have clock smoothing capability to achieve compliance with Bellcore and ITU-T standards. Customers can expect low jitter DS3 or E3 signals from their line-card designs. The DS3/E3 framers support all common framing formats including C-bit parity, M13, ITU-T G.751 and ITU-T G.832. Outputs are also provided in the form of an STS-1 frame which offers overhead termination and generation capabilities. Pseudo Random Bit sequence generation and detection is included for Bit Error Rate Testing.

The XRT94L43 supports a byte-wide interface through the telecom bus standard for both the STS-12/STM-4 data path as well as the STS-3/STM-1 data paths. In addition, the XRT94L43 handles the generation and termination of the payload overhead. It includes generating transmit payload pointers (H1/H2 bytes) with NDF insertion, and computing and inserting BIP-8 (B1/B2 bytes).

The XRT94L43 is implemented in 0.25µ CMOS and runs from a 2.5V supply. All inputs are CMOS except the serial bus/STS-12 telecom bus, which is PECL for high-speed interfacing. I/O supports 3.3V operation and the device comes in a 516 lead PBGA package that functions over industrial temperature ranges (-40 to 85+ C).