DATA SHEET

AP NOTE AN2552

AP NOTE DAN-107

AP NOTE DAN-108

AP NOTE GEN UART

# Communications

**ST16C2552**

**Dual UART with 16-Byte Transmit and Receive FIFOs**

**Features**

- Pin to pin and functionally compatible to National NS16C552
- Software compatible with INS8250, NS16C550
- 1.5 Mbps transmit/receive operation (24MHz Max.)
- 16 byte transmit FIFO.
- 16 byte receive FIFO with error flags.
- Independent transmit and receive UART control
- Four selectable Receive FIFO interrupt trigger levels, fixed XMIT FIFO interrupt trigger level
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD).
- DMA operation and DMA monitoring via package I/O pins, TXRDY/RXRDY
- UART internal register sections A & B may be written to concurrently
- Multi function output allows more package functions with fewer I/O pins
- Programmable character lengths (5, 6, 7, 8) with Even, odd, or no parity

The ST16C2552 (2552) is a dual universal asynchronous receiver and transmitter (UART). The ST16C2552 is an improved version of the NS16C552 UART. The 2552 provides enhanced UART functions with 16 byte FIFO's, a modem control interface, and data rates up to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements.

An internal loop-back capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50 Bps to 1.5 Mbps. The Baud rate generator can be configured for either crystal or external clock input. The 2552 is available in 44, pin PLCC packages. The 2552 provides block mode data transfers (DMA) through FIFO controls. DMA transfer monitoring is provided through the signals -TXRDY and -RXRDY. An Alternate Function Register provides the user with the ability to the write the control registers for both UARTS concurrently.

The 2552 is functionally compatible with the NS16C552. The 2552 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.