DATA SHEET

Communications

XR16C2852

AP NOTE DAN-108

AP NOTE DAN-107

Dual UART with TX and RX FIFO Counters, 128 Bytes of FIFOs and Automatic RS-485 Half Duplex Control

Features

- Pin and functionally compatible to ST16C2552, and National PC16552/NS16C552
- Independent channel A/B control
- Up to 1.5 Mbps data rate operation
- 128 byte transmit FIFO to reduce CPU bandwidth requirement
- 128 byte receive FIFO with error flags to reduce CPU bandwdth requirement
- Programmable transmit and receive FIFO trigger level from 0 to 127
- Automatic RTS/CTS flow control with hysteresis
- Automatic software flow control
- Automatic RS485 half duplex direction control on -RTS pin.
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD, and software controllable line break)
- Infrared (IrDA ver 1.0) transmit and receive data encoder/decoder
- Device identification and revision
- Standard 460.8 Kbps transmit/receive data rate with 7.3728 MHz crystal or external clock source
- +5V or 3.3V operation
- Industrial and commercial temperature grades
- 44-pin PLCC package

The XR16C2852 (2852) is a dual universal asynchronous receiver and transmitter (UART). The 2852 provides enhanced UART functions with 128 byte FIFO, automatic RS-485 half duplex control, a modem control interface, and data rates up to 1.5 Mbps. Onboard status registers provide the user with error indications and operational status. An alternate function register supports concurrent write to UART A and B. System interrupts and modem control features may be tailored by external software to meet specific user requirements.

An internal loopback capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates up to 1.5 Mbps. The baud rate generator can be configured for either crystal or external clock input. The 2852 is available in a 44-pin PLCC package and functionally compatible with the ST16C2552. The 2852 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.