DATA SHEET

AP NOTE DAN-102

AP NOTE DAN-107

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AP NOTE GEN UART

Communications

XR16C864

Quad UART with RX/TX FIFO Counters and 128-Byte FIFO

Features

- Compatibility with the Industry Standard ST16C554/654, ST68C554/654, TL16C554
- 1.5 Mbps transmit/receive operation (24MHz)
- 128 byte transmit FIFO
- 128 byte receive FIFO with error flags
- Automatic RS-485 half-duplex switch
- Independent transmit and receive DMA signals
- Independent transmit and receive FIFO counter
- Automatic software/hardware flow control
- Programmable Xon/Xoff characters
- Software selectable Baud Rate Generator pre-scaleable clock rates of 1X, 4X.
- Four selectable, and Programmable Transmit/Receive FIFO interrupt trigger levels
- Standard modem interface or infrared IrDA encoder/decoder interface
- Software flow control turned off optionally by any (Xon) RX character
- Independent clock input for channel C
- FIFO monitoring and separate IrDA TX outputs
- Sleep mode (200mA stand-by)
- 100-pin QFP packages

The XR16C864 (864) is a universal asynchronous receiver and transmitter (UART) with a dual foot print interface compatible with the ST16C554/654 and ST68C554. The 864 is an enhanced UART with 128 byte FIFO's, Independent Transmit and Receive FIFO counter, RS-485 Support, Independent Transmit and Receive DMA signals, automatic hardware/software flow control, and data rates up to 1.5Mbps.

Onboard status registers provide the user with error indications and operational status, modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics.

The 864 is available in 100 pin QFP packages. The XR16C864 offer faster channel status access by providing separate outputs for TXRDY and RXRDY, offer separate Infrared TX outputs and a musical instrument clock input (MIDICLK). The 864 combines the package interface modes of the 16C554/654 and 68C554/654 series on a single integrated chip.