

Fujitsu Flash MCU BI ROM Protocol of 16LX Family

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History

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Flash MCU BI-ROM Protocol

The F²MC-16LX Flash MCU contains a burn-in ROM (BiROM) program that supports a proprietary protocol to allow download of a user program to on-chip RAM memory (step 1). The user program is then able to manipulate on-chip Flash memory as required (step 2).

Two basic serial modes are supported, synchronous serial and asynchronous serial. It is not important to the protocol which serial mode is in use.

The below diagram illustrates the context.



This application note describes the commands, which are supported by the BiROM of the 16LX Flash MCUs in order to generate an own programming environment.

As already mentioned, two basic serial modes are supported, synchronous serial and asynchronous serial. After reset of the MCU, the mode pins and two port pins select the programming mode respectively. It is not important to the protocol which serial mode is in use. However, communications settings obviously vary:

Synchronous	8 data bits, external clock (500kbs max)
Asynchronous	8 data bits, 1 stop bit, no parity, baud rate: $(mcu clk / 4) / (8 x 13 x 2)$
	(4800 @ 4MHz, 9600 @ 8MHz, 19200 @ 16MHz)

Follow the sequences in the examples to download and execute the user program. Once the user program is running, the BiROM is no longer active and all further communication is user defined. To allow compatibility with all devices, it is important that the user program uses the minimum of resources. Therefore, we recommend your program uses the following memory map:

<u>Memory Map</u>

0100 - 016F	Variables
0170 – 017F	Stack
0180 - 018F	Registers (bank 0)
0190 – end of RAM	User program code and write buffer (512B max)

Common Pin Settings

Pin Name	Logic Level	Description	QFP100	QFP120
MD2,1,0	110	Programming mode	51,50,49	87,88,89
P00	0	Programming mode	85	95 (J19/21) ^{*)}
P01	0	Async, 4800, 8bit, 1 stop, no parity	86	96 (J19/20) ^{*)}
	1	Clk Sync, Ext clock (500kbs max)		
Vss	-	Power supply	81	91 (J19/25) ^{*)}
Vcc	-	Power supply	84	94 (J19/22) ^{*)}

^{*)} Pin numbers in brackets refer to the QFP120 Flash-Test-Board (FLASH-EVA2-120P-M13)

Commands

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte n
76543210	76543210	7 6 5 4 3 2 1 0	76543210	7 6 5 4 3 2 1 0	76543210
Command	Address	Address	Count	Count	Data/Checksum
7-0	15-8	7-0	15-8	7-0	7-0

CommandVarious actions, see table below.AddressStart address of RAM download codeCountNumber of bytes to transfer. 1 = 1 byte.DataData bytes sentChecksumCumulative sum

		С	or	nn	na	nd	S		Description	Comment
0	0	0	1	1	I	-	I	18	Communication	General communications check
									check	
0	0	0	0	0	I	I	I	00	Download	User program is downloaded to RAM
0	1	0	0	0	I	-	I	4x	Execute	User program is executed. Address and count ignored (address
										fixed to 0990h (0190h MB90560))

Command Responses

	Byte 0							
765	j	4	3	2	1	0		
Comn	na	and	Resp					
7-4	4			3	8-0			

Resp Status response from MCU (bits 7-4 return bits 7-4 of command byte)

Response	Description	Comment
0 0 0 1 x1	OK	
0 0 1 0 x2	Command Error	

EXAMPLES

General Communications Check

PC	18	
MCU		11

Download (00h)

	co	mman	d /	co	unt	da	ita	chk	resp
	i	address	5						
PC	00	09	90	00	02	01	02	9E	
MCU									01

This example downloads 2 data bytes, 01_{hex} and 02_{hex} onto RAM location 990_{hex} . See also the cumulated checksum $9E_{hex}$ and response from the MCU.

Execute (40h)

	co	mman	d /	col	unt	
	address					
PC	40	XX	Xx	00	00	
MCU						no response, jump is immediat

Note

When you select the Burn-IN ROM mode for the CPU, and you try to program the upper Flash memory area with code executed in RAM the situation is as follows:

In Burn-IN ROM mode the Burn-IN ROM is always visible at FF0000-FFFFFF. So you cannot program the page FF directly. Therefore Bit 3 of the FMCS register is used. Bit 3 of the FMCS register is used as a upper memory enable. To program the page FF, you have to set this bit first. After this the page FF will be mapped to page FE.