

## declaration to handle the clockmodulator

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### History

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## **declaration regarding handling clock modulator by changing PLL settings**

The delay line of the clock modulator is specified for frequencies between 16 MHz and 48 MHz.

If the input frequency of the delay line is outside these limits then glitches could appear at the output clock of the delay line.

These glitches are caused by the wrong calibrated delay line.

The delay line is calibrated always after the clock modulator is switched on even if the automatic calibration is enabled.

The automatic calibration will be active configurable time intervals. If the clock modulator is not changed and the input frequency is changed then the clock modulator runs with a non-calibrated delay line until the next automatic calibration is activated.

This would lead quite sure to a crash of the application.

Because always switch off clock modulator first and then change PLL-settings.