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Application-Note

„Connecting a graphic controller of the CREMSON-series to a MB91F361-Microcontroller“

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History

Revision	Date	Comment
V 0.1	19march2001	New Document, tm
V 0.2	23march2001	Corrected some Typos, tm

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1. Introduction

Connecting a graphic controller of the CREMSON-series (currently CREMSON MB86290A or SCARLET MB86291) to a FR-Microcontroller, like the MB91F361, is not very difficult.

In principle you just have to connect all bus-interface-lines of the FR to all bus-interface-lines of the graphic controller one by one.

However, there are some details one should take care about, which are:

- write-lines
- ready-line
- 5 Volt / 3.3 Volt Bus-voltage-levels

2. Write-Lines

Having a detailed look to the architectures of the CREMSON-series and the FR-series you will recognize, that the graphic controller is a little-endian architecture and the FR-Microcontroller is a big-endian device.

In 32bit access mode, there is no difference, however using 8bit or 16bit accesses one should be aware of that the write-lines are connected in cross-order.

The following table shows this in detail:

FR-Microcontroller	Graphic controller
WR0	WR3
WR1	WR2
WR2	WR1
WR3	WR0

NOTE: The FUJITSU Software API, which is included in the Starterkit, is always using 32bit access only!

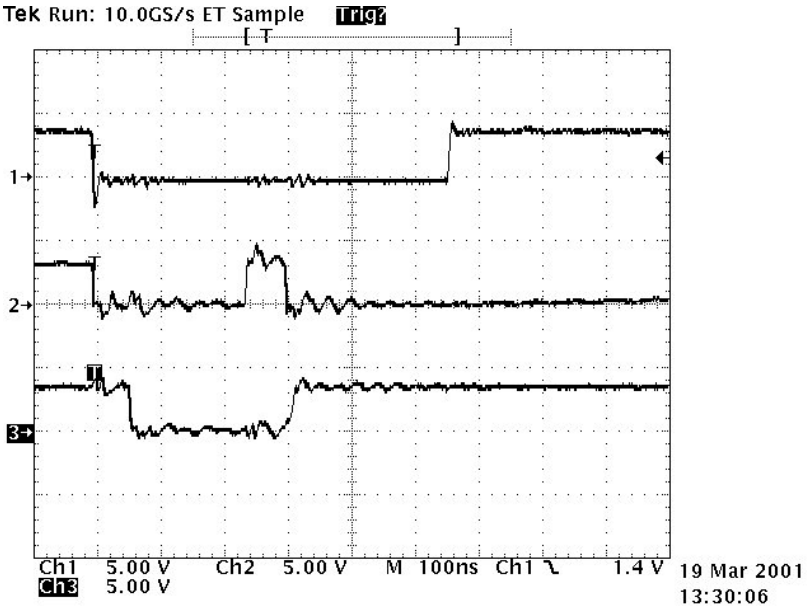
3. Ready-line

3.1 Description

While using the bus of the FR-MCU the external device has (or devices have) to make sure to use the bus in the correct way. Therefore some bus-lines are available to handle this.

One of this lines, the Ready-line, is differently handled at FR-MCU and the graphic controller devices of the CREMSON-series. Connecting the graphic controller´s XRDY-line directly to the RDY-line of the FR will make the bus hang-up.

The following picture shows the ChipSelect (1), XRDY of CREMSON (2) and the RDY of FR (3).



As you can see, the graphic controller is setting its XRDY-line shortly before being ready to HIGH and then when being ready it releases the XRDY-line to LOW (SH3-bus mode). The FR-Microcontroller instead is looking for a HIGH-level after the external device, which is connected to his bus, is ready. So connecting both ready-lines directly together will result in a deadlook after the first READ/WRITE-access.

NOTE: Instead of using the RDY-line, an appropriate number of wait-states can be used to ignore this different behavior. But this will slow down the system performance.

3.2 Using a PAL

On the graphic-subboards for the CREMSON and the SCARLET a PAL is used to connect the XRDY-line to the RDY-line.

To handle the ready-line a small state machine is used. The following source code shows how this state machine is realized:

```
SEQUENCE bus_io  {
/*
 * at powerup starting in first state = first PRESENT statement
 *
 * CRM_Ready and FR_Ready are high-active and CS_in is low-active !!!
 */

        /* State 0 */
    PRESENT pre
         out FR_Ready; /* set FR_Ready = high */
         if !CS_in next pre;
         if  CS_in next CRM_working;


        /* State 1 */
    PRESENT CRM_working
         /*out !FR_Ready  -> not included => FR_Ready = low */
         if !CRM_Ready next CRM_working;
         if  CRM_Ready next CRM_finished;


        /* State 2 */
    PRESENT CRM_finished
         out FR_Ready; /* set FR_Ready = high */
         if  CS_in next CRM_finished;
         if !CS_in next pre;
}
```

At power-up, the state machine is entering <STATE 0>. The RDY-line (FR_Ready) is set to HIGH, which means the device is ready for operation. To enter <STATE 1> a falling edge of the ChipSelect-line (CS_in) must be detected. By the way, don't get confused about the LOW-level active statements above, where !CS_in means CS is HIGH.

After CS_in changes to LOW (=active) the state machine is entering <STATE 1>. Then FR_Ready (RDY) is set to LOW. Waiting for XRDY (CRM_Ready) going to HIGH to enter next state.

Entering <STATE 2> the RDY-line (FR_Ready) is set to HIGH, indicating that the external device finished operation and bus can be released, which is done by the FR setting CS_in to HIGH again.

NOTE: The picture above shows exactly the sequence of one bus-access using this state machine. The shift by one bus-clock-cycle of the outgoing FR_Ready signal is done by the state machine, which needs one clock-cycle to put a new signal to an output-pin.

4. 3.3 Volt bus-voltage-level

4.1 Description

The bus-interface of the graphic controller is completely running at 3.3 Volt. Connecting it to a FR-device you have to make sure that the bus-interface of the FR is working at 3.3 Volt too, using the 3.3Volt-split.

However, using the 3.3Volt-split of the FR-MCU, not all bus-lines are shifted from 5V to 3.3V.

4.2 Bus-lines from FR to CREMSON

The following lines have to be shifted from 5V to 3.3V:

- DMA Acknowledge (DACK)
- DMA end of progress (DEOP)

At the Starterkit this is done by using the PAL, which has 5V tolerant input-pins.

4.3 Bus-lines from CREMSON to FR

The following lines have to be shifted from 3.3V to 5V:

- external Interrupt-lines
- DMA Request (DREQ)

At the Starterkit this is done by using a non-inverting TTL-buffer, which is interpreting the 3.3V as TTL-HIGH.