Recommended operation conditions

Condition A

Parameter	Symbol	Specifications			Unit
		Min.	Typ	Max.	
Supply voltage	VDDL*1	2.3	2.5	2.7	V
	VDDH	3.0	3.3	3.6	
Input voltage (High level)	VIH	2.0		VDDH+0.3	V
	VIHV*2	2.0		5.5	
Input voltage (Low level)	VIL	-0.3		0.8	V
	VILV*2	-0.3		0.8	
Input voltage to VREF	VREF	1.05	1.10	1.15	V
VRO external resistance	RVRO		2.7		k ohm
AOUT external resistance*3	RAOUT		75		ohm
ACOMP external capacitance*4	CACOMP		0.1		uF
Ambient temperature	TA	-40		85	deg.C

*1 Include analog power supply and PLL power supply
*2 HSYNC, VSYNC and EO inputs
*3 AOUTR, AOUTG and AOUTB pins
*4 ACOMPR, ACOMPG and ACOMPB pins

Condition B (When BCLKI is equal or faster than 90MHz.)

Parameter	Symbol	Specifications			Unit
		Min.	Typ	Max.	
Supply voltage	VDDL*1	2.6		2.7	V
	VDDH	3.5		3.6	
Ambient temperature	TA	-40		70	deg.C
Other than the above two		Same as the above table A			

*1 NOT include analog power supply and PLL power supply

DC Characteristics

Same as the table in Rev.1.1 hardware specifications

AC Characteristics

Host interface (Condition A)

[External CL : 20pF]

Parameter	Symbol	Specifications			Unit
		Min	Typ	Max	
Address set up time	tADS	3.0			ns
Address hold time	tADH	1.0			ns
XBS set up time	tBSS	3.0			ns
XBS hold time	tBSH	1.0			ns
XCS set up time	tCSS	3.0			ns
XCS hold time	tCSH	1.0			ns
XRD set up time	tRDS	3.0			ns
XRD hold time	tRDH	1.0			ns
XWE set up time	tWES	3.0			ns
XWE hold time	tWEH	1.0			ns
Write data set up time	tWDS	5.0			ns
Write data hold time	tWDH	1.0			ns
DTACK set up time	tDAKS	3.0			ns
DTACK hold time	tDAKH	1.0			ns
DRACK set up time	tDRKS	3.0			ns
DRACK hold time	tDRKH	1.0			ns
Read data delay time (to XRD)	tRDDZ	4.0		8.5	ns
Read data delay time *1	tRDD	4.0		9.5	ns
XRDY delay time (to XCS) SH3/4	tRDYDZ	3.0		9.0	ns
XRDY delay time (to XCS) V832	tRDYDZ	3.0		13.0	ns
XDRY delay time	tRDYD	3.5		8.5	ns
XINT delay time *2	tINTD	-		-	ns
DREQ delay time	tDQRD	3.5		7.5	ns
MODE hold time *3	tMODH	-		20.0	ns

*1 Cremson outputs the read data 1 cycle prior to the sampling timing of CPU.
*2 XINT is output synchronously to Cremson's internal timing clock. So this is an asynchronous signal to the host CPU.
*3 Hold time to reset release timing.

Maximum delay time parameters in condition B are as follows:

[External CL : 20pF]

Parameter	Symbol	Specifications			Unit
		Min	Typ	Max	
Write data set up time	tWDS	4.0			ns
Read data delay time (to XRD)	tRDDZ			7.5	ns
Read data delay time *1	tRDD			6.0	ns
XRDY delay time (to XCS) SH3/4	tRDYDZ			7.5	ns
XRDY delay time (to XCS) V832	tRDYDZ			10.5	ns
XDRY delay time	tRDYD			7.0	ns
DREQ delay time	tDQRD			6.5	ns

Graphics memory interface

Clock

Parameter	Symbol	Specifications			Unit
		Min	Typ	Max	
MCLKO frequency	tMCLKO	10			ns
MCLKO H pulse width	tHMCLKO	3.5			ns
MCLKO L pulse width	tLMCLKO	3.5			ns
MCLKI delay	tDMCLKI			TBD	ns

Input signals

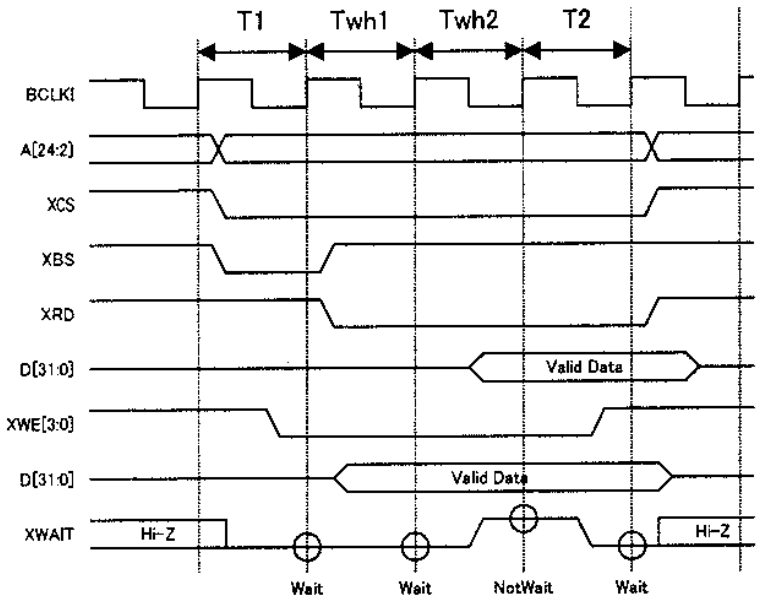
Parameter	Symbol	Specifications			Unit
		Min	Typ	Max	
MD0-63 input set up time	tSMD	3			ns
MD0-63 input hold time	tHMD	1			ns

Output signals

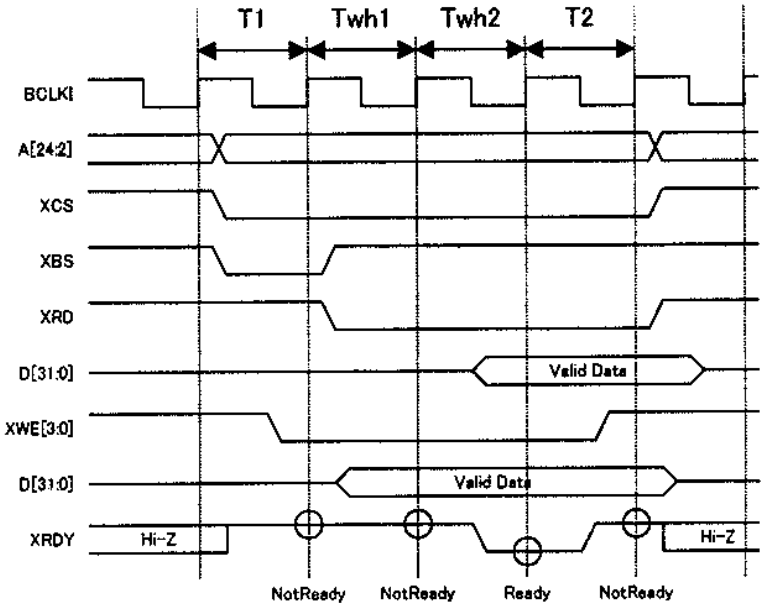
Parameter	Symbol	Specifications			Unit
		Min	Typ	Max	
MA0-13 output delay time	tDMA	0		5	ns
MCKE output delay time	tDMCKE	0		5	ns
MRAS output delay time	tDMRAS	0		5	ns
MCAS output delay time	tDMCAS	0		5	ns
MWE output delay time	tDMWE	0		5	ns
MDQM0-7 output delay time	tDMDQM	0		5	ns
MD0-63 output delay time	tDMD	0		5	ns

CPU Interface Timing Diagrams

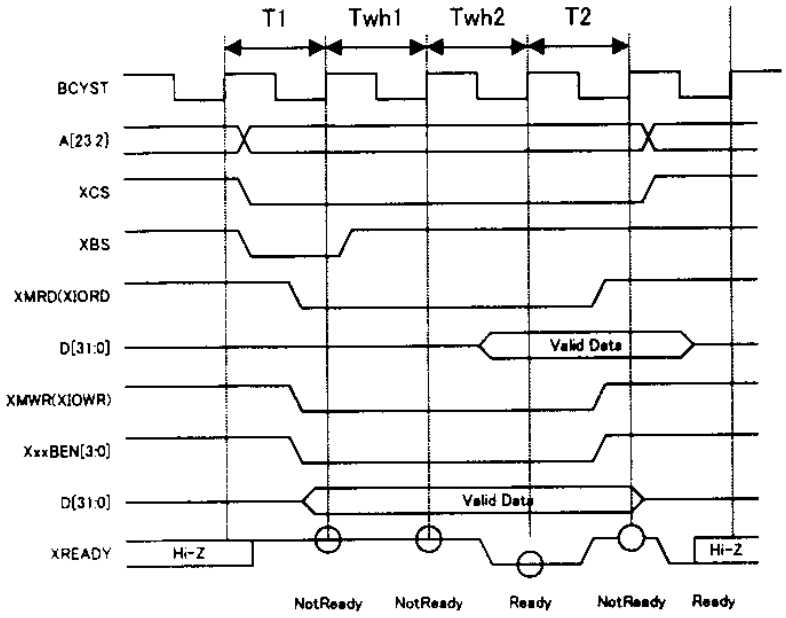
SH-3 Mode :



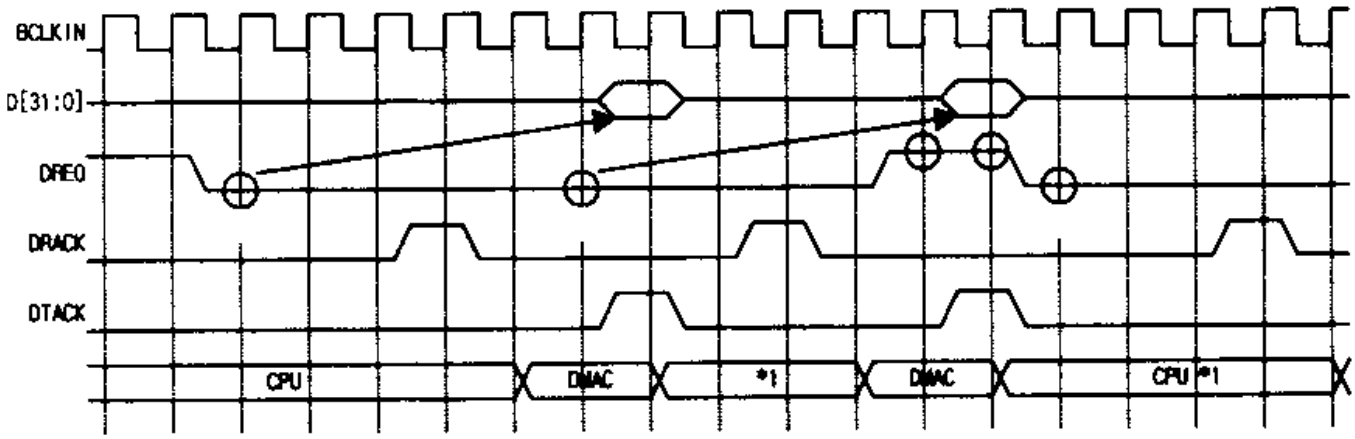
SH-4 Mode :



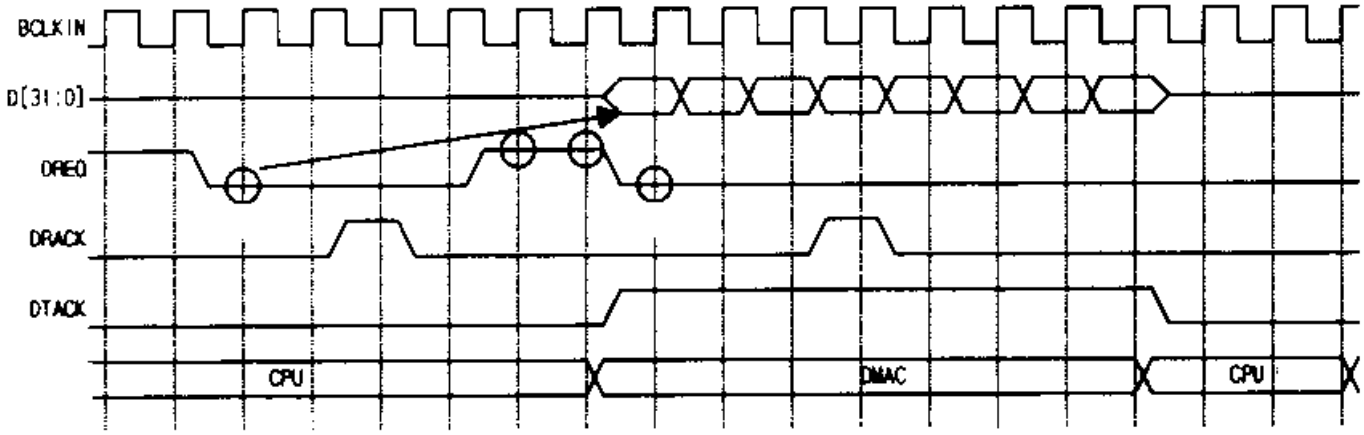
V83x Mode :


T1
Twh1
Twh2
T2
BCYST
A[23:2]
XCS
XBS
XMRD(X)IORD
D[31:0]
Valid Data
XMWR(X)IOWR)
XxxBEN[3:0]
D(31:0]
Valid Data
XREADY
Hi-Z
Hi-Z
NotReady
NotReady
Ready
NotReady
Ready

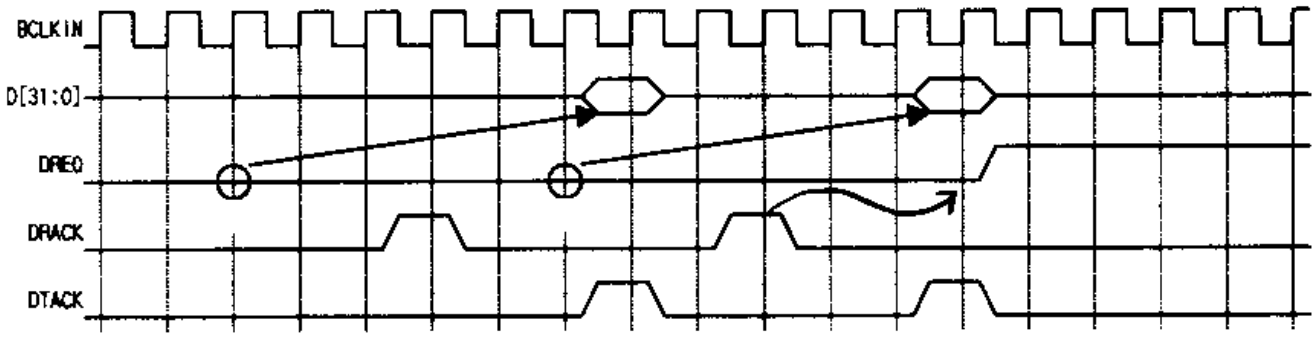
SH-4 Single Address DMA (long word transfer)



SH-4 Single Address DMA (8 long word transfer)



SH-4 Single Address DMA finalizing



Last data