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Application-Note

„Duty Cycle measurements at DLCK-pin (CREMSON-series)“

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History

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1. Introduction

While connecting a display to a graphic controller, in some cases the duty cycle of the provided display clock (DCLK) is very important because some displays need an exact 50 to 50 duty cycle.

At the CREMSON-series the display clock depends on the settings for your display. Calculating the prescaler-value with the 200.45 MHz internal display unit main clock you will get the value of DCLK.

However, only in some cases the duty cycle of the DCLK is 50% high and 50% low.

The following table shows the results of the duty cycle measurement for several prescaler-values. It starts at 0x07, which is used for VGA-resolution.

2. Duty cycle of DCLK

Prescaler-value	measured duty cycle *)
0x07	49 %
0x08	46 %
0x09	41 %
0x0A	36 %
0x0B	34 %
0x0C	38 %
0x0D	43 %
0x0E	46 %
0x0F	49 %
0x10	46 %
0x11	44 %
0x12	41 %
0x13	39 %
0x14	38 %
0x15	36 %
0x16	34 %
0x17	33 %
0x18	35 %
0x19	38 %
0x1A	40 %
0x1B	42 %
0x1C	44 %
0x1D	46 %
0x1E	48 %
0x1F	49 %

Table 1: measured duty cycle of DCLK

NOTE:
*) For example 49% means 49% = high width of DCLK and 51% = low width of DCLK.