Fujitsu

Graphic Controller

frequently asked questions

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MB86290 CREMSON QUESTIONS :

Some pins of CREMSON are different in the board schematics and the manual. What is the correct reference ?

Some signals in Pin-table in the manual (release1 dec-99) are wrong.
Correct pin assignment like described in release2 (may-2000) are :

212 ACOMPB
213 AVD1
214 AOUTB
215 AVS1

222 AVS4
223 AOUTR
224 AVD4
225 VRO
226 VREF
227 ACOMPR

What are the 6 CREMSON testpins (TEST0..5) for ?
Is there anything important to know for a customer ?

These test pins are for our logic and memory scan tests. So customers need to tie these pins to Vdd (keep them in High level).

Is it possible to connect two 16-bit SDRAMs (2x512kx16bit) to the CREMSON to have 4MB memory and 32-bit databus ?

I think it is applicable too.
As we mentioned in our hardware specifications, we have checked that 2pcs of 64Mbit SDRAMs (x16bit) can be applied to form 16MB of memory field in 32bit data bus.

In the schematics of the evaluation board, there are R- and C-components on the databus (MD0..63). Please explain if/why they are needed and which values are necessary !

These resistors and capacitors are shown in the schematic diagram just in case if certain signal termination is required externally. But actually we do not put these termination resistors/capacitors in our actual board design. So they would not be required.

What is the relationship between the table "5.5.1 Applicable Display Resolution" and the "5.2.3 Display Parameters" ? There are registers for each display parameter given (e.g. HTP). But no "display resolution register" or something. Does this mean, the user can freely set any values in the display parameters even inbetween the typical resolutions shown in the table ? What are the limitations e.g for the pre-scaler ?

Various display resolutions are defined by display parameter resisters. For example, horisontal pixels on a raster can be defined by one pixel. Any programmable resolution can be displayed if a display device can accept a video timing generated by given parameters. Note that some CRT display may autoblank if improper video timing is given. What is improper depends on CRT display. The parameter limitations exist on relationship among them. In general apply :

0 < HDB <= HDP < HSP < HSP+HSW+1 < HTP
0 < VDP < VSP < VSP+VSW+1 < VTR

In the external sync-mode, the Cremson-output will be syncronized using HSYNC and VSYNC. Which limitations are given when using external video-signals (max. pixels/lines ; max. vertical frequency etc.) ?

Ext-sync mode can be used with internal PLL clock source.
Clock source is specified by CKS bit on DCM register.
HSYNC input is sampled by internal PLL clock at 200MHz.
In this mode, max 5ns error can occur but it is not visible by our eyes if pixel rate is near 12.5Mpixel/sec or lower.
But it will be a problem at XGA mode or 1024x768 display because of fast pixel rate.

In external sync-mode, which display parameters will be set or become valid (like HSP) ? Which display parameters can still be set by the user (like display resolution) ?

Horizontal display period as time should be nealy equal to source. Horizontal sync pulse position as time should be earlier than HSYNC signal of source. HSW should be max value or 255. Cremson waits HSYNC signal during HSW period. Horizontal total pixels as time should be shorter than source. Vertical total rasters should be less than source. Vertical sync position should be less than source. Vertical sync width should be less than or equal to source.

Question about the CPU-Clock input pin :

If the Cremson is not using the BCKLI (host CPU bus clock) for generating the pixel timing, do we need to connect the BCKLI pin from host CPU to Cremson anyway ?

SRAM interfaces typically do not require clock-inputs.

Yes, you still need to connect BCLKI even though it is not related to the pixel timing. Since all the host interface protocol signals (such as address, BS, CS, RD, WR) are driven by this BCLKI, we need to have this clock to be syncronized to the inputs from the host CPU.

Why does the Cremson has both 2,5 V and 3,3 V power supply pins ?

All I/O pins work on 3,3 V and the 2,5 V is used for core logic only.
2.5V is the internal voltage and IOs are 3.3V compatible.
However HSYNC, VSYNC and EO are also 5V tolerant.

Is the RDY signal relevant during DMA transfers, or can it be ignored during this cycles ?

The RDY signal is only relevant on single address transfers.
Dual address transfers will not use the RDY signal.

I think the time between assertion of DREQ and the DRACK is not fixed to a certain number of bus cycles, the delay depends on what the connected processor or Asic is doing. True or false ?

Correct. There are no fixed cycles for assertion of DREQ and DRACK.

What about the number of clock cycles between assertion of DRACK and DTACK, is this fixed to 3 cycles for longword transfer and 4 cycles for 8 long word transfer (burst mode) or is a variable delay allowed here ?

That's the same as 3. - it's not fixed to 3 or 4 cycles.

The interrupt output is low active. Does this mean that this is an open-drain output ?

No, the interrupt output is not open-drain.
You may also use an external resistor of lower value to pull-up this signal.

Consider a DMA transfer from memory to the Cremson, we can access our memory without using the XRD and XBS signals connected to the Cremson, so these will be at a high level during this transfer. Of course XCS and XWE are always high during DMA. Is this true or is the XRD signal actually monitored by the Cremson during DMA.

So, is it allowed to keep XRD, XWR, XBS, XCS at a high level during DMA-cycles?

Yes, in DMA SINGLE-ADDRESS mode, CREMSON don't use the XRD, XWR, XBS and XCS signals.

Note : CPU can access CREMSON by normal CPU read or write protocol during SINGLE-ADDRESS DMA transfer running.
Then XCS must be kept HIGH level during SINGLE-ADDRESS mode DMA unless the CPU access CREMSON by normal CPU read or write.

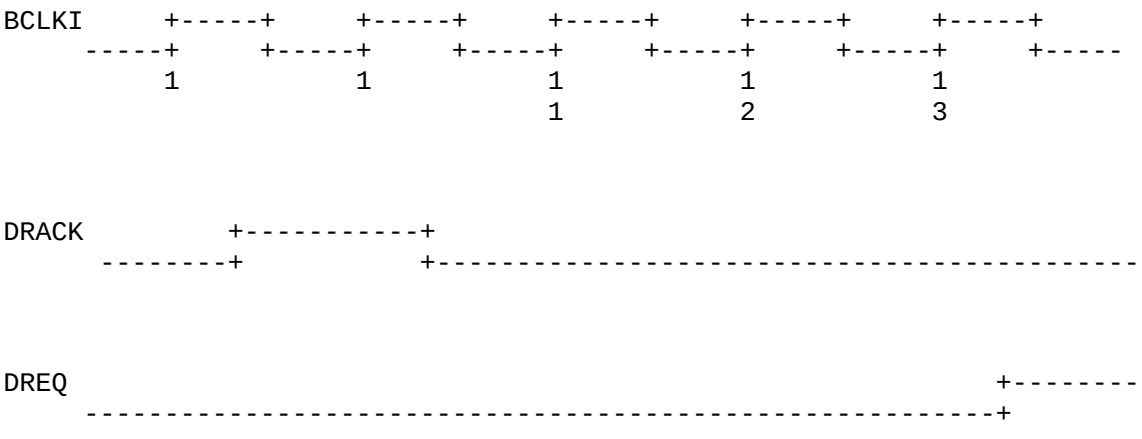
During a Cremson-DMA cycle a connected SH-4 compatible processor uses ist RDY input to communicate with the connected memory devices to get the required data, so my assumption is that the Cremson will hold its RDY output in tri-state during DMA-cycles is this true?

(assuming, of course, that the processor will not try to access the Cremson registers during DMA cycles)

That is correct.
In SingleAddressMode, the CREMSON keeps XRDY in tri-state during DMA-cycles.

If the Cremson sends a DREQ signal to the processor, the processor will respond to that by asserting the DRACK signal, after sampling a high level on the DRACK input the Cremson might decide to negate the DREQ signal because no more bytes need to be transferred. I need to know how many rising clock edges it takes before the Cremson makes DREQ high after reception of DRACK.
The DREQ-signal will go high after 3 cycles from the last DRACK assertion.

See the following chart :



What is the function of ACOMBR/G/B?

ACOMBR/G/B are complement RGB outputs. These pins are for proper termination of the analog DAC outputs and should be connected as explained in the manual (0.1uF to analog GND).

MB86291 SCARLET QUESTIONS :

Is the Scarlet just a "Cremson + embedded SDRAM" ?

No ! Scarlet is NOT just the combination of Cremson and SDRAM. We should be aware about the following major functional upgrade from Cremson to Scarlet:

(1)Full support geometry processor
Prior to the design of Cremson, our graphics team had participated to develop own geometry processor devices to be used in arcade game and PC graphics (all interactive 3D graphics operations).
According to the market requirement to accelerate the total 3D graphics operation (not depending upon the host CPU's floating point computation power), we had determined to integrate 2 sets of Pinolites with enhanced rendering core into one silicon chip.
These Pinolite units are to handle the entire 3D geometry process (transport, loghting, clipping, screen projection, triangle set up) on behalf of host CPU at 1M polygons/sec of sustained performance.
Therefore, even if the burden of the host CPU will be very high, due to all the other operation requirements, still fast enough 2D/3D operation is performed by the Rose/Scarlet.

(2)Digital video capture and flexible scaling
Video capturing feature was eliminated from Cremson at the vry last minute due to the pin count limit.
Now, because of the embedded SDRAM (no more external memory interface), we have enough pins to assign for digital video input and output. This new module is almost the same size as display control module of Cremson.

(3)Enhanced Pixel engine and memory interface bus width. Although Cremson offered only 800MBPS of memory bus band, Scarlet is capable to provide x2 band width. To make a best use of this bus band, drawing unit (DDA,pixel engine, Blt engine) as well as the memory interface unit were all enhanced, so that Rose/Scarlet can deliver x5 performance to Cremson.

Considering all the above factors :

Scarlet = 2xGeoProc + Enhanced Cremson (x5 performance) + Dedicated video capture/scaler + embedded SDRAM of wide bus band.

Therefore the definition of Scarlet is not simply the addition of existing Cremson and conventional SDRAM devices. Please be aware about this many new function blocks are integrated to maximize the speed performance (x5 of performance of Cremson).

Is Scarlet Software-compatible to Cremson ?

Yes. All the register areas and display list formats of the common functions are identical. The added functions like video input and geometry processors are seperated.
Software which was developed using the Cremson evaluation-board MB86290EB-01 can also be used with Scarlet. The only change that has to be made is to the memory mode register (MMR) - see the demos provided for details.
Also special care has to be taken in terms of the limited frame memory size.

Video Capture Unit of Scarlet :

How can analog video signals be input to the interface ?

Rose features an ITU RBT656 (YUV 4:2:2) digital video interface.
An external decoder such as Phillips UAA711x is required to convert the analog video signals to this digital format. The data stream will be read in from the Scarlet by the VI port and then written to graphics memory.
Analog processing, upsampling filters etc. are part of the external decoder.
For details, see the application note about the video input unit of Scarlet !

Video Capture Unit of Scarlet :

Can different video input and display frame rates be used ?

Yes, this is possible. The video input unit can asyncronously write to the frame grabber memory buffer and the circular buffer management will automatically duplicate or leave out frames in order to adjust to the display frame rate.

Can different video input and display resolutions be used ?

Yes, the part to be grabbed from the video stream can be selected using the registers CIHSTR, CIVSTR, CIHEND and CIVEND. The total size to be put in the frame memory is determined by CHP und CVP. The size and position of the picture to be finally displayed can be set by the register values of the W-layer which is dedicated for the video input module.

For details, see the application note about the video input unit of Scarlet !

Can the video input signal be mixed with information by alphablending?

Yes, for example it is possible to put text or graphics on the C-layer alphablended on top of the video (on W-layer).

There will be a I2C interface on the final version of Scarlet. On which pins this interface will be located ?

The pins of Rose and Scarlet no. 184 and 185 are for I2C-IF
For details, see the I2C description of Scarlet !

Scarlet requires 14,32MHz (4* NTSC) input clock. Is it possible to use another crystal (e.g.14,25MHz) ? What is the allowed range of deviation (PLL) ?

The 14.25MHz as input clock is OK.
The allowed range of output frequency of PLL is around 195..202kHz.

What is the weight (in grams) of the final Scarlet chip (mass production version) ?

The typical weight of HQFP208 package is 5.17g.
Errors of plus or minus several percent will arise.

Using SH-3 @ 66 Mhz together with Scarlet :

The "XRDY delay time" is specified with t(RDYD)=7ns (max). In the Hitachi SH3-spec there is a value given for "Wait setup time" = 12ns (min) @ 66MHz operation frequency. Under these worst case conditions, the wait line could eventually cause problems. Did your customers had problems with that ? Do you have any recommendations ?

We've assumed the max. frequency of SH3 bus-clock as 50MHz.
If customer use higher frequency, they need to set the software wait to 3 cycle. We are now checking the behavior of this setting by logic simulation.

Is the load capacitance specified (C=16pF) valid for all ports of Scarlet ?

Yes, all the input load is same.

Power consumption figures and temperature of Scarlet :

Testcase: running 3D graphics demo for 10 minutes :

1. DAC Power down mode off (default)

   1-1. Measurements

   The Temperature of package : 47 degree
   The Temperature of room(Ta): 25 degree
   The current consumption : 630mA @VDDI-pin(2.5V)
   6mA @VCC-pin(2.5V)
   25mA @VDDE-pin(3.3V)

   1-2. Estimates

   The power consumption : 1.672W
   A rise rate of package : 16 degree/W
   The temperature of package : 25(Ta) + 1.672*16 = 51.752degree
   85(Ta) + 1.585*16 = 111.752degree

2. DAC Power down mode on

   2-1. Measurements

   The temperature of package : 47 degree
   The Temperature of room(Ta): 25 degree

The current consumption	:	595mA @VDDI-pin(2.5V) 6mA @VCC-pin(2.5V) 25mA @VDDE-pin(3.3V)

2-2. Estimates

The power consumption	:	1.585W
A rise rate of package	:	16 degree/W
The temperature of package	:	25(Ta) + 1.585*16 = 50.36 degree 85(Ta) + 1.585*16 = 110.36 degree

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DAC power down mode :

If only the digital video interface is used for a digital display, is it possible for power consumption reduction to save the resistors at Vref-, AOUTR/B/G-, ACOMPB- and VRO-pin and leave them open or connect them to GND or Vcc (2.5V or 3.3V?) directly?

The DAC can be set in an undocumented "power down mode".
To active this mode, write "0x00000001" to the register mapped at address "HostBase+0038h".
In this mode, all analog pins can be connected to GND. Those pins are :
AVD, AVS, AOUTR, AOUTG, AOUTB, VREF, ACOMPR, ACOMPG, ACOMPB, and VRO.
