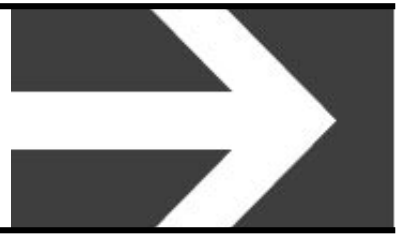
MICROCONTROLLER WORKSHOPS



Graphic Controller 1

PC graphics sets standards

PC graphics vs. Embedded graphics

Why not using PC graphics controllers ?

- **Long term availability**
- **Temperature range**
- **External video memory interface**
- **Bus interface** (AGP, PCI ...)
- **EMI behaviour**
- **High power-consumption**
- **APIs and S/W drivers**

Fujitsu Graphics Controller History

- 1996 : PC graphic project PinoLight (U.S.)
- Feedback from non-PC customers
- 1998 : Workgroup founded to define requirements
- Deliberate market study and user survey
- Reuse of graphics expertise build in the past arcade game/PC graphics activities
- 1999 : First sample of Cremson available

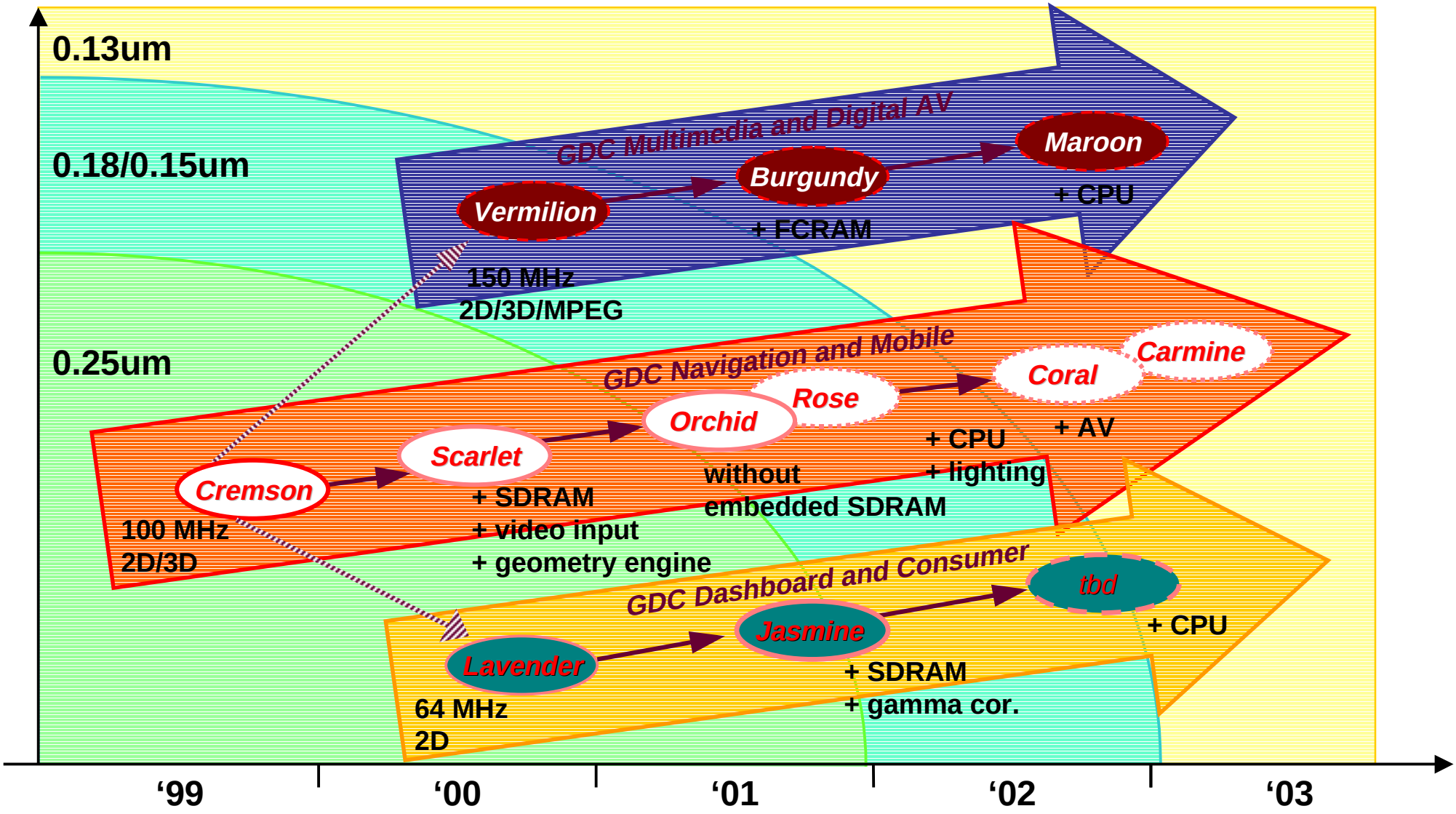
Cremson Graphics Controller Family

Convergent Rendering Engine Ministering Smart Operating Nucleus

- **Dedicated graphic display controllers for navigation systems / automotive embedded systems**
- **Fullfills the “Non-PC-markets” requirements**

- **Cremson was first member of GDC device family**
- **3 Graphic family lines for different requirements**

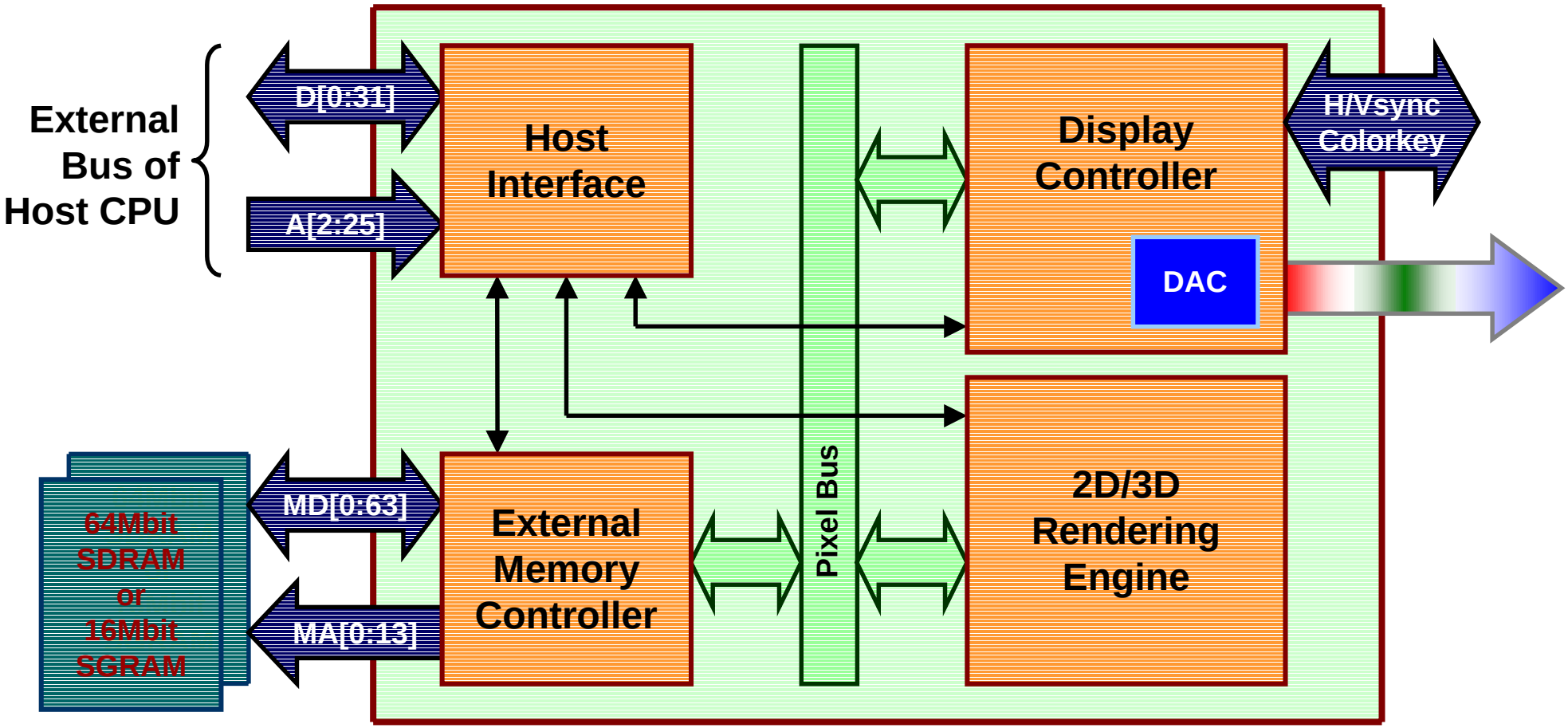
Roadmap


0.13um
0.18/0.15um
0.25um
GDC Multimedia and Digital AV
Vermilion
Burgundy
Maroon
+ CPU
+ FCRAM
150 MHz
2D/3D/MPEG
GDC Navigation and Mobile
Cremson
Scarlet
Orchid
Rose
Coral
Carmine
+ CPU
+ AV
+ lighting
without
embedded SDRAM
+ SDRAM
+ video input
+ geometry engine
100 MHz
2D/3D
GDC Dashboard and Consumer
Lavender
Jasmine
tbd
+ CPU
+ SDRAM
+ gamma cor.
64 MHz
2D
'99
'00
'01
'02
'03

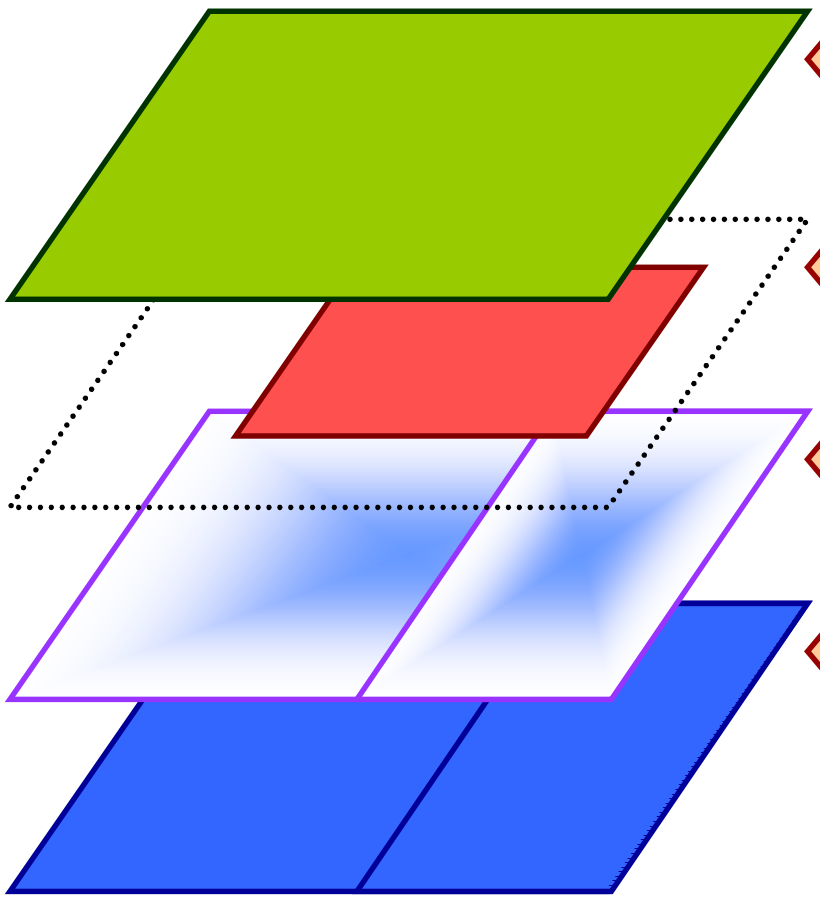
Cremson MB86290A

- 0.25 µm Technology / 2.5V (int), 3.3V (ext)
- Internal core operation frequency : 100MHz
- Display base clock : 200.45.. MHz
- Support up to 1024x768 resolution
- 4 display-layers (6 planes)
- 8 bit/pixel or 16bit/pixel color depth
- Contain 2D/3D graphics accelerators
- To be directly hooked to de-facto CPUs (Fujitsu FR, Hitachi SH3/SH4, NEC V83X)
- HQFP-240 package / - 40 .. +85 degC

Cremson Block diagram



Display layer structure



C (Console) layer
- 8, 16bit/pixel
- Applied to show switches and panel displays

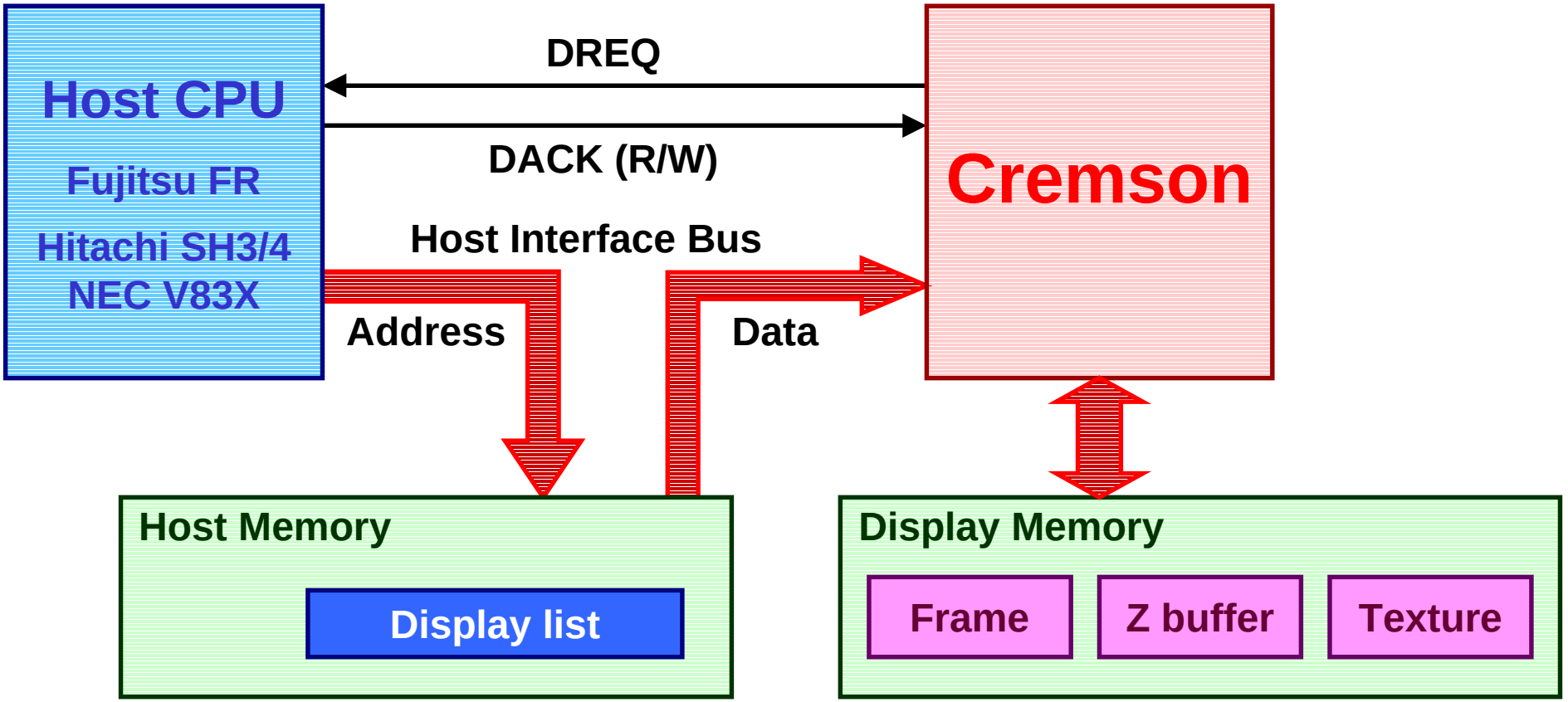
W (Window) layer
- 16bit/pixel
- Applied to overlay graphics or input video image *

M (Middle) layer
- 8, 16bit/pixel
- Supplement for Base, can be divided into two zones

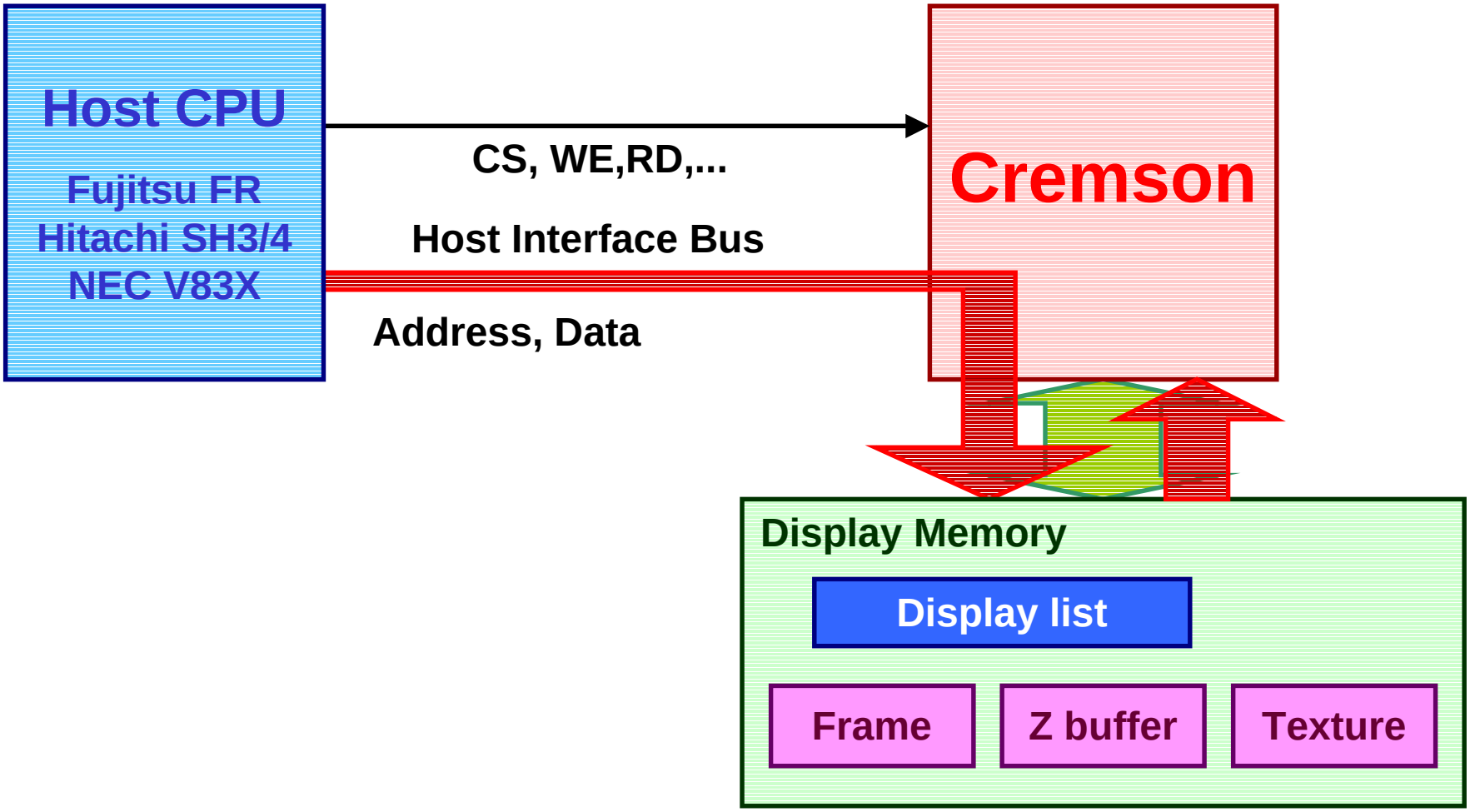
B (Base) layer
- 8, 16bit/pixel
- Fundamental map display layer can be divided into two zones

*To be supported by 2nd generation product Rose or Scarlet

Combination with host CPU



Combination with host CPU (2)

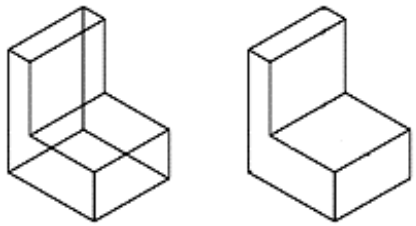


Rendering engine

- **Rendering engine can be initialized to various primitives=drawing functions**
- **2D primitives**

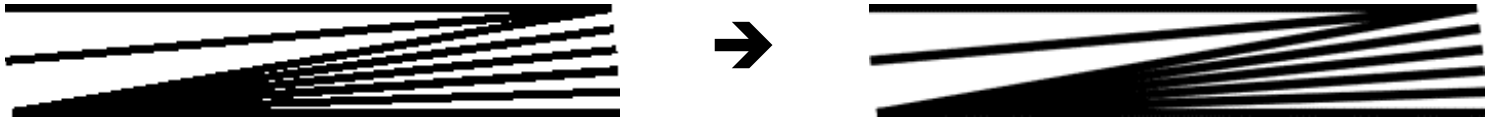
  Point, Line, Polyline, Triangle, Polygon, Fast2DLine, Fast2DTriangle, …
  Additional parameters (colors, line width, etc) set independently
  All vertexes will be used for the same primitive
- **Clipping areas can be defined for 2D operations**
- **3D primitives**

  Point, Line, Triangle, Polygon, ...
- **Hidden 3D-line management**

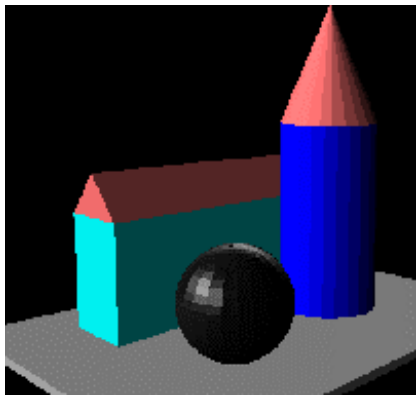


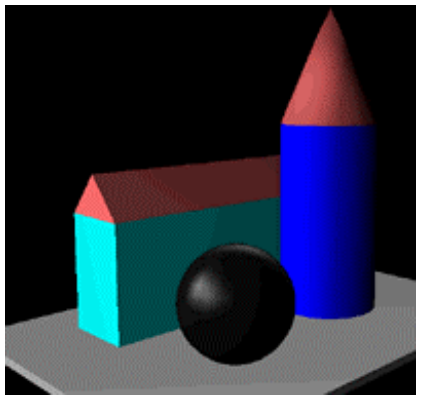
Special functions

- Hardware Anti-Aliasing



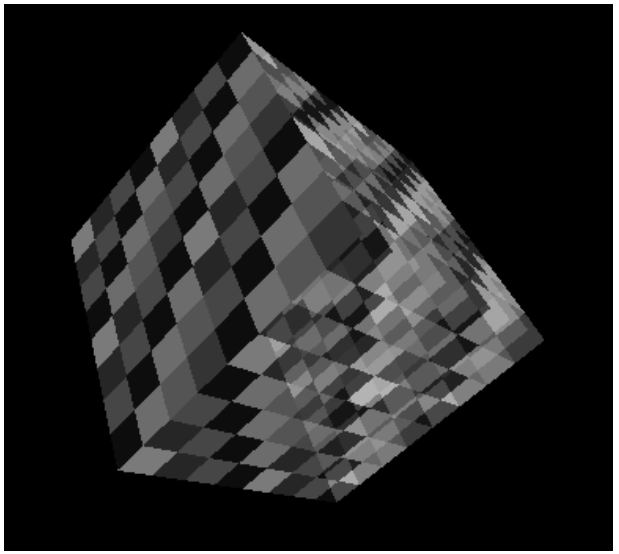
- Alpha-Blending
- 2 Hardware-Cursors
- Chroma-Key
- Flat-Shading and Gouraud-Shading





Special functions

- **Double-buffer management**
- **Line patterns**
- **Texture mapping**
  - using internal texture buffer (8kByte)
  - up to 256x256 pixels texture size
  - texture wrapping (out of range operation)
  - point or bi-linear filtering
  - perspective correction
  - texture blending
- **Hidden surface management**
- **Bitpattern draw**
- **Layer scrolling**



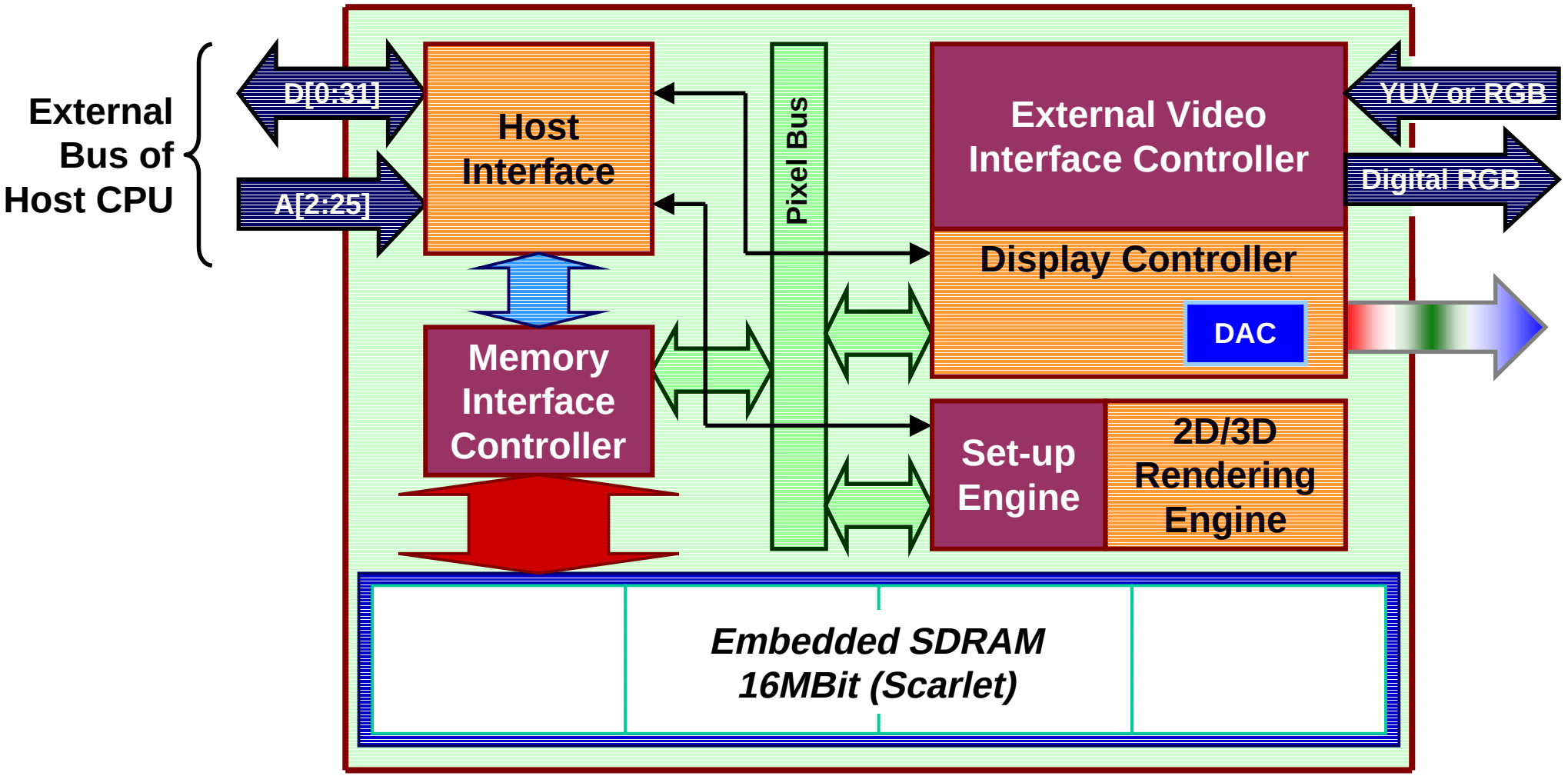
Comparison

		Fujitsu *Cremson*	Hitachi Q2/Q2i/Q2SD	NEC uPD72254Y
Operation frequency		Max. 100MHz	33MHz (SD 66MHz)	Max. 66MHz
Dot clock		Max. 66MHz	Operation frequency / 2	Unknown
Display	Resolution	Max. 1024 x 768	320 x 240	Max. 800 x 600
	Color	8bit pallet : 256/16M 64K	8bit pallet : 256/16M 64K	8bit pallet : 256/16M 64K
	Overlay	4 layers, 6 planes	2 layers	5 layers
	Hardware cursor	64 x 64 x 2 (5bit/pix)	No	Unknown
2D rendering	Line Draw	5.0Mline/s (10pix)	480Kline/s (10pix)	2.0Mline/sec (Unknown)
	Polygon Fill	500kp/s (25 x 20 triangle)	23kp/s (25 x 20 rectangle)	120kp/s (Unknown)
	Random shape	Yes	No	No
	Antialias	Yes	No	No
	Bit Blt	Yes	No	Yes
3D rendering		Yes	No	Z-check, Gouraud only
Host I/F	Applicable CPU	FR, SH3/4, V83X	SH1 to 3 (SD:SH3/4)	SH4 MPX mode only ?
	Data bus	32bit	16bit	32bit (A/D Multiplex)
Memory I/F	Address/Data	11bit / 32, 64bit	12bit / 16bit	11bit / 32bit
	Applicable memory devices	16Mbit SGRAM 1-2 64Mbit SDRAM 1-2	EDO (SD for Q2SD) 4Mbit/16Mbit 1 - 2	8Mbit SGRAM 1 64Mbit SDRAM 2
Video I/F	DAC	Mount (up to 110MHz)	Not mount	Not mount
	Video input	Support by 2nd generation	No	Yes

Scarlet MB86291

- **Upward compatible to Cremson**
  - All Cremson API commands can be used without modification
- **16MBit (2MByte) embedded SDRAM to deliver x2 band width**
- **Contain full 3D graphics geometry processor**
  - Support all geometry calculations
    Transform, Clip, Setup, …
  - Deliver 1Mpolygon/sec performance
- **Digital video input/output function**
  - Input video format : ITU-RBT656
  - Digital output : RGB (8bit/color parallel)
- **Package : HQFP208 / -40…+85 degC**

Scarlet Blockdiagram



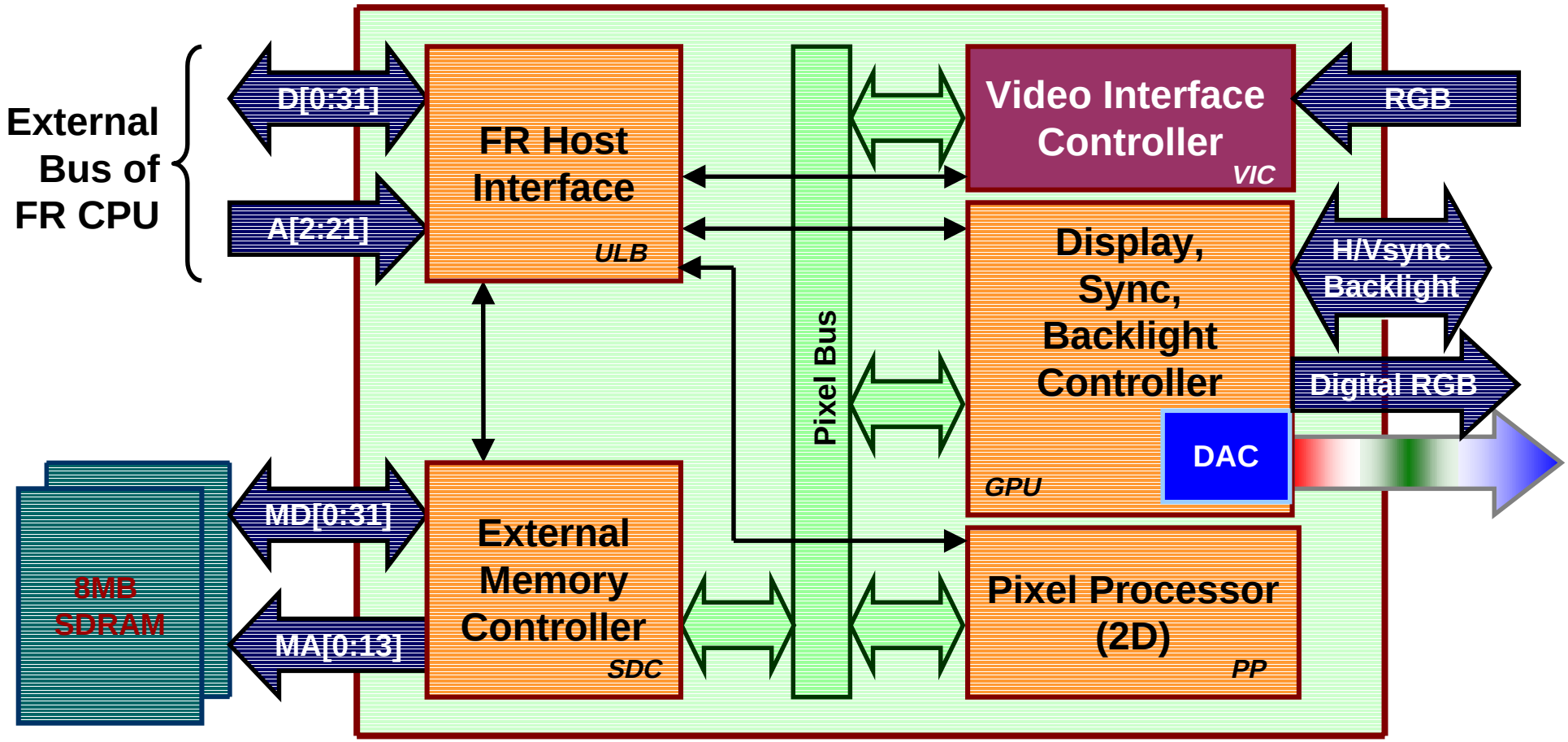
Preview : Orchid

- Upward compatible to Scarlet
- External SDRAM and FCRAM interface for up to 32MByte external memory
- Contains the same video input unit
- Contains the same geometry processor
- Digital output : RGB (8bit/color parallel) only (no RGB Analog output)
- Package : HQFP256 / -40…+85 degC

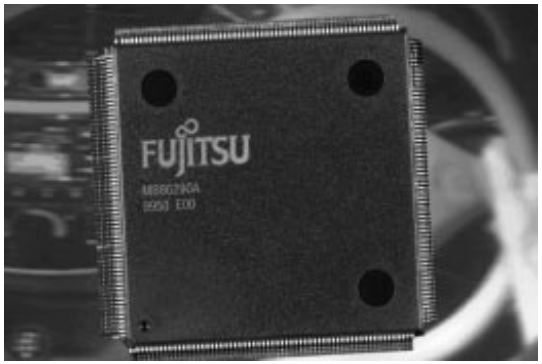
Lavender MB87J2120

- 0.25 µm Technology / 64MHz operation freq
- 4 display-layers (out of 16 logical layers)
- Contain 2D graphics accelerators
- Decompression of bitmaps
- Video input (RGB555 or RGB888 format)
- CPU interface for Fujitsu FR (e.g. MB91F361)
- 32-Bit external SDRAM interface (8MByte)
- Flexible display support including bitstream formatter and backlight control
- BGA256 package / - 40 .. +85 degC

Lavender Block diagram

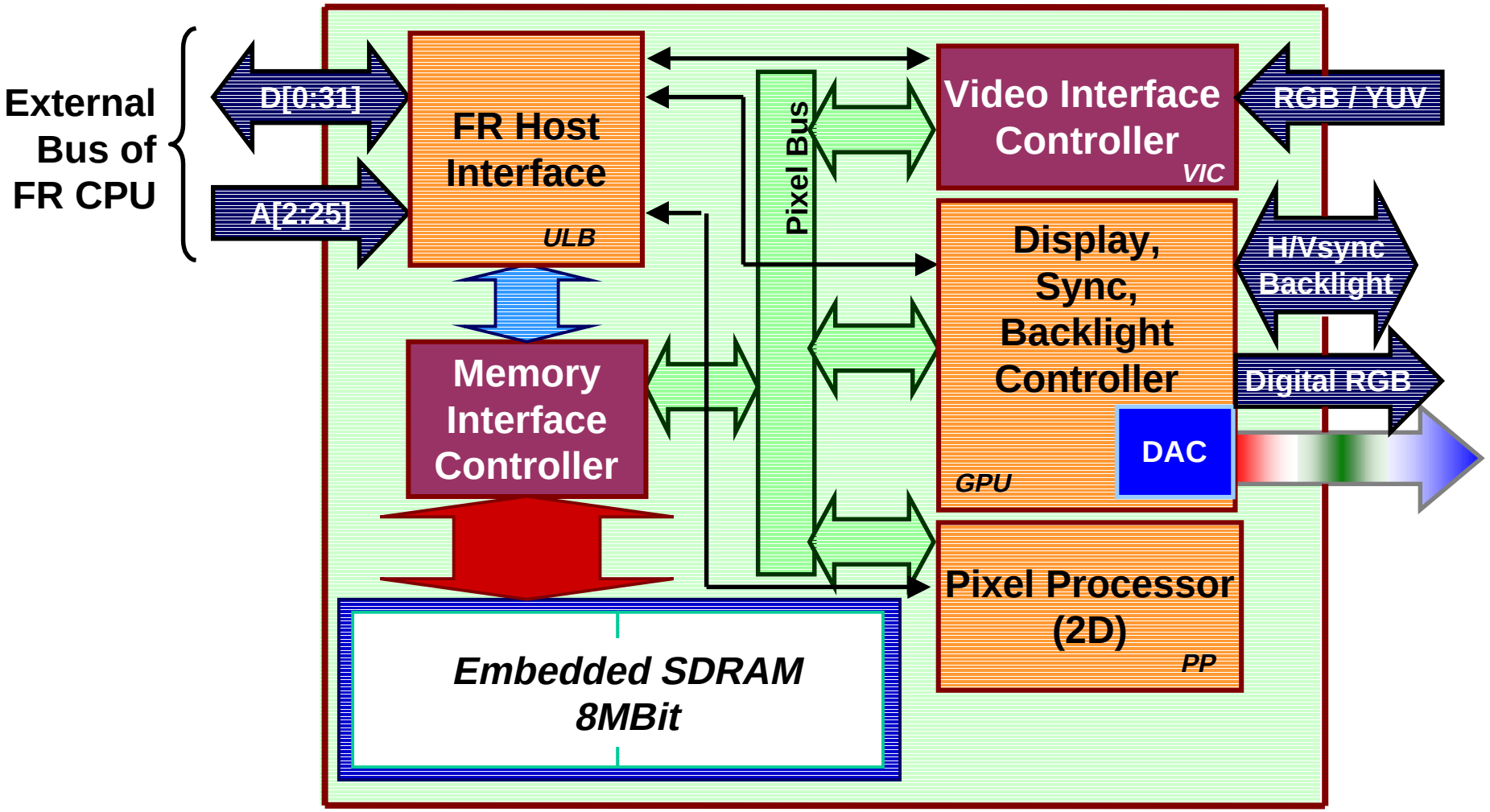


Jasmine MB87P2020



- 0.25 µm Technology / 64MHz operation freq
- Full compatible to Lavender (same layer concept and pixel engine)
- 8MBit (1MByte) Embedded SDRAM
- Enhanced Video input (YUV formats supported)
- Gamma correction function
- CPU interface for Fujitsu FR (e.g. MB91F361)
- Flexible display support including bitstream formatter and backlight control
- QFP208 package / - 40 .. +85 degC

Jasmine Block diagram



Device Family Car Navigation

THE POSSIBILITIES ARE INFINITE FUJITSU

	Cremson	Scarlet	Orchid	Coral
Technology	0.25µm (CS71E)	0.25µm (CS70DLS)	0.25µm (CS71E)	0.18µm (CS80DL)
Frequency	100MHz	100MHz	100MHz	133MHz
Target performance	800Mpix/s 500k polygon/s	1.6Gpix/s 1M polygon/s	1.6Gpix/s 1M polygon/s	3.2Gpix/s 4.5M polygon/s
Main features	- Full 2D/3D graphics engine - Line antialias - Frame alpha blending - Flat/gouraud shading - Bilinear txture mapping - 16bit Z buffering - 2x cursors - 4 layers (6 segments) overlay	- Upward compatible to Cremson - Embedded SDRAM Rose:32Mbit Scarlet:16Mbit - Full geometry processor - Video capture - Digital V out	- All features of Scarlet, but without embedded SDRAM - Binary compatible to Cremson/Scarlet	- Combination of Rose core and FR CPU - Embedded I/O control functions - All binary compatible to Rose/Scarlet and Orchid - audio/video hardware assistance
Schedule	ES: Sep ‘99 CS: Jan ‘00 MP: Mar ‘00	ES: Oct ‘00 CS: Jan ‘01 MP: Mar ‘01	ES: May ‘01 CS: Oct ‘01 MP: Jan ‘02	ES: May ‘02 CS: Oct ‘02 MP: Jan ‘03

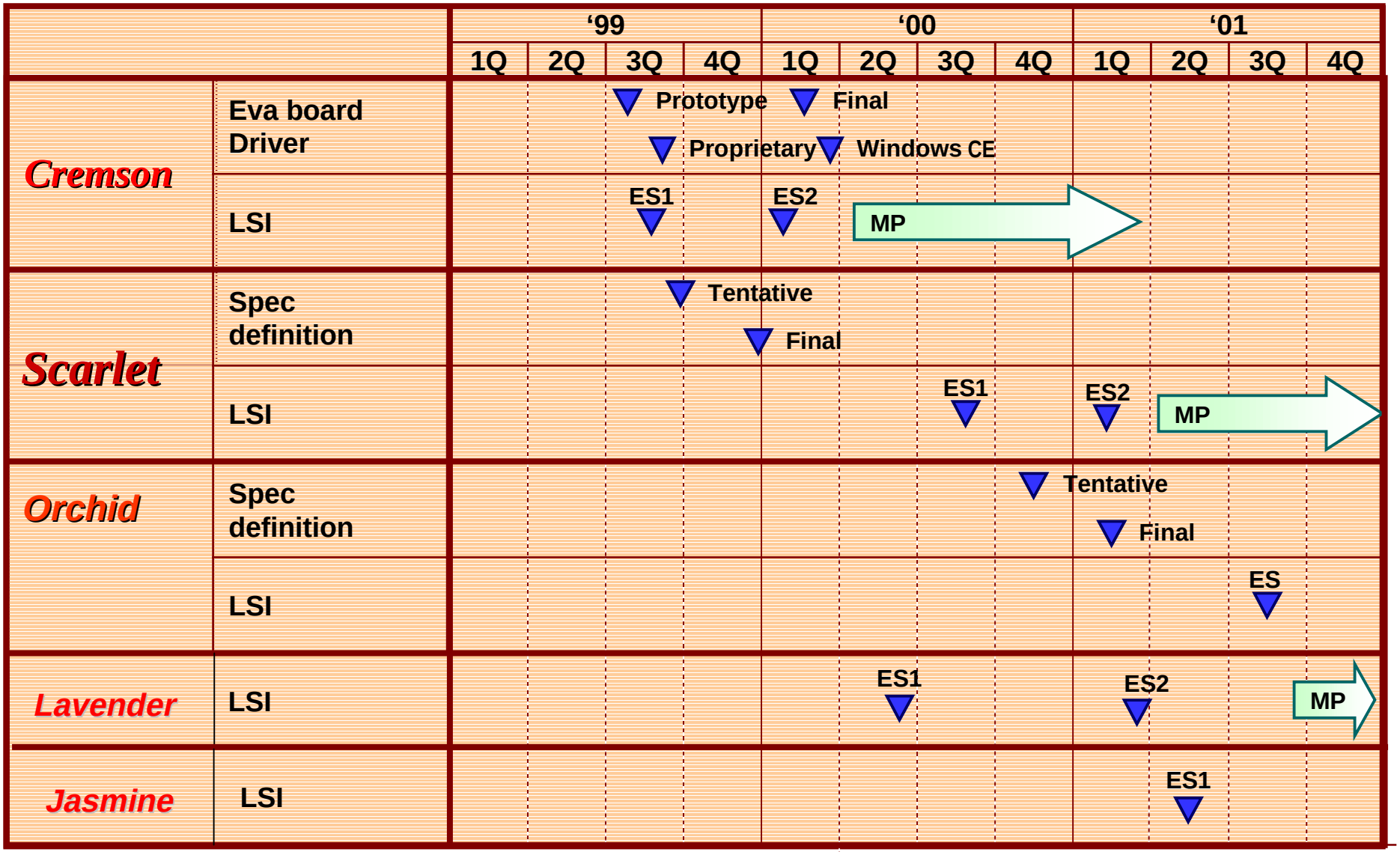
Device Family Media

	Vermilion	Burgundy	Maroon
Technology	0.18µm (CS80A)	0.13µm (CS90DL)	0.13µm (CS90DL)
Frequency	81MHz	108MHz	135MHz
Target power dissipation	Max 0.4W @81MHz (all functions active)	Max 0.4W @108MHz (all functions active)	Max 0.6W @135MHz (all functions active)
Main feature	2D Graphics - Video input capture and scaling control - Over sampling and full frame convolution - Fast Blt - Anti aliasing Video decoder - MPEG4? or Existing MPEG2 technology Audio - Linear PCM or MP3	- Upward compatible to Vermilion - On chip embedded FCRAM for graphics frame memory and video and audio stream memory - Host interface optimized to new FR-V CPU which will be integrated together with W-CDMA base band logic and Bluetooth controller	- A single chip integration of entire system components - Upward compatible to Burgundy - Combine FR-V core, access control I/O resources and backend data flow control together
Schedule	ES: Jul '01 CS: Dec '01 MP: Apr '02	ES: Jul '02 CS: Dec '02 MP: Apr '03	ES: Jul '03 CS: Dec '03 MP: Apr '04

Device Family Dashboard

	Lavender	Jasmine	tbd
Technology	0.25µm (CS71E)	0.25µm (CS71E)	0.18µm (CS80DL)
Frequency	64MHz	64MHz	100MHz
Target performance	200Mpix/s	200 Mpix/s	? Mpix/s
Main features	- 2D graphics engine - flexible display interface - decompression of bitmaps - digital and analog video output - digital video input - 4 layers (16 segments) overlay	- Embedded SDRAM (8MBit) - Gamma correction function - Compatible to Lavender - multiple color tables - enhanced functions	- Combination of Lavender and FR CPU - Compatible to Lavender
Schedule	ES: July '00 MP: ?	ES: May '01 MP: ?	ES: CS: MP:

Development schedule



Graphics Driver Software

- **Proprietary display driver**
  - Dedicated driver program to maximize the hardware performance
  - Source code is licensed at certain license fee
  - Binary code is free of charge (Windows NT version is attached to the Cremson evaluation board)
- **Windows CE display driver**
  - Cooperative deal with Microsoft on SH4 platform
  - “GDI-sub” to activate Cremson’s hardware assist is completed
  - x10 performance is achieved by Cremson’s hardware assist
  - 3D driver function calls are under development