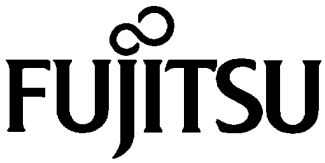
MB86291S <Scarlet>
I2C Interface Specification

Revision 1.01
April 8, 2001



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1 Overview

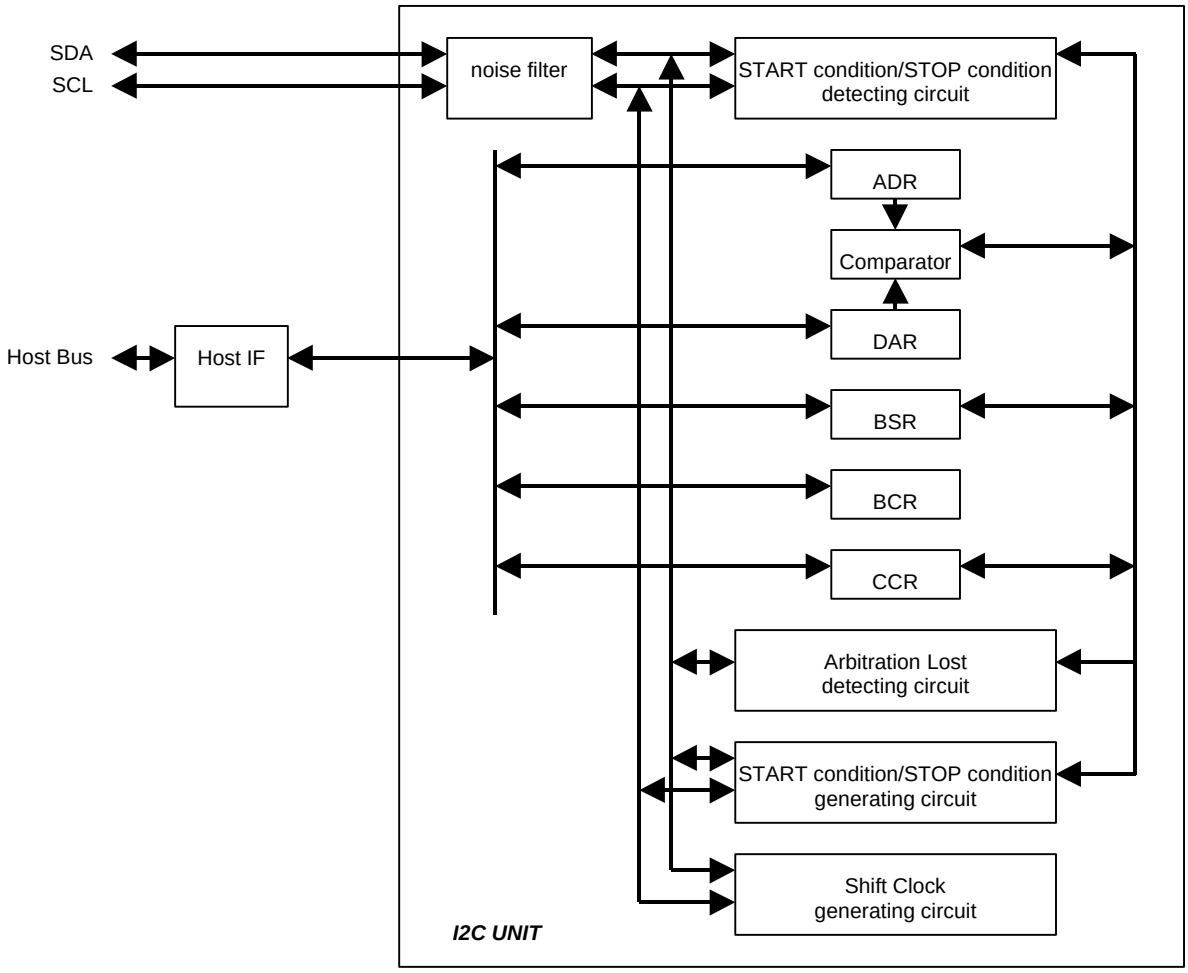
1.1 Features of I2C

- master transmission and reception
- slave transmission and reception
- arbitration
- clock synchronization
- detection of slave address
- detection of general call address
- detection of transfer direction
- repeated generation and detection of START condition
- detection of bus error
- correspondence to standard-mode (100kbit/s) / high-speed-mode (400kbit/s)

2 Block diagram

2.1 block diagram

The block diagram is shown below:



2.2 block function overview

- START condition / STOP condition detecting circuit
  This circuit performs detection of START condition and STOP condition from the state of SDA and SCL.

- START condition / STOP condition generating circuit
  This circuit performs generation of START condition and STOP condition by changing the state of SDA and SCL.

- Arbitration Lost detecting circuit
  This circuit compares the data output to SDA line with the data input into SDA line at the time of data transmission, and it checks whether these data is in agreement. When not in agreement, it generates arbitration lost.

- Shift Clock generating circuit
  This circuit performs generating timing count of the clock for serial data transfer, and output control of SCL clock by setup of a clock control register.

- Comparater
  Comparater compares whether the received address and the self-address appointed to be the address register is in agreement, and whether the received address is a global address.

- ADR
  ADR is the 7-bit register which appoints a slave address.

- DAR
  DAR is the 8-bit register used by serial data transfer.

- BSR
  BSR is the 8-bit register for the state of I2C bus etc. This register has following functions:
  - detection of repeated START condition
  - detection of arbitration lost
  - storage of acknowledge bit
  - data transfer direction
  - detection of addressing
  - detection of general call address
  - detection of the 1st byte

- BCR
  BCR is the 8-bit register which performs control and interruption of I2C bus. This register has following functions:
  - request / permission of interruption
  - generation of START condition
  - selection of master / slave
  - permission to generate acknowledge

- CCR
  CCR is the 7-bit register used by serial data transfer. This register has following functions:
  - permission of operation
  - setup of a serial clock frequency
  - selection of standard-mode / high-speed-mode

- noise filter
  This noise filter consists of a 3 step shift register. When all three value that carried out the continuation sampling of the SCL/SDA input signals is “1”, the filter output is “1”. Conversely when all three value is “0”, the filter output is “0”. To other samplings it holds the state before 1 clock.

3 Signals

table 3-1 ▪ external signal list

Name	I/O	Description	notes
SDA	I	Serial Data Line	
SCL	I/O	Serial Clock Line	
XINT	O	Interrupti request signal. When this signal is ”0”, it indicates an interruption request. SH3/4 asserts LOW-active and V832 asserts HI-active.	

Pinning outline on MB86291S :

Pin 99 : XINT
Pin 184: SDA
Pin 185: SCL
Pin 186: XI2CEN → **Pin 186 must be connected to GND to activate the I2C module !**

Input voltage level is 3.3V. Please be careful – do NOT connect to 5V !

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4 example application

4.1 connection diagram

The connection diagram is shown below.

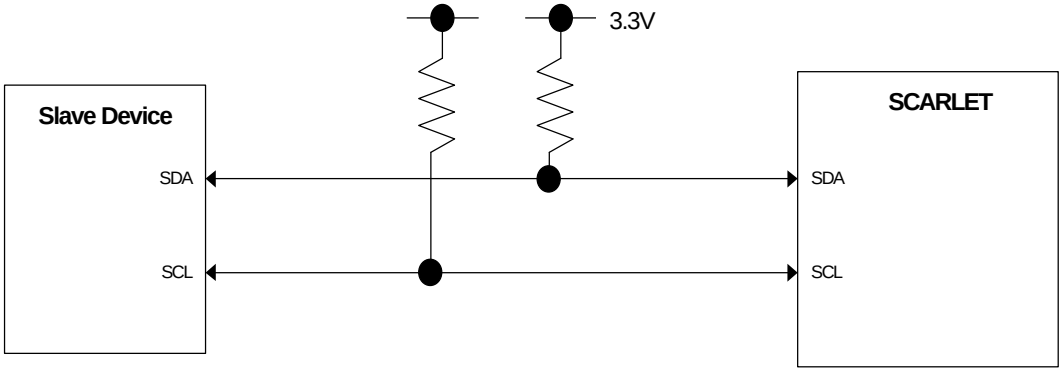


Fig. 4-1 ▪ connection diagram

5 Function overview

Two bi-directional buses, serial data line (SDA) and serial clock line (SCL), carry information at I2C-bus. Scarlet I2C interface has SDA input (SDAI) and SDA output (SDAO) for SDA and is connected to SDA line via open-drain I/O cell. And this interface also has SCL input (SCLI) and SCL output (SCLO) for SCL line and is connected to SCL line via open-drain I/O cell. The wired theory is used when the interface is connected to SDA line and SCL line.

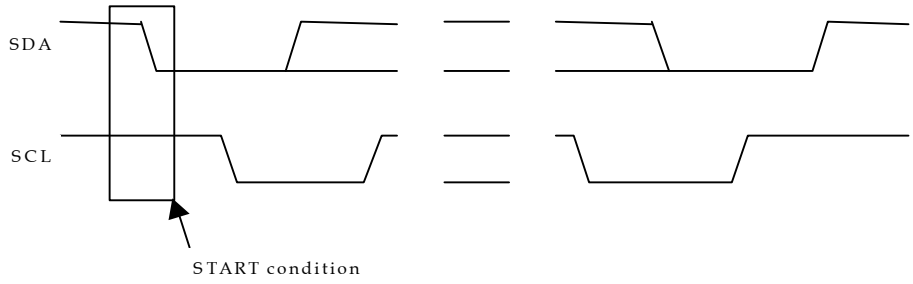
5.1 START condition

If “1” is written to MSS bit while the bus is free, this module will become a master mode and will generate START condition simultaneously. In a master mode, even if a bus is in a use state (BB=1), START condition can be generated again by writing “1” to SCC bit.

There are two conditions to generate START condition.

- “1” writing to MSS bit in the state where the bus is not used (MSS=0 & BB=0 & INT=0 & AL=0)
- “1” writing to SCC bit in the interruption state in a master mode (MSS=1 & BB=1 & INT=1 & AL=0)

If “1” writing is performed to MSS bit in an idol state, AL bit will be set to “1”. “1” writing to MSS bit other than the above is disregarded.



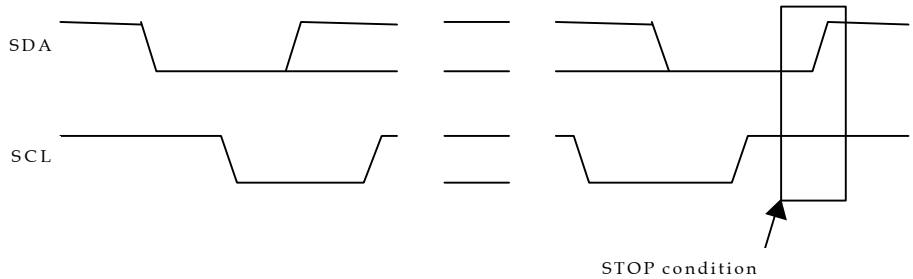
5.2 STOP condition

If “0” is written to MSS bit in a master mode (MSS=1), this module will generate STOP condition and will become a slave mode.

There is a condition to generate STOP condition.

- “0” writing to MSS bit in the interruption state in a master mode (MSS=1 & BB=1 & INT=1 & AL=0)

“0” writing to MSS bit other than the above is disregarded.



5.3 addressing

In a master mode, it is set to BB="1" and TRX="0" after generation of START condition, and the contents of DAR register are output from MSB. When this module receives acknowledge after transmission of address data, the bit-0 of transmitting data (bit-0 of DRA register after transmission) is reversed and it is stored in TRX bit.

- transfer format of slave address

A transfer format of slave address is shown below:

MSB							LSB	
A6	A5	A4	A3	A2	A1	A0	R/W	ACK
▪	slave address					▪		

- map of slave address

A map of slave address is shown below:

slave address	R/W	Description
▪ ▪ ▪ ▪ ▪ ▪ ▪	▪	General call address
▪ ▪ ▪ ▪ ▪ ▪ ▪	▪	START byte
▪ ▪ ▪ ▪ ▪ ▪ ▪	X	CBUS address
▪ ▪ ▪ ▪ ▪ ▪ ▪	X	Reserved
▪ ▪ ▪ ▪ ▪ ▪ ▪	X	Reserved
▪ ▪ ▪ ▪ ▪ XX	X	Reserved
▪ ▪ ▪ ▪ XXX ▪ ▪ ▪ ▪ XXX	X	Available slave address
▪ ▪ ▪ ▪ ▪ XX	X	10-bit slave addressing*1
▪ ▪ ▪ ▪ ▪ XX	X	Reserved

*1 This module does not support 10-bit slave address.

5.4 synchronization of SCL

When two or more I2C devices turn into a master device almost simultaneously and drive SCL line, each devices senses the state of SCL line and adjusts the drive timing of SCL line automatically in accordance with the timing of the latest device.

5.5 arbitration

When other masters have transmitted data simultaneously at the time of master transmission, arbitration takes places. When its own transmitting data is “1” and the data on SDA line is “0”, the master considers that the arbitration was lost and sets “1” to AL. And if the master is going to generate START condition while the bus is in use by other master, it will consider that arbitration was lost and will set “1” to AL.
When the START condition which other masters generated is detected by the time the master actually generated START condition, even when it checked the bus is in nonuse state and wrote in MSS=”1”, it considers that the arbitration was lost and sets “1” to AL.

When AL bit is set to “1”, a master will set MSS=”0” and TRX= “0” and it will be a slave receiving mode.
When the arbitration is lost (it has no royalty of a bus), a master stops a drive of SDA. However, a drive of SCL is not stopped until 1 byte transfer is completed and interruption is cleared.

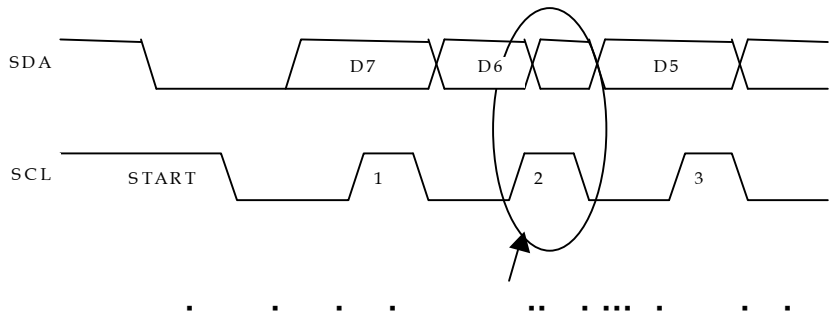
5.6 acknowledge

Acknowledge is transmitted from a reception side to a transmission side. At the time of data reception, acknowledge is stored in LRB bit by ACK bit.
When the acknowledge from a master reception side is not received at the time of slave transmission, it sets TRX=”0” and becomes slave receiving mode. Thereby, a master can generate STOP condition when a slave opens SCL.

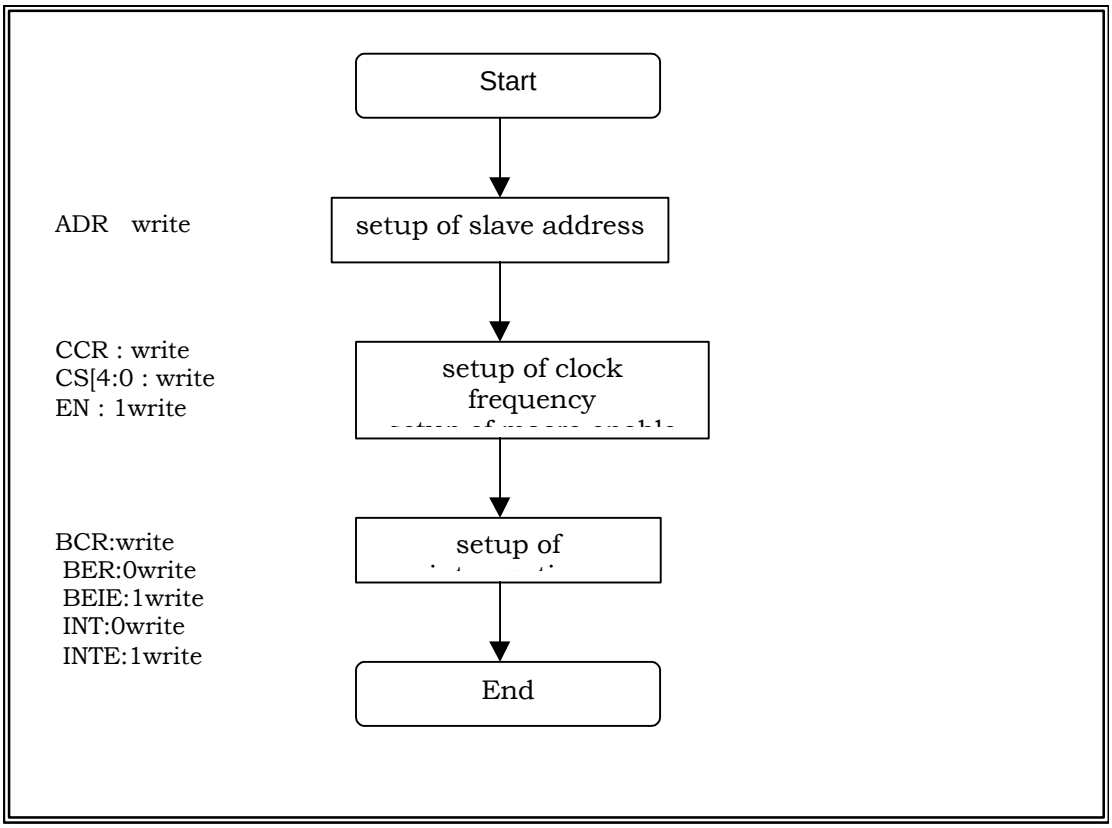
5.7 bus error

When the following conditions are satisfied, it is judged as a bus error, and this interface will be in a stop state.

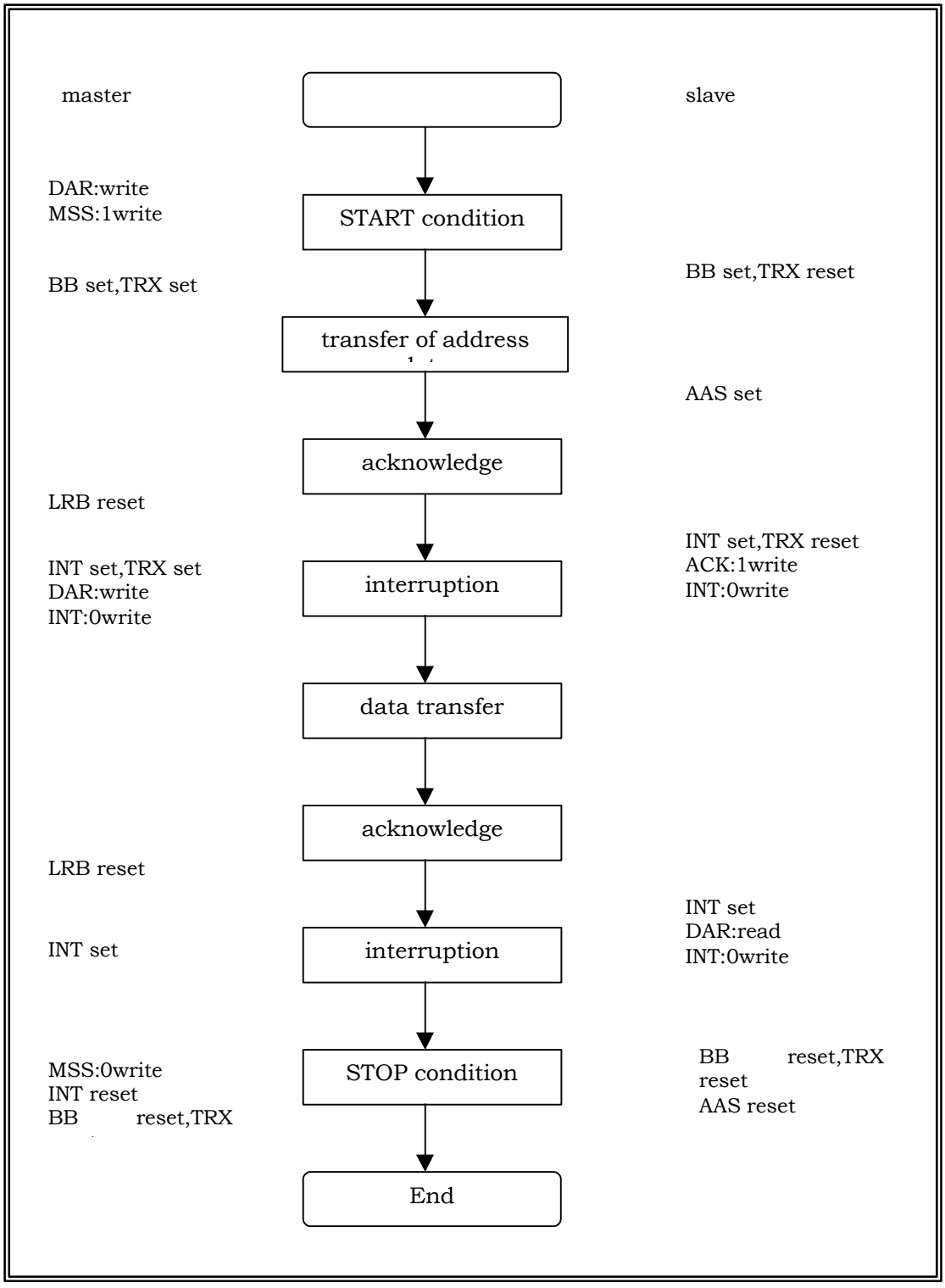
- detection of the basic regulation violation on I2C-bus under data transfer (including ACK bit)
- detection of STOP condition in a master mode
- detection of the basic regulation violation on I2C-bus at the time of bus idol



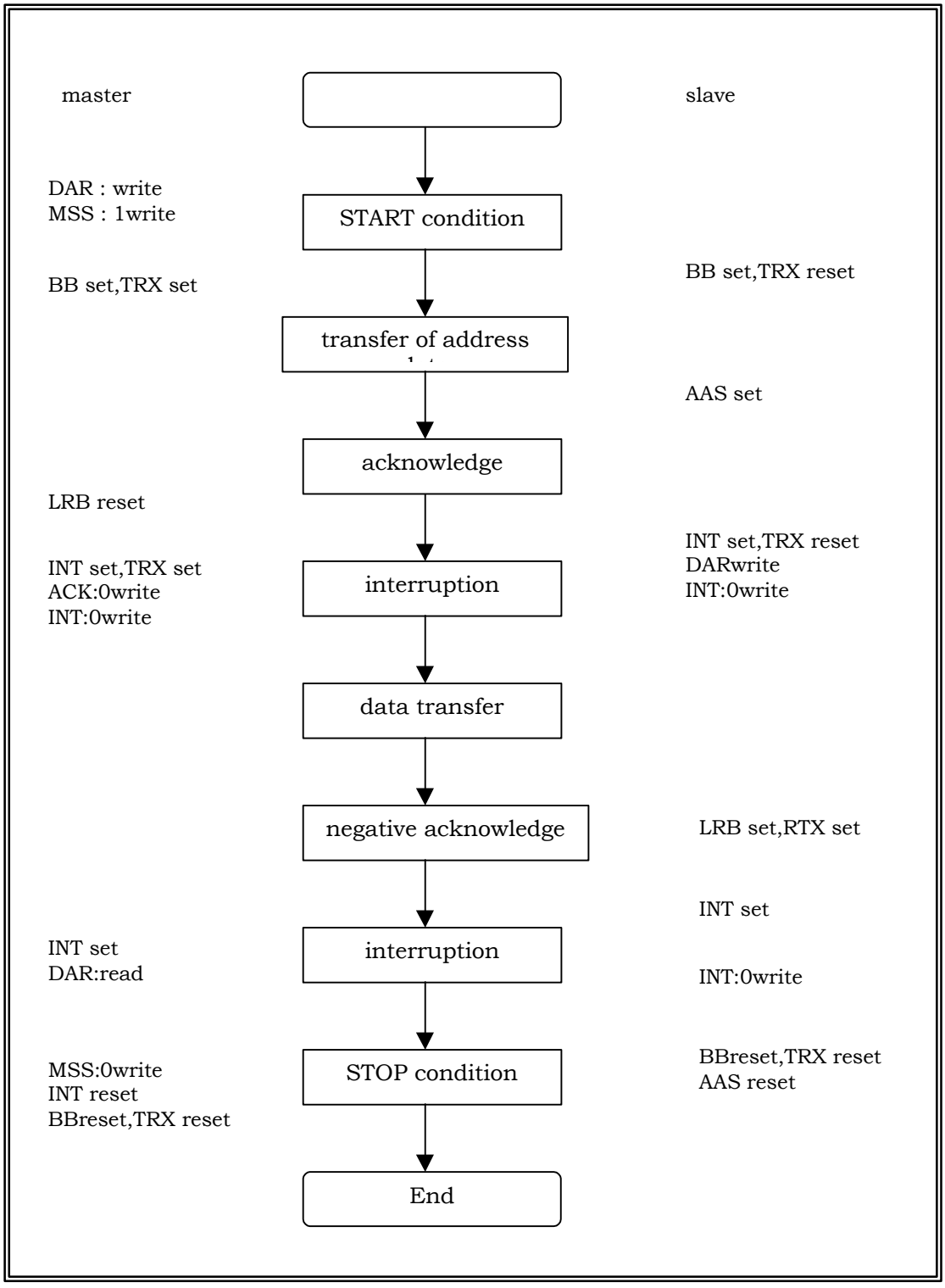
5.8 initialize



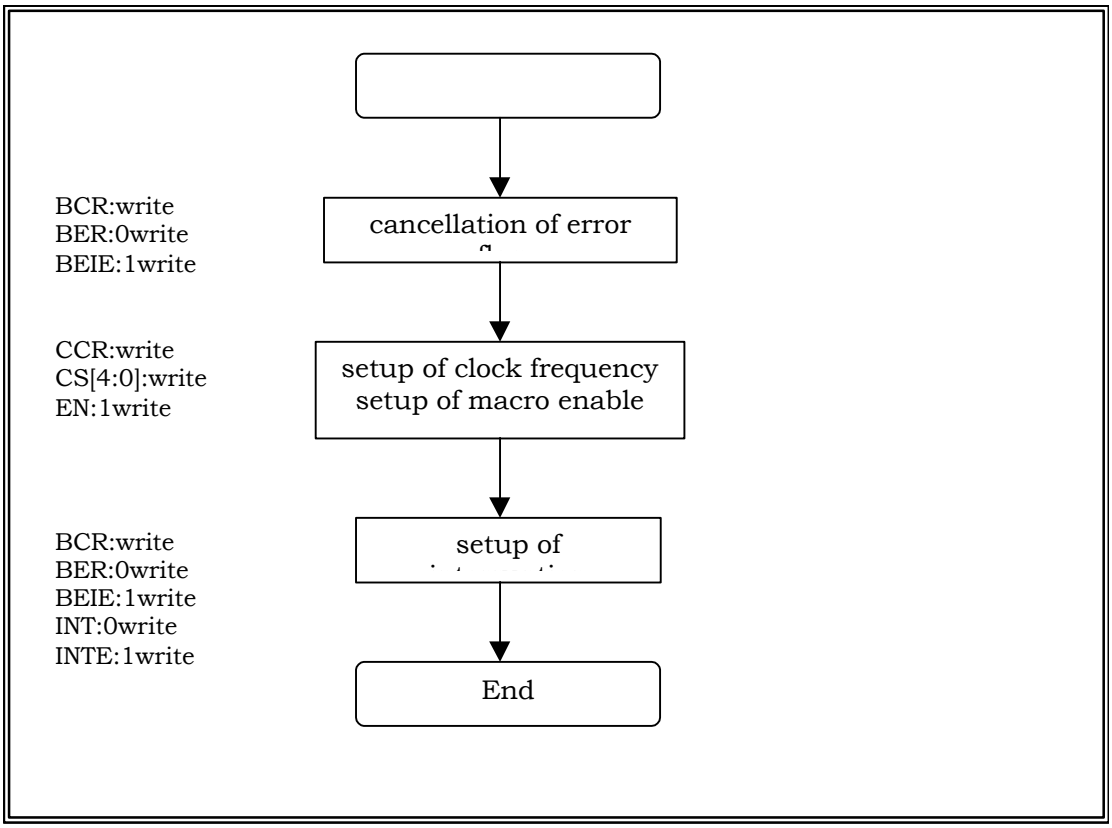
5.9 1-byte transfer from master to slave



5.10 1-byte transfer from slave to master



5.11 recovery from bus error



6 Registers

6.1 register map

I2C Interface offset address head = 1FCC000 (SH3・SH4), 0FCC000 (V83x,SPARClite)

byte address	data							
	31	24	23	16	15	8	7	0
000h	Reserved						BSR	
004h	Reserved						BCR	
008h	Reserved						CCR	
00Ch	Reserved						ADR	
010h	Reserved						DAR	
014h	Access prohibition							
018h	Access prohibition							
01Ch	Access prohibition							

6-1・register list

6.2 registers

BSR (Bus Status Register)

Register address	I2CbaseAddress + 000h							
Bit #	7	6	5	4	3	2	1	0
Bit field name	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT
・/・	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

All bits on this register are cleared while bit EN on CCR register is “0”.

Bit7 BB (Bus Busy)
Indicate state of I2C-bus
0・STOP condition was detected.
1・START condition (The bus is in use.) was detected.

Bit・ RSC (Repeated START Condition)
Indicate repeated START condition
This bit is cleared by writing “0” to INT bit, the case of not addressed in a slave mode, the detection of START condition under bus stop, and the detection of STOP condition.
0・Repeated START condition was not detected.
1・START condition was detected again while the bus was in use.

Bit5 AL(Arbitration Lost)
Detect Arbitration lost
This bit is cleared by writing “0” to INT bit.
0・Arbitration lost was not detected.
1・Arbitration occurred during master transmission, or “1” writing was performed to MSS bit while other systems were using the bus.

Bit4 LRB (Last Received Bit)
Store Acknowledge
This bit is cleared by detection of START condition or STOP condition.

Bit3 TRX (Transmit / Receive)
Indicate data receipt and data transmission.
0・receipt
1・transmission

Bit2 AAS (Address As Slave)
Detect addressing
This bit is cleared by detection of START condition or STOP condition.
0・Addressing was not performed in a slave mode.
1・Addressing was performed in a slave mode.

Bit1 GCA (General Call Address)
Detect general call address (00h)
This bit is cleared by detection of START condition or STOP condition.
0・General call address was not received in a slave mode.
1・General call address wad received in a slave mode.

Bit0 FBT (First Byte Transfer)
Detect the 1st byte
Even if this bit is set to “1” by detection of START condition, it is cleared by writing “0” on INT bit or by not being addressed in a slave mode.
0・Received data is not the 1st byte.
1・Received data is the 1st byte (address data).

BCR (Bus Control Register)

Register address	I2CbaseAddress + 0004h							
Bit #	7	6	5	4	3	2	1	0
Bit field name	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
▪ / ▪	R/W0	R/W	R0/W1	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit7 BER (Bus Error)

Flag bit for request of bus error interruption
When this bit is set, EN bit on CCR register will be cleared, this module will be in a stop state and data transfer will be discontinued.
write case
0 ▪ A request of buss error interruption is cleared.
1 ▪ Don't care.
read case
0 ▪ A bus error was not detected.
1 ▪ Undefined START condition or STOP condition was detected while data transfer.

Bit6 BEIE (Bus Error Interruption Enable)

Permit bus error interruption
When both this bit and BER bit are "1", the interruption is generated.
0 ▪ Prohibition of bus error interruption
1 ▪ Permission of bus error interruption

Bit5 SCC (Start Condition Continue)

Generate START condition
write case
0 ▪ Don't care.
1 ▪ START condition is generated again at the time of master transmission.

Bit4 MSS (Master Slave Select)

Select master / slave mode
When arbitration lost is generated in master transmission, this bit is cleared and this module becomes a slave mode.
0 ▪ This module becomes a slave mode after generating STOP condition and completing transfer.
1 ▪ This module becomes a master mode, generates START condition and starts transfer.

Bit3 ACK (ACKnowledge)

Permit generation of acknowledge at the time of data reception
This bit becomes invalid at the time of address data reception in a slave mode.
0 ▪ Acknowledge is not generated.
1 ▪ Acknowledge is generated.

Bit2 GCAA ▪ General Call Address Acknowledge ▪

Permit generation of acknowledge at the time of general call address reception
0 ▪ Acknowledge is not generated.
1 ▪ Acknowledge is generated.

Bit1 INTE (INTerrupt Enable)

Permit interruption
When this bit is "1" interruption is generated if INT bit is "1".
0 ▪ Prohibition of interrupt
1 ▪ Permission of interrupt

Bit0 INT (INTrrupt)

Flag bit for request of interruption for transfer end
When this bit is "1" SCL line is maintained at "L" level. If this bit is cleared by being written "0", SCL line is released and the following byte transfer is started. Moreover, it is reset to "0" by generating of START condition or STOP condition at the time of a master.
write case
0 ▪ The flag is cleared.
1 ▪ Don't care.
read case
0 ▪ The transfer is not ended.
1 ▪ It is set when 1 byte transfer including the acknowledge bit is completed and it corresponds to the following conditions.

- It is a bus master.
- It is an addressed slave.

- It was going to generate START condition while other systems by which arbitration lost happened used the bus.

competition of SCC, MSS and INT bit

Competition of the following byte transfer, generation of START condition and generation of STOP condition happens by the simultaneous writing of SCC, MSS and INT bit. The priority at this case is as follows.

1) the following byte transfer and generation of STOP condition
   If “0” is written to INT bit and “0” is written to MSS bit, priority will be given to “0” writing to MSS bit and STOP condition will be generated.

2) the following byte transfer and generation of START condition
   If “0” is written to INT bit and “1” is written to SCC bit, priority will be given to “1” writing to SCC bit and START condition will be generated.

3) generation of START condition and STOP condition
   The simultaneous writing of “1” to SCC bit and “0” to MSS bit is prohibition.

CCR (Clock Control Register)

Register address	I2CbaseAddress + 0008h							
Bit #	7	6	5	4	3	2	1	0
Bit field name	-	HSM	EN	CS4	CS3	CS2	CS1	CS0
- / -	R1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	-	-	-	-	-

Bit7 nonuse
"1" is always read at read.

Bit6 HSM (High Speed Mode)
Select standard-mode / high-speed-mode
0 - Standard-mode
1 - High-speed-mode

Bit5 EN (Enable)
Permission of operation
When this bit is "0", each bit of BSR and BCR register (except BER and BEIE bit) is cleared. This bit is cleared when BER bit is set.
0 - Prohibition of operation
1 - Permission of operation

Bit4 CS4 - 0 (Clock Period Select4 - 0)

Set up the frequency of a serial transfer clock
Frequency fscl of a serial transfer clock is shown as the following formula. Please set up fscl not to exceed the value shown below at the time of master operation.
- standard-mode - 100KHz
- high-speed-mode - 400KHz

standard-mode

$$fscl = \frac{f}{(2 \quad m)+2}$$

high-speed-mode

$$fscl = \frac{f}{int(1.5 \quad m)+2}$$

f:I2C system clock = 16.6MHz

Note :
+2 cycles are minimum overhead to confirm that the output level of SCL terminal changed. When the delay of the positive edge of SCL terminal is large or when the clock is extended by the slave device, it becomes larger than this value.

The value of m becomes like the following page to the value of CS 4-0.

CS4	CS3	CS2	CS1	CS0	M	
					standard	high-speed
0	0	0	0	0	65	inhibited
0	0	0	0	1	66	inhibited
0	0	0	1	0	67	inhibited
0	0	0	1	1	68	inhibited
0	0	1	0	0	69	inhibited
0	0	1	0	1	70	inhibited
0	0	1	1	0	71	inhibited
0	0	1	1	1	72	inhibited
0	1	0	0	0	73	9
0	1	0	0	1	74	10
0	1	0	1	0	75	11
0	1	0	1	1	76	12
0	1	1	0	0	77	13
0	1	1	0	1	78	14
0	1	1	1	0	79	15
0	1	1	1	1	80	16
1	0	0	0	0	81	17
1	0	0	0	1	82	18
1	0	0	1	0	83	19
1	0	0	1	1	84	20
1	0	1	0	0	85	21
1	0	1	0	1	86	22
1	0	1	1	0	87	23
1	0	1	1	1	88	24
1	1	0	0	0	89	25
1	1	0	0	1	90	26
1	1	0	1	0	91	27
1	1	0	1	1	92	28
1	1	1	0	0	93	29
1	1	1	0	1	94	30
1	1	1	1	0	95	31
1	1	1	1	1	96	32

Address ▪ Register(ADR)

Register address	I2CbaseAddress + 000Ch							
Bit #	7	6	5	4	3	2	1	0
Bit field name	▪	A6	A5	A4	A3	A2	A1	A0
▪ / ▪	R1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	▪	▪	▪	▪	▪	▪	▪

Bit7 nonuse
"1" is always read at read.

Bit6 ▪ 0 A6 ▪ 0 (Address6 ▪ 0)
Store slave address
In a slave mode it is compared with DAR register after address data reception, and when in agreement, acknowledge is transmitted to a master.

Data Register ▪ DAR ▪

Register address	I2CbaseAddress + 0010h							
▪ ▪ ▪ ▪ ▪	7	6	5	4	3	2	1	0
▪ ▪ ▪ ▪ ▪ ▪ ▪ ▪ ▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪
▪ ▪ ▪	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
▪ ▪ ▪	▪	▪	▪	▪	▪	▪	▪	▪

Bit7 ▪ 0 D7 ▪ 0 (Data7 ▪ 0)
Store serial data
This is a data register for serial data transfer. The data is transferred from MSB. At the time of data reception (TRX=0) the data output is set to "1". The writing side of this register is a double buffer. When the bus is in use (BB=1), the write data is loaded to the register for serial transfer for every transfer. At the time of read-out, the receiving data is effective only when INT bit is set because the register for serial transfer is read directly at this time.

7 Timing

7.1 timing chart

I2C bus timing

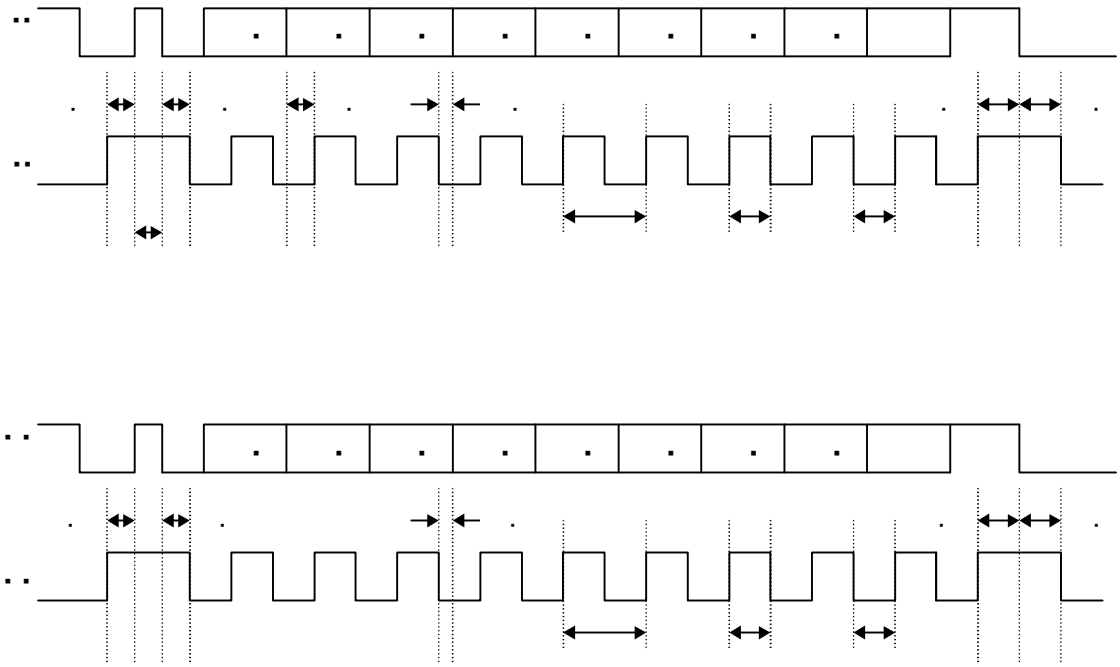


Fig. 7-1 ▪ figure of I2C bus timing

interrupt ion timing

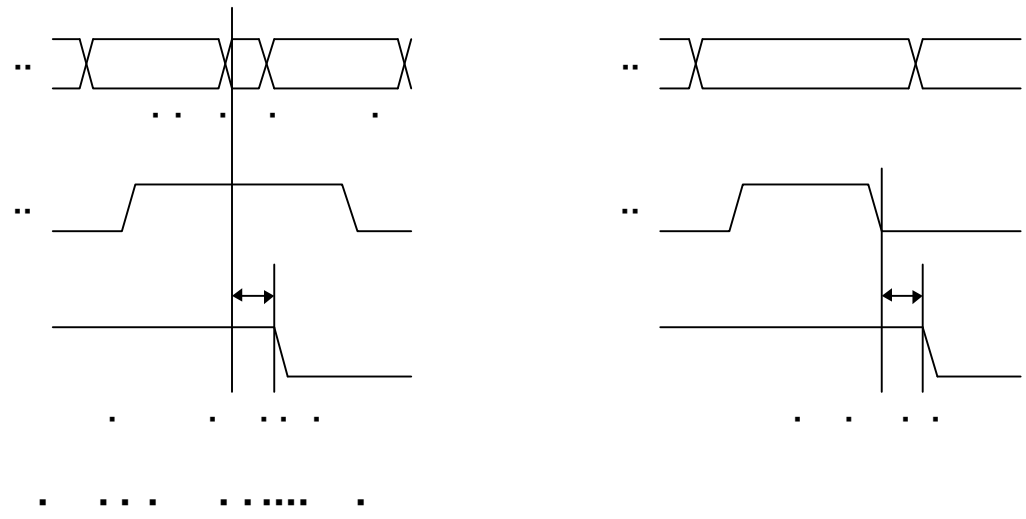


Fig. 7-2 ▪ figure of interruption timing

7.2 timing table

I2C bus timing

symbol			MIN	MAX	unit
T_{S2SDAI}	SDA(I) setup time	standard	▪ ▪ ▪		ns
		high-speed	▪ ▪ ▪		ns
T_{H2SDAI}	SCL(I) hold time	standard	▪		ns
		high-speed	▪		ns
T_{CSCLI}	SCL(I) cycle time	standard	▪ ▪ ▪ ▪		▪ s
		high-speed	▪ ▪ ▪		▪ s
T_{WHSCLI}	SCL(I) H period	standard	▪ ▪ ▪		▪ s
		high-speed	▪ ▪ ▪		▪ s
T_{WLSCLI}	SCL(I) L period	standard	▪ ▪ ▪		▪ s
		high-speed	▪ ▪ ▪		▪ s
T_{CSCLO}	SCL(O) cycle time	standard	2*m+2(*2)		$PCLK_{*1}$
		high-speed	int(1.5*m)+2(*2)		$PCLK_{*1}$
T_{WHSCLO}	SCL(O) H period	standard	m+2(*2)		$PCLK_{*1}$
		high-speed	int(0.5*m)+2(*2)		$PCLK_{*1}$
T_{WLSCLO}	SCL(O) L period	standard	m(*2)		$PCLK_{*1}$
		high-speed	m(*2)		$PCLK_{*1}$
T_{W2SCLI}	SCL(I) setup time	standard	▪ ▪ ▪		▪ s
		high-speed	▪ ▪ ▪		▪ s
T_{H2SCLI}	SCL(I) hold time	standard	▪ ▪ ▪		▪ s
		high-speed	▪ ▪ ▪		▪ s
T_{WBFI}	bus free time	standard	▪ ▪ ▪		▪ s
		hirh-speed	▪ ▪ ▪		▪ s
T_{S2SCLO}	SCL(O) set up time	standard	m+2(*2)		$PCLK_{*1}$
		high-speed	int(0.5*m)+2(*2)		$PCLK_{*1}$
T_{H2SCLO}	SCL(O) hold time	standard	m-2(*2)		$PCLK_{*1}$
		high-speed	int(0.5*m)-2(*2)		$PCLK_{*1}$
T_{H2SDAO}	SDA(O) hold time		▪		$PCLK_{*1}$

*1 ▪ PCLK is an internal clock of I2C module. (16.6MHz)
*2 ▪ Refer to the clock control register (CCR) for the value of m.

timing of interrupt

symbol		MIN	MAX	unit
T_{PHINTR}	XINT delay (bus error)		▪	PCLK
T_{PHINTR}	XINT delay (except bus error)		▪	PCLK

8 Notes

8.1 about a 10-bit slave address

This module does not support the 10-bit slave address. Therefore, please do not specify the slave address of from 78H to 7bH to this module. If it is specified by mistake, a normal transfer cannot be performed although acknowledge bit is returned at the time of 1 byte reception.

8.2 about competition of SCC, MSS, and INT bit

Competition of the following byte transfer, generation of START condition, and generation of STOP condition happens by the simultaneous writing of SCC, MSS, and INT bit. At this time the priority is as follows.

1) the following byte transfer and generation of STOP condition
   If “0” is written to INT bit and “0” is written to MSS bit, priority will be given to “0” writing to MSS bit and STOP condition will be generated.
2) the following byte transfer and generation of START condition
   If “0” is written to INT bit and “1” is written to SCC bit, priority will be given to “1” writing to SCC bit and START condition will be generated.
3) generation of START condition and generation of STOP condition
   The simultaneous writing of “1” in SCC bit and “0” to MSS bit is prohibition.

8.3 about setup of S serial transfer clock

When the delay of the positive edge of SCL terminal is large or when the clock is extended by the slave device, it may become smaller than setting value (calculation value) because of generation of overhead.