FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12528-3E

*8-bit Proprietary Microcontroller*

**CMOS**

# F²MC-8L MB89143A/144A Series

# MB89143A/144A

## ■ DESCRIPTION

The MB89143A/144A has been developed as a general-purpose version of the F²MC-8L* family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain peripheral functions such as dual-clock control system, five operating speed control stages, timers, a serial interface, an A/D converter, buzzer output, high voltage driver, watch prescaler, and an external interrupt. The MB89143A/144A is applicable to a wide range of applications from welfare products to industrial equipment.

*: F²MC stands for FUJITSU Flexible Microcontroller.

## ■ FEATURES

- Minimum execution time: 0.50 µs/8.0-MHz oscillation
- Interrupt servicing time: 4.50 µs/8.0-MHz oscillation
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- Dual-clock control system
- High-voltage ports: 24 channel

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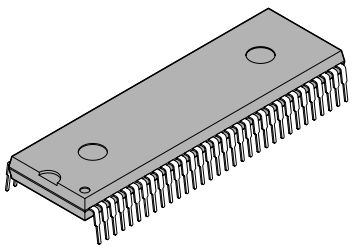
## ■ PACKAGE

64-pin Plastic SH-DIP



(DIP-64P-M01)

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- Two types of timers
  8/16-bit timer/counter (also usable as two 8-bit timers)
  21-bit time-base timer
- One 8-bit serial interface
  Switchable transfer direction allows communication with various equipment.
- 8-bit A/D converter: 8 channels
  Successive approximation type
- External interrupt: 2 channels
  Two channels are independent and capable of wake-up from low-power consumption modes. (Rising edge/falling edge/both edges selectability)
  –0.3 V to +7.0 V can be applied to INT1 (N-ch open-drain)
- Low-power consumption modes
  Subclock mode (The main clock stops, and the device operates at the subclock.)
  Watch mode (Only the watch prescaler is operating.)
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
- Watch prescaler
- Buzzer output
- Watchdog reset, reset output, and power-on reset functions

## ■ PRODUCT LINEUP

| Parameter \ Part number | MB89143A | MB89144A | MB89P147 | MB89PV140 |
|---|---|---|---|---|
| Classification | Mass production products (mask ROM products) | | One-time PROM product | Piggyback/evaluation product (for evaluation and development) |
| ROM size | 8 K × 8 bits | 12 K × 12 bits | 32 K × 8 bits Internal PROM | 32 K × 8 bits External ROM (Piggyback) |
| RAM size | 256 × 8 bits | | 1 K × 8 bits Internal | |
| CPU functions | Number of instructions: 136<br>Instruction bit length: 8 bits<br>Instruction length: 1 to 3 bytes<br>Data bit length: 1, 8, 16 bits<br>Minimum execution time: 0.5 µs/8 MHz to 8.0 µs/8 MHz, 61 µs/32.768 kHz<br>Interrupt processing time: 4.5 µs/8 MHz to 72.0 µs/8 MHz, 562.5 µs/32.768 kHz<br>Note: The above times change according to the gear function. | | | |
| Ports | High-voltage output ports (P-ch open-drain): 24 (P40 to P47, P50 to P57, and P60 to P67)<br>Buzzer output (P-ch open-drain, high-voltage):1<br>Output ports (CMOS): 4 (P20 to P23)<br>Input ports (CMOS): 2 (P70 and P71, function as X0A and X1A pins when dual-clock system is used.)<br>I/O ports (CMOS): 23 (P00 to P07, P10 to P17, P30, and P32 to P37)<br>I/O port (N-channel open-drain): 1 (P31)<br>Total: 55 | | | |
| Time-base timer | Capable of generating four different intervals (at 8.0-MHz oscillation): 0.26 ms, 0.51 ms, 1.02 ms, and 0.524 s | | | |
| 8/16-bit timer counter | 8/16-bit timer operation (Operating clock, internal clock, external trigger)<br>8/16-bit event counter operation (Rising edge/falling edge/both edges selectability) | | | |
| 8-bit Serial I/O | 8 bits<br>LSB first/MSB first selectability<br>One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 4, 8, 16 system clock cycles) | | | |
| A/D converter | 8-bit resolution × 8 channels<br>A/D conversion mode (with conversion time of 22 µs/8 MHz, and highest gear speed)<br>Continuous activation by external activation capable | | 10-bit resolution × 12 channels<br>A/D conversion mode (with conversion time of 16.5 µs/8 MHz, and highest gear speed)<br>Sense mode (with conversion time of 9.0 µs/8 MHz, and highest gear speed)<br>Continuous activation enabled by external activation capable | |
| External interrupt | 2 independent channels (edge selection, interrupt vector, source flag)<br>Rising edge/falling edge/both edges selectability<br>Built-in analog noise canceller<br>Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.) | | | |
| Buzzer output | 1.95 or 3.91 kHz selectable (at 8-MHz oscillation)<br>Output to a high-voltage pin | | | |

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| Part number / Parameter | MB89143A | MB89144A | MB89P147 | MB89PV140 |
|---|---|---|---|---|
| Watchdog reset | Internal reset in 524 ms to 1049 ms (at 8 MHz oscillation) when the program runway occurs | | | |
| 8-bit PWM timer | None | | 8-bit timer operation/8-bit resolution PWM operation | |
| 12-bit MPG timer | None | | 12-bit resolution PWM operation/reload timer operation/PPG operation | |
| Standby mode | Sleep mode, stop mode, and watch mode | | | |
| Process | CMOS | | | |
| Package | DIP-64P-M01 | | | MDP-64C-P02 |
| EPROM for use | | | | MBM27C256A-20 |
| Operating voltage* | 4.0 V to 6.0 V | | 2.7 V to 6.0 V | |

* : Varies with conditions such as the operating frequency. (See section “■ ELECTRICAL CHARACTERISTICS”.)

## ■ PACKAGE AND CORRESPONDING PRODUCTS

| Package | MB89143A<br>MB89144A | MB89P147 | MB89PV140 |
|---|---|---|---|
| DIP-64P-M01 | ○ | ○ | × |
| MDP-64C-P02 | × | × | ○ |

○ : Available × : Not available

Note: For more information about each package, see section “■ PACKAGE DIMENSION”.

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89143A/144A, the upper half of the register bank cannot be used.
- The stack area etc. are set at the upper limit of the RAM.

### 2. Functions

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following point:

- The A/D converter in the MB89143A/144A is an 8-bit resolution type. The MB89143A/144A contains neither the 8-bit PWM timer nor the 12-bit MPG timer.

### 3. Current Consumption

- In the case of the MB89PV140, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see section “■ ELECTRICAL CHARACTERISTICS”.)

### 4. Mask Options

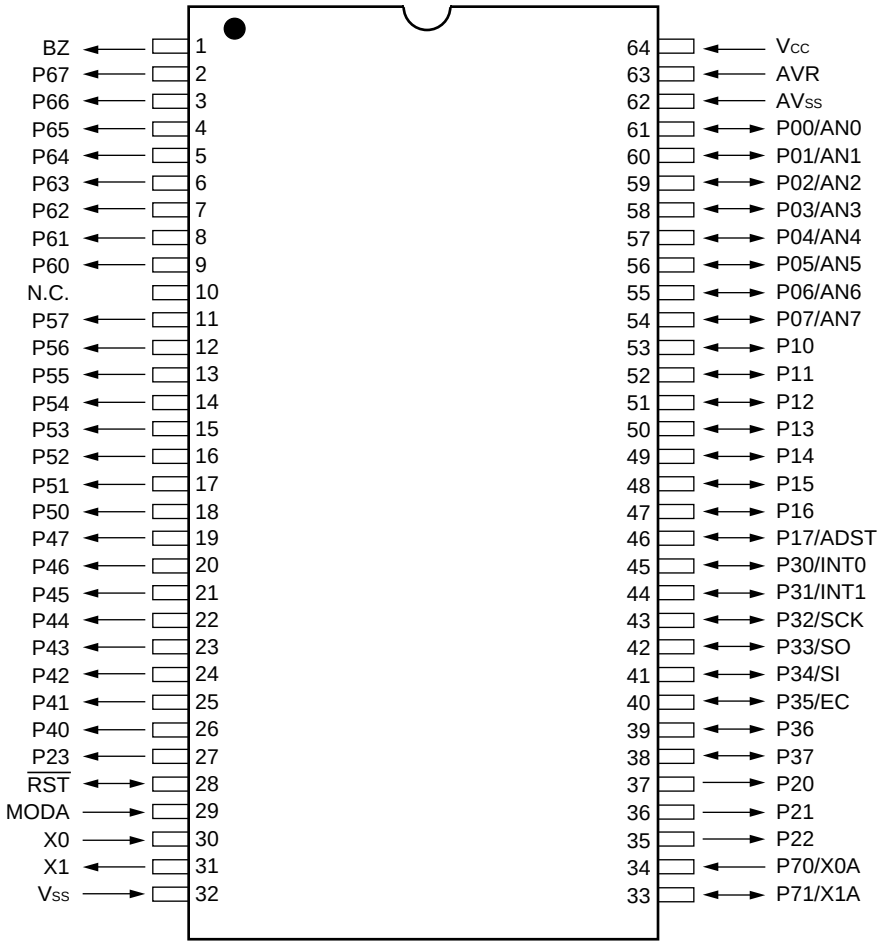
Functions that can be selected as options and how to designate these options vary by the product. Before using options check section “■ MASK OPTIONS”.

Take particular care on the following point:

- A pull-up resistor option is not provided for the MB89PV140.

## ■ PIN ASSIGNMENT (MB89143A/4A only)

(Top view)




Note: When used as general-purpose ports, the P70/X0A and P71/X1A function as input-only ports.

(DIP-64P-M01)

## ■ PIN DESCRIPTION (MB89143A/4A only)

| Pin no. SDIP* | Pin name | Circuit type | Function |
|---|---|---|---|
| 30 | X0 | A | Main clock oscillator pins<br>Use a crystal oscillator. |
| 31 | X1 | | |
| 29 | MODA | B | Operating mode selection pin<br>Connect directly to $V_{SS}$ in normal operation. |
| 28 | $\overline{RST}$ | C | Reset I/O pin<br>This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source.<br>The internal circuit is initialized by the input of “L”.<br>This pin is with a noise canceller. |
| 54 to 61 | P07/AN7 to P00/AN0 | F | General-purpose I/O ports<br>These ports are a hysteresis input type. Also serve as an analog input. |
| 46 | P17/ADST | H | General-purpose I/O port<br>This port is a hysteresis input type. Also serves as an A/D converter external activation. |
| 47 to 53 | P16 to P10 | H | General-purpose I/O ports<br>These ports are a hysteresis input type. |
| 34, 33 | P70/X0A, P71/X1A | J | Selectable either general-purpose input ports or the subclock oscillator pins by the mask option. These ports are a hysteresis input type when used as general-purpose input ports. |
| 27, 35 to 37 | P23 to P20 | D | General-purpose output ports |
| 38, 39 | P37, P36 | H | General-purpose I/O ports<br>These ports are a hysteresis input type. |
| 40 | P35/EC | | General-purpose I/O port<br>This port is a hysteresis input type. Also serves as the external clock input for the 8/16-bit timer/counter. |
| 41 | P34/SI | | General-purpose I/O port<br>This port is a hysteresis input type. Also serves as the serial data input for the 8-bit serial interface. |
| 42 | P33/SO | | General-purpose I/O port<br>This port is a hysteresis input type. Also serves as the serial data output for the 8-bit serial interface. |
| 43 | P32/SCK | | General-purpose I/O port<br>This port is a hysteresis input type. Also serves as the serial transfer clock for the 8-bit serial interface. |

* : DIP-64P-M01

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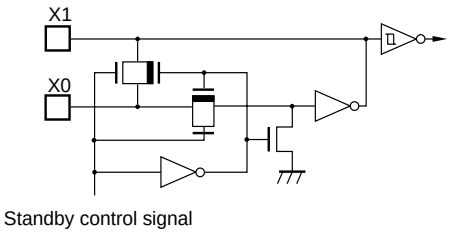
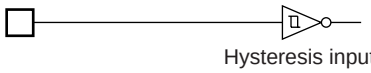
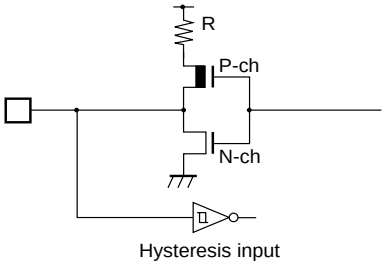
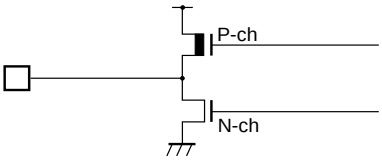
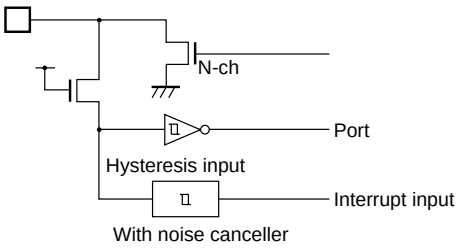
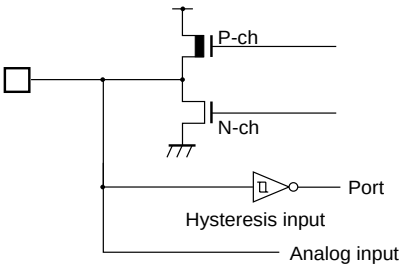
| Pin no. SDIP* | Pin name | Circuit type | Function |
|---|---|---|---|
| 44 | P31/INT1 | E | General-purpose I/O port<br>This port is an N-ch open-drain output and hysteresis input type. Also serves as an external interrupt. The interrupt input is a hysteresis input type and with a built-in noise canceller. |
| 45 | P30/INT0 | I | General-purpose I/O port<br>This port is a hysteresis input type. Also serves as an external interrupt. The interrupt input is a hysteresis input type and with a built-in noise canceller. |
| 1 | BZ | G | Buzzer output-only pin<br>P-ch high-voltage open-drain output port |
| 19 to 26,<br>11 to 18,<br>2 to 9 | P47 to P40,<br>P57 to P50,<br>P67 to P60 | G | P-ch high-voltage open-drain output port |
| 10 | N.C. | — | Be sure to leave them open. |
| 64 | $V_{CC}$ | — | Power supply pin<br>Also serves as an A/D converter power supply. |
| 32 | $V_{SS}$ | — | Power supply (GND) pin |
| 63 | AVR | — | A/D converter reference voltage input pin |
| 62 | $AV_{SS}$ | — | A/D converter power supply pin<br>Use this pin at the same voltage as $V_{SS}$. |

* : DIP-64P-M01

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V |
| B |  | • CMOS input |
| C |  | • At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V<br>• CMOS hysteresis input |
| D |  | • CMOS output |
| E |  | • N-ch open-drain output<br>• CMOS hysteresis input<br>• The interrupt input is with a noise canceller. |
| F |  | • CMOS output<br>• CMOS hysteresis input |

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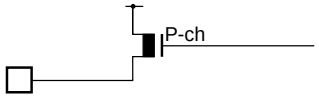
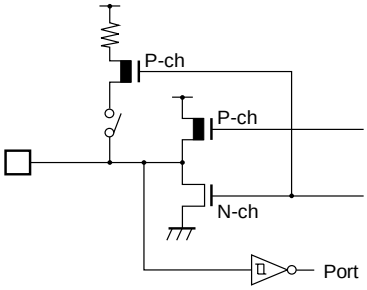
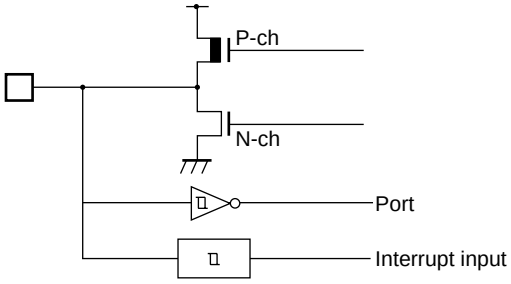
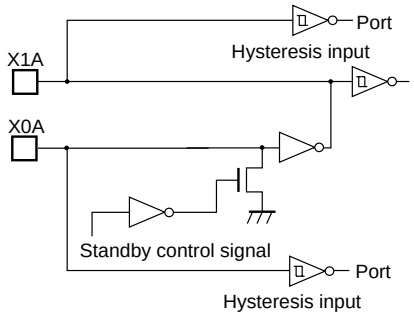
| Type | Circuit | Remarks |
|---|---|---|
| G |  | • P-ch high-voltage open-drain output |
| H |  | • CMOS output<br>• CMOS hysteresis input<br>• Pull-up resistor optional<br>(Only for P14 to P17 and P32 to P37) |
| I |  | • CMOS output<br>• CMOS hysteresis input<br>• The interrupt input is with a noise canceller. |
| J |  | • The oscillation feedback resistor is not provided.<br>• CMOS hysteresis input when subclock is not used |

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ ELECTRICAL CHARACTERISTICS” is applied between $V_{CC}$ and $V_{SS}$. (However, up to 7.0 V can be applied to P31/INT1 pin, regardless of $V_{CC}$.)

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AVR) and analog input from exceeding the digital power supply ($V_{CC}$) when the analog system power supply is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

### 3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be $AV_{SS}$ = AVR = $V_{SS}$ even if the A/D and D/A converters are not in use.

### 4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

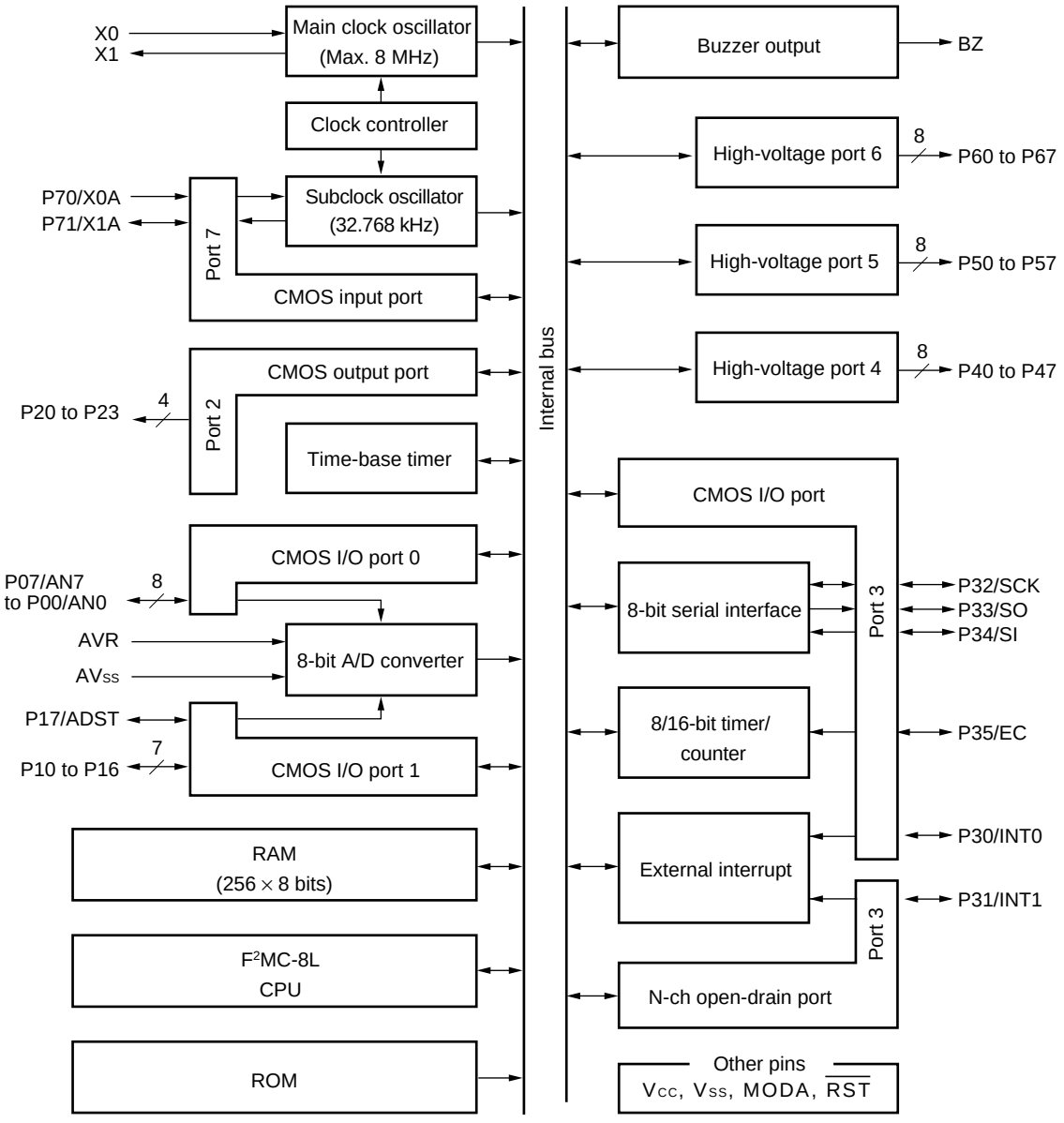
### 5. Power Supply Voltage Fluctuations

Although $V_{CC}$ power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that $V_{CC}$ ripple fluctuations (P-P value) will be less than 10% of the standard $V_{CC}$ value at the commercial frequency(50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and wake-up from stop mode.

## ■ BLOCK DIAGRAM (MB89143A/4A only)

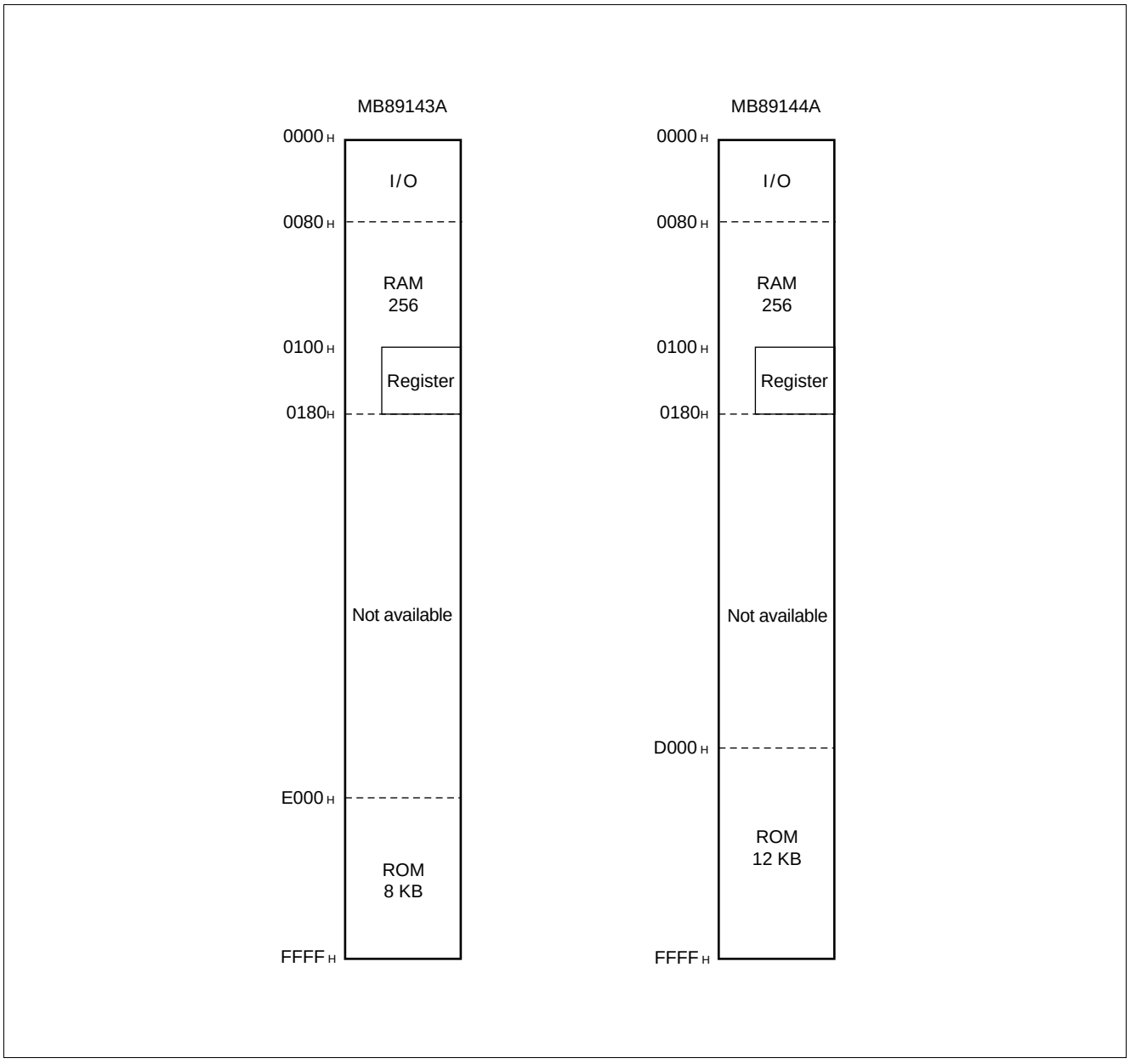



Note: The A/D converter is an 8-bit, 8-channel type.

## ■ CPU CORE

### 1. Memory Space

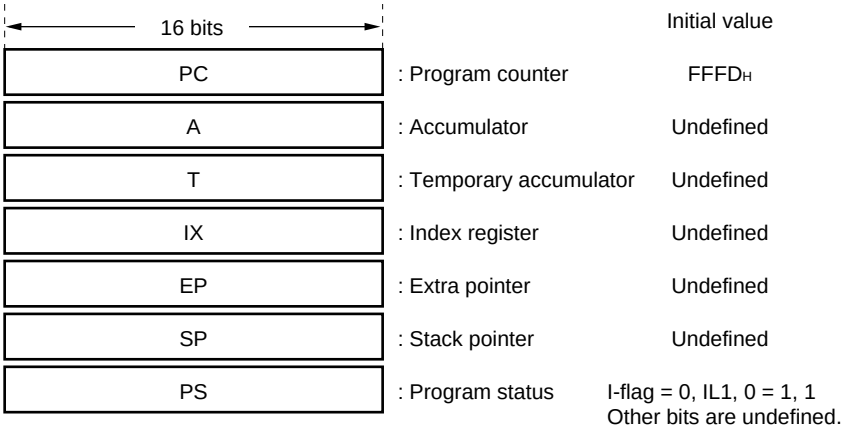
The microcontrollers of the MB89143A/144A series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89143A/144A series is structured as illustrated below.



## 2. Registers

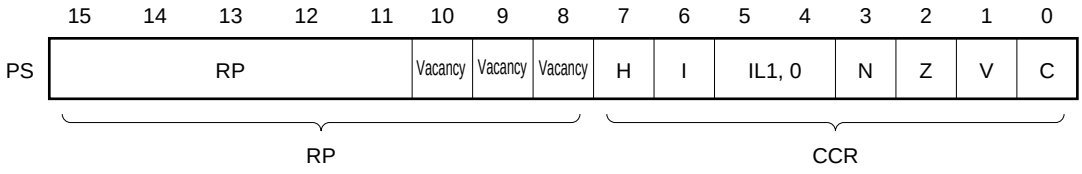
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

| | |
|---|---|
| Program counter (PC): | A 16-bit register for indicating instruction storage positions |
| Accumulator (A): | A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used. |
| Temporary accumulator (T): | A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used. |
| Index register (IX): | A 16-bit register for index modification |
| Extra pointer (EP): | A 16-bit pointer for indicating a memory address |
| Stack pointer (SP): | A 16-bit register for indicating a stack area |
| Program status (PS): | A 16-bit register for storing a register pointer, a condition code |



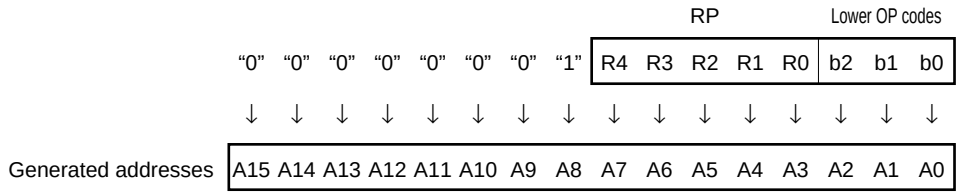

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

**Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

**Rule for Conversion of Actual Addresses of the General-purpose Register Area**




The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | IL0 | Interrupt level | High-low |
|---|---|---|---|
| 0 | 0 | 1 | High |
| 0 | 1 | | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | Low = no interrupt |

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set to 1 when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set to 1 if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

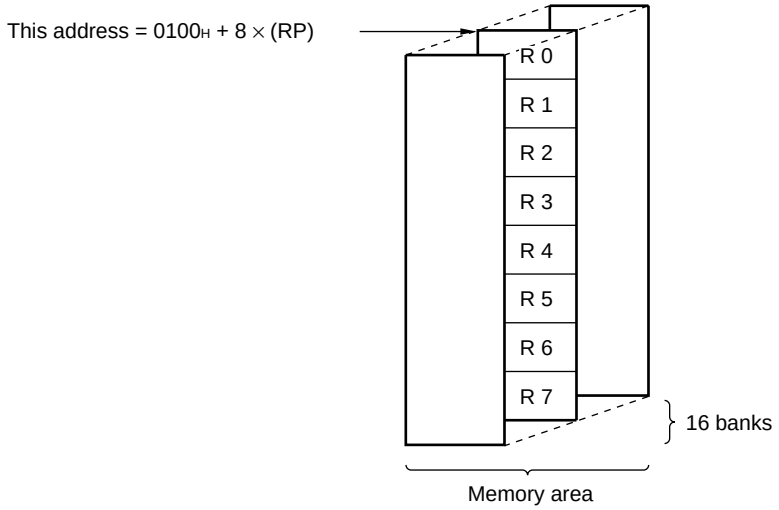
C-flag: Set to 1 when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation.
Cleared otherwise.
Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89143A/144A. The bank currently in use is indicated by the register bank pointer (RP).

**Register Bank Configuration**



## ■ I/O MAP

| Address | Read/write | Register name | Register description |
|---|---|---|---|
| 00H | (R/W) | PDR0 | Port 0 data register |
| 01H | (W) | DDR0 | Port 0 data direction register |
| 02H | (R/W) | PDR1 | Port 1 data register |
| 03H | (W) | DDR1 | Port 1 data direction register |
| 04H | (R/W) | PDR2 | Port 2 data register |
| 05H, 06H | Vacancy | | |
| 07H | (R/W) | SYCC | System clock control register |
| 08H | (R/W) | STBC | Standby control register |
| 09H | (R/W) | WDTE | Watchdog timer control register |
| 0AH | (R/W) | TBCR | Time-base timer control register |
| 0BH | (R/W) | WPCR | Watch prescaler control register |
| 0CH | (R/W) | PDR3 | Port 3 data register |
| 0DH | (W) | DDR3 | Port 3 data direction register |
| 0EH | (R/W) | BUZR | Buzzer register |
| 0FH | (R/W) | EIC | External interrupt control register |
| 10H | (R/W) | PDR4 | Port 4 data register |
| 11H | (R/W) | PDR5 | Port 5 data register |
| 12H | (R/W) | PDR6 | Port 6 data register |
| 13H | (R) | PDR7 | Port 7 data register |
| 14H to 17H | Vacancy | | |
| 18H | (R/W) | T3CR | Timer 3 control register |
| 19H | (R/W) | T2CR | Timer 2 control register |
| 1AH | (R/W) | T3DR | Timer 3 data register |
| 1BH | (R/W) | T2DR | Timer 2 data register |
| 1CH | (R/W) | SMR | Serial mode register |
| 1DH | (R/W) | SDR | Serial data register |
| 1EH | (R/W) | ADC1 | A/D converter control register 1 |
| 1FH | (R/W) | ADC2 | A/D converter control register 2 |
| 20H | (R/W) | ADDH | A/D data register (H) |
| 21H | (R/W) | ADDL | A/D data register (L) |
| 22H | (W) | PCR0 | Port input control register 0 |
| 23H | (W) | PCR1 | Port input control register 1 |
| 24H to 7BH | Vacancy | | |
| 7CH | (W) | ILR1 | Interrupt level setting register 1 |
| 7DH | (W) | ILR2 | Interrupt level setting register 2 |
| 7EH | (W) | ILR3 | Interrupt level setting register 3 |
| 7FH | Vacancy | | |

Note: Do not use vacancies.

## ■ ELECTRICAL CHARACTERISTICS (MB89143A/4A only)

### 1. Absolute Maximum Ratings

($AV_{SS}$ = $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power supply voltage | $V_{CC}$<br>AVR | $V_{SS}$ – 0.3 | $V_{SS}$ + 7.0 | V | AVR ≤ $V_{CC}$ +0.3*1 |
| Input voltage | $V_{I1}$ | $V_{SS}$ – 0.3 | $V_{CC}$ + 0.3 | V | P00 to P07, P10 to P17, P30, P32 to P37, P70, P71 |
| | $V_{I2}$ | $V_{SS}$ – 0.3 | 7 | V | P31 |
| | $V_{I3}$ | $V_{CC}$ – 40 | $V_{CC}$ + 0.3 | V | P40 to P47, P50 to P57, P60 to P67, BZ*2 |
| Output voltage | $V_{O1}$ | $V_{SS}$ – 0.3 | $V_{CC}$ + 0.3 | V | P00 to P07, P10 to P17, P20 to P23, P30 to P37 |
| | $V_{O2}$ | — | $V_{CC}$ + 0.3 | V | P40 to P47, P50 to P57, P60 to P67, BZ*2 |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | –100 | mA | |
| “H” level total average output current | $\Sigma I_{OHAV}$ | — | –75 | mA | Average value (operating current × operation rate) |
| “H” level maximum output current | $I_{OH}$ | — | –12 | mA | P00 to P07, P30, P32 to P37, P10 to P17, P20 to P23 |
| “H” level average output current | $I_{OHAV}$ | — | –6 | | Average value (operating current × operation rate) |
| “H” level maximum output current | $I_{OH}$ | — | –20 | mA | P40 to P47, P50 to P57, P60 to P67, BZ |
| “H” level average output current | $I_{OHAV}$ | — | –10 | | Average value (operating current × operation rate) |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 50 | mA | |
| “L” level total average output current | $\Sigma I_{OLAV}$ | — | 30 | mA | Average value (operating current × operation rate) |
| “L” level maximum output current | $I_{OL}$ | — | 12 | mA | P00 to P07, P10 to P17, P20 to P23, P30 to P37 |
| “L” level average output current | $I_{OLAV}$ | — | 6 | | |
| Power consumption | $P_D$ | — | 470 | mW | SH-DIP64: DIP-64P-M01 |
| Operating temperature | $T_A$ | –40 | +85 | °C | |
| Storage temperature | Tstg | –55 | +150 | °C | |

*1: Take care so that AVR does not exceed $V_{CC}$ + 0.3 V, and does not exceed $V_{CC}$ when power is turned on.

*2: $V_I$ and $V_O$ must not exceed $V_{CC}$ + 0.3 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($AV_{SS}$ = $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power supply voltage | $V_{CC}$ | 4.0* | 6.0* | V | Normal operation assurance range* at highest gear speed |
| | | 3.5* | 6.0* | V | Normal operation assurance range* at highest gear speed |
| | | 2.5 | 6.0 | V | When in watch mode or subclock operation mode |
| | | 1.5 | 6.0 | V | Retains the RAM state in stop mode |
| A/D converter reference input voltage | AVR | 0.0 | $V_{CC}$ | V | |
| Operating temperature | $T_A$ | –40 | +85 | °C | |

* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and “5. A/D Converter Electrical Characteristics.”

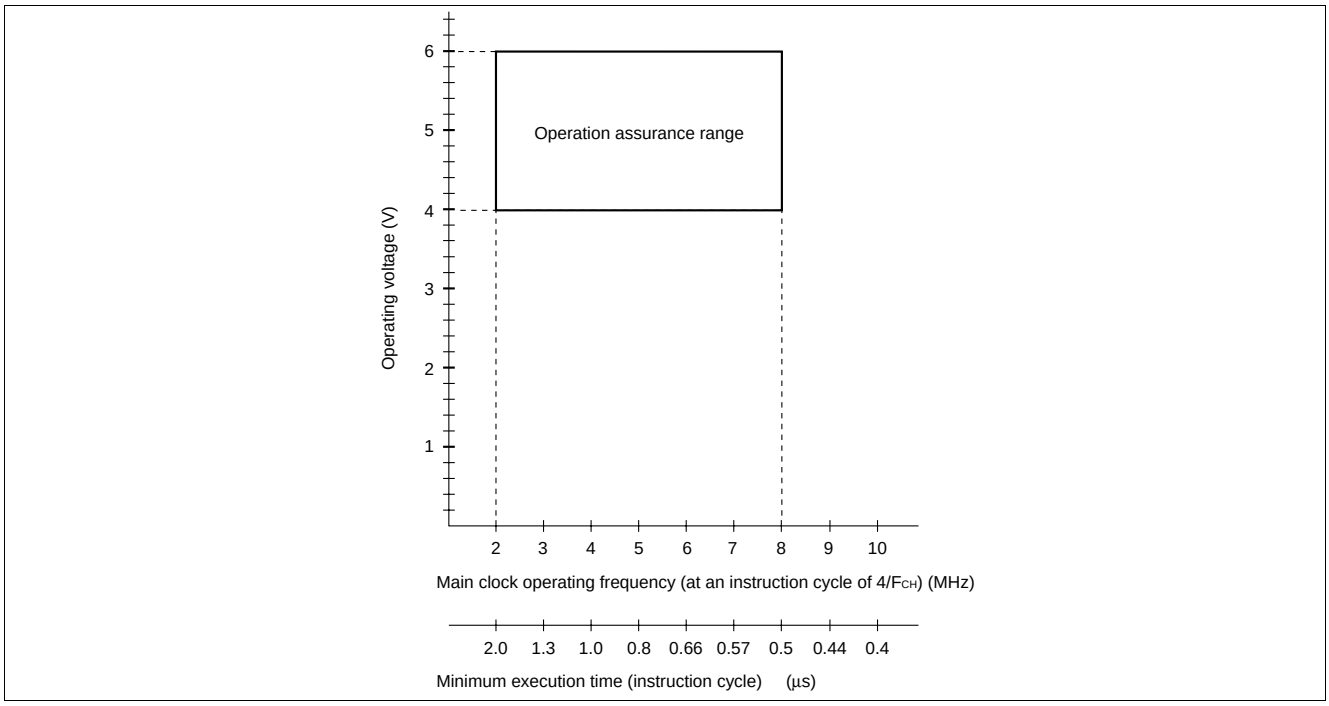



**Figure 1 Operating Voltage vs. Main Clock Operating Frequency**

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/$F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

(AVR = $V_{CC}$ = 5.0 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| "H" level input voltage | $V_{IHS}$ | P00 to P07, P10 to P17, P30 to P37, P70, P71, X0, $\overline{RST}$, X1, MODA | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{ILS}$ | P00 to P07, P10 to P17, P30 to P37, P70, P71, X0, $\overline{RST}$, X1, MODA | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | |
| Open-drain output pin application voltage | $V_{D1}$ | P31 | — | $V_{SS}$ – 0.3 | — | 7.0 | V | |
| "H" level output voltage | $V_{OH1}$ | P00 to P07, P10 to P17, P20 to P23, P30 to P37 | $I_{OH}$ = –2.0 mA | 2.4 | — | — | V | Except P31 |
| | $V_{OH2}$ | P40 to P47, P50 to P57, P60 to P67 | $I_{OH}$ = –10 mA | 3.0 | — | — | V | |
| "L" level output voltage | $V_{OL1}$ | P00 to P07, P10 to P17, P20 to P23, P30 to P37 | $I_{OL}$ = 1.8 mA | — | — | 0.4 | V | |
| | $V_{OL2}$ | $\overline{RST}$ | $I_{OL}$ = 4.0 mA | — | — | 0.6 | V | |
| Input leakage current | $I_{LI1}$ | P00 to P07, P10 to P17, P30 to P37, P70, P71 | 0 V < $V_I$ < $V_{CC}$ | — | — | ±5 | µA | Except pins with pull-up resistor |
| | $I_{LI2}$ | P14 to P17, P32 to P37 | $V_I$ = 0.0 V | –200 | –100 | –50 | µA | Only for pins with pull-up resistor |
| Output leakage current | $I_{LO1}$ | P40 to P47, P50 to P57, P60 to P67 | $V_I$ = $V_{CC}$ – 35 V | — | — | –10 | µA | |
| Pull-up resistance | $R_{PULL}$ | $\overline{RST}$, P14 to P17, P32 to P37 | $V_I$ = 0.0 V | 25 | 50 | 100 | kΩ | |
| Power supply current | $I_{CC1}$ | $V_{CC}$ | $F_{CH}$ = 8 MHz, $V_{CC}$ = 5.0 V, $t_{inst}$ = 0.5 µs, when A/D conversion is stopped | — | 9 | 15 | mA | |

Note: The power supply current is measured at the external clock.

*(Continued)*

*(Continued)*

(AVR = $V_{CC}$ = 5.0 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Power supply current | $I_{CC2}$ | $V_{CC}$ | $F_{CH}$ = 8 MHz, $V_{CC}$ = 3.5 V, $t_{inst}$ = 8.0 µs, when A/D conversion is stopped | — | 1.5 | 2 | mA | |
| | $I_{CCS1}$ | | Sleep mode: $F_{CH}$ = 8 MHz, $V_{CC}$ = 5.0 V, $t_{inst}$ = 0.5 µs | — | 3 | 7 | mA | |
| | $I_{CCS2}$ | | Sleep mode: $F_{CH}$ = 8 MHz, $V_{CC}$ = 3.5 V, $t_{inst}$ = 8.0 µs | — | 1 | 1.5 | mA | |
| | $I_{CCL}$ | | $F_{CL}$ = 32.768 kHz, $V_{CC}$ = 3.0 V, Subclock mode | — | 50 | 150 | µA | |
| | $I_{CCLS}$ | | $F_{CL}$ = 32.768 kHz, $V_{CC}$ = 3.0 V, Subclock mode | — | 25 | 50 | µA | |
| | $I_{CCT}$ | | $F_{CL}$ = 32.768 kHz, $V_{CC}$ = 3.0 V<br>• Watch mode<br>• Main clock stop mode at dual-clock system | — | 3 | 15 | µA | |
| | $I_{CCH}$ | | $F_{CL}$ = 32.768 kHz, $T_A$ = +25°C<br>• Subclock stop mode<br>• Main clock stop mode at single-clock system | — | — | 10 | µA | |
| | $I_{CCA}$ | | $F_{CH}$ = 8 MHz, $V_{CC}$ = 5.0 V, $T_A$ = +25°C, $t_{inst}$ = 0.5 µs, when A/D conversion is activated | — | 11.5 | 19.5 | mA | When the gear function is used, the power supply current varies with the measurement point. |
| | $I_R$ | AVR | $F_{CH}$ = 8 MHz, $T_A$ = +25°C, when A/D conversion is activated | — | 200 | — | µA | |
| | $I_{RH}$ | | $F_{CH}$ = 8 MHz, $T_A$ = +25°C, when A/D conversion is stopped | — | — | 10 | µA | |
| Input capacitance | $C_{IN}$ | Other than $AV_{SS}$, AVR, $V_{CC}$, and $V_{SS}$ | f = 1 MHz | — | 10 | — | pF | |

Note: The power supply current is measured at the external clock.

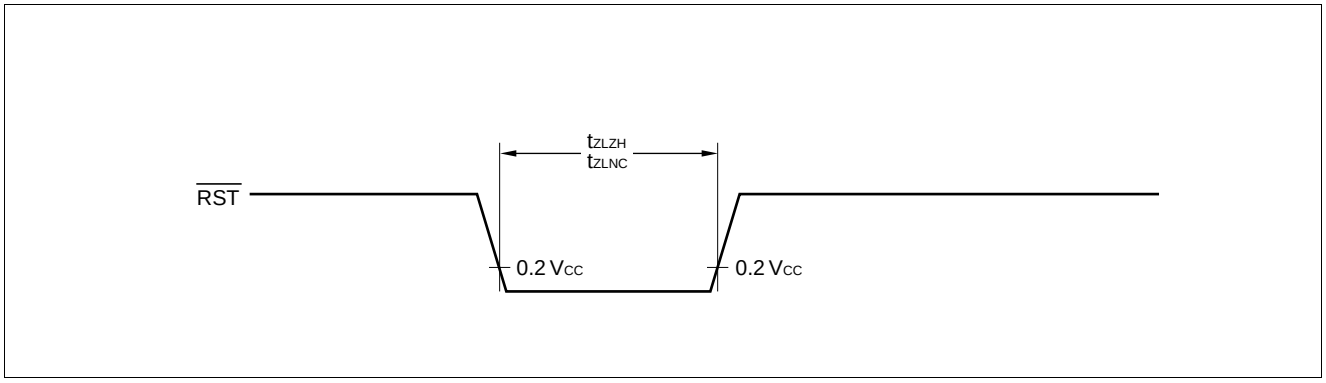
## 4. AC Characteristics

### (1) Reset Timing

(AVR = $V_{CC}$ = 5.0 V±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| $\overline{RST}$ "L" pulse width | $t_{ZLZH}$ | — | 48 $t_{XCYL}$ | — | — | ns | |
| $\overline{RST}$ noise limit width | $t_{ZLNC}$ | — | 20 | 40 | 60 | ns | |

Note: $t_{XCYL}$ is the oscillation cycle ($1/F_{CH}$) to input to the X0 pin.

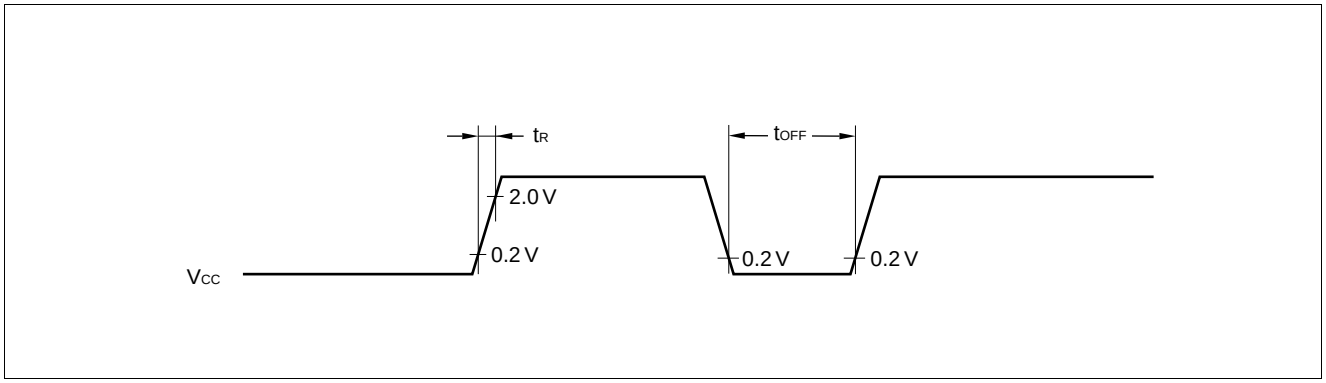



### (2) Power-on Reset

($AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Power supply rising time | $t_R$ | — | — | 50 | ms | Power-on reset function only |
| Power supply cut-off time | $t_{OFF}$ | — | 1 | — | ms | Due to repeated operations |

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

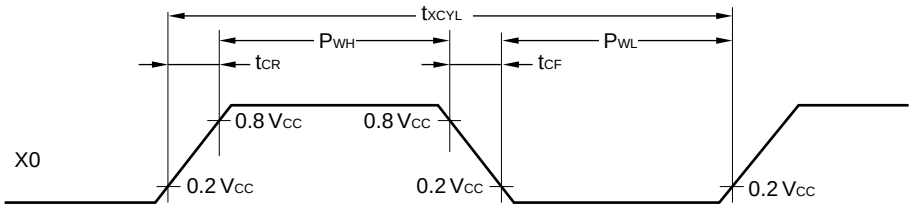


### (3) Clock Timing

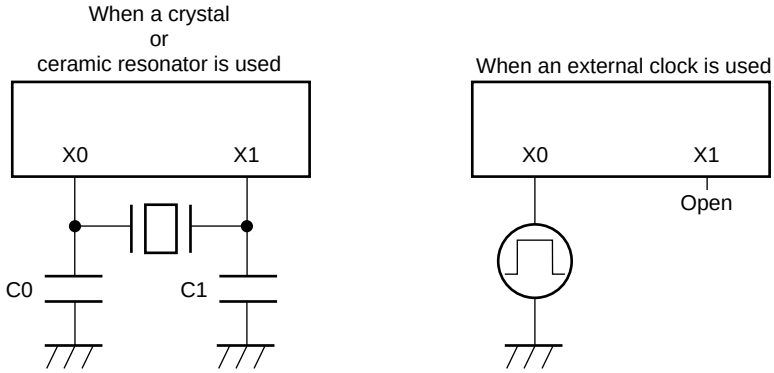
($AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Clock frequency | $F_{CH}$ | X0, X1 | — | 2 | — | 8 | MHz | |
| | $F_{CL}$ | X0A, X1A | — | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{XCYL}$ | X0, X1 | — | 125 | — | 500 | ns | |
| | $t_{LXCYL}$ | X0A, X1A | — | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$<br>$P_{WL}$ | X0 | — | 30 | — | — | ns | External clock |
| | $P_{WHL}$<br>$P_{WLL}$ | X0A | — | — | 15.2 | — | ns | |
| Input clock rising/ falling time | $t_{CR}$<br>$t_{CF}$ | X0, X0A | — | — | — | 10 | ns | External clock |

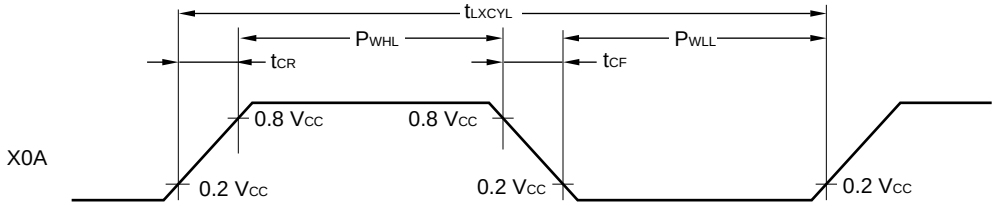
**X0 and X1 Timings and Conditions**



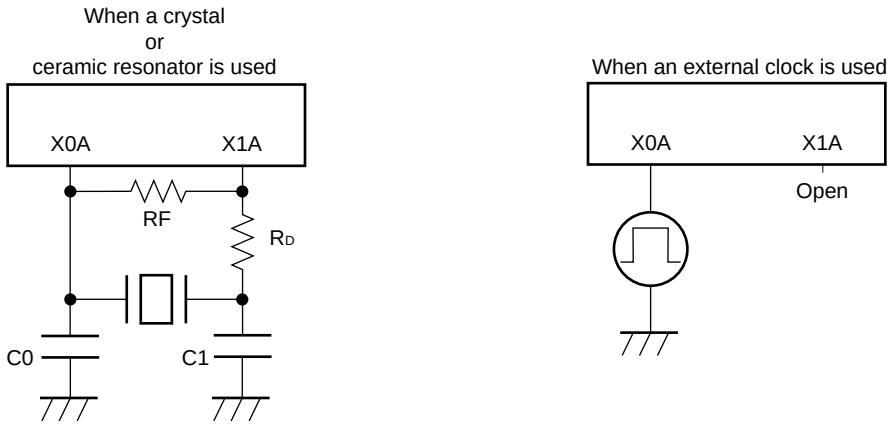

**Main Clock Conditions**



**X0A and X1A Timings and Conditions**




**Subclock Conditions**




Note: The subclock oscillator feedback resistor is connected externally in dual-clock products.

### (4) Instruction Cycle

| Parameter | Symbol | Value (typical) | Unit | Remarks |
|---|---|---|---|---|
| Instruction cycle time | $t_{inst}$ | $4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $32/F_{CH}$ | µs | $(4/F_{CH})$ $t_{inst}$ = 0.5 µs when operating at $F_{CH}$ = 8 MHz |
| | | $2/F_{CL}$ | µs | $t_{inst}$ = 61.036 µs when operating at $F_{CL}$ = 32.768 kHz |

Note: When operating at 8 MHz, the cycle varies with the set execution time.

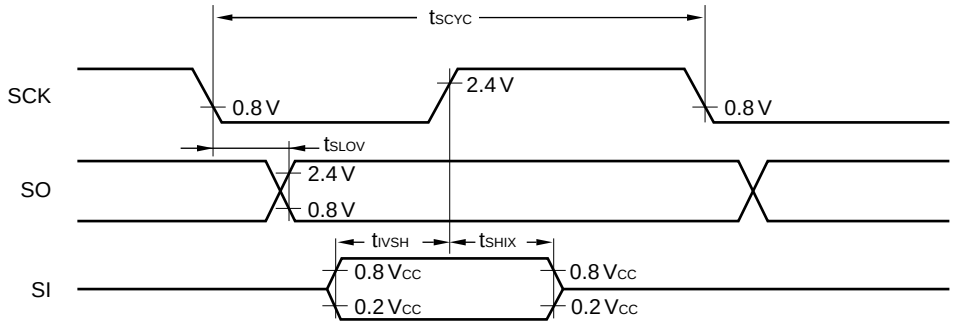
### (5) Serial I/O timing

(AVR = $V_{CC}$ = 5.0 V±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

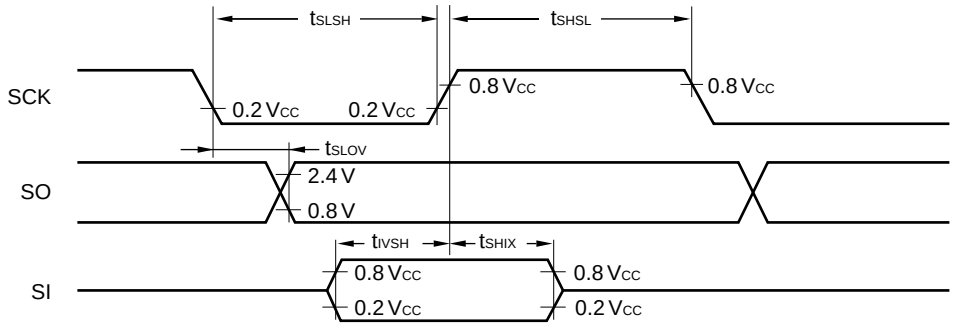
| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal shift clock mode | 2 $t_{inst}$* | — | µs | |
| SCK ↓ → SO time | $t_{SLOV}$ | SCK, SO | | –200 | 200 | ns | |
| Valid SI → SCK ↑ | $t_{IVSH}$ | SI, SCK | | 1/2 $t_{inst}$* | — | µs | |
| SCK ↑ → valid SI hold time | $t_{SHIX}$ | SCK, SI | | 1/2 $t_{inst}$* | — | µs | |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK | External shift clock mode | 1 $t_{inst}$* | — | µs | |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK | | 1 $t_{inst}$* | — | µs | |
| SCK ↓ → SO time | $t_{SLOV}$ | SCK, SO | | 0 | 200 | ns | |
| Valid SI → SCK ↑ | $t_{IVSH}$ | SI, SCK | | 1/2 $t_{inst}$* | — | µs | |
| SCK ↑ → valid SI hold time | $t_{SHIX}$ | SCK, SI | | 1/2 $t_{inst}$* | — | µs | |

* : For information on $t_{inst}$, see “(4) Instruction Cycle.”

**Internal Shift Clock Mode**



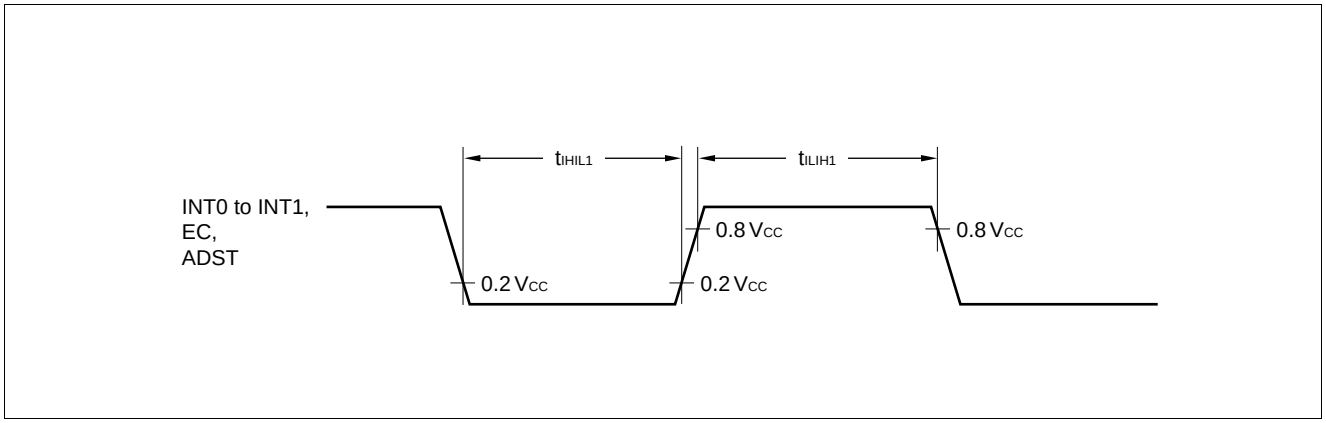

**External Shift Clock Mode**



### (6) Peripheral Input Timing

(AVR = $V_{CC}$ = 5.0 V±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Peripheral input “H” pulse width 1 | $t_{ILIH1}$ | EC, ADST, INT0 to INT1 | — | 2 $t_{inst}$ | — | µs | |
| Peripheral input “L” pulse width 1 | $t_{IHIL1}$ | EC, ADST, INT0 to INT1 | — | 2 $t_{inst}$ | — | µs | |

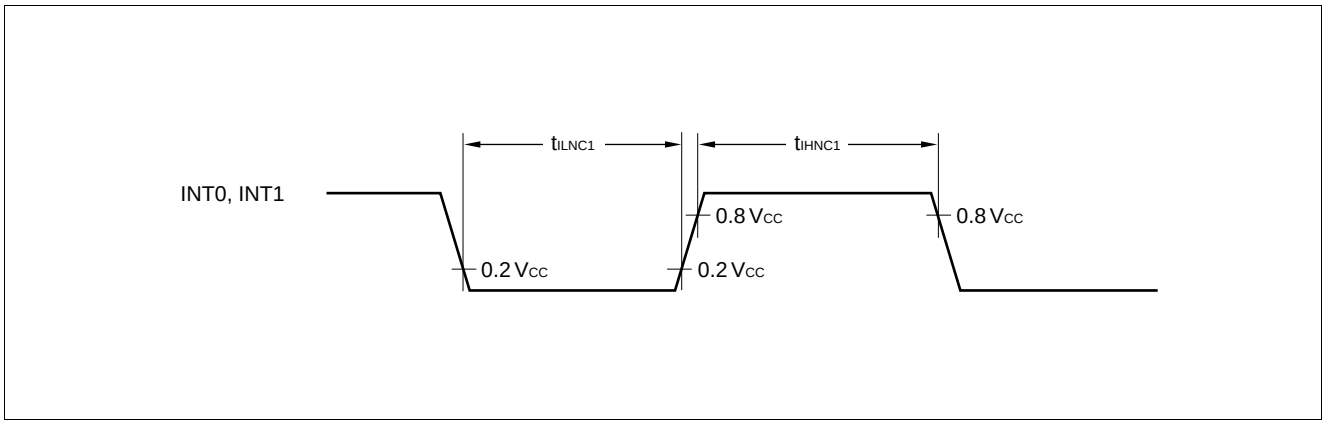



### (7) Peripheral Input Noise Limit Width

(AVR = $V_{CC}$ = 5.0 V±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Peripheral input “H” level noise limit width 1 | $t_{IHNC1}$ | INT1, INT0 | 50 | 100 | 250 | ns | |
| Peripheral input “L” level noise limit width 1 | $t_{ILNC1}$ | INT1, INT0 | 50 | 100 | 250 | ns | |

Note: The minimum values is always canceled, while values over the maximum value are not canceled.



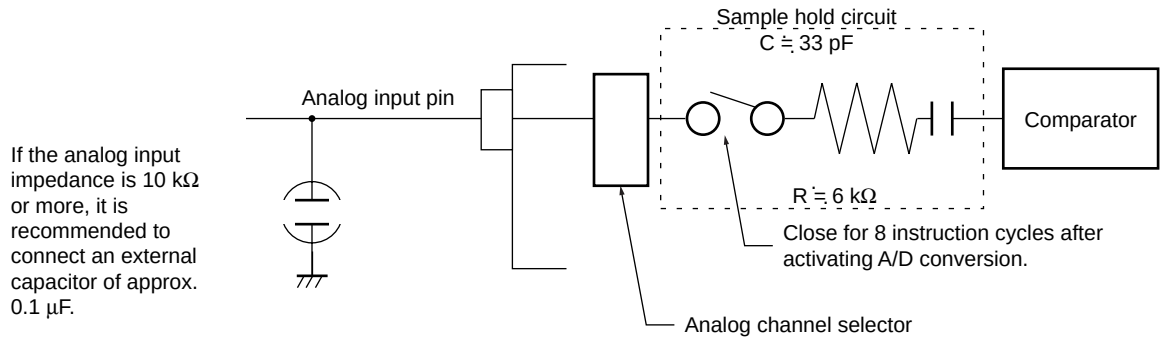
## 5. A/D Converter Electrical Characteristics

($V_{CC}$ = 5.0 V±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $F_{CH}$ = 8 MHz, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Resolution | — | — | — | — | — | 8 | bit | |
| Total error | — | — | — | — | — | ±3.0 | LSB | |
| Linearity error | — | — | — | — | — | ±1.0 | LSB | |
| Differential linearity error | — | — | — | — | — | ±0.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | — | $AV_{SS}$ – 1.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 2.5 LSB | mV | |
| Full-scale transition voltage | $V_{FST}$ | AN0 to AN7 | — | AVR – 3.5 LSB | AVR – 1.5 LSB | AVR + 0.5 LSB | mV | |
| Interchannel disparity | — | — | — | — | — | 1.0 | LSB | |
| A/D conversion time | — | — | — | — | 44 $t_{inst}$ | — | µs | |
| Sense mode conversion time | — | — | — | — | 12 $t_{inst}$ | — | µs | |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | AVR = $V_{CC}$ = 5.0 V | — | — | 10 | µA | |
| Analog input voltage | — | AN0 to AN7 | — | 0 | — | AVR | V | |
| Reference voltage | — | AVR | — | 4.5 | — | $V_{CC}$ | V | |
| Reference-voltage supply current | $I_R$ | AVR | AVR = 5.0 V | — | 200 | — | µA | |

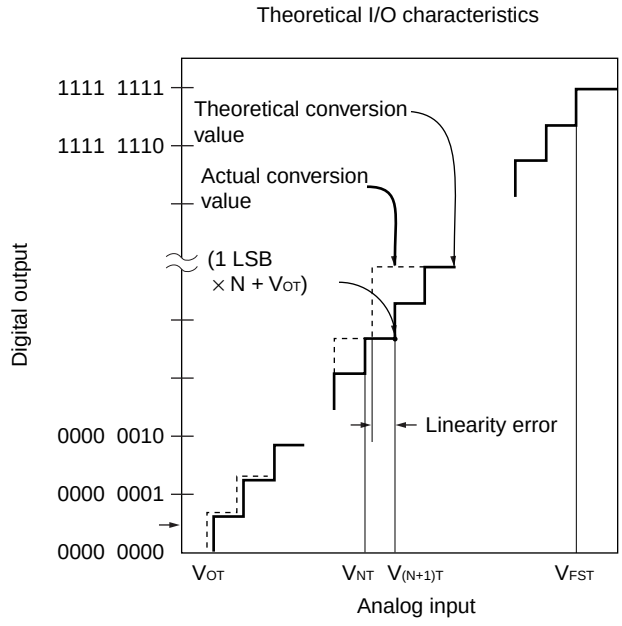
Notes:
- The smaller the | AVR – $AV_{SS}$ |, the greater the error would become relatively.
- The output impedance of the external circuit for the analog input must satisfy the following conditions:
  Output impedance of the external circuit < Approx. 10 kΩ
  If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 22 µs at 8 MHz oscillation).

**Analog Input Equivalent Circuit**



## 6. A/D Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
- Linearity error
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error
  The difference between actual and theoretical value
  This error is caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise.




$$1\ \text{LSB} = \frac{\text{AVR}}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1\ \text{LSB} \times N + 0.5\ \text{LSB})}{1\ \text{LSB}}$$

## ■ MASK OPTIONS

| No. | Part number / Parameter | MB89143A/144A | MB89PV140 | | MB89P147V1 |
|---|---|---|---|---|---|
| | Specification method | Specify when ordering masking | 101 | 102 | Set in EPROM |
| 1 | Clock mode selection<br>Single-clock mode<br>Dual-clock mode | Can be set | Single clock | Dual clock | Can be set |
| 2 | Pull-up resistors<br>P14 to P17,<br>P32 to P37 | Specify by pin | Without pull-up resistor | Without pull-up resistor | Can be set per pin |
| 3 | Power-on reset<br>With<br>Without | With power-on rest | With power-on reset | With power-on reset | Can be set |
| 4 | Reset output<br>With<br>Without | Can be set | With reset output | With reset output | Can be set |
| 5 | Pull-down resistors<br>P40 to P47<br>P50 to P57<br>P60 to P67 | Without pull-down resistor | Without pull-down resistor | Without pull-down resistor | Without pull-down resistor |

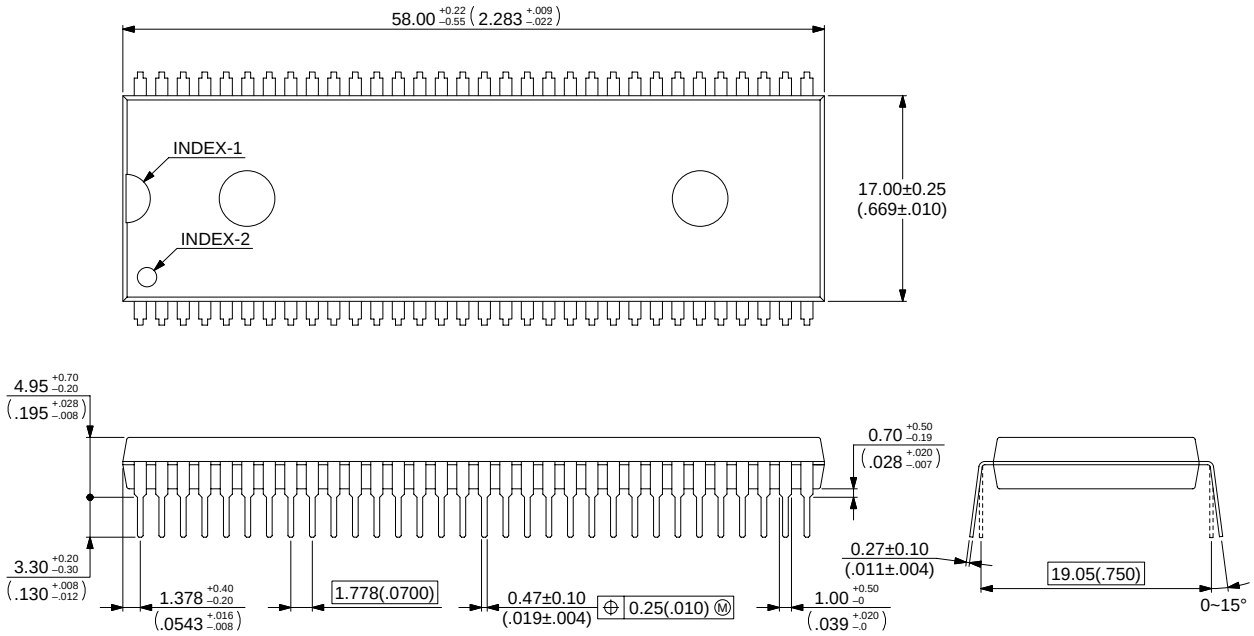
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB89143AP-SH<br>MB89144AP-SH<br>MB89P147V1P-SH | 64-pin Plastic SH-DIP<br>(DIP-64P-M01) | |

## ■ PACKAGE DIMENSION

64-pin Plastic SH-DIP
(DIP-64P-M01)

Note: Pins width and pins thickness include plating thickness.




Dimensions in mm (inches)

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