FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12543-2E

8-bit Proprietary Microcontrollers

CMOS

F²MC-8L MB89580B/580BW Series

MB89583B/585B/589B/P585B/P589B/ MB89583BW/585BW/P585BW

■ DESCRIPTION

The MB89580B/BW series is a line of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, these microcontrollers contain a variety of peripheral functions, such as PLL clock control, timers, a serial interface, a PWM timer, and the USB function. In particular, these microcontrollers contain one USB function channel to support both high and low speeds.

■ FEATURES

- **Package type**
  64-pin LQFP package (0.5 mm pitch) and 64-pin QFP package (0.65 mm pitch)

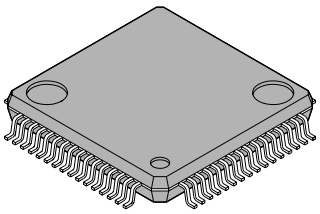
- **High-speed operations at low voltage**
  Minimum execution time : 0.33 µs (Automatically generates a 12 MHz main clock and a 48 MHz USB interface synchronization clock with an externally supplied 6 MHz clock and the internal PLL circuit.)

- **F²MC-8L CPU core**
  Instruction set that is optimum to the controllers
  -Multiplication and division instructions
  -16-bit arithmetic operations
  -branch instructions by bit testing
  -bit manipulation instructions, etc.

(Continued)

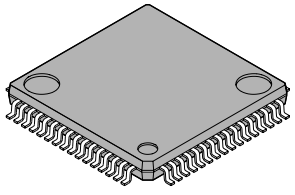
■ PACKAGE

64-pin plastic LQFP



(FPT-64P-M03)

64-pin plastic QFP



(FPT-64P-M09)

(Continued)

- **PLL clock control**
  The internal PLL clock circuit allows the use of low-speed clocks which are advantageous to noise characteristics.
  (6 MHz externally-supplied clock : Internal system clock oscillated at 12 MHz)

- **Various timers**
  8-bit PWM timer (can be used as either 8-bit PWM timer × 2 channels or PPG timer × 1 channel)
  Internal 21-bit timebase timer

- **Internal USB transceiver circuit** (**Compatible with high and low speeds**)

- **USB function**
  Compliant to USB Protocol Revision 1.0
  Support for both low and full speeds (selectable)
  Allows four endpoints to be specified at maximum.
  Types of transfer supported : control/interrupt/bulk/isochronous
  Built-in DMAC (Maps the buffer for each endpoint on to the internal RAM to directly access the memory for function's send and receive data.)

- **UART/serial interface**
  Built-in UART/SIO function (selectable by switching)

- **External interrupt**
  External interrupt (level detection × 8 channels)
  Eight inputs are independent of one another and can also be used for resetting from low-power consumption mode (the L-level detection feature available) .

- **Low power consumption** (**standby mode supported**)
  Stop mode (There is almost no current consumption since oscillation stops.)
  Sleep mode (This mode stops the running CPU.)

- **A maximum of 53 general-purpose I/O ports**
  General-purpose I/O ports (CMOS) : 34
  General-purpose output ports (CMOS) : 8
  General-purpose I/O ports (Nch open drain) : 3
  General-purpose input ports (CMOS 3.3 V input-compatible) : 8

- **Parallel ports**
  Also serve as eight of the general-purpose I/O ports (CMOS)
  Interrupt function available
  Allows asynchronous read and write by external signals

- **Power supply**
  Supply voltage : 3.0 to 5.5 V

■ PRODUCT LINEUP

Parameter \ Part number	MB89583B	MB89585B	MB89P585B	MB89589B	MB89P589B	MB89583BW	MB89585BW	MB89P585BW
ROM size	8 KB	16 KB				8 KB	16 KB	
RAM size	512 B	1 KB		18 KB		512 B	1 KB	
Package	LQFP-64 (FPT-64P-M03)			QFP-64 (FPT-64P-M09)		LQFP-64 (FPT-64P-M03)		
Operation at USB reset	High impedance state					Low-level output		
Others	MASK product		OTP/EVA product	MASK product	OTP/EVA product	MASK product		OTP/EVA product
CPU functions	Number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum execution time : 0. 33 µs (6 MHz) Interrupt processing time : 3 µs (6 MHz)							
Peripheral functions: General-purpose ports	General-purpose I/O ports (34 : CMOS, 3 : Nch open drain) General-purpose output ports (8 : CMOS) General-purpose input ports (8 : CMOS 3.3 V input)							
Peripheral functions: Parallel ports	Shares eight (P40 through P47) of the above general-purpose I/O ports. Allows asynchronous read and write by external signals. An interrupt function is available to set data.							
Peripheral functions: USB function	Can be set to full/low speed. Four endpoints at maximum Power supply mode : Can be set to own power supply/bus power supply mode. FIFO 8 bits × 8 built in Built-in DMAC (Can be set to DMA transfer to the internal RAM or to the external FIFO.)							
Peripheral functions: PWM timer	8-bit PWM timer operation × 2 channels (can also be used as a PPG × 1 channel timer)							
Peripheral functions: UART SIO	Allows switching between UART (clock-synchronous/asynchronous data transfer allowed) and SIO (simple serial transfer) .							
Peripheral functions: Timebase timer	21-bit timebase timer							
Peripheral functions: Clock output	Allows output of two main clock divisions							
Standby mode	Sleep mode and Stop mode							

■ PACKAGES AND CORRESPONDING PRODUCTS

Package	MB89583B	MB89585B	MB89P585B	MB89589B	MB89P589B	MB89583BW	MB89585BW	MB89P585BW
FPT-64P-M03	○	○	○	×	×	○	○	○
FPT-64P-M09	×	×	×	○	○	×	×	×

○ : Available × : Not available

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the OTP product, verify its differences from the product that will actually be used.

2. Current Consumption

When operated at low speeds, a product mounted with either one-time PROM or EPROM consumes more current than a product mounted with a mask ROM. However, in sleep/stop mode the current consumption is the same.

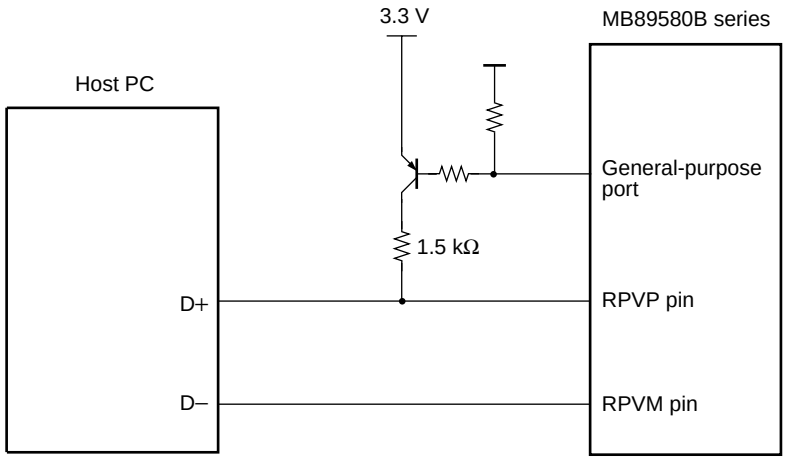
For detailed information on each package, see "■ PACKAGE DIMENSIONS."

3. Differences Between the MB89580B series and the MB89580BW Series

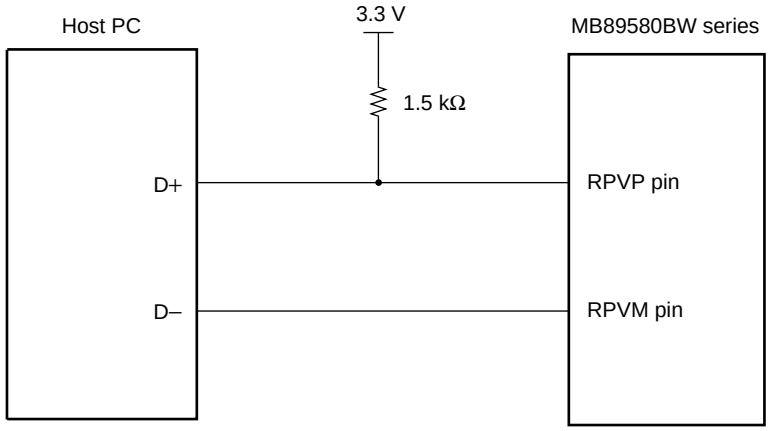
MB89580B series : Remains in high impedance state until USB connection takes place. Before the USB connection, use one general-purpose port output to control pullup resistance connection of this port by software.

MB89580BW : Outputs at low level until USB connection takes place.

- Example MB89580B product connection



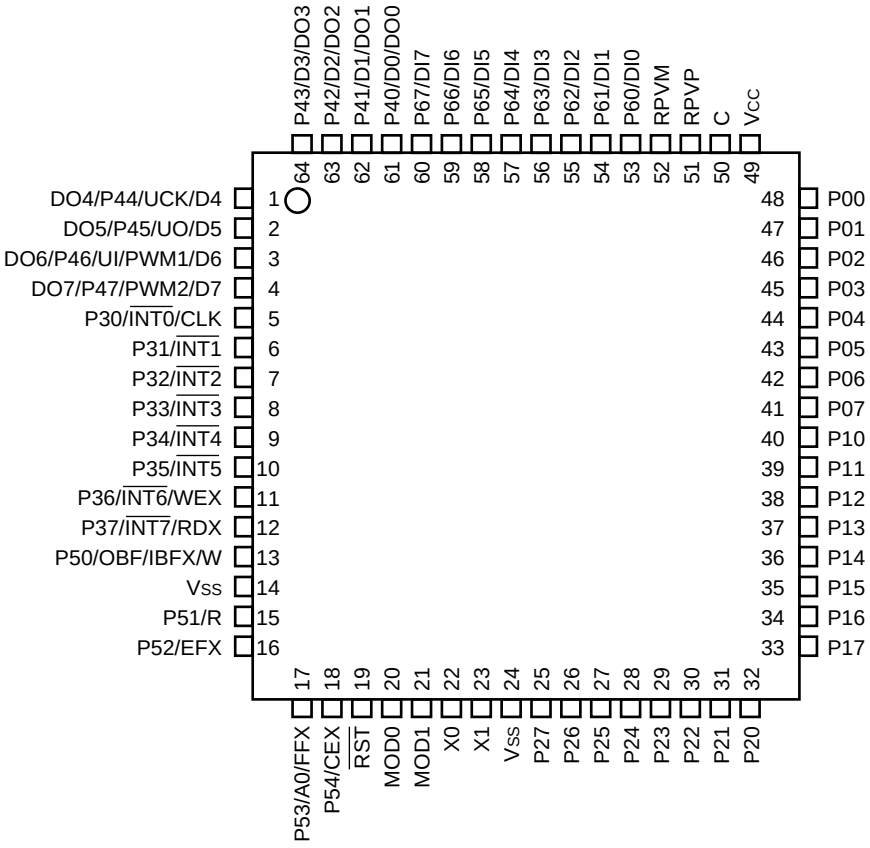
- Example MB89580BW product connection



Note : Full speed is assumed in the above examples.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-64P-M03)
(FPT-64P-M09)

■ PIN DESCRIPTION

Pin No.	Pin name	Circuit type	Function
1	P44/UCK/D4/DO4	E	General-purpose CMOS I/O pin UART/S10 clock I/O This pin also serves as a parallel interface/external FIFO data output pin.
2	P45/UO/D5/DO5	B	General-purpose CMOS I/O pin UART/S10 serial data output This pin also serves as a parallel interface/external FIFO data output pin.
3	P46/UI/PWM1/D6/DO6	E	General-purpose CMOS I/O pin UART/S10 serial data input PWM timer This pin also serves as a parallel interface/external FIFO data output pin.
4	P47/PWM2/D7/DO7	B	General-purpose CMOS I/O pin PWM timer This pin also serves as a parallel interface/external FIFO data output pin.
5	P30/$\overline{\text{INT0}}$/CLK	E	General-purpose CMOS I/O pin Clock output pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
6	P31/$\overline{\text{INT1}}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
7	P32/$\overline{\text{INT2}}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
8	P33/$\overline{\text{INT3}}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
9	P34/$\overline{\text{INT4}}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
10	P35/$\overline{\text{INT5}}$	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection)
11	P36/$\overline{\text{INT6}}$/WEX	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection) This pin also serves as the parallel interface write strobe input pin.
12	P37/$\overline{\text{INT7}}$/RDX	E	General-purpose CMOS I/O pin This pin also serves as an external interrupt input pin. The external interrupt input is a hysteresis input. (Level detection) This pin also serves as the parallel interface read strobe input pin.
13	P50/OBF/IBFX/W	B	General-purpose CMOS I/O pin Interrupt output to the parallel interface host. This pin also serves the OUT FIFO data strobe pin.

(Continued)

Pin No.	Pin name	Circuit type	Function
14	V_{SS}	—	Power supply pin (GND)
15	P51/R	B	General-purpose CMOS I/O pin. This pin also serves the IN FIFO data strobe pin.
16	P52/EFX	K	General-purpose Nch open drain I/O pin. This pin also serves as the IN FIFO data enable input pin.
17	P53/A0/FFX	K	General-purpose Nch open drain I/O pin. Parallel interface's data select input This pin also serves as the OUT FIFO data enable input pin.
18	P54/CEX	K	General-purpose Nch open drain I/O pin. This pin also serves as the parallel interface device select input pin.
19	$\overline{RST}$	I	Reset pin. (Reset on the negative logic low level.)
20	MOD0	F	An operating mode designation pin. Connect directly to Vss.
21	MOD1	F	An operating mode designation pin. Connect directly to Vss.
22	X0	A	Pins for the crystal oscillator (6 MHz)
23	X1		
24	V_{SS}	—	Power supply pin (GND)
25	P27	B	General-purpose CMOS output pin
26	P26	B	General-purpose CMOS output pin
27	P25	B	General-purpose CMOS output pin
28	P24	B	General-purpose CMOS output pin
29	P23	B	General-purpose CMOS output pin
30	P22	B	General-purpose CMOS output pin
31	P21	B	General-purpose CMOS output pin
32	P20	B	General-purpose CMOS output pin
33	P17	B	General-purpose CMOS I/O pin
34	P16	B	General-purpose CMOS I/O pin
35	P15	B	General-purpose CMOS I/O pin
36	P14	B	General-purpose CMOS I/O pin
37	P13	B	General-purpose CMOS I/O pin
38	P12	B	General-purpose CMOS I/O pin
39	P11	B	General-purpose CMOS I/O pin
40	P10	B	General-purpose CMOS I/O pin
41	P07	B	General-purpose CMOS I/O pin
42	P06	B	General-purpose CMOS I/O pin
43	P05	B	General-purpose CMOS I/O pin
44	P04	B	General-purpose CMOS I/O pin

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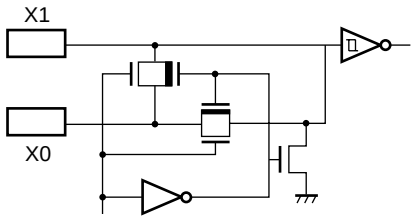
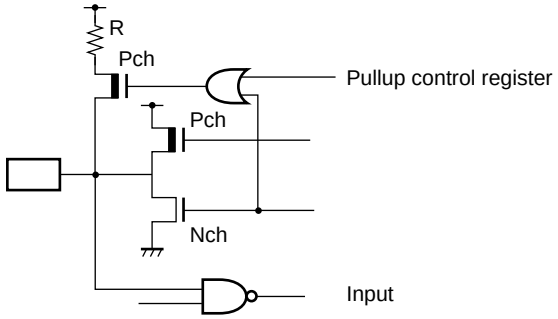
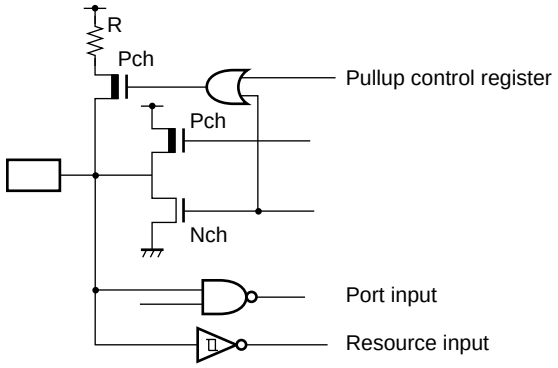
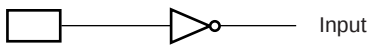
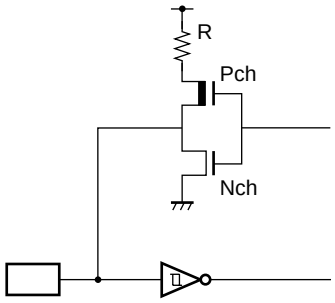
Pin No.	Pin name	Circuit type	Function
45	P03	B	General-purpose CMOS I/O pin
46	P02	B	General-purpose CMOS I/O pin
47	P01	B	General-purpose CMOS I/O pin
48	P00	B	General-purpose CMOS I/O pin
49	V_{CC}	—	Power supply pin
50	C	—	Connect an external capacitor of 0.1 μF. When using with 3.3 V power supply, connect this pin with the Vcc pin to set to 3.3 V input.
51	RPVP	USBDRV	USB route port + pin
52	RPVM	USBDRV	USB router port – pin
53	P60/DI0	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin. (LSB)
54	P61/DI1	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
55	P62/DI2	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
56	P63/DI3	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
57	P64/DI4	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
58	P65/DI5	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
59	P66/DI6	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin.
60	P67/DI7	F	General-purpose CMOS input pin (3.3 V input) This pin also serves as an external FIFO data input pin. (MSB)
61	P40/D0/DO0	B	General-purpose CMOS I/O pin This pin serves as a parallel interface/external FIFO data output pin.
62	P41/D1/DO1	B	General-purpose CMOS I/O pin This pin serves as a parallel interface/external FIFO data output pin.
63	P42/D2/DO2	B	General-purpose CMOS I/O pin This pin serves as a parallel interface/external FIFO data output pin.
64	P43/D3/DO3	B	General-purpose CMOS I/O pin This pin serves as a parallel interface/external FIFO data output pin.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation feedback resistance Approx. 1 MΩ
B		CMOS I/O
E		CMOS I/O Hysteresis input
F		CMOS input
I		Hysteresis I/O Pullup resistance

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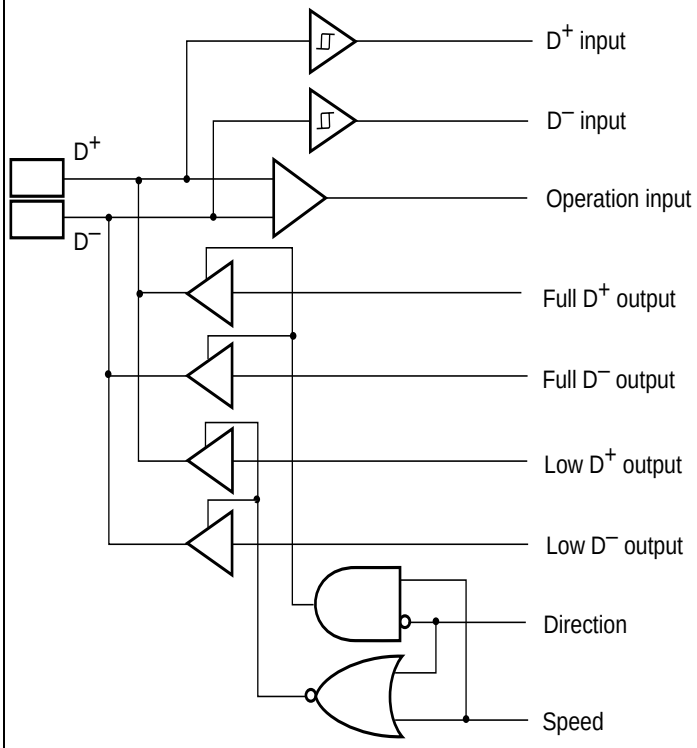
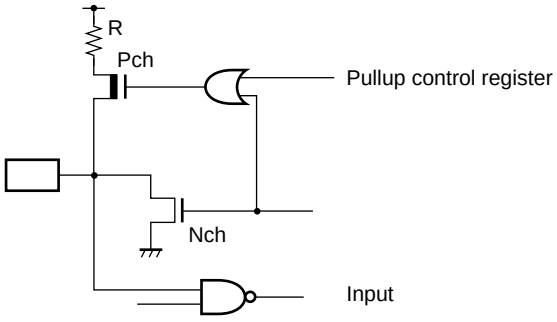
Type	Circuit	Remarks
USBDRV		USB I/O
K		Nch open drain I/O

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than Vcc or lower than Vss is applied to input or output pins other than the medium- and high-voltage pins or if voltage higher than the rating is applied between Vcc and Vss.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also take care to prevent the analog input from exceeding the digital power supply (Vcc) when the power supply to the analog power system is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions and latchup leading to permanent damage to the pins. These unused pins should be connected to a pullup or pulldown resistance of at least 2 kΩ between the pin and the power supply.

Unused I/O pins should be placed in output state to leave it open or pins that are in input state should be handled the same as unused input pins.

3. Power Supply Voltage Fluctuations

Although Vcc power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that Vcc ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

■ ONE-TIME PROM AND EPROM MICROCONTROLLER PROGRAMMING SPECIFICATIONS

PROM mode is available on the MB89P585B/BW microcontrollers. The use of a dedicated adapter allows you to program the devices with a general-purpose ROM programmer. However, keep in mind that electronic signature mode is not available.

1. ROM programmer adapter and its compatible programmers

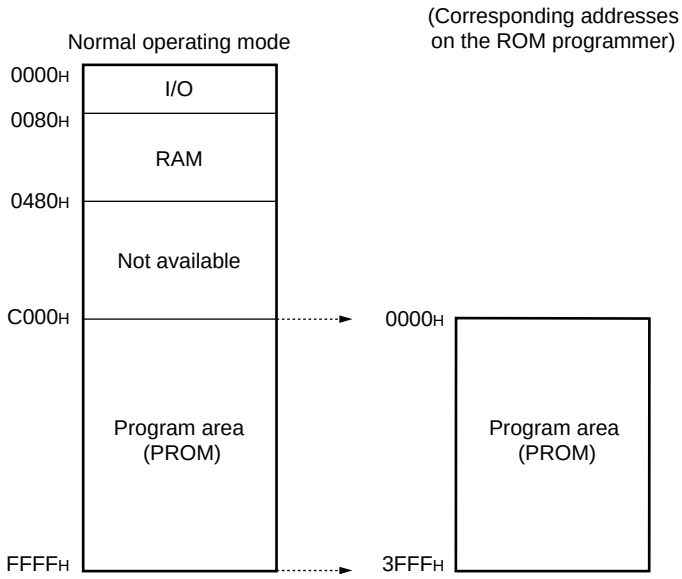
Package	Compatible adapter	Compatible programmers and models
	Sun Hayato Co, Ltd.	Ando Denki K. K.
FTP-64P-M03	ROM2-64LQF-32DP-8LA	AF9708 (Version 1.40 or higher) AF9709 (Version 1.40 or higher) AF9723 (Version 1.50 or higher)

Inquiry:

Sun Hayato Co., Ltd. : TEL. 81-3-3986-0403

Ando Denki K. K. : TEL. 81-3-3733-1160

2. Memory map in PROM mode



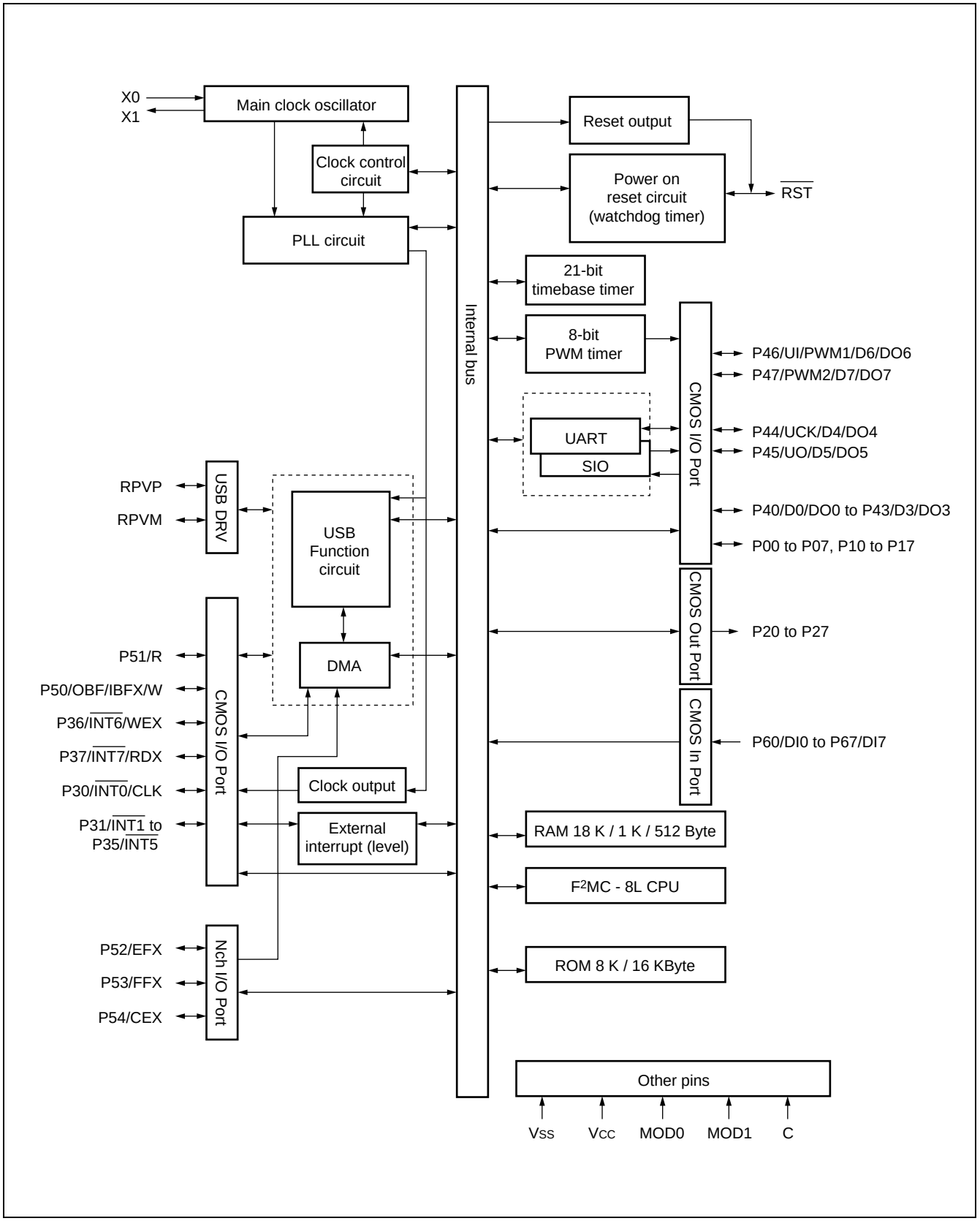
3. Programming the EPROM (Using the Ando Denki K.K. programmer)

(1) Set the EPROM programmer type code to 17209.

(2) Load program data on to the EPROM programmer at 0000_H to $3FFF_H$.

(3) Program $C000_H$ to $FFFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM



■ CPU CORE

1. Memory Space

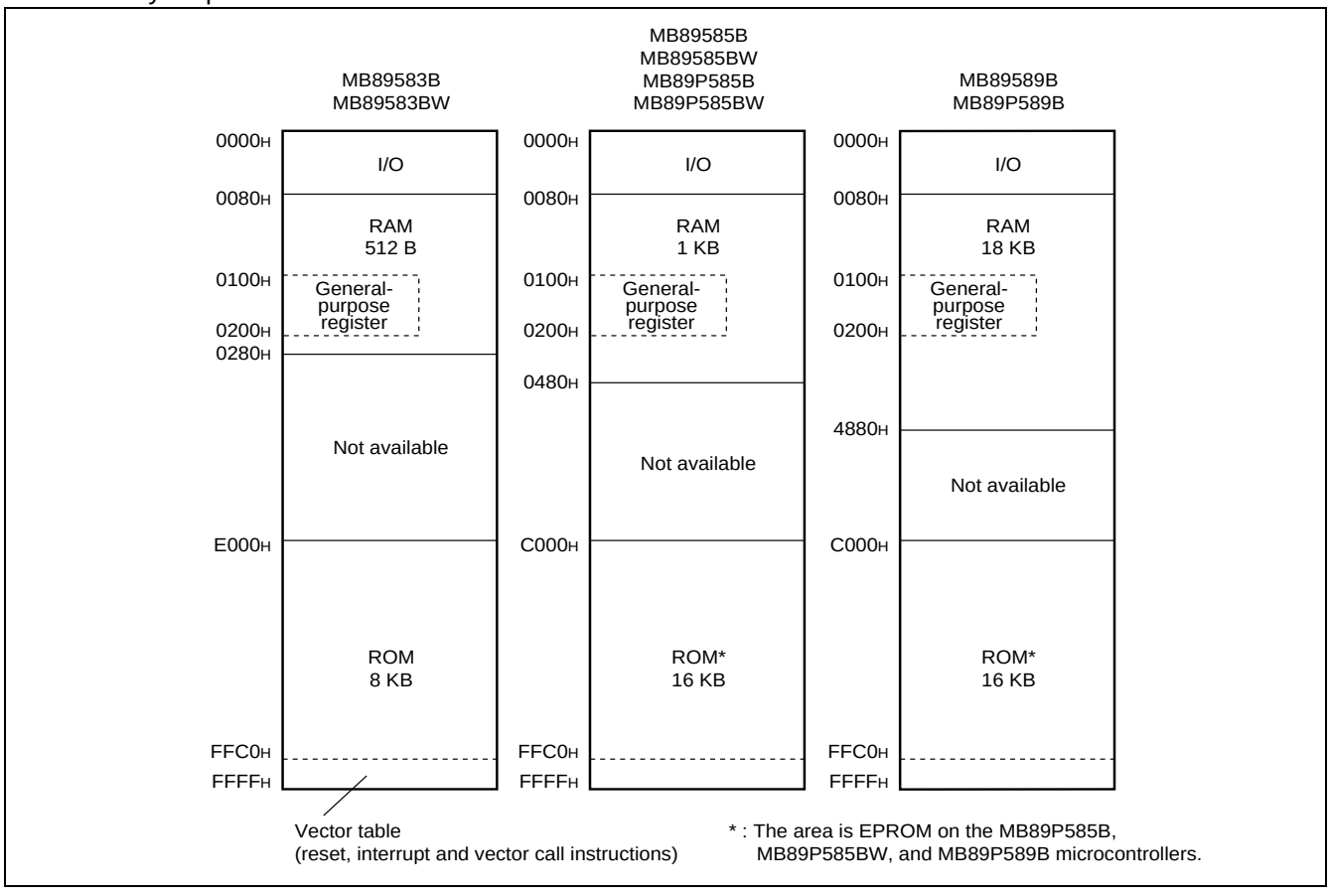
The MB89580B/BW microcontrollers offer a memory space of 64 Kbytes consisting of the I/O, RAM and ROM areas. The memory space contains areas that are used for specific purposes, such as a general-purpose register and a vector table.

- I/O area (addresses : 0000_H through $007F_H$)
  This area is assigned with the control and data registers, for example, of peripheral functions to be built in. The I/O area is as accessible as the memory since the area is assigned to a part of the memory space. Direct addressing also allows the area to be accessed faster.

- RAM area
  As an internal data area, a static RAM is built in.
  The internal RAM capacity varies with the product type.
  The area 80_H to FF_H can be accessed at high speed with direct addressing.
  The area 100_H to $1FF_H$ can be used a general-purpose register area. (The usable area is limited depending on the product.)
  When reset, RAM data becomes undefined.

- ROM area
  As an internal program area, a ROM is built in.
  The internal ROM capacity varies with the product type.
  The area $FFCO_H$ to $FFFF_H$ should be used for a vector table, for example.

- Memory map

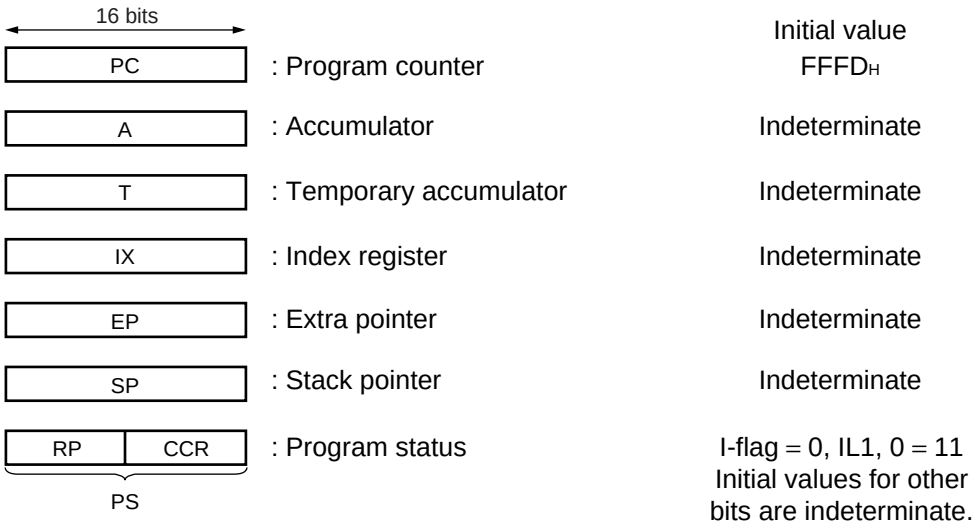


2. Registers

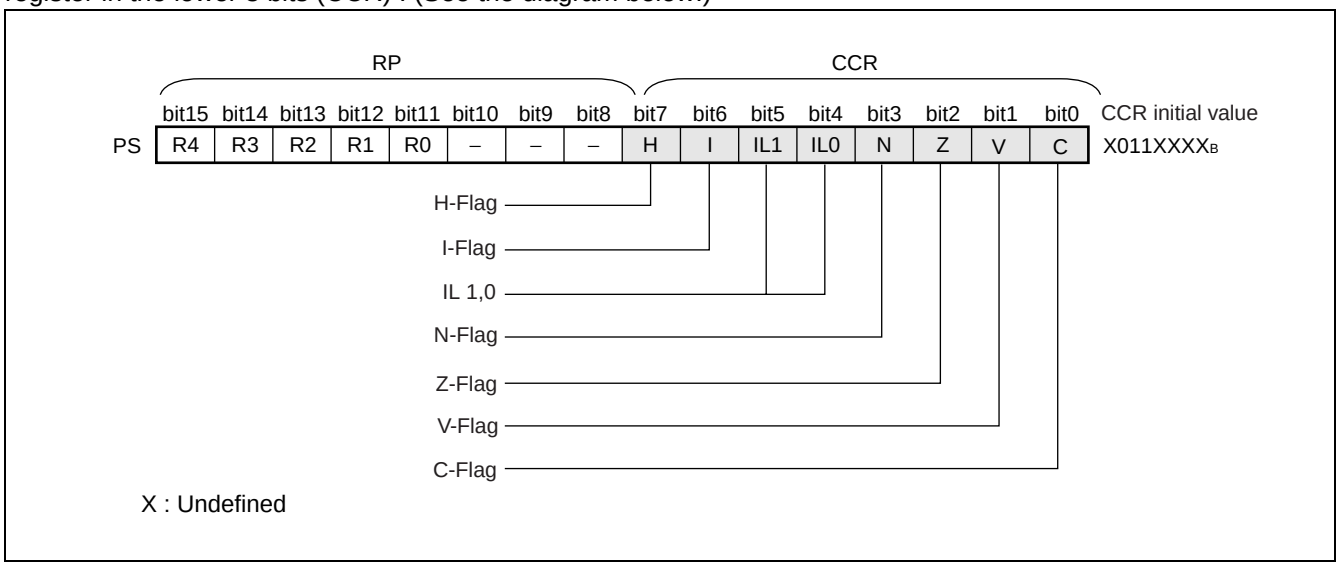
The MB89580B/BW series has two types of registers; the registers dedicated to specific purposes in the CPU and the general-purpose registers.

The dedicated registers are as follows:

Program counter (PC)	:	A 16-bit register to indicate locations where instructions are stored.
Accumulator (A)	:	A 16-bit register for temporary storage of operations. In the case of an 8-bit data processing instruction, the lower one byte is used.
Temporary accumulator (T)	:	A 16-bit register which performs operations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used.
Index register (IX)	:	A 16-bit register for index modification.
Extra pointer (EP)	:	A 16-bit register to point to a memory address.
Stack pointer (SP)	:	A 16-bit register to indicate a stack area.
Program status (PS)	:	A 16-bit register to store a register pointer or a condition code.

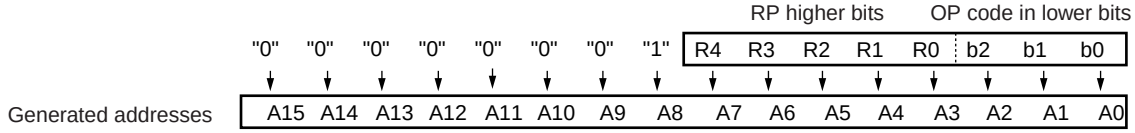


The PS register can further be divided into the register bank pointer in the higher 8 bits (RP) and the condition code register in the lower 8 bits (CCR) . (See the diagram below.)



The RP points to the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule shown next.

Rule for Conversion of Actual Addresses in the General-purpose Register Area



The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at the time of an interrupt.

- H flag : The flag is set to “1” when an arithmetic operation results in a carry from bit 3 to bit 4 or in a borrow from bit 4 to bit 3. The bit is cleared to “0” in other instances. The flag is for decimal adjustment instructions; do not use for other than additions and subtractions.
- I flag : Interrupt is enabled when this flag is set to “1.” Interrupt is disabled when this flag is set to “0.” The flag is set to “0” when reset.
- IL1, 0 : Indicates the level of the interrupt currently enabled. An interrupt is processed only if its level is higher than the value this bit indicates.

IL1	IL0	Interrupt level	High-low
0	0	1	Higher ↕ Lower = no interruption
0	1		
1	0	2	
1	1	3	

N flag : The flag is set to “1” when an arithmetic operation results in setting of the MSB to “1” or is cleared to “0” when the MSB is set to “1.”

Z flag : The flag is set to “1” when an arithmetic operation results in “0” or is set to “0” in other instances.

V flag : The flag is set to “1” when an arithmetic operation results in two’s complement overflow or is cleared to “0” if no overflow occurs.

C flag : The flag is set to “1” when an arithmetic operation results in a carry from bit 7 or in a borrow to bit 7. The flag is cleared to “0” if neither of them occurs. In the case of a shift instruction, the flag is set to the shift-out value.

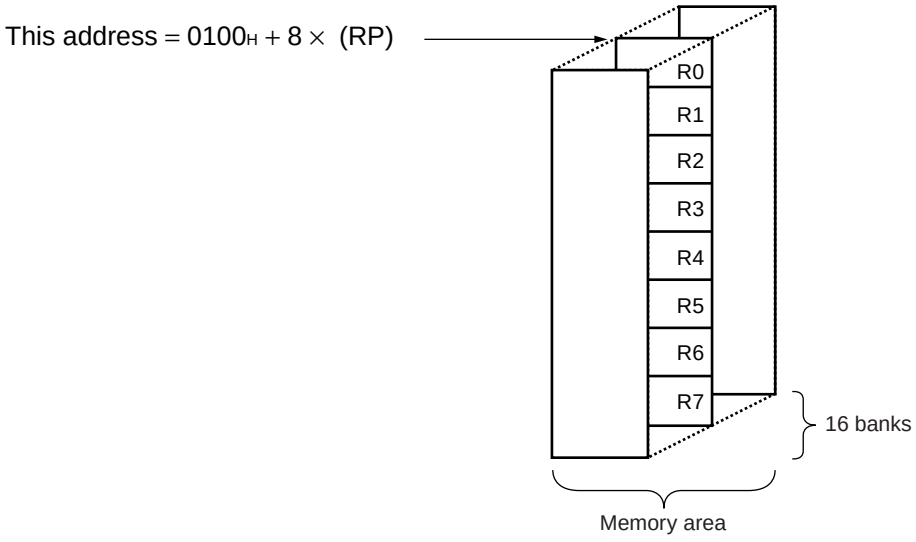
The following general-purpose registers are provided:

General-purpose registers : 8-bit data storage registers

The general-purpose registers are 8 bits in length and located in the register banks in the memory. One bank contains eight registers and the MB89580B/BW microcontrollers allow a total of 16 banks to be used at maximum.

The bank currently in use is indicated by the register bank pointer (RP) .

Register Bank Configuration



■ I/O MAP

Address	Register name	Register description	Read/write	Initial value
00H	PDR0	Port 0 data register	R/W	XXXXXXXX
01H	DDR0	Port 0 direction register	W	00000000
02H	PDR1	Port 1 data register	R/W	XXXXXXXX
03H	DDR1	Port 1 direction register	W	00000000
04H	PDR2	Port 2 data register	R/W	00000000
05H	Vacancy			
06H	Vacancy			
07H	SYCC	System clock control register	R/W	XXX11X00
08H	STBC	Standby control register	R/W	0001XXXX
09H	WDTC	Watchdog timer control register	R/W	0 XXXXXXX
0AH	TBTC	Timebase timer control register	R/W	00XXX000
0BH	Vacancy			
0CH	PDR3	Port 3 data register	R/W	XXXXXXXX
0DH	DDR3	Port 3 direction register	R/W	00000000
0EH	Vacancy			
0FH	Vacancy			
10H	PDR4	Port 4 data register	R/W	XXXXXXXX
11H	DDR4	Port 4 direction register	R/W	00000000
12H	PDR5	Port 5 data register	R/W	XXX11 1XX
13H	DDR5	Port 5 direction register	R/W	XXXXXX 00
14H	PDR6	Port 6 data register	R/W	XXXXXXXX
15H	PDCR	Parallel port data control register	R/W	XXX00000
16H to 20H	Vacancy			
21H	PURR0	Port 0 pullup option setting register	R/W	11111111
22H	PURR1	Port 1 pullup option setting register	R/W	11111111
23H	PURR2	Port 2 pullup option setting register	R/W	11111111
24H	PURR3	Port 3 pullup option setting register	R/W	11111111
25H	PURR4	Port 4 pullup option setting register	R/W	11111111
26H	PURR5	Port 5 pullup option setting register	R/W	XXX 11111
27H	CTR1	PWM control register 1	R/W	00000000
28H	CTR2	PWM control register 2	R/W	000X0000
29H	CTR3	PWM control register 3	R/W	X000XXXX
2AH	CMR1	PWM compare register 1	W	XXXXXXXX
2BH	CMR2	PWM compare register 2	W	XXXXXXXX

(Continued)

Address	Register name	Register description	Read/write	Initial value
2C$_H$	CKR	Clock output control register	R/W	XXXXXXX0
2D$_H$	SCS	Serial clock switching register	R/W	XXXXXXX0
2E$_H$	Vacancy			
2F$_H$	SMC1	Serial mode control register 1	R/W	00000000
30$_H$	SMC2	Serial mode control register 2	R/W	00000000
31$_H$	SSD	Serial status and control register	R	00001XXX
32$_H$	SIDR/SODR	Serial input/serial output data register	R/W	XXXXXXXX
33$_H$	SRC	Serial rate control register	R/W	XXXXXXXX
34$_H$ to 3B$_H$	Vacancy			
3C$_H$	EIE	External interrupt control register	R/W	00000000
3D$_H$	EIF	External interrupt flag register	R/W	XXXXXXX0
3E$_H$ to 3F$_H$	Vacancy			
40$_H$	DMDR	USB power supply mode register	R/W	XXXXXXX0
41$_H$ to 4E$_H$	Vacancy			
4F$_H$	DBARH	DMA base address register H	R/W	000000XX
50$_H$	UMDR	USB reset mode register	R/W	1000XX00
51$_H$	DBAR	DMA base address register	R/W	XXXXXXXX
52$_H$	TDCR0	Transfer data count register 0	R/W	X0000000
53$_H$	TDCR11	Transfer data count register 11	R/W	00000000
54$_H$	TDCR12	Transfer data count register 12	R/W	XXXXXX00
55$_H$	TDCR21	Transfer data count register 21	R/W	00000000
56$_H$	TDCR22	Transfer data count register 22	R/W	XXXXXX00
57$_H$	TDCR3	Transfer data count register 3	R/W	X0000000
58$_H$	UCTR	USB control register	R/W	00000000
59$_H$	USTR1	USB status register 1	R/W	00000000
5A$_H$	USTR2	USB status register 2	R	XXXXXX00
5B$_H$	UMSKR	USB interrupt mask register	R/W	00000000
5C$_H$	UFRMR1	USB frame status register 1	R	XXXXXXXX
5D$_H$	UFRMR2	USB frame status register 2	R	XXXXXXXX
5E$_H$	EPER	USB endpoint enable register	R/W	XXXX0001
5F$_H$	EPBR0	Endpoint 0 setup register	R/W	X0000000
60$_H$	EPBR11	Endpoint setup register 11	R/W	0X000000
61$_H$	EPBR12	Endpoint setup register 12	R/W	00000000

(Continued)

(Continued)

Address	Register name	Register description	Read/write	Initial value
62H	EPBR21	Endpoint setup register 21	R/W	0X000000
63H	EPBR22	Endpoint setup register 22	R/W	00000000
64H	EPBR31	Endpoint setup register 31	R/W	XX0000XX
65H	EPBR32	Endpoint setup register 32	R/W	X0000000
66H to 7BH	Vacancy			
7CH	ILR1	Interrupt level setting register 1	W	11111111
7DH	ILR2	Interrupt level setting register 2	W	11111111
7EH	ILR3	level setting register 3	W	11111111
7FH	Vacancy			

- Information about read/write
  R/W : Read/write enabled, R : Read only, W : Write only
- Information about initial values
  0 : The initial value of this bit is “0.” 1 : The initial bit of this bit is “1.” X : The initial value of this bit is undefined.

Note : Vacancies are not for use.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	Other than P60 to P67
		V_{SS} – 0.5	V_{SS} + 4.0	V	P60 to P67
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	ΣI_{OH}	—	–50	mA	
“H” level total average output current	ΣI_{OHAV}	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

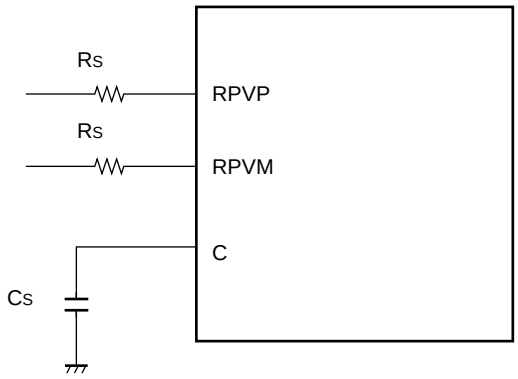
2. Recommended Operating Conditions

(V_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	3.0	—	5.5	V	
Operating temperature	T_A	–40	—	+85	°C	
Smoothing capacitor	C_S	0.1	—	1.0	µF	At Vcc = 5.0 V*
Series resistance	R_S	—	16	—	Ω	When the USB function is in use

* : Use either a ceramic capacitor or a capacitor with similar frequency characteristics. The capacity of the smoothing capacitor for the Vcc pin should be greater than that of the Cs. When using with a supply voltage of 3.3 V, connect pin C with Vcc to input 3.3 V.

- C, RPVP and RPVM Pin Connection Diagram



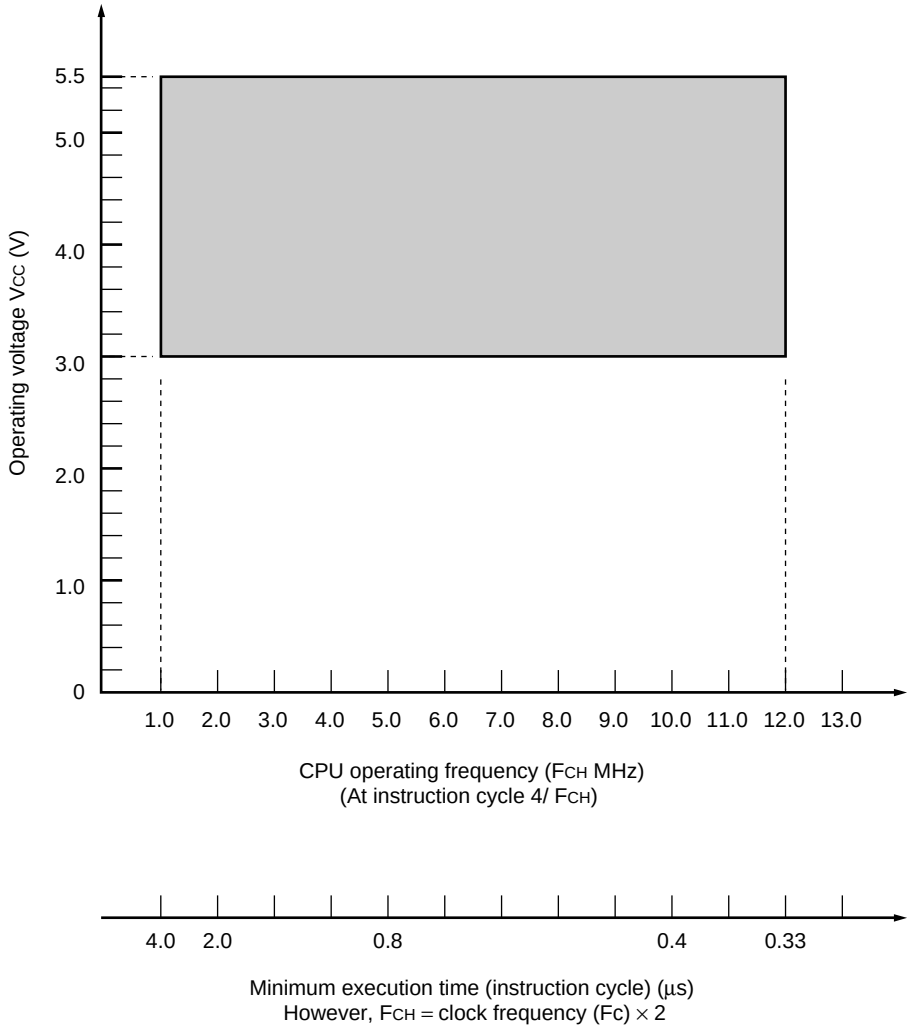


Figure 1 Operating voltage - operating frequency

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, MOD0, MOD1	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, $\overline{INT0}$ to $\overline{INT7}$, UCK, UI	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IH1}	P60 to P67	—	V_{SS} + 2.0	—	V_{SS} + 3.8	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, MOD0, MOD1	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, $\overline{INT0}$ to $\overline{INT7}$, UCK, UI	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{IL1}	P60 to P67	—	V_{SS} – 0.5	—	V_{SS} + 0.8	V	
Open-drain output application voltage	V_{D1}	P52 to P54	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50, P51	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50 to P54, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	

(Continued)

(Continued)

(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input leakage current (Hi-Z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50, P51, P60 to P67	$0.0 < V_I < V_{CC}$	–5	—	+5	µA	When no pullup resistance is specified
Open-drain output leakage current	I_{LIOD}	P52 to P54	$0.0 < V_I < V_{SS} + 5.5$	—	—	+5	µA	
Pullup resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	$\overline{RST}$ is excluded when pullup resistance available is specified.
Power supply current	I_{CC}	V_{CC}	F_{CH} = 12.0 MHz, V_{CC} = 5.0 V, t_{inst} = 0.333 µs	—	25	38	mA	MB89P585B/BW, MB89585B/BW, MB89583B/BW MB89P589B, MB89589B
	I_{CCS1}		F_{CH} = 12.0 MHz, V_{CC} = 5.0 V, t_{inst} = 0.333 µs	—	20	30	mA	Sleep mode
	I_{CCH}		T_A = 25 °C	—	5	20	µA	Stop
Input capacitance	C_{IN}	Other than Vcc and Vss	f = 1 MHz	—	10	—	pF	

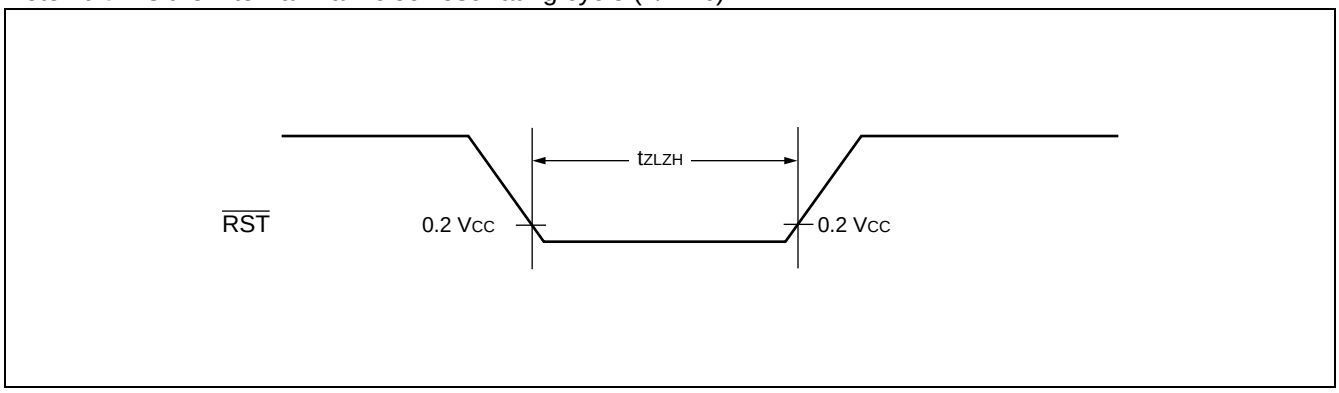
4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{HCLY}	—	ns	

Note : t_{HCYL} is the internal main clock oscillating cycle (1/2 Fc) .

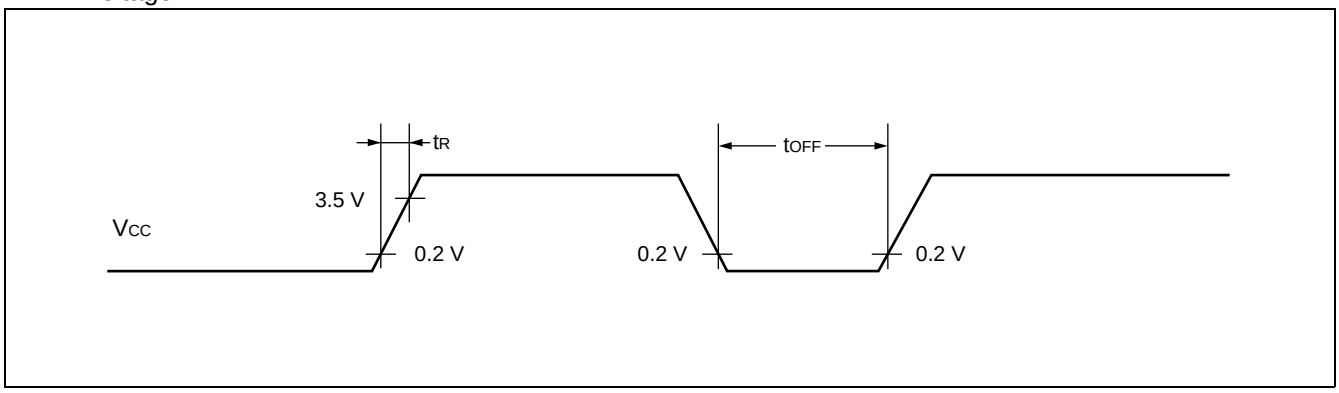


(2) Power-on Reset and Power On Time

(V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	0.066	50	ms	
Power supply cutoff time	t_{OFF}	—	4	—	ns	Due to repeated operations

Note : The power supply must be up within the selected oscillation stabilization time.
When the supply voltage needs to be varied while operating, it is recommended to smoothly start up the voltage.

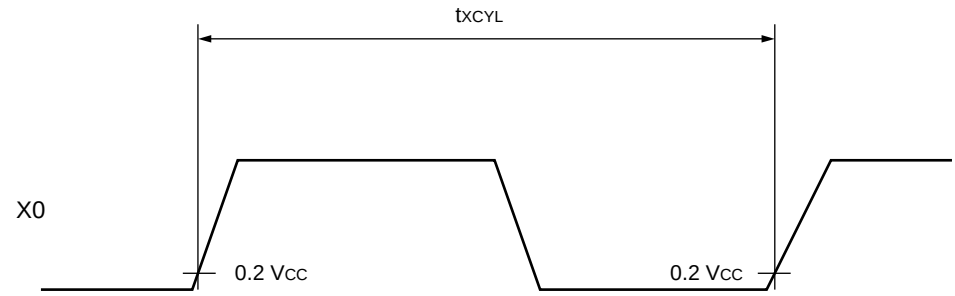


(3) Clock Timing

(V_{SS} = 0 V, T_A = –40 °C to +85 °C)

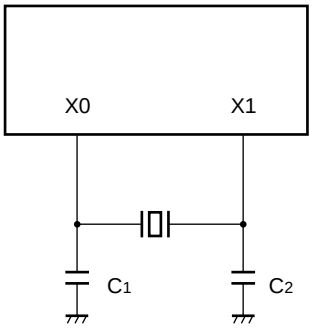
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_C	X0, X1	—	—	6	—	MHz	
Clock cycle time	t_{XCYL}	X0, X1		—	166.6	—	ns	
Internal main clock frequency	F_{CH}	—		—	12	—	MHz	Twice the Fc
Internal clock cycle	t_{HCYL}	—		—	83.3	—	ns	t_{XCYL}/2

- X0 and X1 Timing and Conditions



- Clock Conditions

When a crystal resonator is used



(4) Instruction Cycle

(V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (Min. execution time)	t_{inst}	4 / F_{CH}, 8 / F_{CH}, 16 / F_{CH}, 64 / F_{CH}	µs	When operating at F_{CH} = 12 MHz t_{inst} = 0.33 µs (4 / F_{CH})

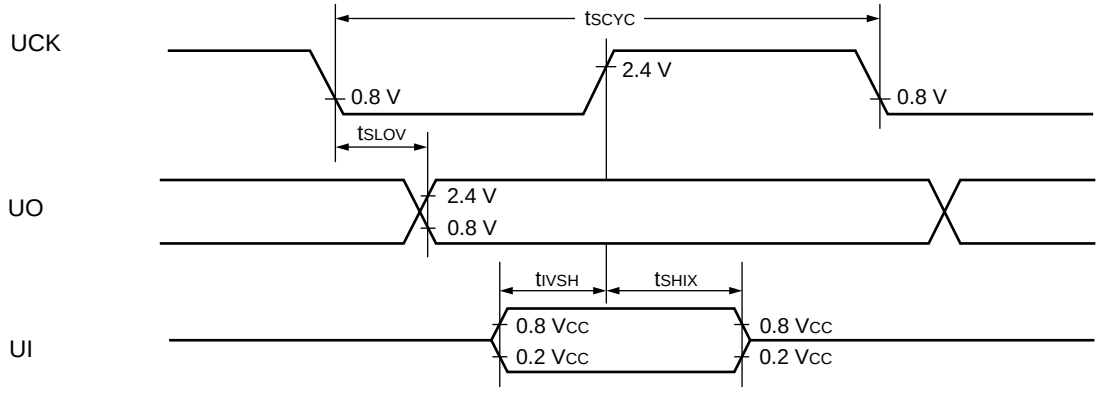
(5) UART Serial I/O Timing

(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

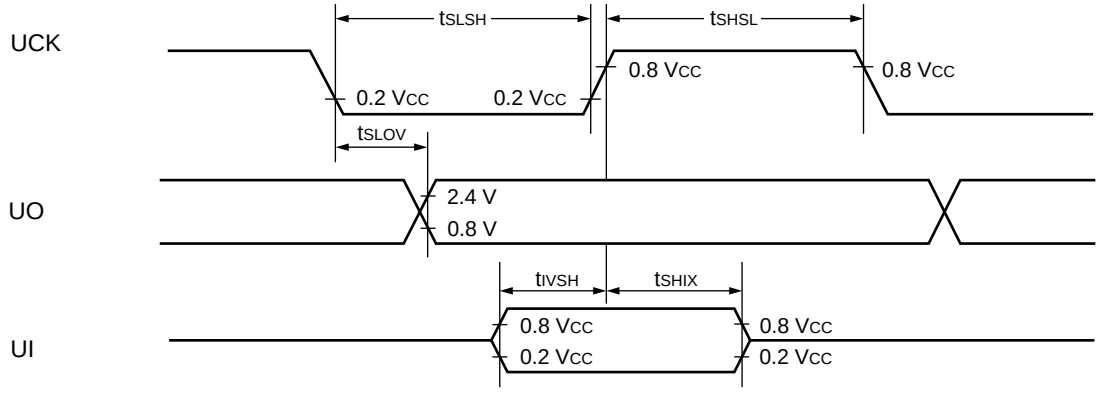
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	UCK	Internal shift clock mode	2 t_{inst}	—	µs	
UCK ↓ → UO	t_{SLOV}	UCK, UO		–200	200	ns	
Valid UI → UCK↑	t_{IVSH}	UI, UCK		200	—	ns	
UCK ↑ → valid UI hold time	t_{SHIX}	UCK, UI		200	—	ns	
Serial clock “H” pulse width	t_{SHSL}	UCK	External shift clock mode	1 t_{inst}	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}	—	µs	
UCK ↓ → UO time	t_{SLOV}	UCK, UO		0	200	ns	
Valid UI → UCK↑	t_{IVSH}	UI, UCK		200	—	ns	
UCK ↑ → valid UI hold time	t_{SHIX}	UCK, UI		200	—	ns	

* : For information about t_{inst}, see “Instruction Cycle.”

- Internal shift clock mode



- External shift clock mode

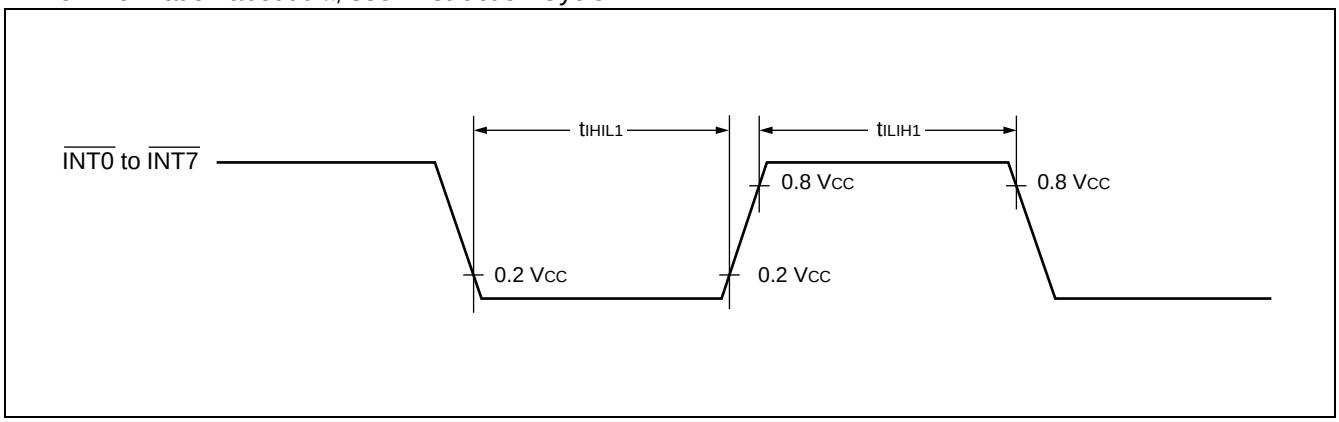


(6) Peripheral Input Timing

(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	$\overline{INT0}$ to $\overline{INT7}$	—	2 t_{inst}	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		—	2 t_{inst}	—	µs	

* : For information about t_{inst}, see “Instruction Cycle.”

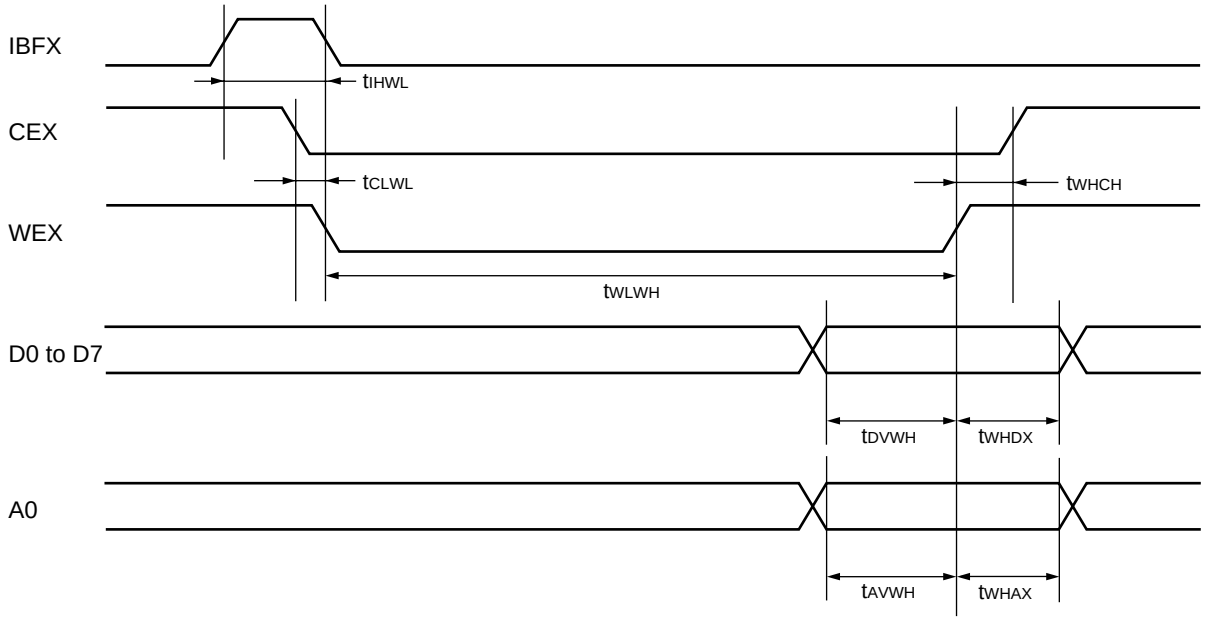


(7) Parallel Port Timing

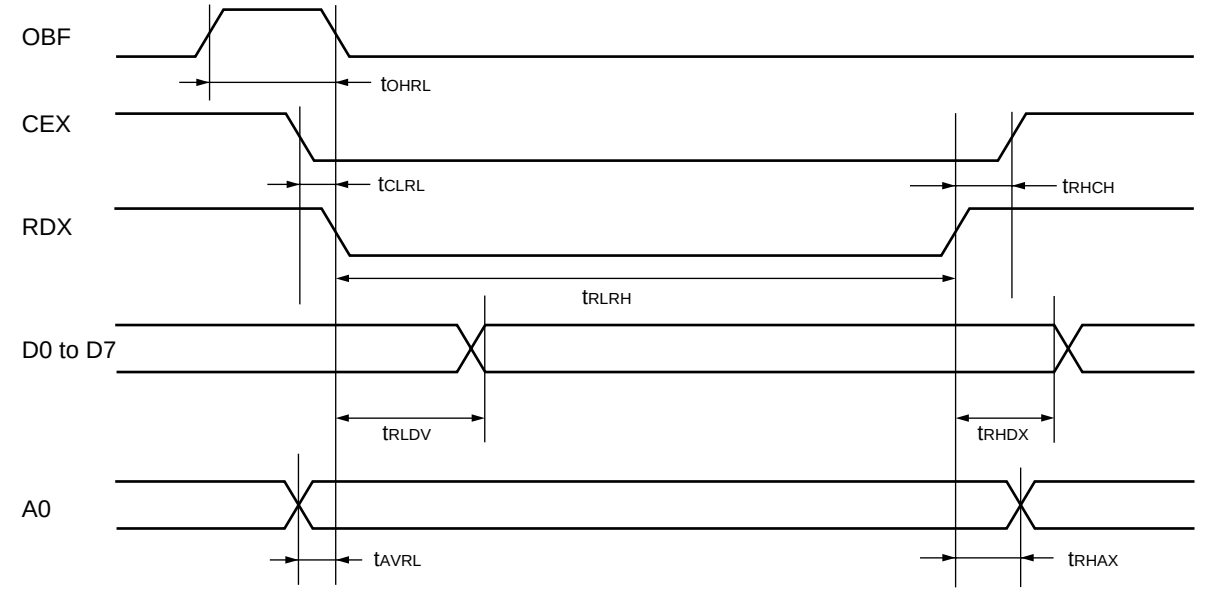
(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
IBFX ↑ → WEX ↓ timing	t_{IHWL}	IBFX WEX	—	1 / 2•t_{inst}	—	µs	
CEX ↓ → WEX ↓ delay	t_{CLWL}	CEX WEX	—	0	—	ns	
WEX ↑ → CEX ↑ delay	t_{WHCH}	CEX WEX	—	0	—	ns	
WEX pulse width	t_{WLWH}	WEX	—	40	—	ns	
Write data setup	t_{DVWH}	D0 to D7 WEX	—	10	—	ns	
Write data hold	t_{WHDX}	D0 to D7 WEX	—	10	—	ns	
Write address setup	t_{AVWH}	A0 WEX	—	10	—	ns	
Write address hold	t_{WHAX}	A0 WEX	—	10	—	ns	
OBF ↑ → RDX ↓ timing	t_{OHRL}	OBF RDX	—	1 / 2•t_{inst}	—	µs	
CEX ↓ → RDX ↓ delay	t_{CLRL}	CEX RDX	—	0	—	ns	
RDX ↑ → CEX ↑ delay	t_{RHCH}	CEX RDX	—	0	—	ns	
RDX pulse width	t_{RLRH}	RDX	—	40	—	ns	
Read data delay	t_{RLDV}	D0 to D7 RDX	—	—	15	ns	
Read data hold	t_{RHDX}	D0 to D7 RDX	—	0	—	ns	
Read address setup	t_{AVRL}	A0 RDX	—	10	—	ns	
Read address hold	t_{RHAX}	A0 RDX	—	10	—	ns	

- Write Timing



- Read Timing

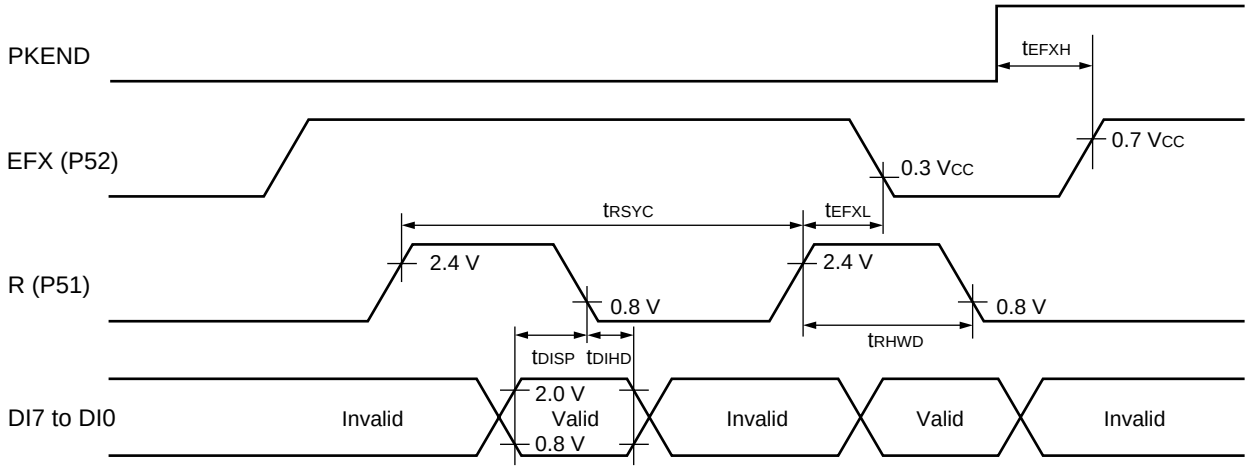


(8) External FIFO Connection Timing

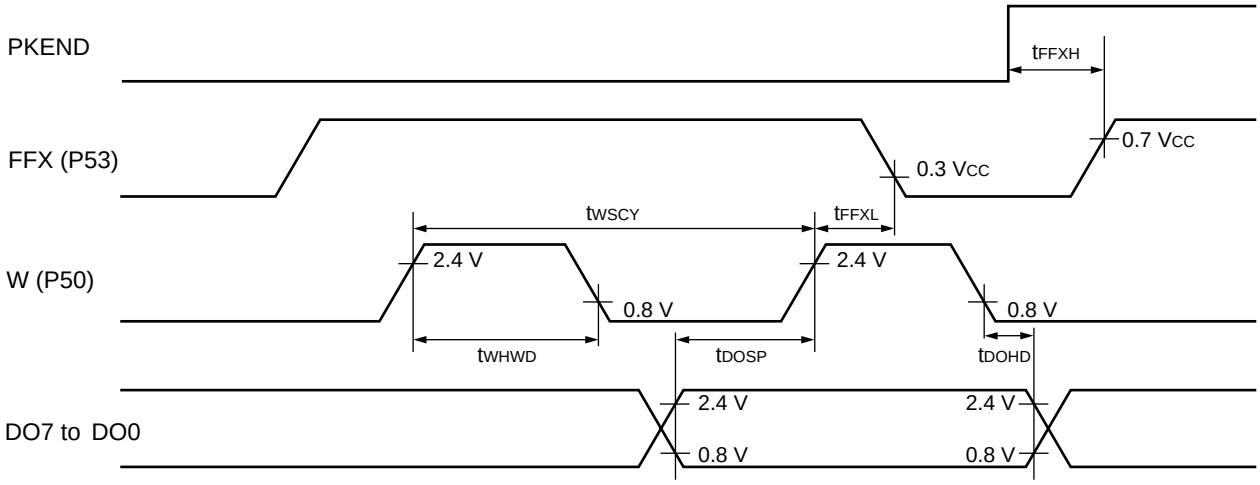
(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = –40 °C to +85 °C, F_C = 6 MHz)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
FIFO empty resetting timing	t_{EFXH}	EFX	Not including the initial resetting after reset	0	—	ns	Resetting before PKEND is not allowed.
FIFO empty timing	t_{EFXL}	EFX, R	—	0	360	ns	
Read cycle time	t_{RSCY}	R	—	645	—	ns	
Read clock “H” pulse width	t_{RHWD}		—	145	—	ns	
Valid DI → R ↓ setup time	t_{DISP}	DI7 to DI0, R	—	50	—	ns	
R ↓ → valid DI hold time	t_{DIHD}		—	0	—	ns	
FIFO full reset timing	t_{FFXH}	FFX	—	0	—	ns	Resetting before PKEND is not allowed.
FIFO full timing	t_{FFXL}	FFX, W	—	0	360	ns	
Write recycle time	t_{WSCY}	W	—	645	—	ns	
Write clock “H” pulse width	t_{WHWD}		—	145	—	ns	
Valid DO → W ↑ setup time	t_{DOSP}	DO7 to DO0, W	—	200		ns	
W ↓ → valid DO hold time	t_{DOHD}		—	40		ns	

• Read Data from External FIFO



• Write Data to External FIFO



■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:
- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:
- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

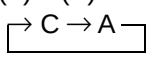
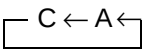
OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Note During byte transfer to A, T ← A is restricted to low bytes.
Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1		–	–	–	+ + – +	03
ROLC A	2	1		–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SPA	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8	/	XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

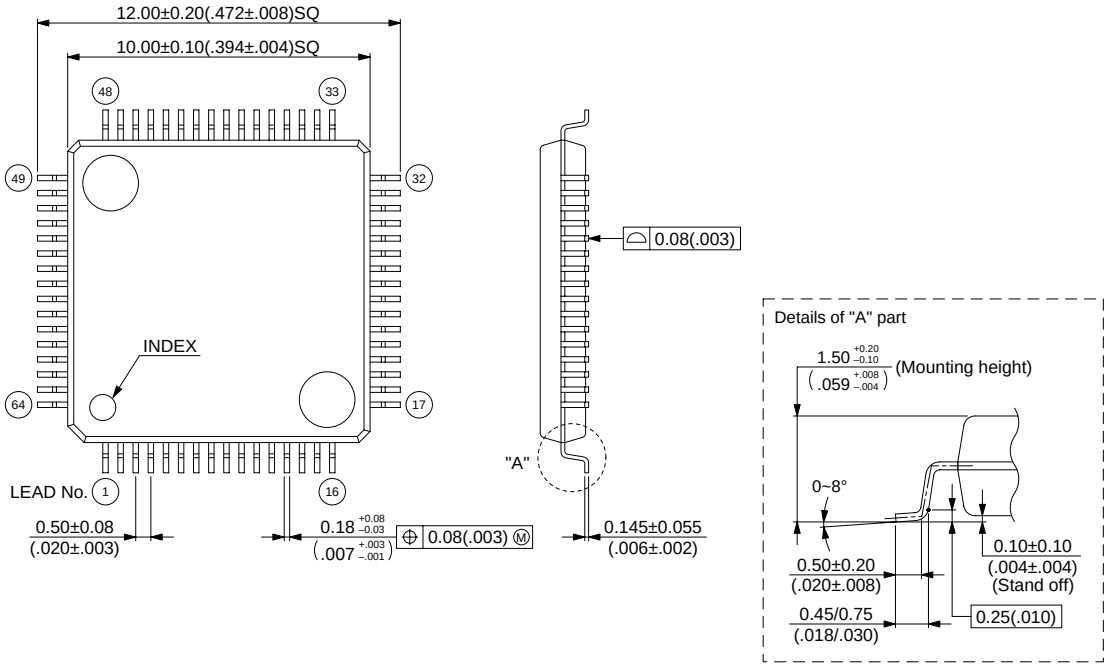
■ ORDERING INFORMATION

Part number	Package	Remarks
MB89589BPFM MB89P589BPFM	64-pin plastic QFP (FPT-64P-M09)	
MB89583BPFV MB89585BPFV MB89P585BPFV MB89583BWPFV MB89585BWPFV MB89P585BWPFV	64-pin plastic LQFP (FPT-64P-M03)	

■ PACKAGE DIMENSION

64-pin plastic LQFP
(FPT-64P-M03)

Note: Pins width and pins thickness include plating thickness.



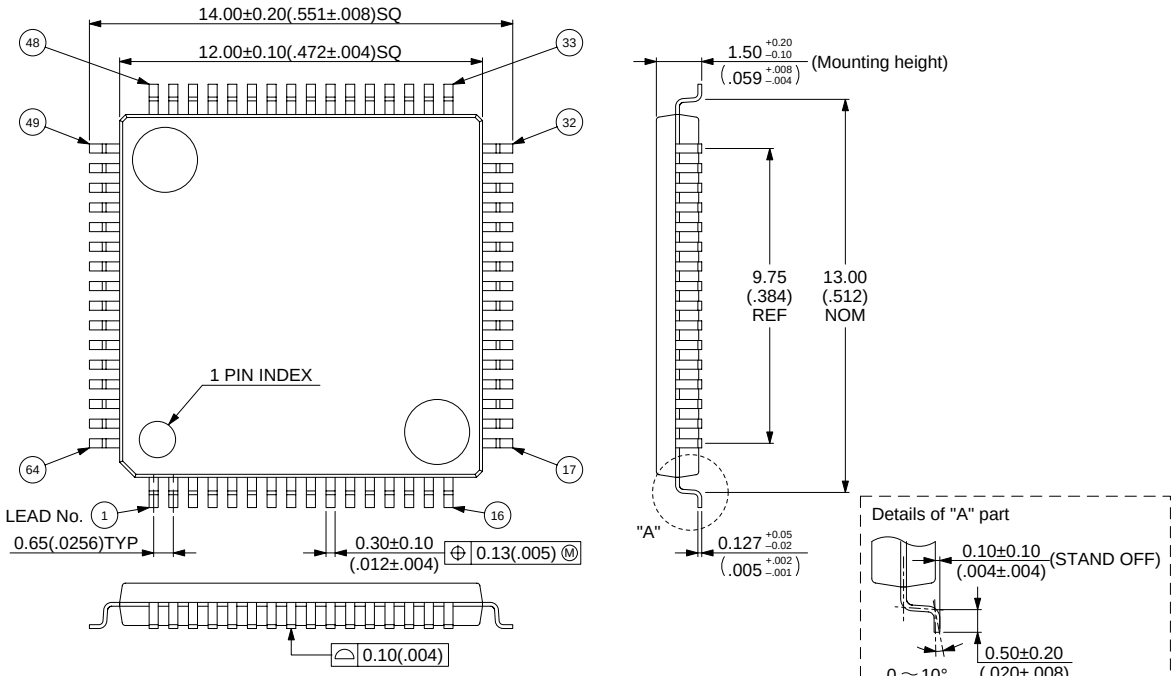
Dimensions in mm (inches)

(Continued)

(Continued)

64-pin plastic QFP
(FPT-64P-M09)

Note: Pins width and pins thickness include plating thickness.



Dimensions in mm (inches)

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