FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12508-3E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89601R Series

MB89601R/603/P601/PV620

■ DESCRIPTION

The MB89601R series is compact one-chip microcontrollers using the F²MC-8L* CPU core for which can operate at low voltage but at high speed. The microcontrollers contain peripheral functions such as timers, a serial interface and an external interrupt and are applicable to welfare products, especially portable devices required savings in board space.

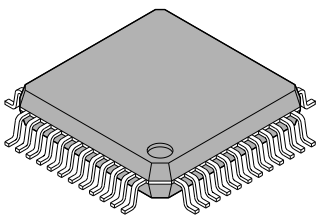
*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- High-speed processing at low voltage
  Minimum execution time: 0.5 µs/3.5 V at 8 MHz
- F²MC-8L family CPU core
- Timer
  8-bit PWM timer (also usable as a reload timer)
- Serial interface
  Switchable transfer direction allows communication with various equipment.
- External interrupt
  Capable of wake-up from low-power consumption modes (with an edge detection function)
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)

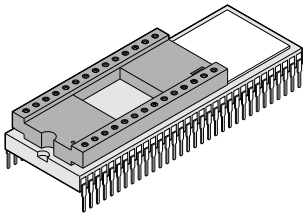
■ PACKAGE

48-pin Plastic SQFP



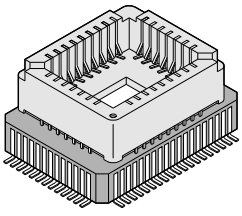
(FPT-48P-M05)

64-pin Ceramic MDIP



(MDP-64C-P02)

64-pin Ceramic MQFP



(MQP-64C-P01)

■ PRODUCT LINEUP

Parameter \ Part number	MB89601R	MB89603	MB89P601	MB89PV620*1
Classification	Mass production products (mask ROM products)		One-time PROM product	Piggyback/evaluation product (for evaluation and development)
ROM size (internal ROM)	4 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	4 K × 8 bits (external ROM, programming with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	80 × 8 bits			1 K × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.5 µs/8 MHz Interrupt processing time: 4.5 µs/8 MHz			
Ports	Input ports: 1 (also serve as peripherals.) Output ports: none I/O ports (N-ch open-drain): 8 (3 ports also serve as peripherals) Output ports (CMOS): none I/O ports (CMOS): 24 (1 port also serves as peripherals.) Total: 33			5 (4 ports also serve as peripherals.) 8 (8 ports also serve as peripherals.) 8 (4 ports also serve as peripherals.) 8 (8 ports also serve as peripherals.) 24 (24 ports also serve as peripherals.) 53
8-bit PWM timer	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.5 to 8 µs) 8-bit resolution PWM operation (conversion cycle: 128 to 2048 µs)			
8-bit pulse-width count timer	none			8-bit timer operation 8-bit reload timer operation 8-bit pulse-width measurement operation
16-bit timer/counter	none			16-bit timer operation 16-bit event conter
8-bit serial I/O	8 bits LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 1.0 µs, 4.0 µs, 16.0 µs)			SI/O × 2 channels
8-bit A/D converter	none			8-bit resolution × 8 channels A/D conversion mode Sense mode Reference voltage input
External interrupt	Edge selection, interrupt vector, source flag Rising edge/falling edge selectability Used also for wake-up from stop/sleep modes. (Edge detection is also permitted in stop mode.)			External interrupt × 4 channels

(Continued)

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Part number / Parameter	MB89601R	MB89603	MB89P601	MB89PV620*1
Standby mode	Sleep mode, stop mode			
Process	CMOS			
Operating voltage*1	2.2 V to 6.0 V	2.7 V to 6.0 V		
EPROM for use				MBM27C256A-20TV MBM27C256A-20CZ

*1: The piggyback/evaluation product is applicable to the MB89620 series.
*2: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89601R MB89603 MB89P601	MB89PV620
DIP-48P-M05	○	×
MDP-64C-P02	×	○
MQP-64C-P01	×	○

○ : Available × : Not available
Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89601R, MB89603, MB89P601, upper than 0140_H of each register bank cannot be used.
- The stack area, etc., is set at the upper limit of the RAM.
- External area is used.

2. Current Consumption

- In the case of the MB89PV620, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics.")

3. Mask Options

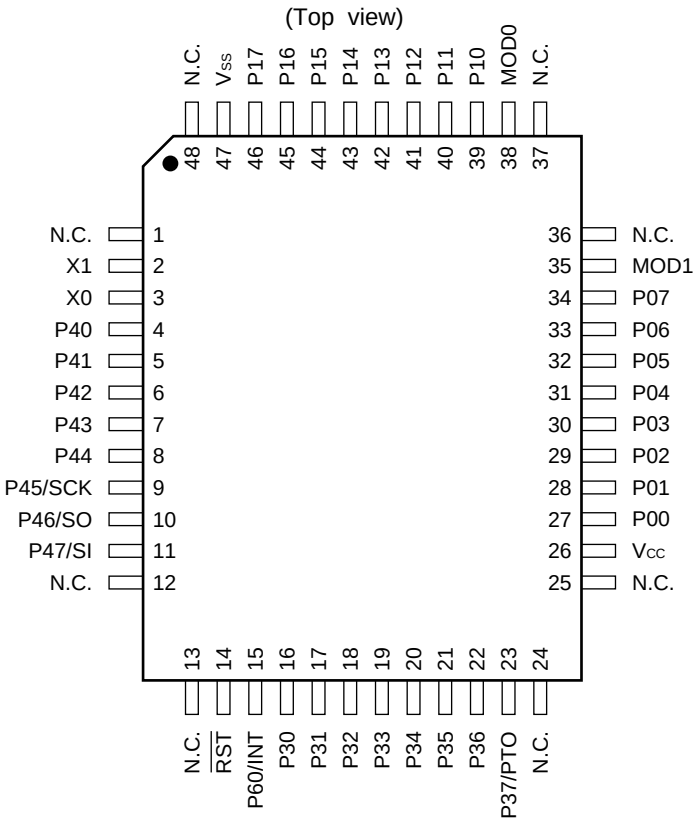
Functions that can be selected as options and how to designate these options vary by the product.

Before using options check "■ Mask Options."

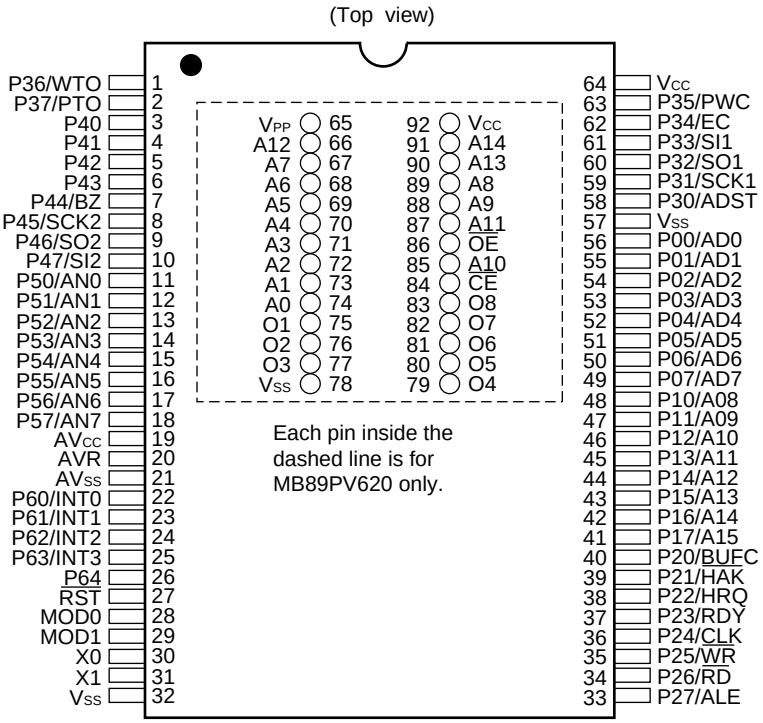
Take particular care on the following point:

- Options are fixed on the MB89PV620 and MB89P601.

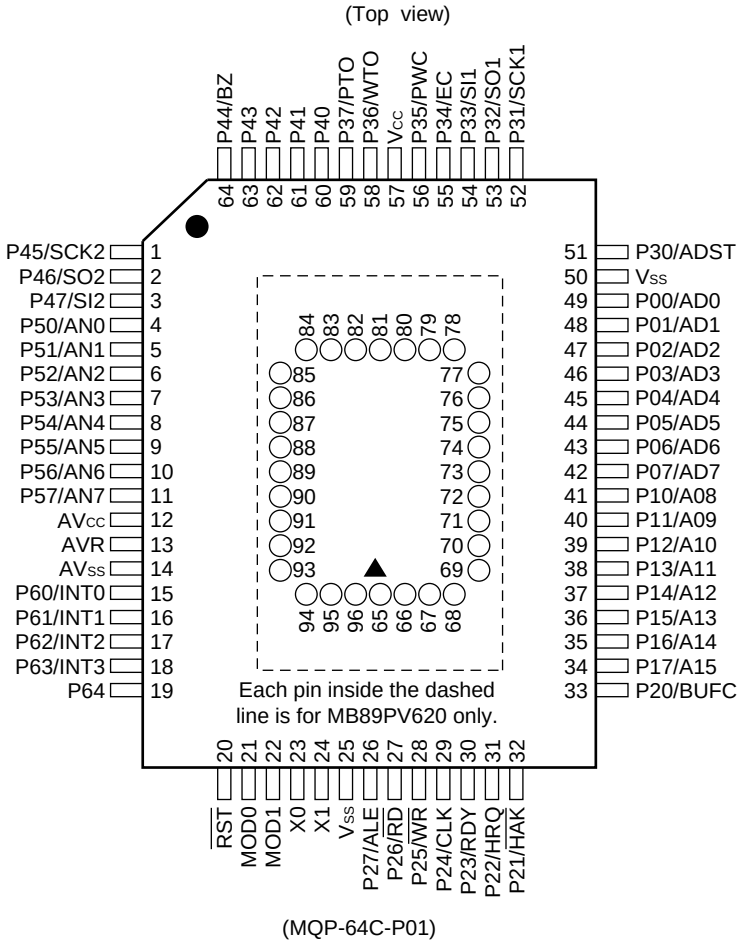
■ PIN ASSIGNMENT



(FPT-48P-M05)



(MDP-64C-P02)



(MQP-64C-P01)

- **Pin assignment on package top (MB89PV620 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

- **MB89601R/603/P601**

Pin no. SQFP*	Pin name	Circuit type	Function
3	X0	A	Cystal oscillator pins
2	X1		
38	MOD0	B	Operating mode selection pins Connect directly to V_{SS}.
35	MOD1		
14	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
27 to 34	P00 to P07	D	General-purpose I/O ports
39 to 46	P10 to P17		
16 to 22	P30 to P36	E	General-purpose I/O ports This port is a hysteresis input type. A software pull-up resistor is provided as an option.
23	P37/PTO		General-purpose I/O port This port is a hysteresis input type. Also serves as the toggle output for the 8-bit PWM timer. A software pull-up resistor is provided as an option.
4 to 8	P40 to P44	G	N-ch open-drain I/O port This port is a hysteresis input type.
9	P45/SCK		N-ch open-drain I/O port This port is a hysteresis input type. Also serves as the clock I/O for the serial I/O.
10, 11	P46/SO, P47/SI		N-ch open-drain I/O port This port is a hysteresis input type. Also serves as the data output for the serial I/O.
15	P60/INT	I	General-purpose input-only port Also serves as an external interrupt input. This port is a hysteresis input type.
26	V_{CC}	—	Power supply pin
47	V_{SS}	—	Power supply (GND) pin
1, 12, 13, 24, 25, 36, 37, 48	N.C.	—	Be sure to leave them open.

* : FPT-48P-M05

- **MB89PV620**

Pin no.		Pin name	Circuit type	Function
MDIP*1	MQFP*2			
30	23	X0	A	Crystal oscillator pins
31	24	X1		
28	21	MOD0	B	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
29	22	MOD1		
27	20	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
56 to 49	49 to 42	P00/AD0 to P07/AD7	D	General-purpose I/O ports When an external bus is used, this port function as multiplex pins of lower address output and data I/O.
48 to 41	41 to 34	P10/A08 to P17/A15	D	General-purpose I/O ports When an external bus is used, this port function as a upper address output.
40	33	P20/BUFC	F	General-purpose output-only port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
39	32	P21/$\overline{HAK}$	F	General-purpose output-only port When an external bus is used, this port can also be used as a hold-acknowledge by setting the BCTR.
38	31	P22/HRQ	D	General-purpose output-only port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
37	30	P23/RDY	D	General-purpose output-only port When an external bus is used, this port functions as a ready input.
36	29	P24/CLK	F	General-purpose output-only port When an external bus is used, this port functions as a clock output.
35	28	P25/$\overline{WR}$	F	General-purpose output-only port When an external bus is used, this port functions as a write signal output.
34	27	P26/$\overline{RD}$	F	General-purpose output-only port When an external bus is used, this port functions as a read signal output.

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*1: MDP-64C-P02
*2: MQP-64C-P01

(Continued)

Pin no.		Pin name	Circuit type	Function
MDIP*1	MQFP*2			
33	26	P27/ALE	F	General-purpose output-only port When an external bus is used, this port functions as an address latch signal output.
58	51	P30/ADST	E	General-purpose I/O port Also serves as the external activation input for the A/D converter. This port is a hysteresis input type.
59	52	P31/SCK1	E	General-purpose I/O port Also serves as the clock I/O for the serial I/O 1. This port is a hysteresis input type.
60	53	P32/SO1	E	General-purpose I/O port Also serves as the data output for the serial I/O 1. This port is a hysteresis input type.
61	54	P33/SI1	E	General-purpose I/O port Also serves as the data input for the serial I/O 1. This port is a hystereisis input type.
62	55	P34/EC	E	General-purpose I/O port Also serves as the external clock input for the 16-bit timer/counter. This port is a hysteresis input type.
63	56	P35/PWC	E	General-purpose I/O port Also serves as the measured-pulse input for the 8-bit pulse width-counter. This port is a hysteresis input type.
1	58	P36/WTO	E	General-purpose I/O port Also serves as the toggle output for the 8-bit pulse-width counter. This port is a hysteresis input type.
2	59	P37/PTO	E	General-purpose I/O port Also serves as the toggle output for the 8-bit PWM timer. This port is a hysteresis input type.
3 to 6	60 to 63	P40 to P43	G	N-ch open-drain I/O ports This port is a hysteresis input type.
7	64	P44/BZ	G	N-ch open-drain I/O port Also serves as a buzzer output. This port is a hysteresis input type.
8	1	P45/SCK2	G	N-ch open-drain I/O port Also serves as the clock I/O for the serial I/O 2. This port is a hysteresis input type.
9	2	P46/SO2	G	N-ch open-drain I/O port Also serves as the data output for the serial I/O 2. This port is a hysteresis input type.

(Continued)

*1: MDP-64C-P02
*2: MQP-64C-P01

(Continued)

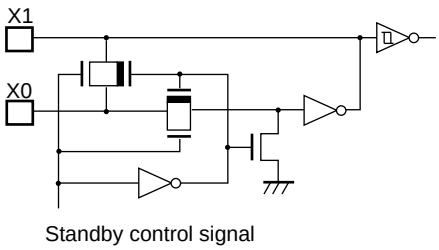
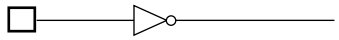
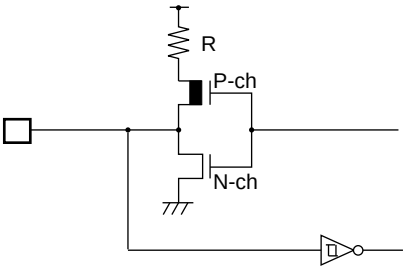
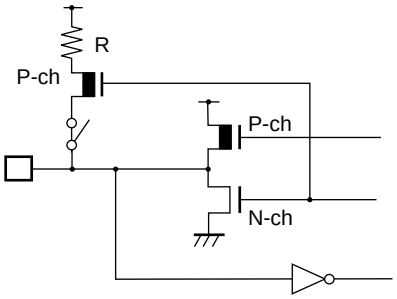
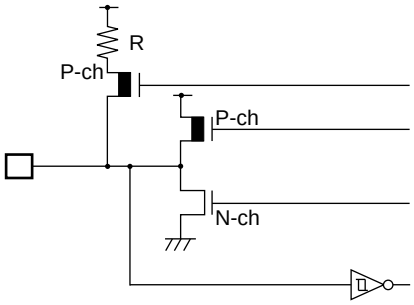
Pin no.		Pin name	Circuit type	Function
MDIP*1	MQFP*2			
10	3	P47/SI2	G	N-ch open-drain I/O port Also serves as the data I/O for the serial I/O 2. This port is a hysteresis input type.
11 to 18	4 to 11	P50/AN0 to P57/AN7	H	N-ch open-drain output-only ports Also serves as the analog input for the A/D converter.
22 to 25	15 to 18	P60/INT0 to P63/INT3	I	General-purpose input-only ports Also serves as an external interrupt input. This port is a hysteresis input type.
26	19	P64	I	General-purpose input-only port This port is a hysteresis input type.
64	57	V_{CC}	—	Power supply pin
32, 57	25, 50	V_{SS}	—	Power supply (GND) pins
19	12	AV_{CC}	—	A/D converter power supply pin
20	13	AVR	—	A/D converter reference voltage input pin
21	14	AV_{SS}	—	A/D converter power supply pin. Use this port at the same voltage as V_{SS}.

*1: MDP-64C-P02
*2: MQP-64C-P01

- **External EPROM pins (MB89PV620 only)**

Pin no.		Pin name	I/O	Function
MDIP	MQFP			
65	66	V_{PP}	O	"H" level output pin
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
75 76 77	77 78 79	O1 O2 O3	I	Data input pins
78	80	V_{SS}	O	Power supply (GND) pin
79 80 81 82 83	82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins
84	87	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
85	88	A10	O	Address output pin
86	89	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
87 88 89	91 92 93	A11 A9 A8	O	Address output pins
90	94	A13	O	
91	95	A14	O	
92	96	V_{CC}	O	EPROM power supply pin
—	65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• CMOS I/O • Pull-up resistor optional (MB89601R/603 only)
E		• CMOS output • Hysteresis input • Software pull-up resistor optional

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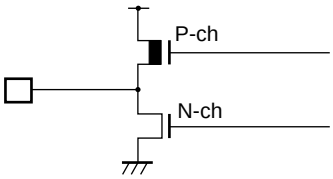
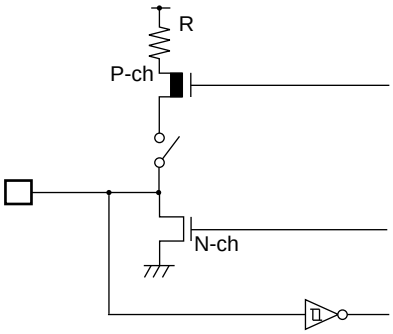
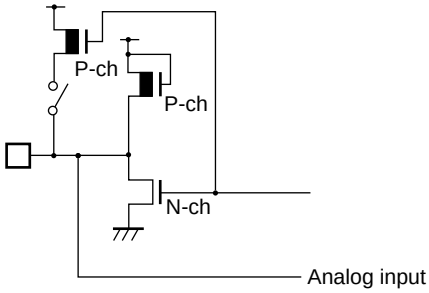
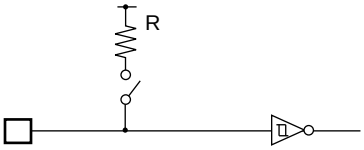
Type	Circuit	Remarks
F		• CMOS output
G		• N-ch open-drain output • Hysteresis input • Pull-up resistor optional (MB89601R/603 only)
H		• N-ch open-drain output • Analog input • Pull-up resistor optional
I		• Hysteresis input • Pull-up resistor optional (MB89601R/603 only)

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than P40 to P47, P60 or if higher than the voltage which shows on section "■ Electrical Characteristics" is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P601

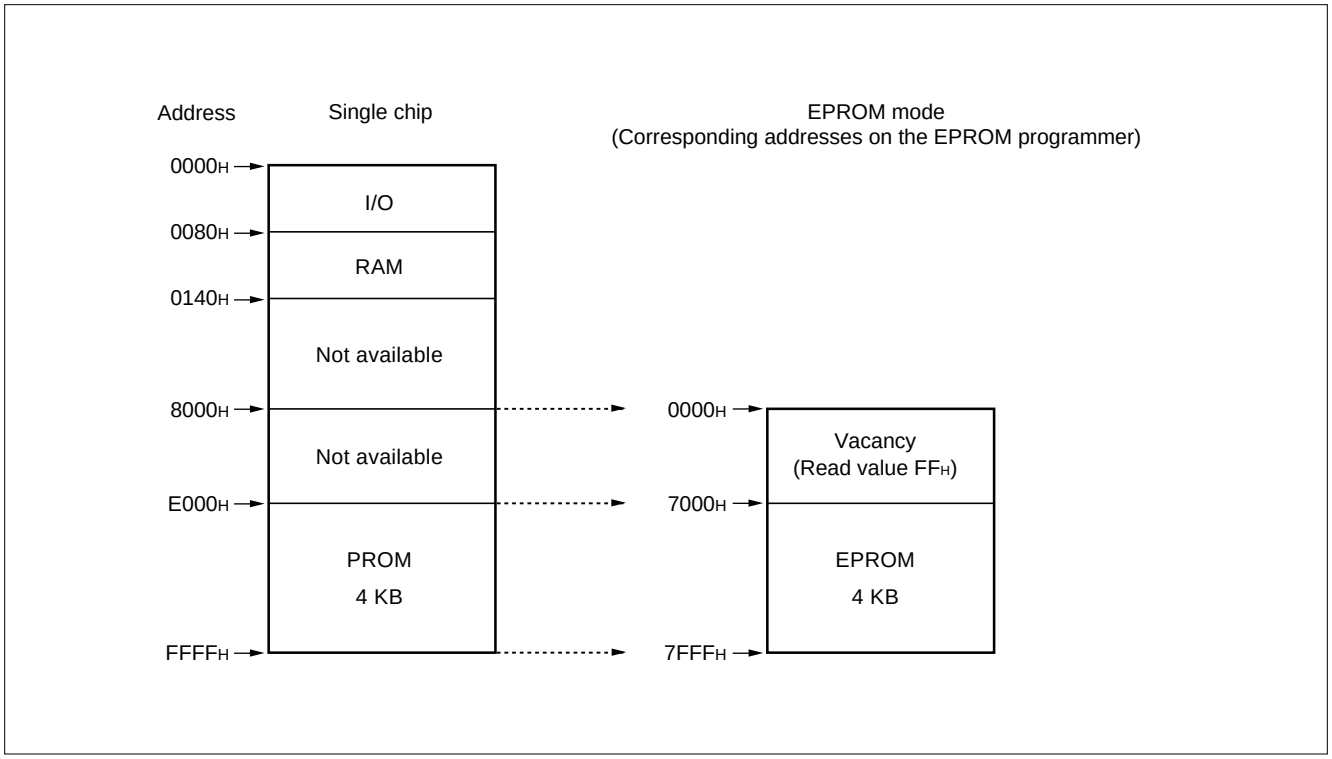
The MB89P601 is an OTPROM version of the MB89601R series.

1. Features

- 4-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 4-Kbyte PROM is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P601 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

When the operating ROM area for a single chip is 32 Kbytes (8000_H to $FFFF_H$) the PROM can be programmed as follows:

- **Programming procedure**

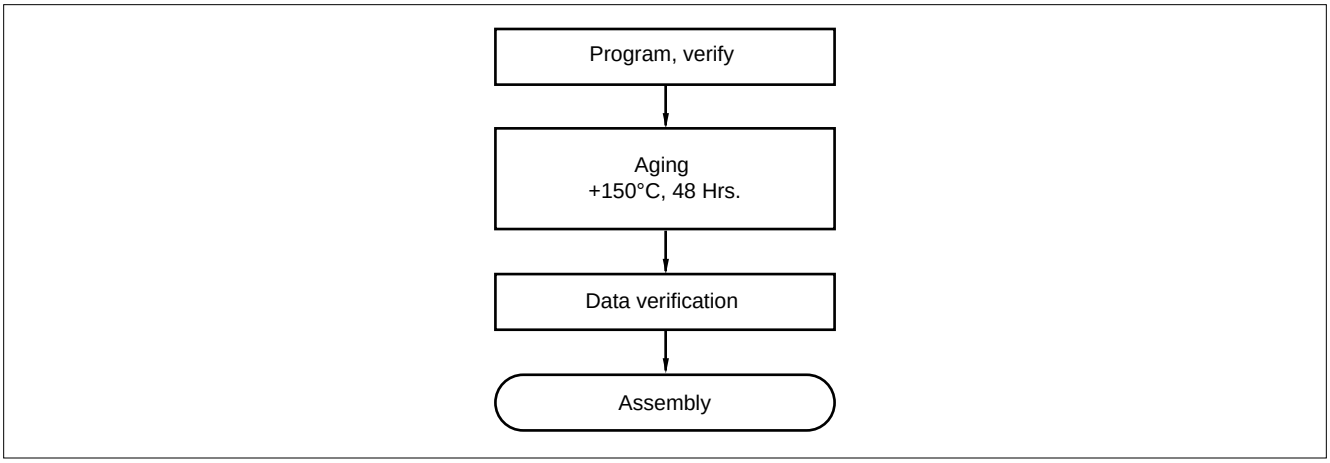
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 7000_H to $7FFF_H$ (note that addresses $E000_H$ to $FFFF_H$ while operating as a single chip assign to 7000_H to $7FFF_H$ in EPROM mode).

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-48P-M05	ROM-48QF-28DP-8L

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760
Note: Connect the adapter jumper pin to V_{SS} when using.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV, MBM27C256A-20CZ

2. Programming Socket Adapter

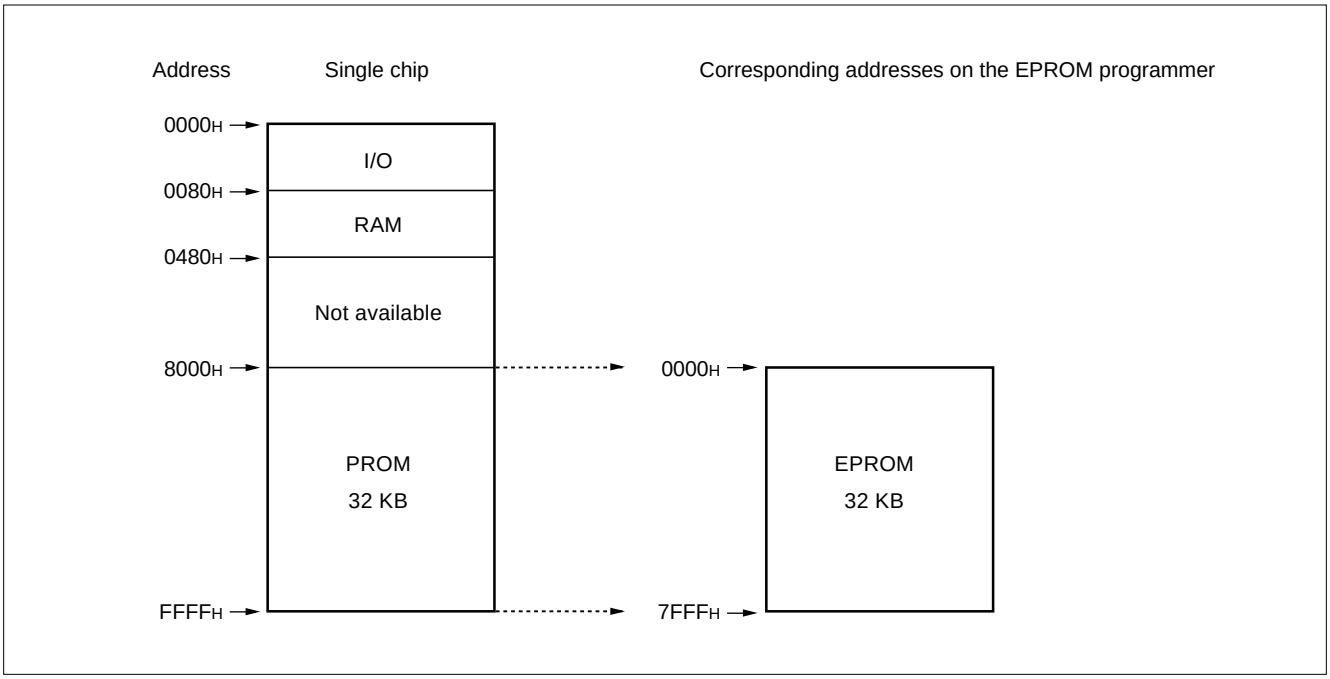
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32(Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, is diagrammed below.



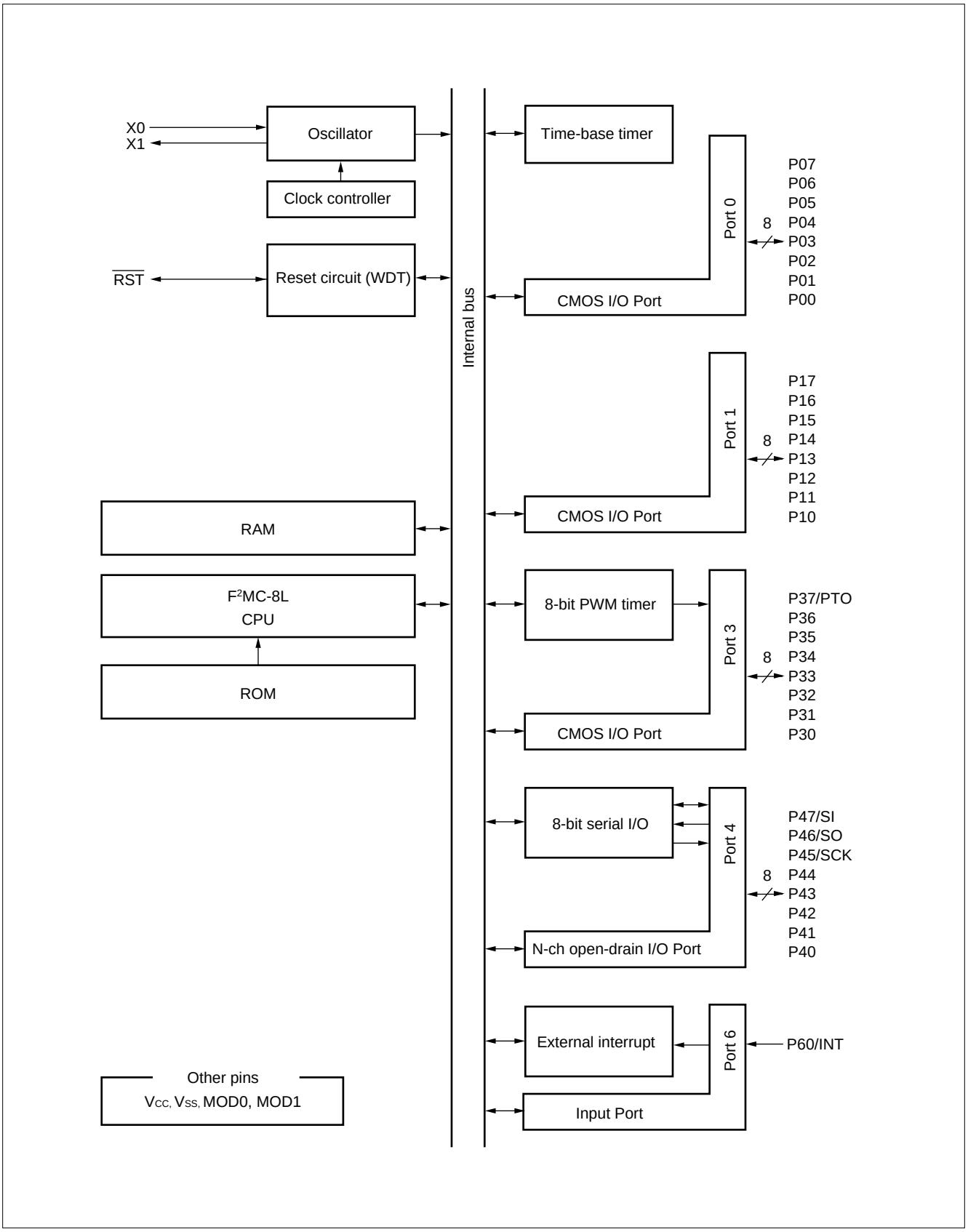
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0006_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

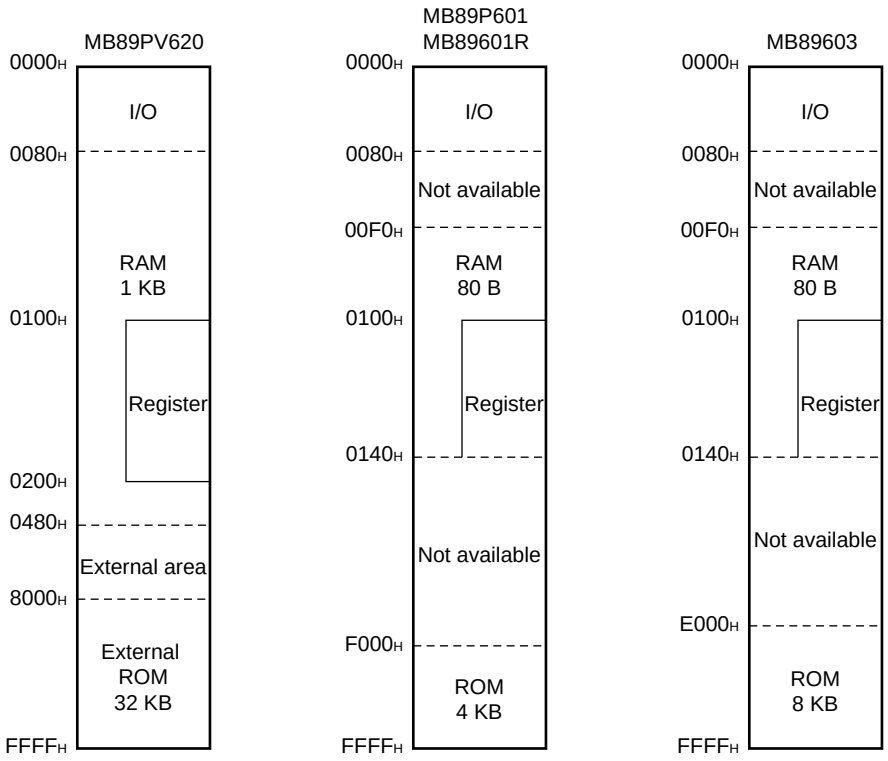


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89601R series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89601R series is structured as illustrated below.

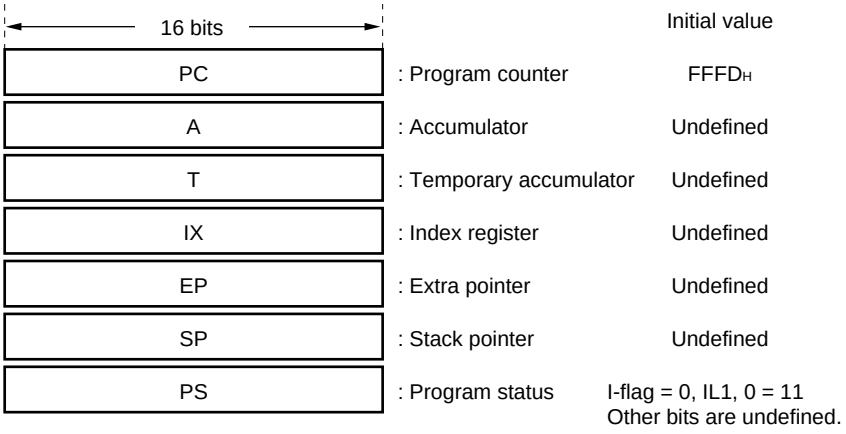
Memory Space



2. Registers

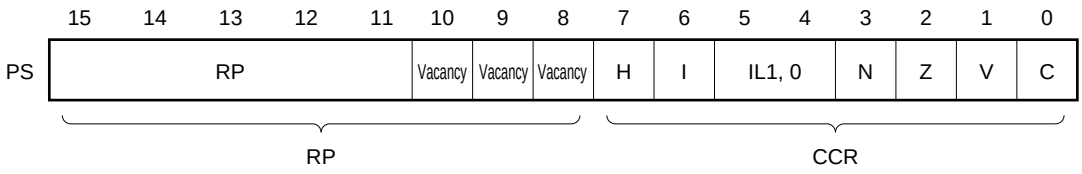
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



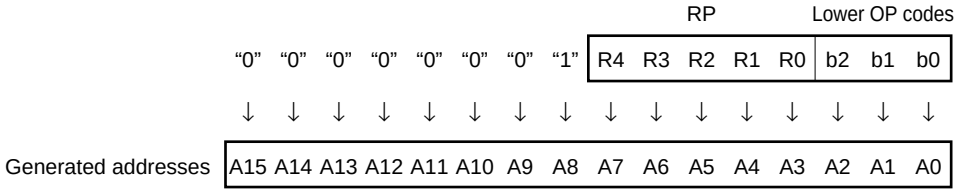
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High ↕ Low = no interrupt
0	1		
1	0	2	
1	1	3	

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

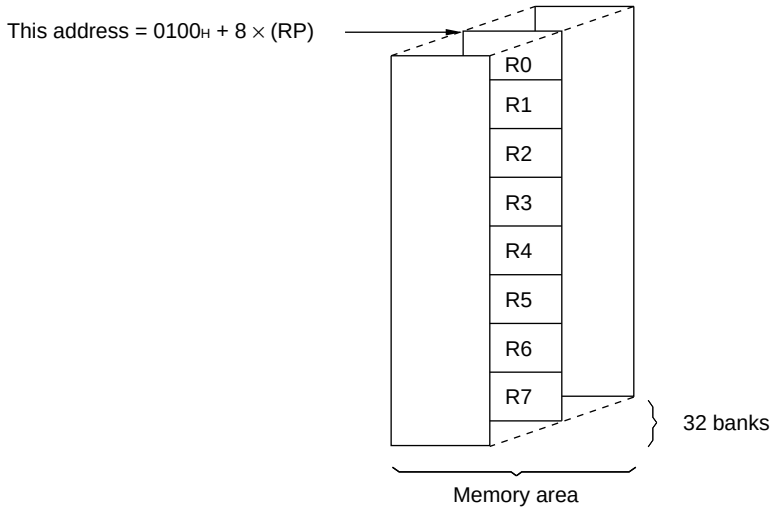
C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to 32 banks can be used on the architecture, but only 8 banks can be used on the MB89601R series due to the restricted internal RAM size. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration



Note: For software development, take care that the usable register banks on the MB89601R/603 are different from that on the MB89PV620. On the MB89PV620, up to 32 banks can be used.

■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	SPCR	Port 3 pull-up register
05H			Vacancy
06H			Vacancy
07H			Vacancy
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Clock interrupt control register
0BH			Vacancy
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH			Vacancy
10H			Vacancy
11H	(R)	PDR6	Port 6 data register
12H	(R/W)	CNTR	PWM control register
13H	(W)	COMR	PWM compare register
14H			Vacancy
15H			Vacancy
16H			Vacancy
17H			Vacancy
18H			Vacancy
19H			Vacancy
1AH			Vacancy
1BH			Vacancy
1CH			Vacancy
1DH			Vacancy
1EH	(R/W)	SMR	Serial mode register
1FH	(R/W)	SDR	Serial data register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
20_H			Vacancy
21_H			Vacancy
22_H			Vacancy
23_H			Vacancy
24_H	(R/W)	EIC	External interrupt control register
25_H to $7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P40 to P47, P60
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P47, P60
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P40 to P47
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P47
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

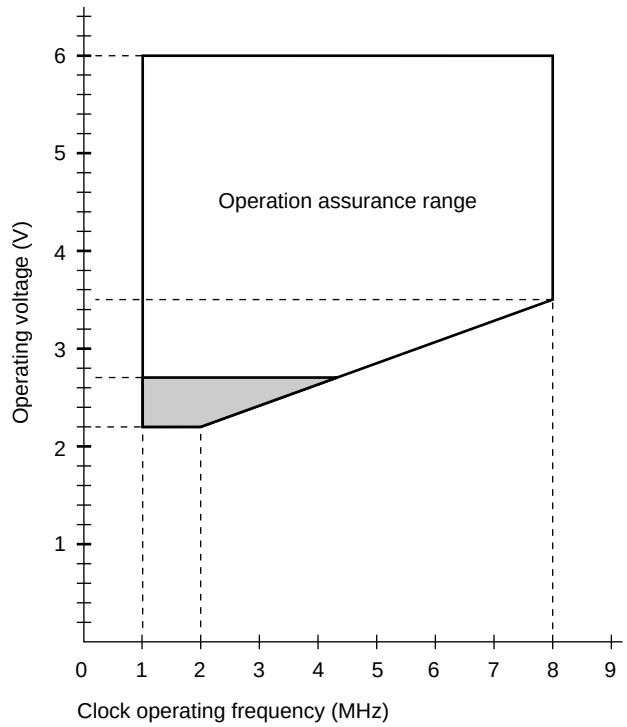
Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*	6.0	V	Normal operation assurance range* MB89601R/603
		2.7*	6.0	V	Normal operation assurance range* MB89P601
		1.5	6.0	V	Retains the RAM state in stop mode
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency. See Figure 1.



Note: The shaded area is assured only for the MB89601R/603.

Figure 1 Operating Voltage vs. Clock Operating Frequency

3. DC Characteristics

(V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS1}	P30 to P37, MOD0, MOD1, $\overline{RST}$	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS2}	P40 to P47, P60	—	0.8 V_{CC}	—	V_{SS} + 6.0	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P30 to P37, MOD0, MOD1, $\overline{RST}$, P40 to P47, P60	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P40 to P47	—	V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P30 to P37	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47	I_{OL} = +1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = +4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P60, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P60, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	

(Continued)

(Continued)

(V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*	I_{CC}	V_{CC}	F_C = 8 MHz Normal operating mode	—	9	15	mA	
			F_C = 8 MHz	—	10	18	mA	MB89P601
	I_{CCS}		F_C = 8 MHz Sleep mode	—	3	4	mA	External clock
	I_{CCH}		T_A = +25°C Stop mode	—	—	10	µA	
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	10	—	pF	

* : The power supply current is measured at the external clock.
Note: A pull-up resistor for P00 to P07, P10 to P17, P40 to P47 and P60 is selectable on MB89601R/603 only.

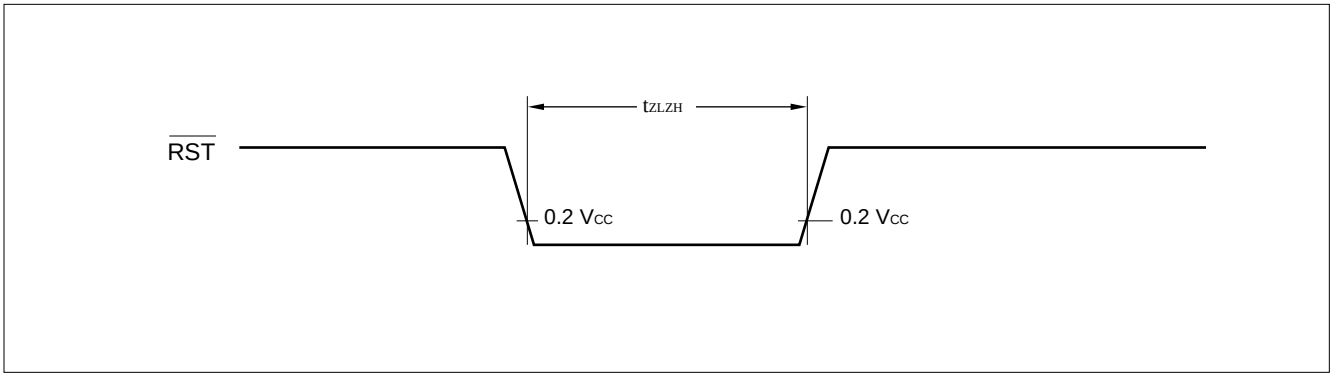
4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{XCYL}	—	ns	

Note: t_{XCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.

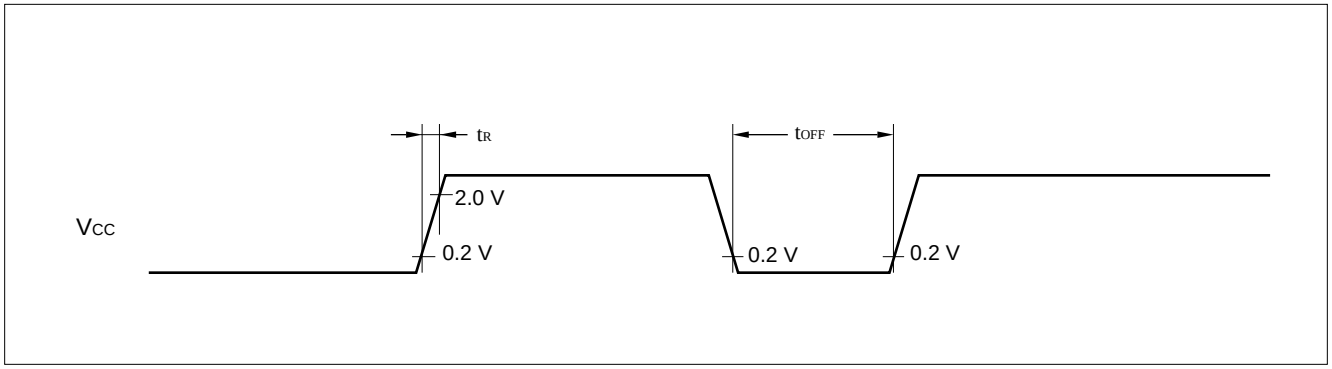


(2) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Abrupt change in power supply voltage may cause a power-on reset.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

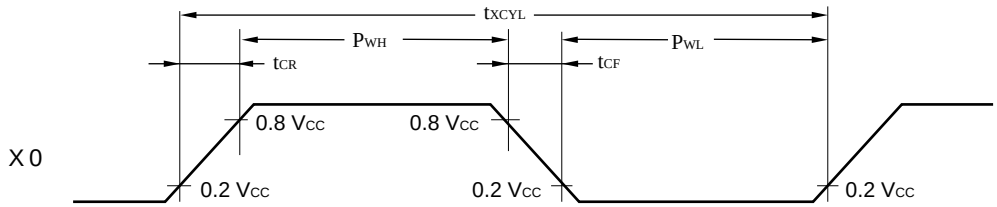


(3) Clock Timing

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

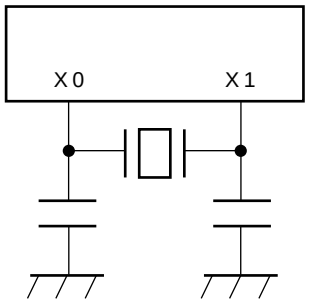
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	8	MHz	
Clock cycle time	t_{XYCL}	X0, X1	—	125	—	ns	
Input clock pulse width	P_{WH} P_{WL}	X0	—	20	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	10	ns	External clock

X0 and X1 Timing and Conditions

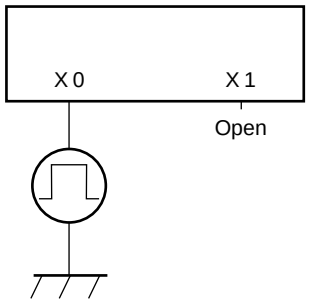


Clock Conditions

When a crystal
or
ceramic resonator is used



When an external clock is used



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	4/F_C	µs	t_{inst} = 0.5 µs when operating at F_C = 8 MHz

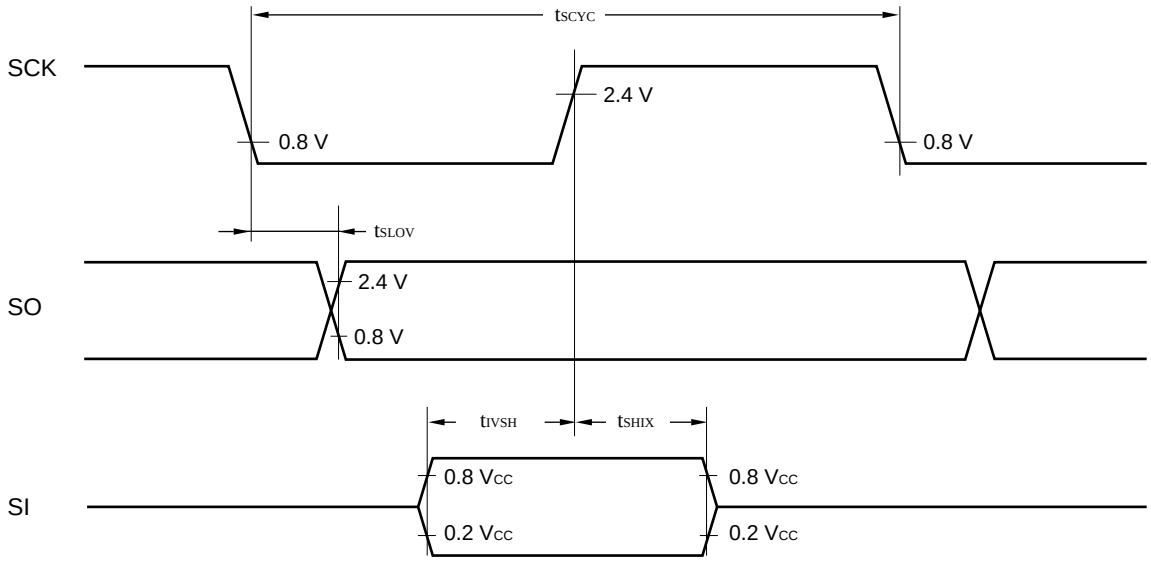
(5) Serial I/O Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

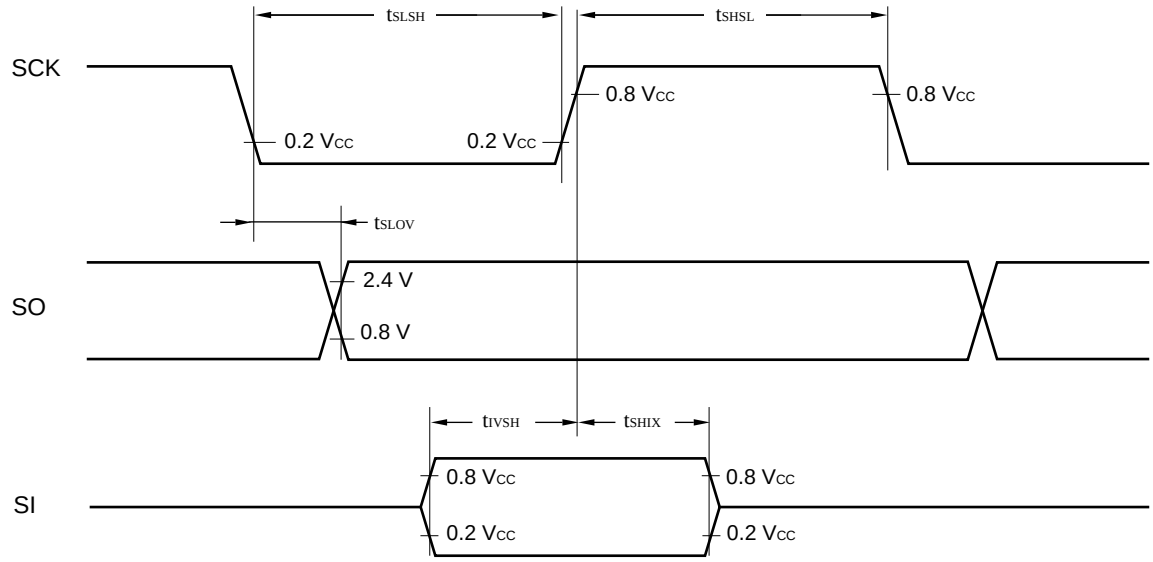
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK		1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

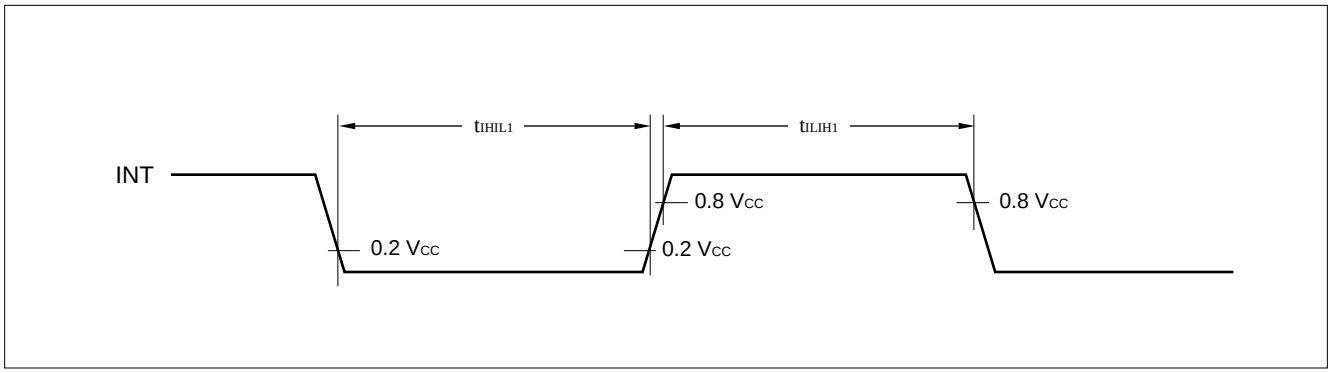


(6) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

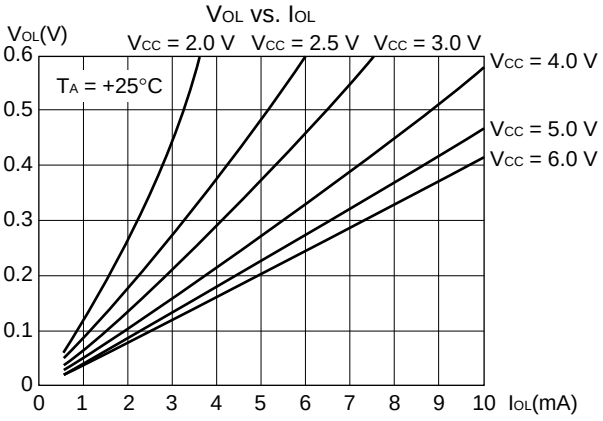
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT	—	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}			2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

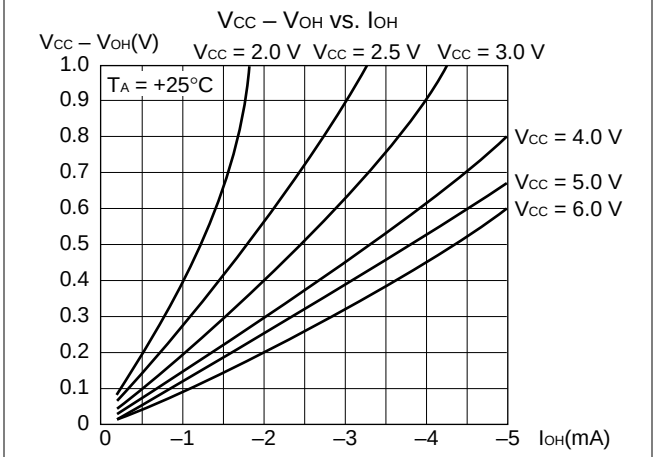


■ EXAMPLE CHARACTERISTICS

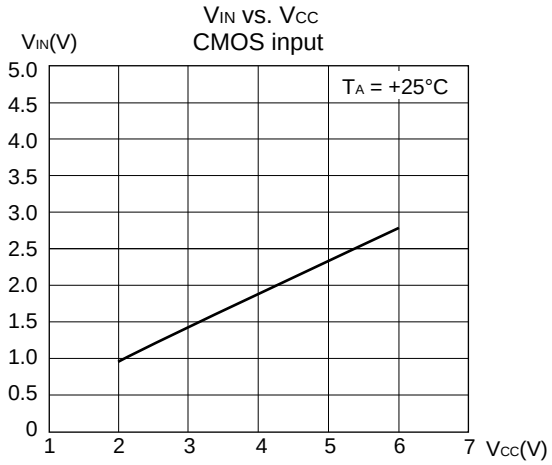
(1) “L” Level Output Voltage

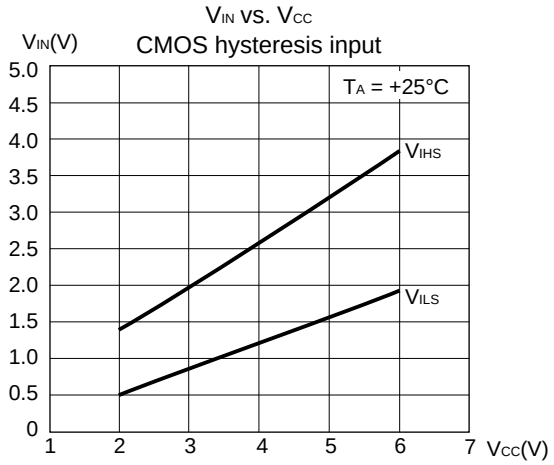


(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage

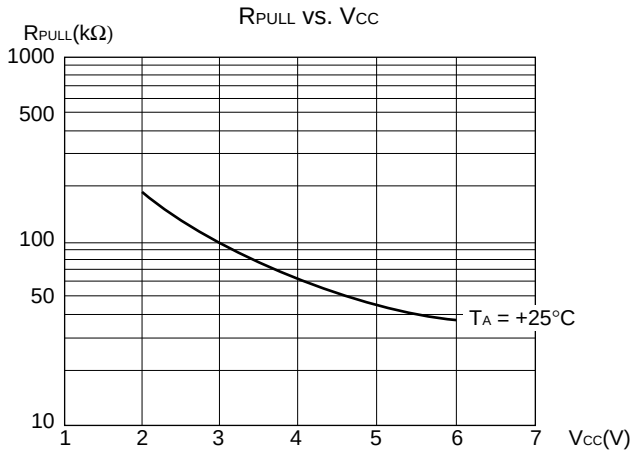




VIHS: Threshold when input voltage in hysteresis characteristics is set to “H” level

VILS: Threshold when input voltage in hysteresis characteristics is set to “L” level

(4) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 1 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 2 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir:0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir:1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir:2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir:3	BBC dir:3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir:4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir:5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	MOV @IX+d,A	XOR A,@IX+d	AND A,@IX+d	OR A,@IX+d	MOV @IX+d,#d8	CMP @IX+d,#d8	CLRB dir:6	BBC dir:6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:7	BBC dir:7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir:0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir:1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir:2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir:3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir:4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir:5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir:6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir:7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89601R MB89603	MB89P601	MB89PV620
	Specifying procedure	**Specify when ordering masking**	**Setting not possible**	**Setting not possible**
1	Pull-up resistors { P00 to P07, P10 to P17, P40 to P47[*2], P60[*2]	Selectable by pin	Fixed to without pull-up resistor	Fixed to without pull-up resistor
	P30 to P33[*1]	Selectable by pin (Software pull-up resistor)	Can be set per pin (Software pull-up resistor)	
	P33 to P37[*1]	Selectable by 4 pins (Software pull-up resistor)	Can be set per 4 pins (Software pull-up resistor)	
2	Power-on reset selection { With power-on reset Without power-on reset	Selectable	Fixed to with power-on reset	Fixed to with power-on reset
3	Selection of the oscillation stabilization time { Crystal oscillator: (2^{18}/F_C) Ceramic oscillator: (2^{12}/F_C)	Selectable	Fixed to crystal oscillator (2^{18}/F_C)	Fixed to crystal oscillator (2^{18}/F_C)
4	Reset pin output { With reset output Without reset output	Selectable	Fixed to with reset output	Fixed to with reset output

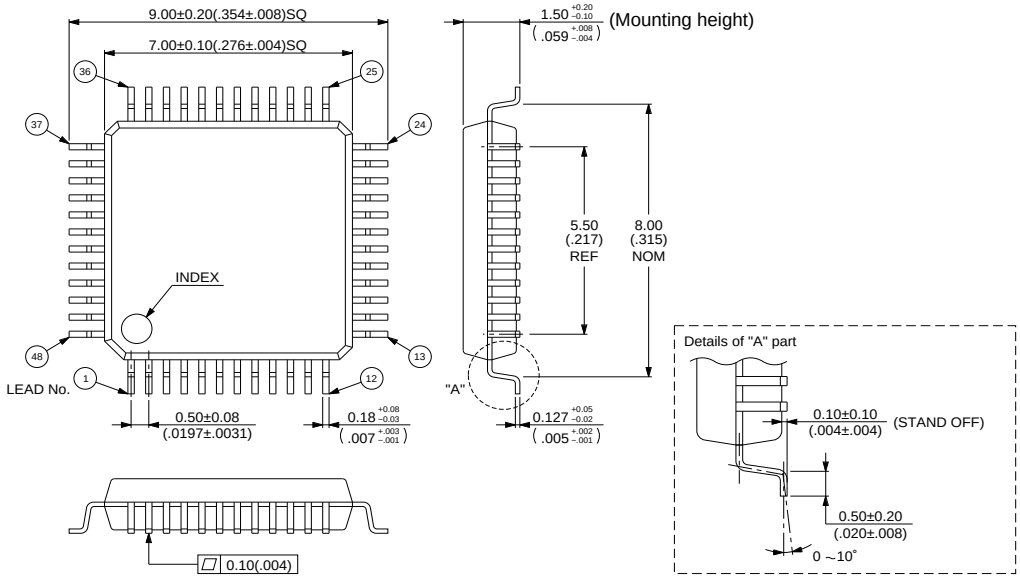
*1: A pull-up resistor for P30 to P37 is not set when ordering masking. It is set by software.
*2: When a pull-up resistor for P40 to P47 and P60 is selected, the input signal exceeding V_{CC} voltage is not possible.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89P601PFV MB89601PFV	48-pin Plastic SQFP (FPT-48P-M05)	
MB89PV620C-SH	64-pin Ceramic MDIP (MDP-64C-P02)	
MB89PV620CF	64-pin Ceramic MQFP (MQP-64C-P01)	

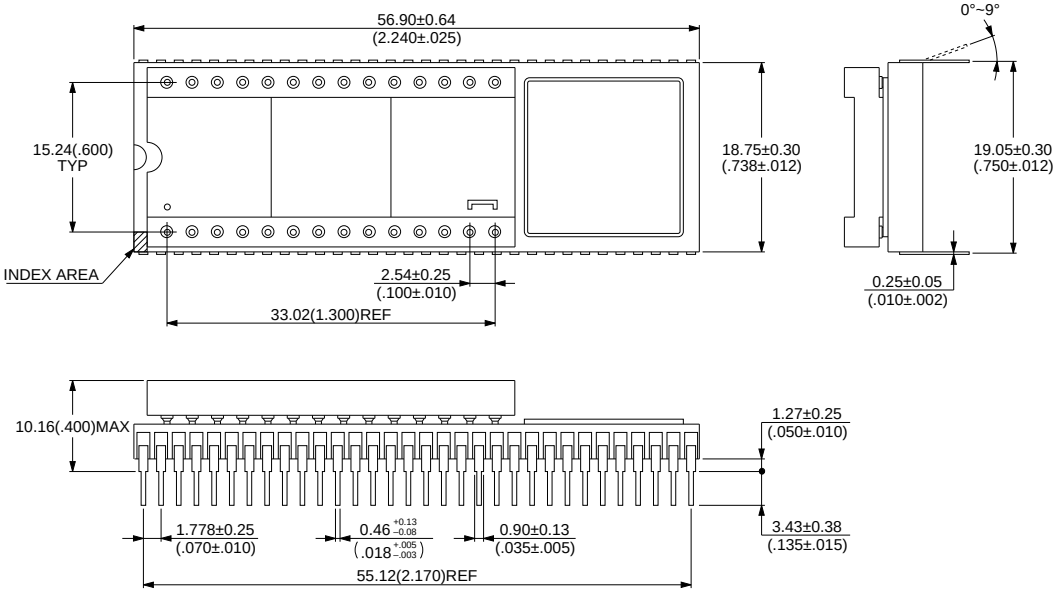
■ PACKAGE DIMENSIONS

48 pin, Plastic LQFP
(FPT-48P-M05)



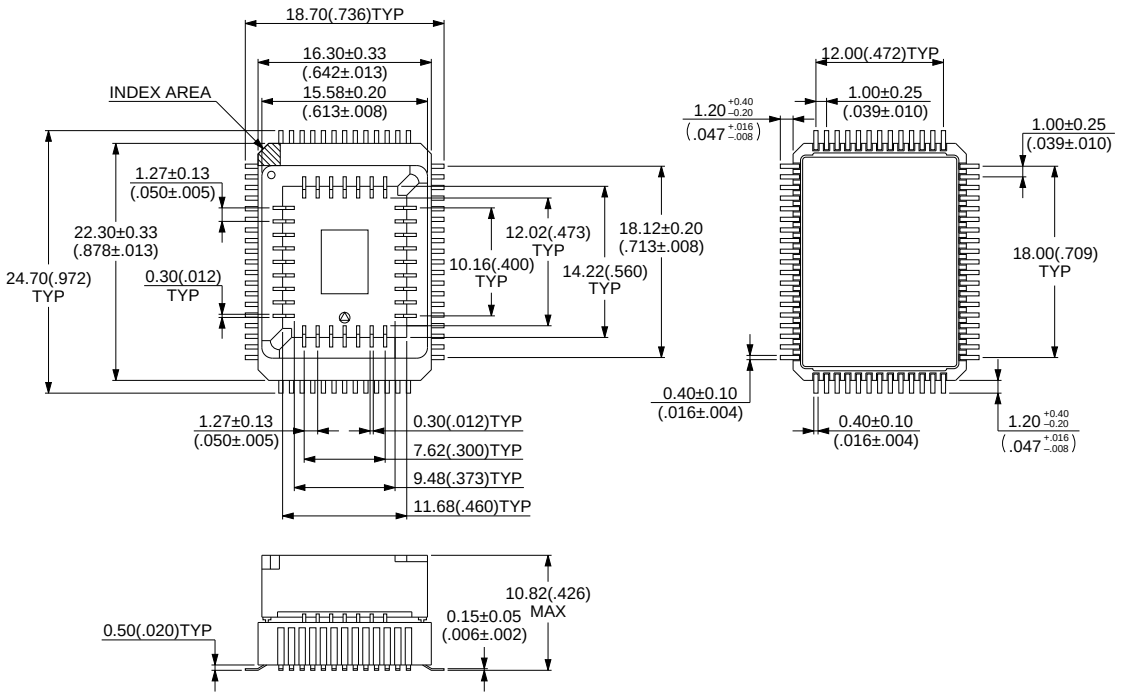
Dimensions in mm (inches).

64-pin Ceramic MDIP
(MDP-64C-P02)



Dimensions in mm (inches)

64-pin Ceramic MQFP
(MQP-64C-P01)



Dimensions in mm (inches)

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