FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12527-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89863 Series

MB89863

■ DESCRIPTION

The MB89863 is a single-chip microcontroller using the F²MC-8L CPU core which can operate at low voltage but at high speed. The microcontroller contains peripheral functions such as a timers unit, timers, a UART, an A/D converter, and an external interrupt. The MB89863 is optimum to the pulse output for the control of an AC inverter motor, etc.

■ FEATURES

- F²MC-8L family CPU core

  Instruction set optimized for controllers { Multiplication and division instructions / 16-bit arithmetic operations / Test and branch instructions / Bit manipulation instructions, etc.

- Timer unit
  Outputs a non-overlap, three-phase waveforms to control an AC inverter motor.
  Also usable as a PWM timer (4 channels)
- 8-bit PWM timers: 2 channels
  Also usable as a reload timer
- UART
  Full-duplex double buffer
  Synchronous and asynchronous data transfer

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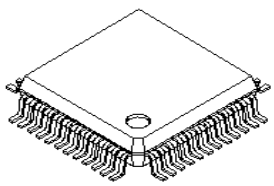
■ PACKAGE

48-pin Plastic QFP



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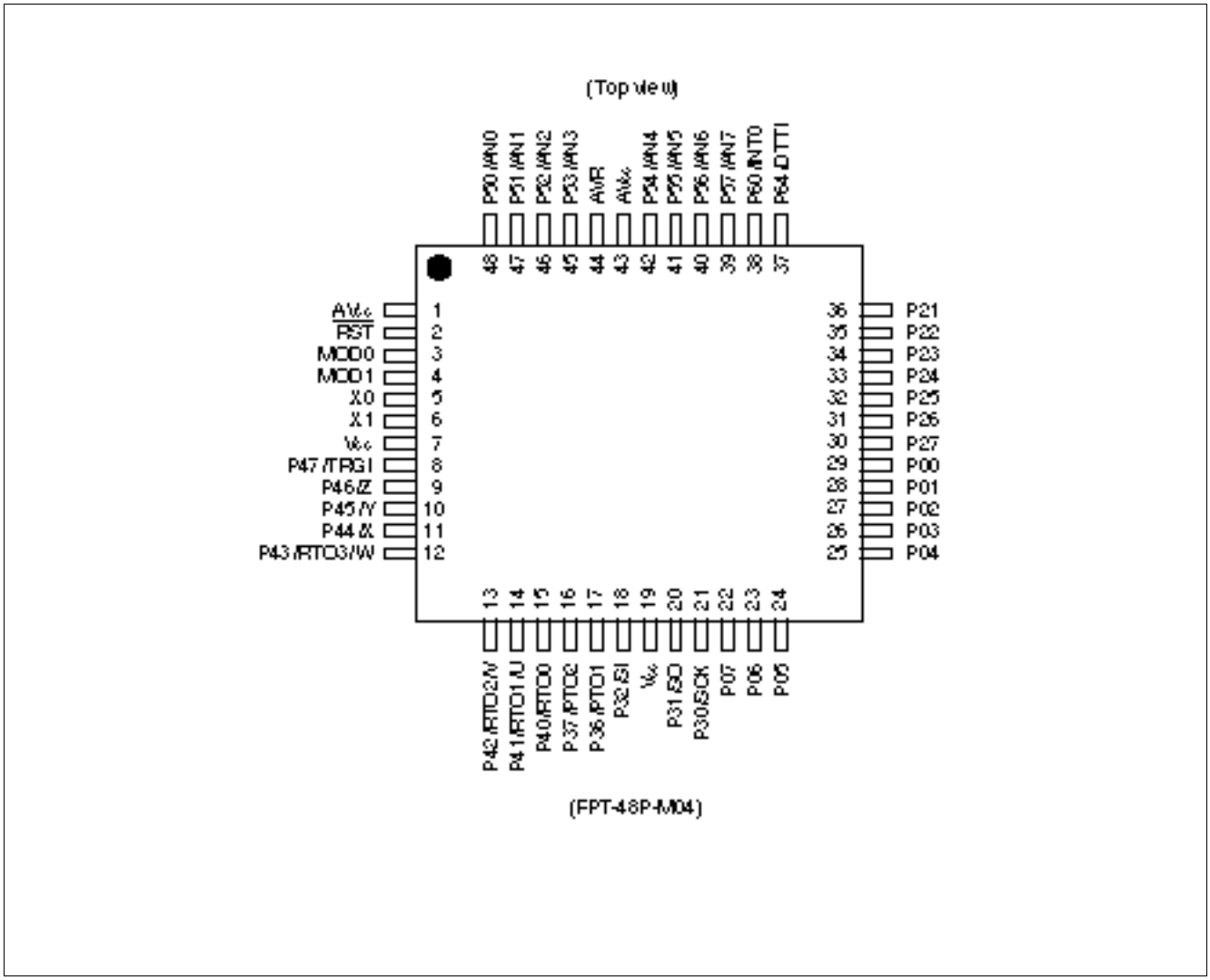
- 10-bit A/D converter
  Conversion time: 33 instruction cycles
  Activation by a timer unit capable
- External interrupt: 1 channel
  Usable for wake-up from low-power consumption modes (with an edge detection function)
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption)
  Sleep mode (the CPU stops to reduce the current consumption to approx. 1/3 of normal.)

■ PRODUCT LINEUP

Part number / Parameter	MB89863	MB89P857	MB89W857
Classification	Mass production product (mask ROM product)	One-time PROM products/EPROM products, also used for evaluation	
ROM size	8 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM programming with general-purpose EPROM programmer)	
RAM size	256 × 8 bits	1 K × 8 bits	
CPU functions	Number of instructions: 136 Instruction length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits		
Minimum execution time	0.95 µs/4.2 MHz 0.5 µs/8 MHz	0.4 µs/10 MHz	
Interrupt processing time	8.57 µs/4.2 MHz 4.5 µs/8 MHz	3.6 µs/10 MHz	
I/O ports	Max. 38	Max. 53	
Timer unit	10-bit up/down count timer × 1 Compare registers with buffer × 4 Compare clear registers with buffer, zero detection pin control, 4 output channels, non-overlap three-phase waveform output, independent three-phrase dead-time timer		
8-bit PWM timer 1, 8-bit PWM timer 2	8-bit reload timer operation (toggled output capable, operating clock cycle: 1 to 64 instruction cycles) 8-bit resolution PWM operation (conversion cycle: 255 to 16320 instruction cycles)		
UART	8 bits Clock-synchronous/asynchronous data transfer capable		
8-bit serial I/O	—	8 bits, LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 2, 8, 32 instruction cycles)	
10-bit A/D converter	10-bit resolution × 8 channels A/D conversion time of 33 instruction cycles Continuous activation by a compare channel 0 in timer unit or an external activation capable (On the MB89863, the external activation is incapable.)		
External interrupt	1 channel	4 channels	
	Rising edge/falling edge selectability Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)		
Standby mode	Sleep mode, stop mode		
Process	CMOS		
Package	QFP-48	SHDIP-64	
Operating voltage	5.0 V ±10%	2.7 to 5.5 V	

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no. QFP48	Pin name	Circuit type	Function
5	X0	A	Crystal oscillator pins (max. 8 MHz)
6	X1		
3	MOD0	B	Operating mode selection pins Connect directly to V_{SS}. These pins are with a pull-down resistor.
4	MOD1		
2	$\overline{RST}$	C	Reset I/O pin. This port is a hysteresis input type. The internal circuit initialized by the input of “L”. This pin is with a pull-up resistor.
22 to 29	P07 to P00	D	General-purpose I/O ports
30 to 36	P27 to P21	F	General-purpose output ports
21	P30/SCK	E	General-purpose I/O port Also serves as the I/O for the UART. This port is a hysteresis input type.
20	P31/SO	E	General-purpose I/O port Also serves as the data output for the UART. This port is a hysteresis input type.
18	P32/SI	E	General-purpose I/O port Also serves as the data input for the UART. This port is a hysteresis input type.
17	P36/PTO1	E	General-purpose I/O port Also serves as the pulse output for the 8-bit PWM 1. This port is a hysteresis input type.
16	P37/PTO2	E	General-purpose I/O port Also serves as the pulse output for the 8-bit PWM 2. This port is a hysteresis input type.
15	P40/RTO0	E	General-purpose I/O port Also serves as the pulse output for the timer unit. This port is a hysteresis input type.
14	P41/RTO1/U	E	General-purpose I/O port Also serves as the pulse output or non-overlap 3-phase waveform output for the timer unit. This port is a hysteresis input type.
13	P42/RTO2/V	E	General-purpose I/O port Also serves as the pulse output or non-overlap 3-phase waveform output for the timer unit. This port is a hysteresis input type.
12	P43/RTO3/W	E	General-purpose I/O port Also serves as the pulse output or non-overlap 3-phase waveform output for the timer unit. This port is a hysteresis input type.
11	P44/X	E	General-purpose I/O port Also serves as the non-overlap 3-phase waveform output. This port is a hysteresis input type.

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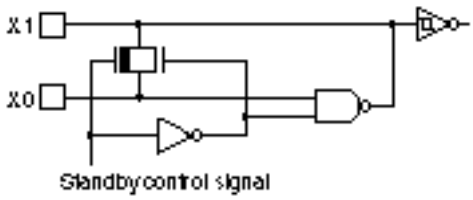
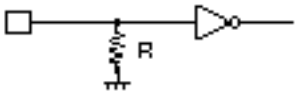
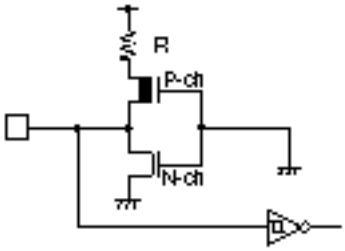
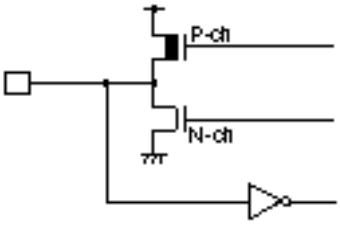
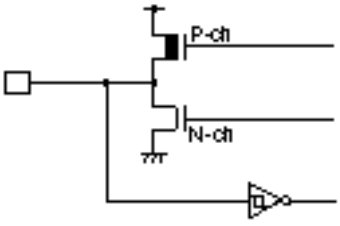
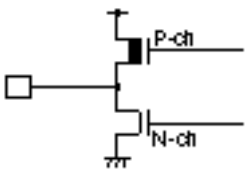
Pin no. QFP48	Pin name	Circuit type	Function
10	P45/Y	E	General-purpose I/O port Also serves as the non-overlap 3-phase waveform output. This port is a hysteresis input.
9	P46/Z	E	General-purpose I/O port Also serves as the non-overlap 3-phase waveform output. This port is a hysteresis input type.
8	P47/TRGI	E	General-purpose I/O port Also serves as the trigger input for the timer unit. This port is a hysteresis input type.
39 to 42, 45 to 48	P57/AN7 to P54/AN4, P53/AN3 to P50/AN0	G	N-channel open-drain output ports Also serve as analog input for the A/D converter.
38	P60/INT0	H	General-purpose input port Also serves as an external interrupt input. This port is a hysteresis input type.
37	P64/DTTI	H	General-purpose input port Also serves as a dead-time timer disable input. This port is a hysteresis input type. DTTI input is with a noise canceller.
7	V_{CC}	—	Power supply pin
19	V_{SS}	—	Power supply (GND) pin
1	AV_{CC}	—	A/D converter power supply pin
44	AVR	—	A/D converter reference voltage input pin
43	AV_{SS}	—	A/D converter power supply (GND) pin Use this pin at the same voltage as V_{SS}.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• At an oscillation feedback resistor of approximately 1 MΩ
B		• CMOS input • Built-in pull-down resistor
C		• Output pull-up resistor (P-ch) • Hysteresis input
D		• CMOS output • CMOS input
E		• CMOS output • Hysteresis input
F		• CMOS output

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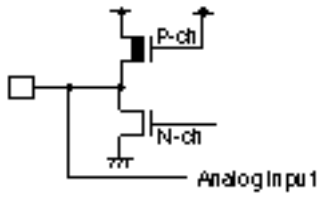
Type	Circuit	Remarks
G		• N-ch open-drain output • Analog input
H		• Hysteresis input

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

4. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and wake-up from stop mode.

5. Power Supply and Analog Input for A/D Converter

Take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

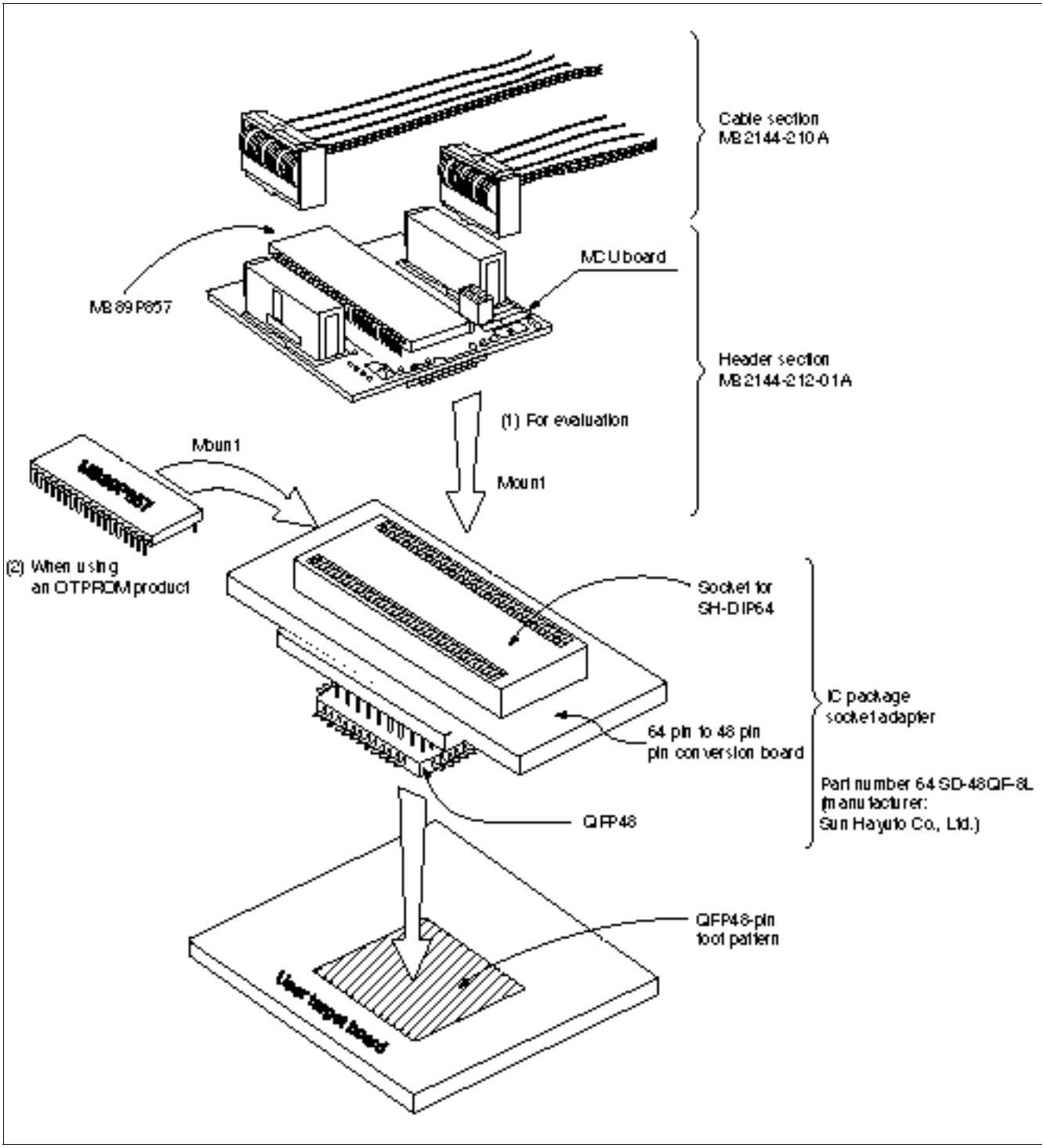
6. Treatment of Power Supply Pins on Microcontrollers with A/D Converter

Connect to be $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = V_{SS}$ when the A/D converter is not in use.

■ DEVELOPMENT ENVIRONMENT

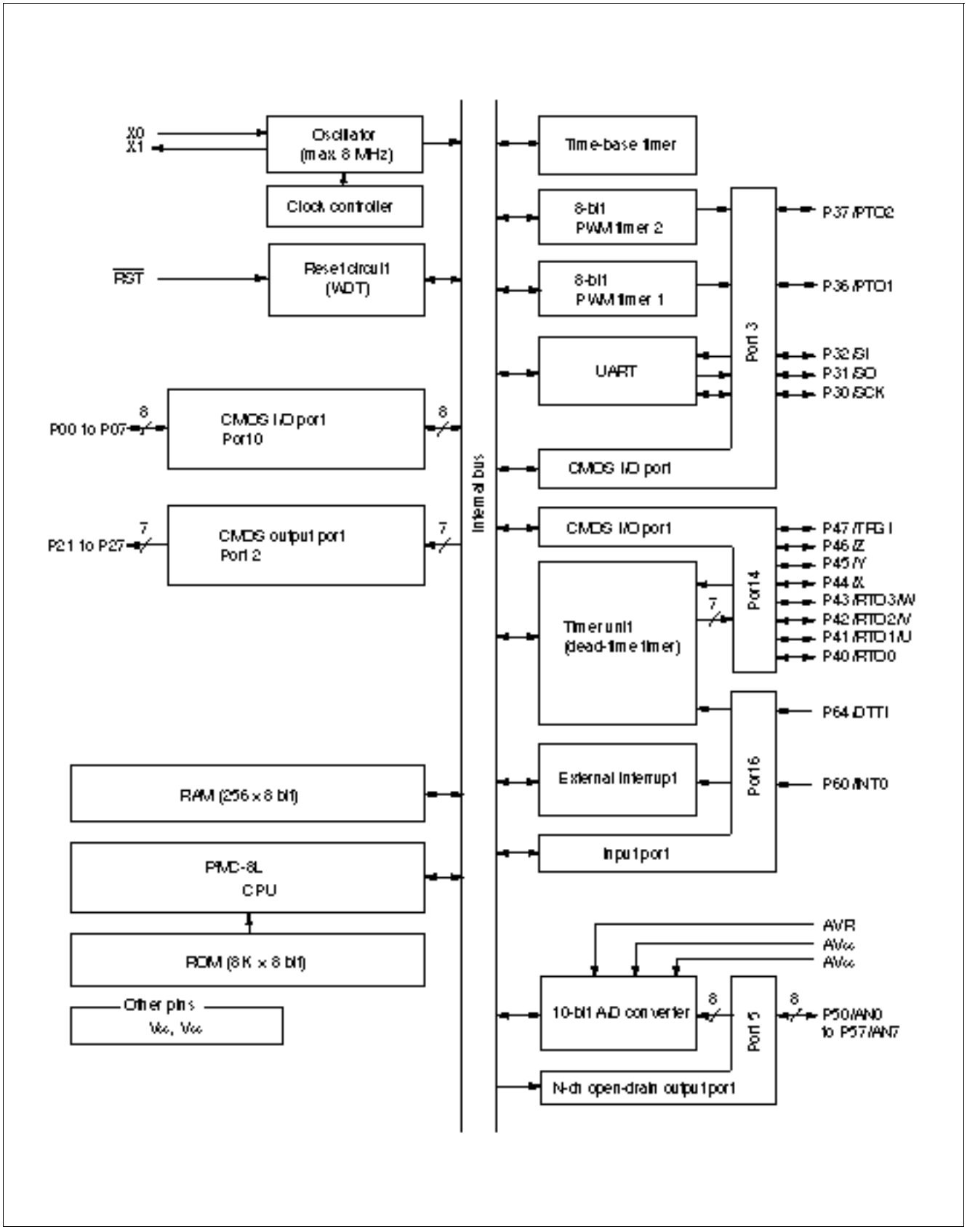
The MB8963 is a mask ROM product.

When using an evaluation tool or an OTPROM product for software development, use the MB89P857 or MB89W857 with the socket adapter (Part number 64SD-48QF-8L manufactured by Sun Hayato Co., Ltd.) dedicated to the MB89863 (as shown in the following example).



For programming to the MB89P/W857, refer to the F²MC-8L MB89860/850 Series Data Sheet.

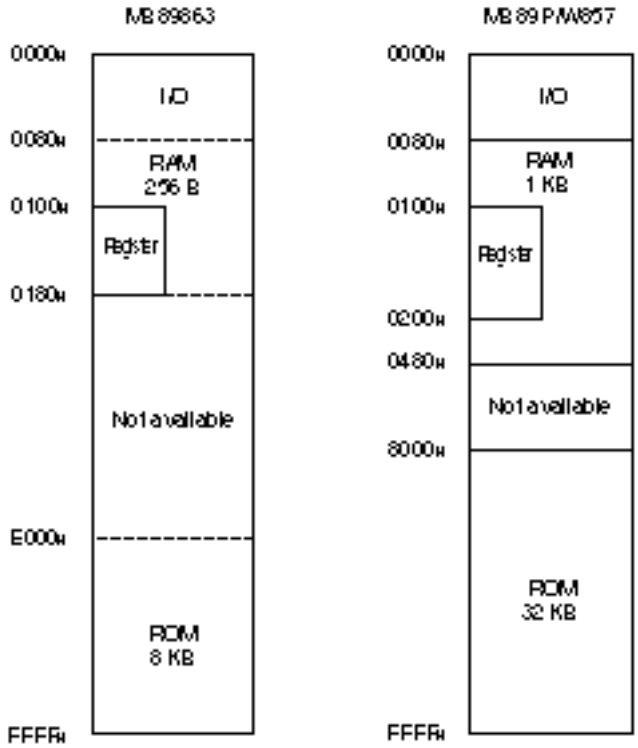
■ BLOCK DIAGRAM



■ CPU CORE

1. Memory Space

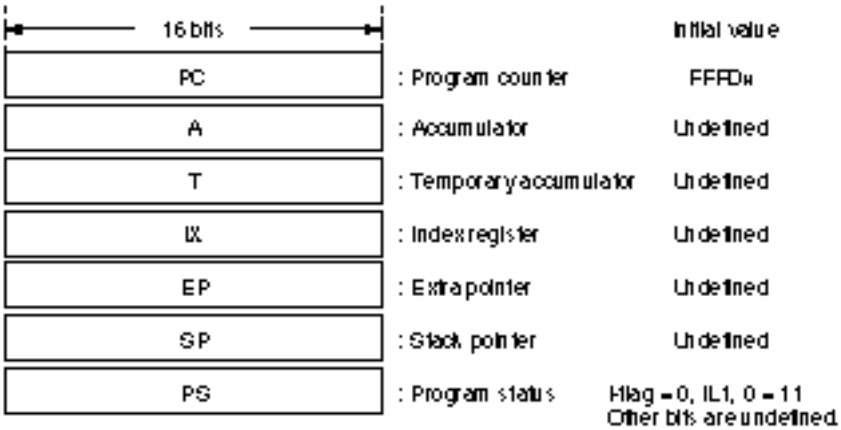
The microcontrollers of the MB89863 offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89863 is structured as illustrated below.



2. Registers

The MB89863 has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code

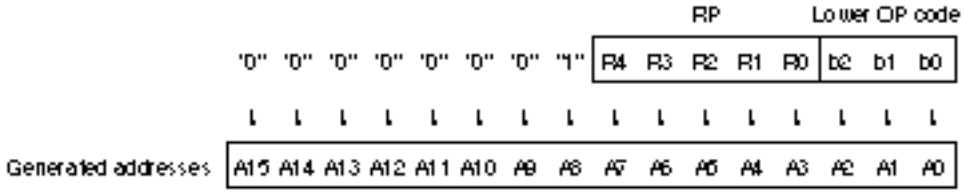


The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89863. The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration

■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H			Vacancy
03H			Vacancy
04H	(R/W)	PDR2	Port 2 data register
05H			Vacancy
06H			Vacancy
07H			Vacancy
08H	(R/W)	STBC	Standby control register
09H	(W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Time-base timer control register
0BH			Vacancy
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 data direction register
10H	(R/W)	PDR5	Port 5 data register
11H			Vacancy
12H	(R)	PDR6	Port 6 data register
13H			Vacancy
14H			Vacancy
15H			Vacancy
16H			Vacancy
17H to1BH			Vacancy
1CH	(R/W)	CTR1	PWM control register 1
1DH	(W)	CMR1	PWM compare register 1
1EH	(R/W)	CTR2	PWM control register 2
1FH	(W)	CMR2	PWM compare register 2
20H	(R/W)	SMC	UART serial mode control register
21H	(R/W)	SRC	UART serial rate control register
22H	(R/W)	SSD	UART serial status/data register
23H	(R/W)	SIDR/SODR	UART serial data register

Note: Do not use vacancies.

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Address	Read/write	Register name	Register description
24H			Vacancy
25H			Vacancy
26H	(R/W)	EIC1	External interrupt control register 1
27H			Vacancy
28H	(R/W)	ADC1	A/D converter control register 1
29H	(R/W)	ADC2	A/D converter control register 2
2AH	(R/W)	ADDH	A/D converter data register (H)
2BH	(R/W)	ADDL	A/D converter data register (L)
2CH			Vacancy
2DH	(W)	ZOCTR	Zero detection output control register
2EH	(W)	CLRBRH	Compare clear buffer register (H)
2FH	(W)	CLRBRL	Compare clear buffer register (L)
30H	(R/W)	TCSR	Timer control status register
31H	(R/W)	CICR	Compare interrupt control register
32H	(R/W)	TMCR	Timer mode control register
33H	(R/W)	COER	Compare/port selection register
34H	(R/W)	CMCR	Compare buffer mode control register
35H	(R/W)	DTCR	Dead-time timer control register
36H	(W)	DTSR	Dead-time setting register
37H	(R/W)	OCTBR	Output control buffer register
38H	(W)	OCPBR0H	Output compare buffer register 0 (H)
39H	(W)	OCPBR0L	Output compare buffer register 0 (L)
3AH	(W)	OCPBR1H	Output compare buffer register 1 (H)
3BH	(W)	OCPBR1L	Output compare buffer register 1 (L)
3CH	(W)	OCPBR2H	Output compare buffer register 2 (H)
3DH	(W)	OCPBR2L	Output compare buffer register 2 (L)
3EH	(W)	OCPBR3H	Output compare buffer register 3 (H)
3FH	(W)	OCPBR3L	Output compare buffer register 3 (L)
40H to7BH			Vacancy
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	Must not exceed V_{CC}*.
	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	AVR must not exceed AV_{CC} + 0.3 V.
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 0.3	V	
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV1}	—	4	mA	P00 to P07, P21 to P27, P30 to P32, P36, P37, P50 to P57
	I_{OLAV2}	—	15	mA	P40 to P47
“L” level total average output current	$\sum I_{OLAV1}$	—	15	mA	P00 to P07, P21 to P27, P30 to P32, P36, P37, P50 to P57
	$\sum I_{OLAV2}$	—	45	mA	P40 to P47
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	
“H” level total maximum output current	$\sum I_{OH}$	—	–20	mA	
Power consumption	P_D	—	230	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: Use AV_{CC} and V_{CC} set at the same voltage.
AV_{CC} does not exceed V_{CC}, such as when power is turned on.

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	4.5	5.5	V	
	AVR	0.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

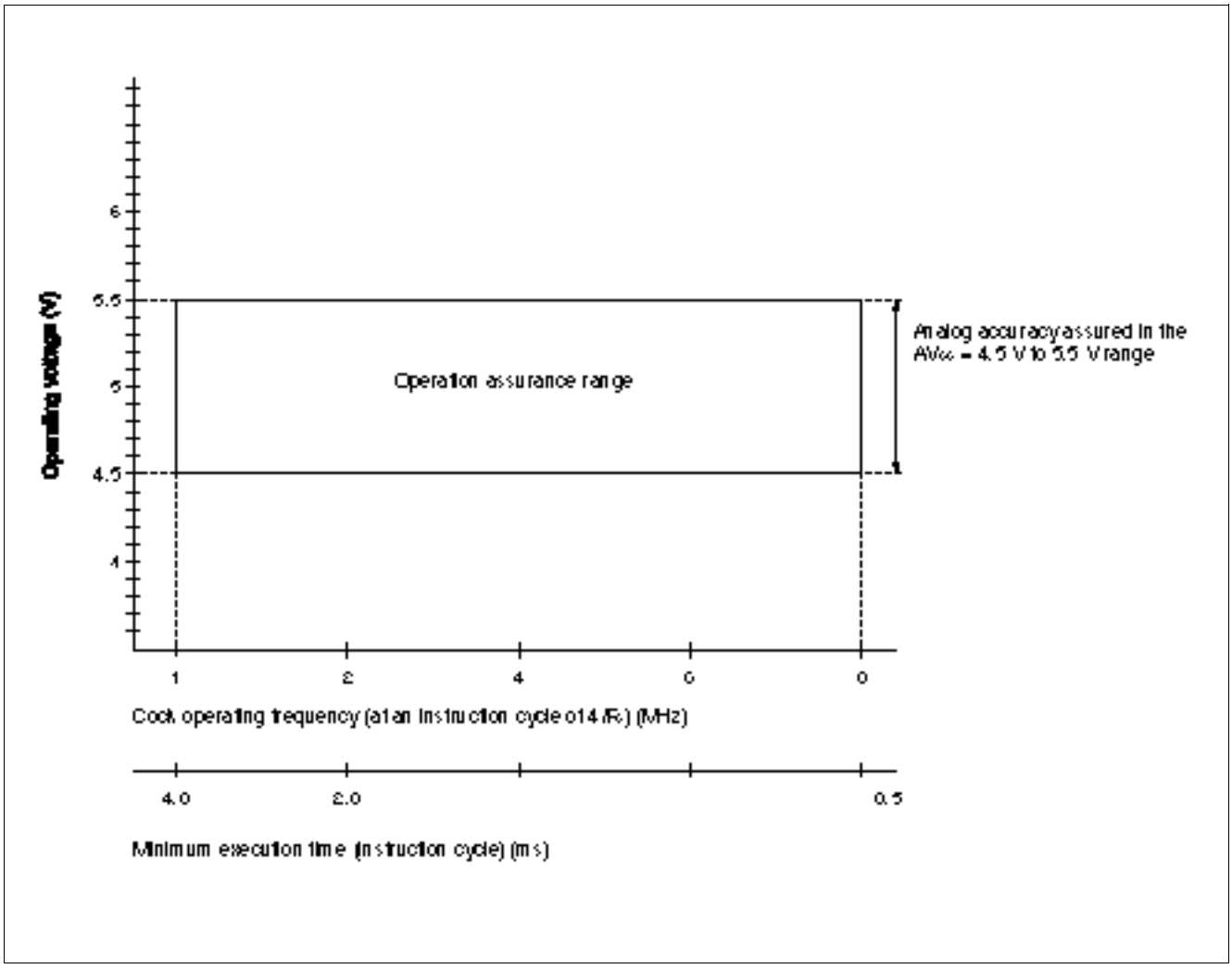


Figure 1 Operating Voltage vs. Clock Operating Frequency

3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, P30 to P32, P36, P37, P40 to P47 P60, P64	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, P30 to P32, P36, P37, P40 to P47 P60, P64	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
"H" level output voltage	V_{OH}	P00 to P07, P21 to P27, P30 to P32, P36, P37, P40 to P47	$I_{OH} = -2.0$ mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P21 to P27, P30 to P32, P36, P37, P50 to P57	$I_{OL} = 1.8$ mA	—	—	0.4	V	
	V_{OL2}	P40 to P47	$I_{OL} = 15$ mA	—	—	1.5	V	
Input leakage current	I_{LI1}	P00 to P07, P21 to P27, P30 to P32, P36, P37, P40 to P47, P50 to P57, P60, P64	0.45 V < V_I < V_{CC}	—	—	±5	µA	
Pull-up resistance	R_{PULL}	$\overline{RST}$	$V_I = 0.0$ V	25	50	100	kΩ	

Power supply current	I_{CC}	V_{CC}	Normal operation (external clock) F_C = 4.2 MHz	—	5	15	mA	
			Normal operation (external clock) F_C = 8 MHz	—	7	18	mA	
	I_{CCS}		Sleep mode (external clock) F_C = 4.2 MHz	—	1	8	mA	
			Sleep mode (external clock) F_C = 8 MHz	—	2	10	mA	
	I_{CCH}		Stop mode T_A = 25 °C	—	—	10	µA	
	I_A	AV_{CC}	F_C = 8 MHz, when A/D conversion is activated	—	6	—	mA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, V_{SS}	f = 1 MHz	—	10	—	pF	

Note: Connect the MOD0 and MOD1 pins directly to V_{SS}.

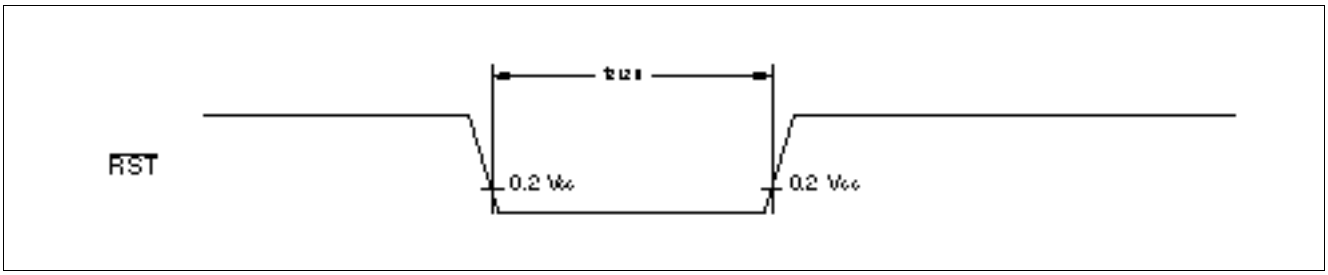
4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{XCYL}*	—	ns	

* : t_{XCYL} is the oscillation cycle (1/Fc) to input to the X0 pin.

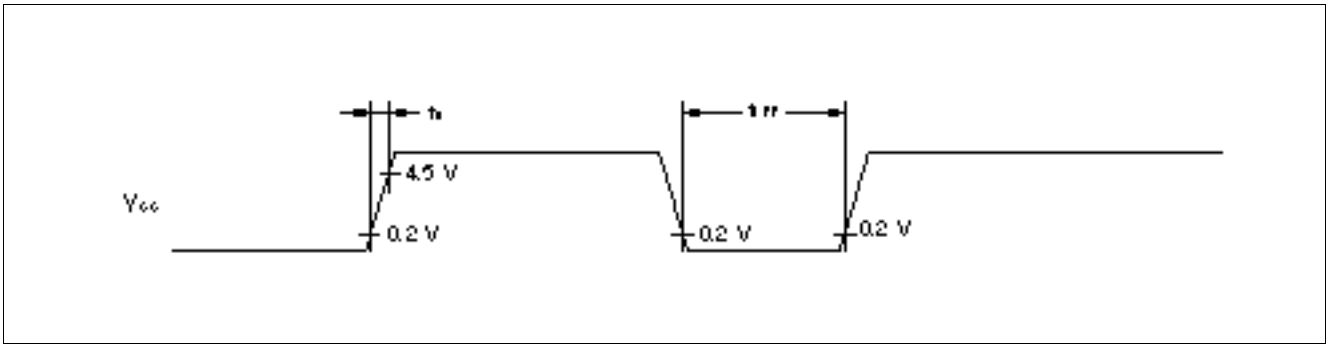


(2) Power-on Reset

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

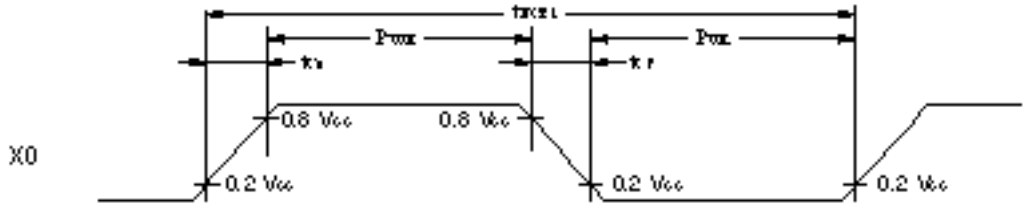


(3) Clock Timing

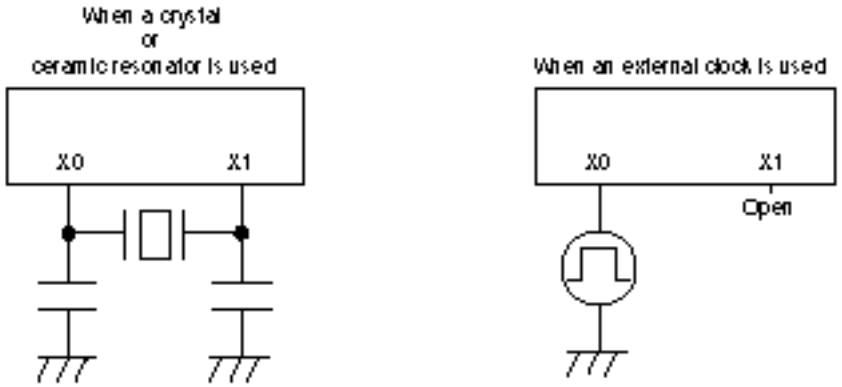
($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	8	MHz	
Clock cycle time	t_{XCYL}			125	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0		35	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}			—	10	ns	External clock

X0 and X1 Timing Conditions



Clock Conditions



(4) Instruction Cycle

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Instruction cycle (minimum execution time)	t_{inst}	0.50	—	4	µs	

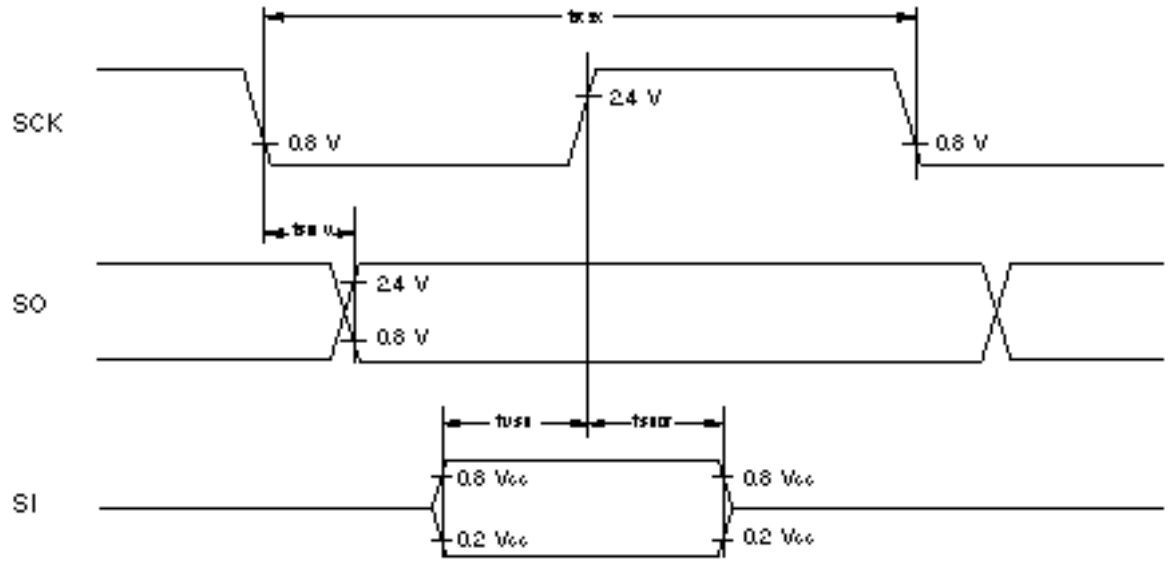
(5) UART

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

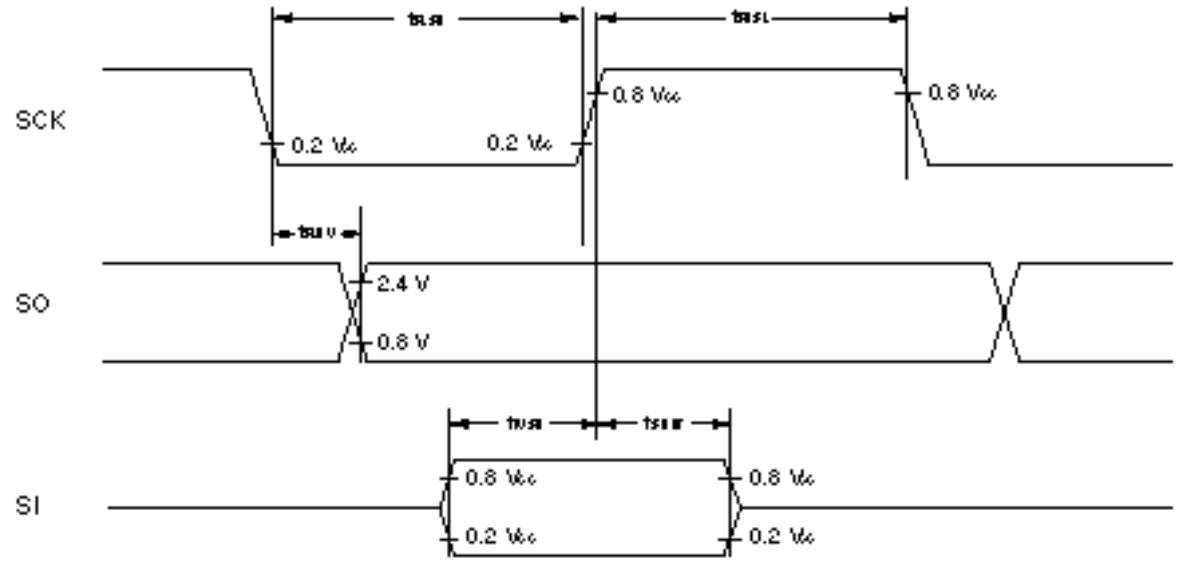
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

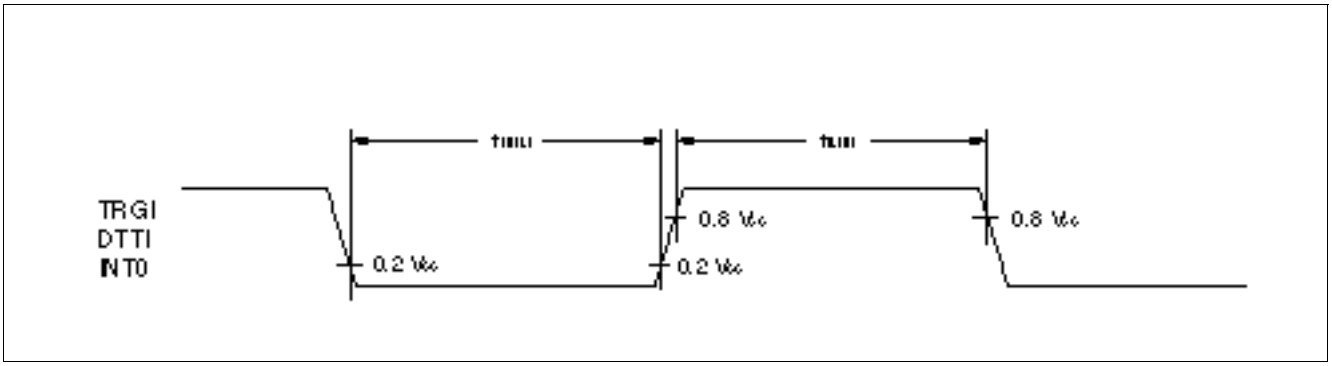


(6) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	TRGI, DTTI, INT0	—	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}			2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

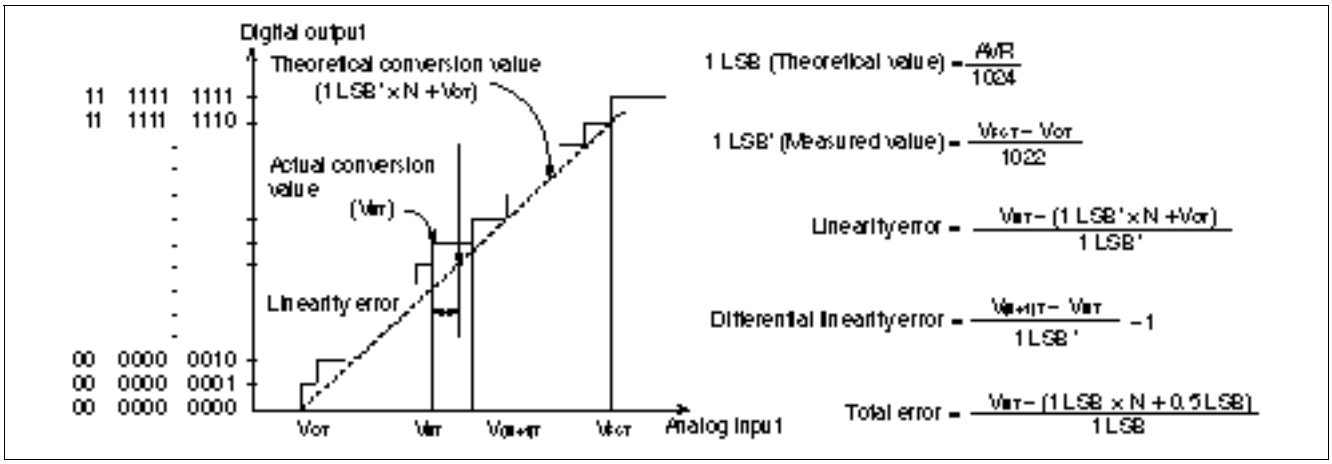
(AV_{CC} = V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C, F_C = 4.2 MHz)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	10	bit	
Linearity error	—	—		—	—	±2.0	LSB	
Differential linearity error	—	—		—	—	±1.5	LSB	
Total error	—	—		—	—	±3.0	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7		AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}	AN0 to AN7		AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	mV	
Interchannel disparity	—	—		—	—	4	LSB	
A/D mode conversion time	—	—		—	33 t_{inst}*	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7		—	—	10	µA	
Analog input voltage	—	AN0 to AN7		0	—	AVR	V	
Reference voltage	—	AVR		0	—	AV_{CC}	V	
Reference voltage supply current	I_R	AVR	AVR = 5.0 V	—	200	—	µA	

* : For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

(1) A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



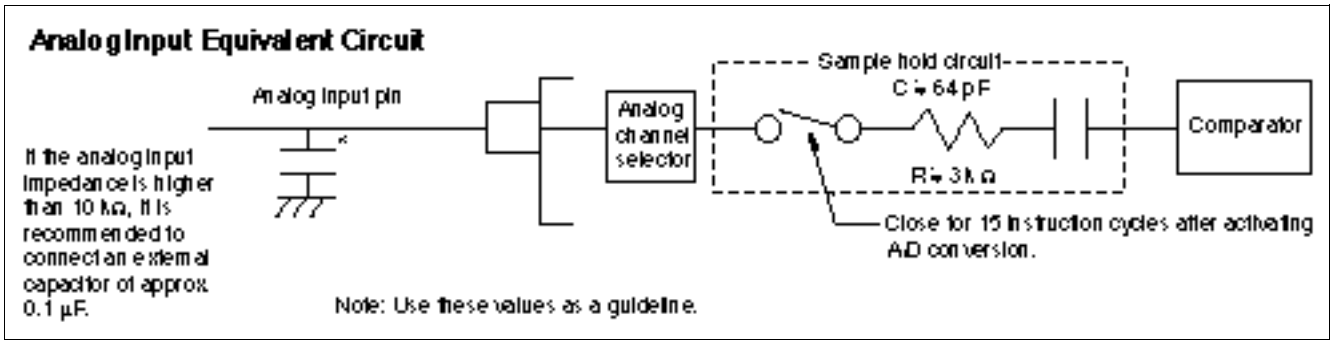
(2) Precautions

- **Input impedance of the analog input pins**

  The A/D converter used for the MB89863 contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for 15 instruction cycles after activating A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 µF for the analog input pin.

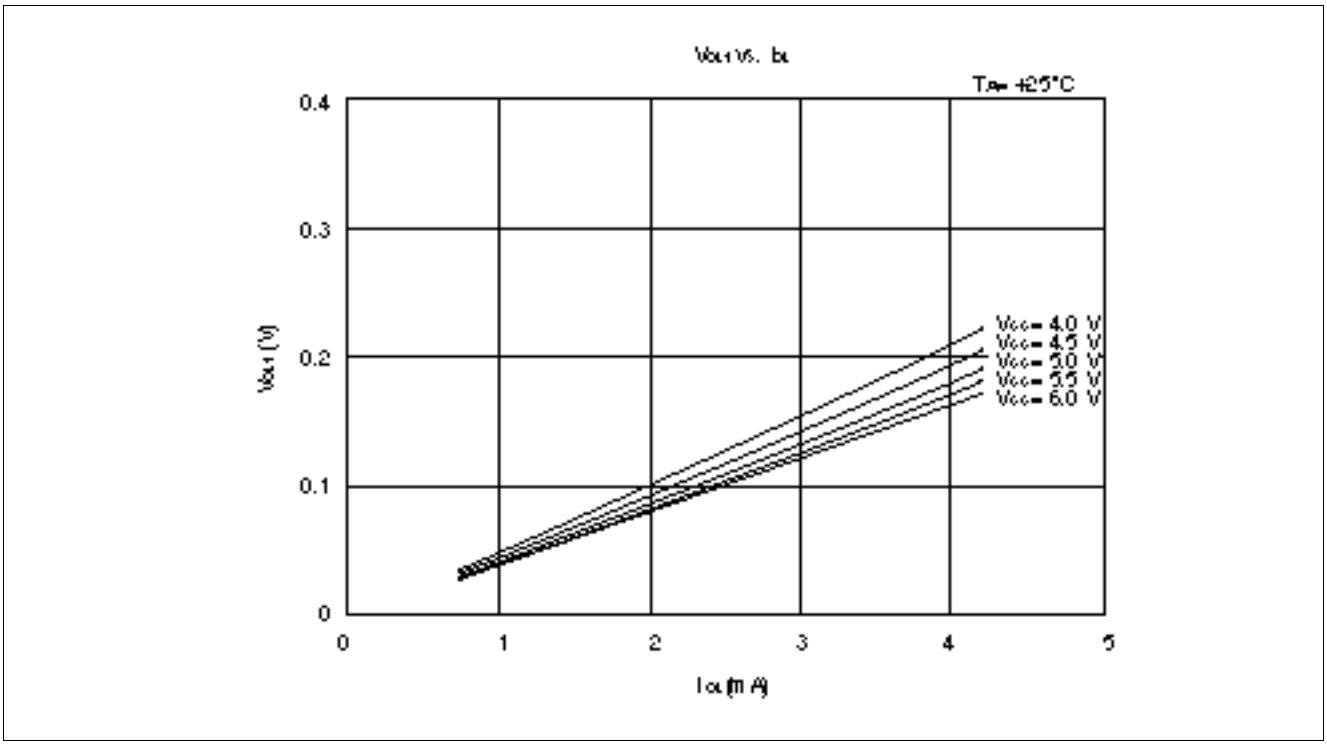


- **Error**

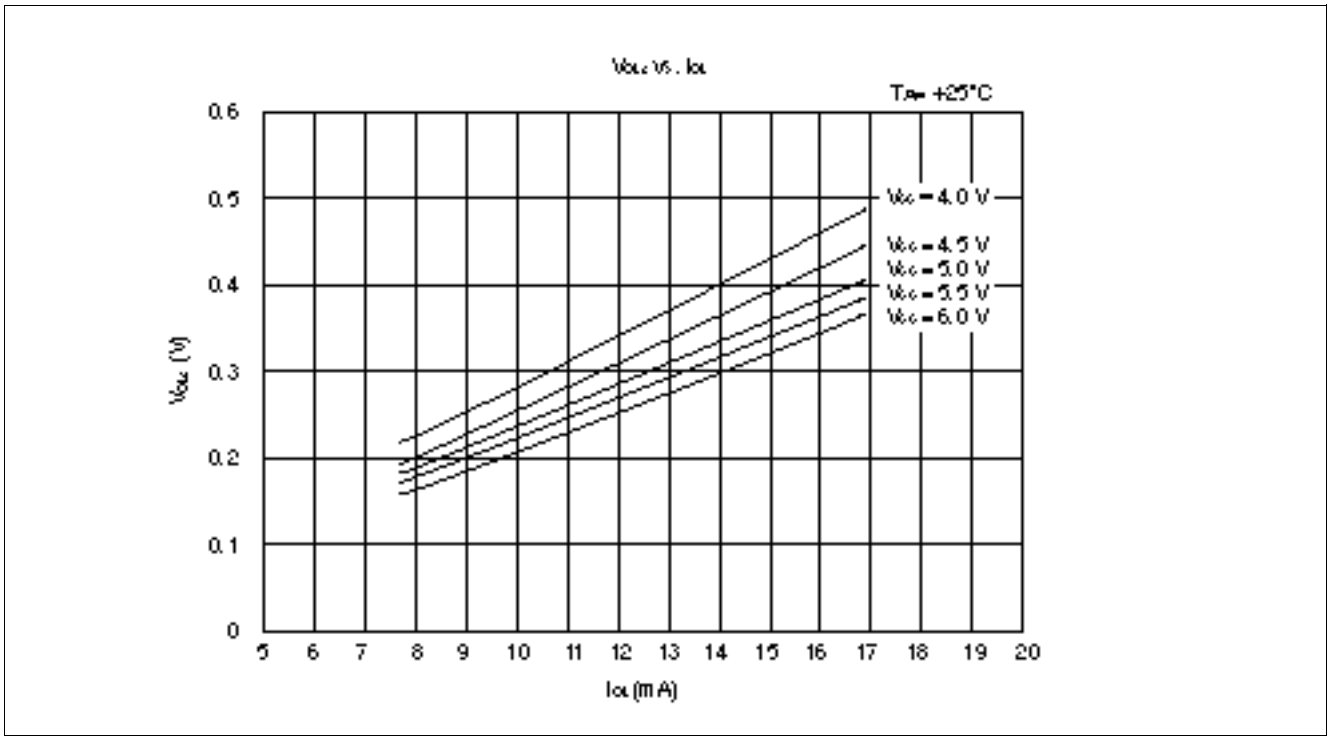
  The smaller the | AVR – AV_{SS} |, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

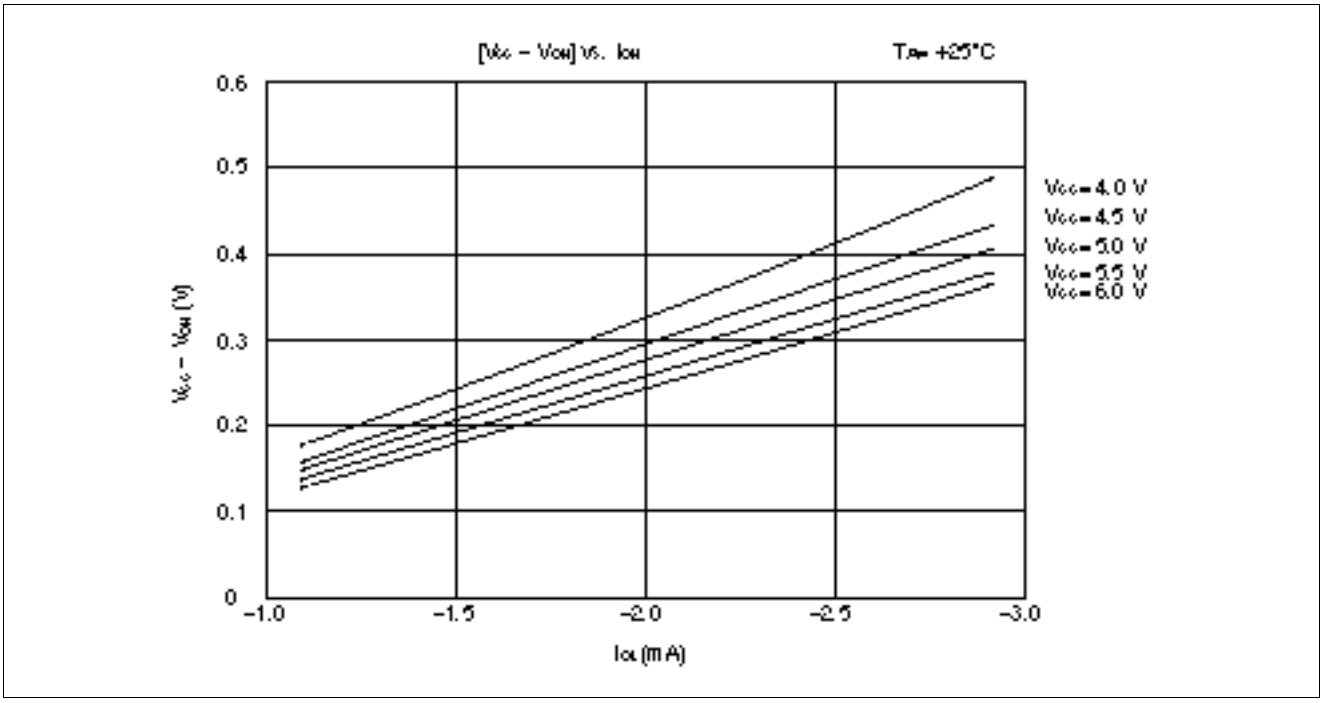
(1) “L” Level Output Voltage (except Port 4)



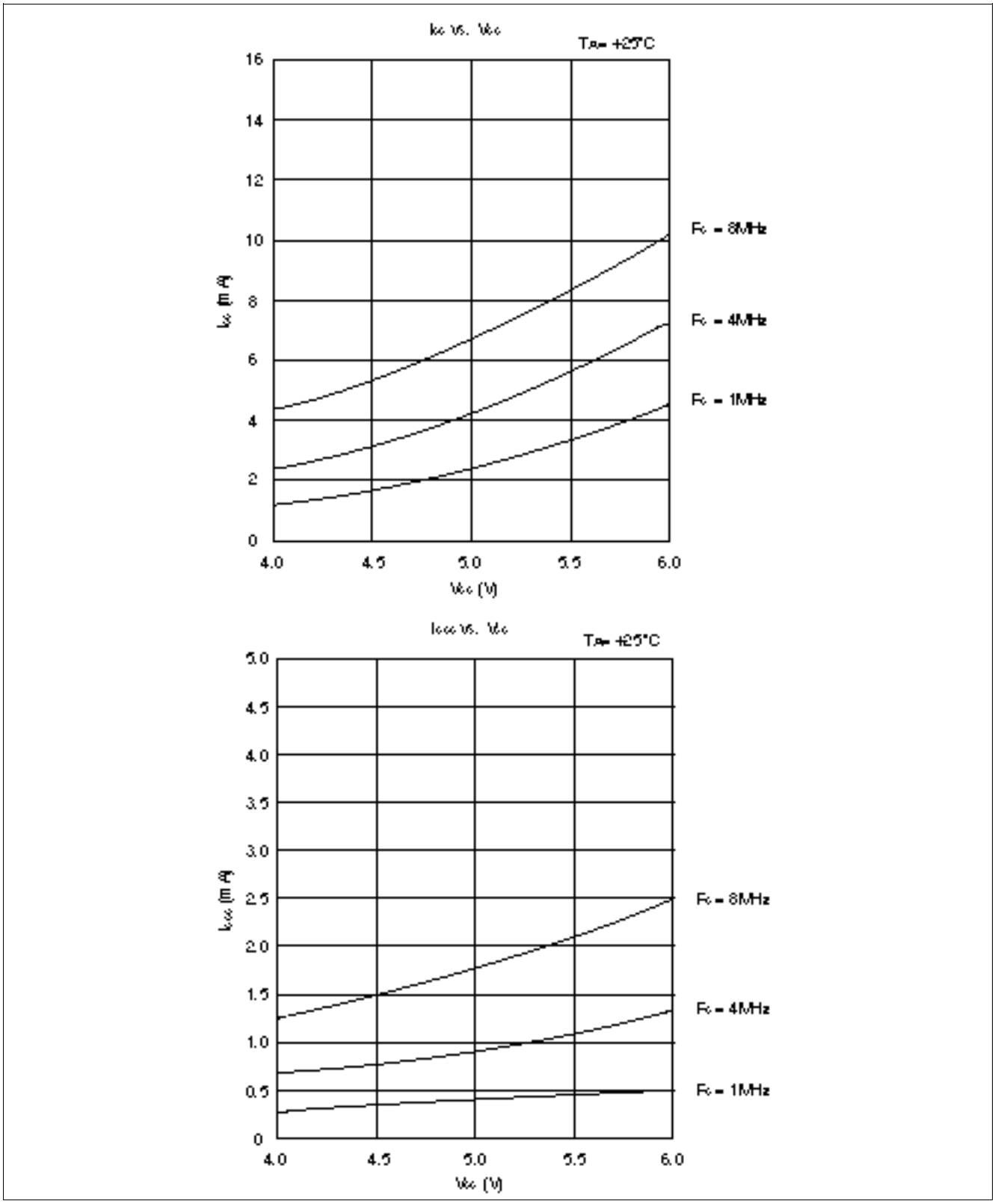
(2) “L” Level Output Voltage (port 4)



(3) “H” Level Output Voltage



(4) Power Supply Current (External Clock)



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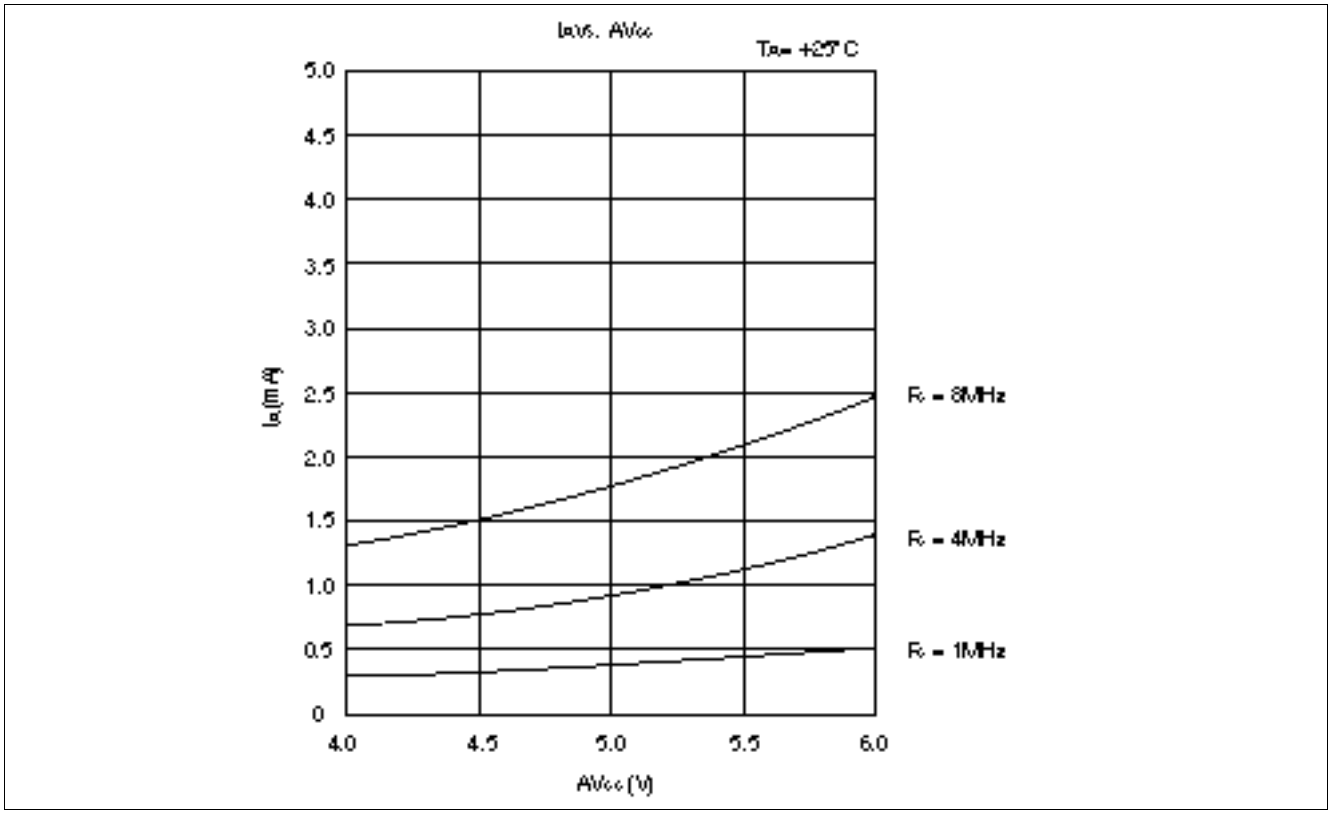
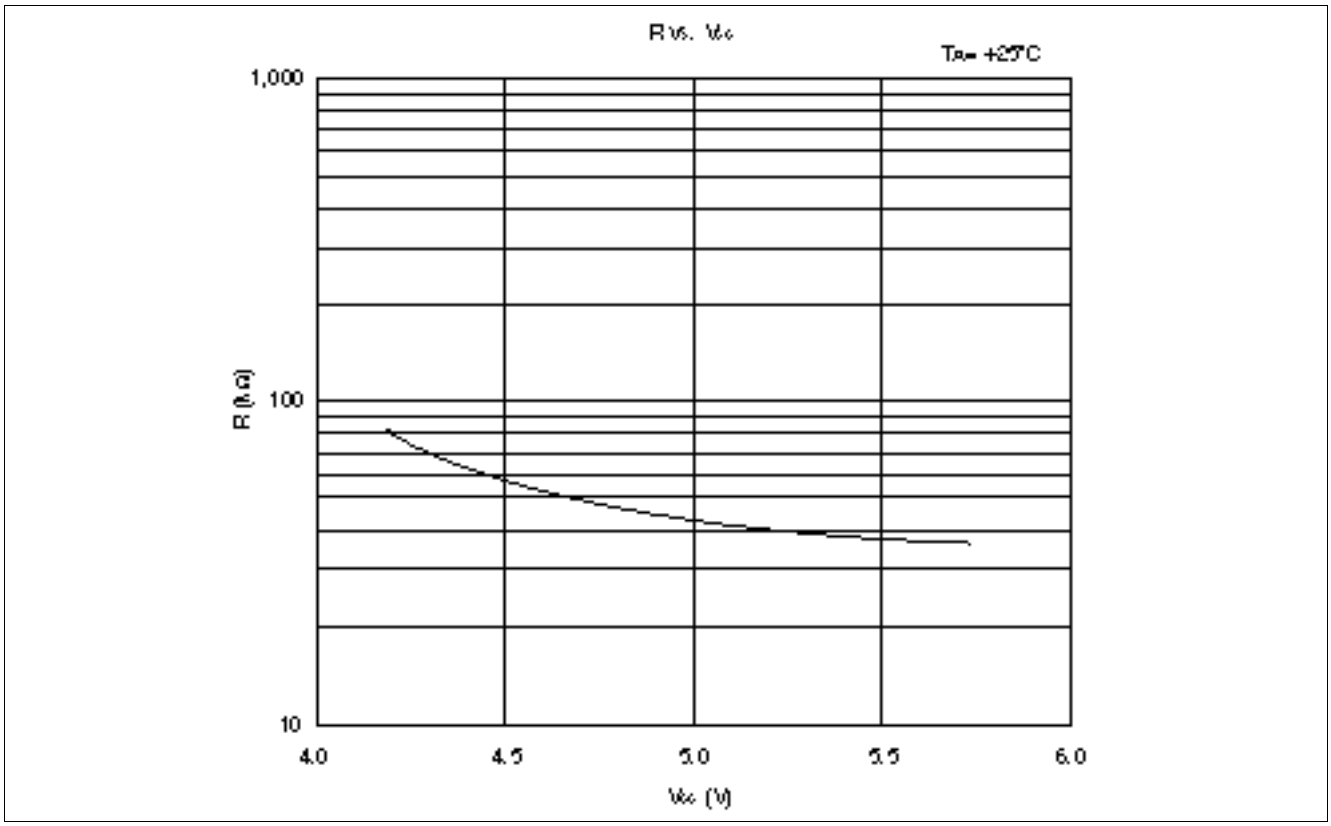


(6) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F^{2}MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A →	–	–	–	+ + – +	03
ROLC A	2	1	← C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Table 4 Branch Instructions (17 instructions)

Mnemonic	#	Operation	TL	TH	AH	N	Z	V	C	OP code
BZ/BEQ rel	2	If Z = 1 then PC ← PC + rel	—	—	—	—	—	—	—	FD
BNZ/BNE rel	2	If Z = 0 then PC ← PC + rel	—	—	—	—	—	—	—	FC
BC/BLO rel	2	If C = 1 then PC ← PC + rel	—	—	—	—	—	—	—	F9
BNC/BHS rel	2	If C = 0 then PC ← PC + rel	—	—	—	—	—	—	—	F8
BN rel	2	If N = 1 then PC ← PC + rel	—	—	—	—	—	—	—	FB
BP rel	2	If N = 0 then PC ← PC + rel	—	—	—	—	—	—	—	FA
BLT rel	2	If V ∀ N = 1 then PC ← PC + rel	—	—	—	—	—	—	—	FF
BGE rel	2	If V ∀ N = 0 then PC ← PC + rel	—	—	—	—	—	—	—	FE
BBC dir: b,rel	3	If (dir: b) = 0 then PC ← PC + rel	—	—	—	—	—	—	—	B0 to B7
BBS dir: b,rel	3	If (dir: b) = 1 then PC ← PC + rel	—	—	—	—	—	—	—	B8 to BF
JMP @A	1	(PC) ← (A)	—	—	—	—	—	—	—	E0
JMP ext	3	(PC) ← ext	—	—	—	—	—	—	—	21
CALLV #vct	1	Vector call	—	—	—	—	—	—	—	E8 to EF
CALL ext	3	Subroutine call	—	—	—	—	—	—	—	31
XCHW A,PC	1	(PC) ← (A),(A) ← (PC) + 1	—	—	—	—	—	—	—	F4
RET	1	Return from subrountine	—	—	—	—	—	—	—	20
RETI	1	Return from interrupt	—	—	—	Restore				30

Table 5 Other Instructions (9 instructions)

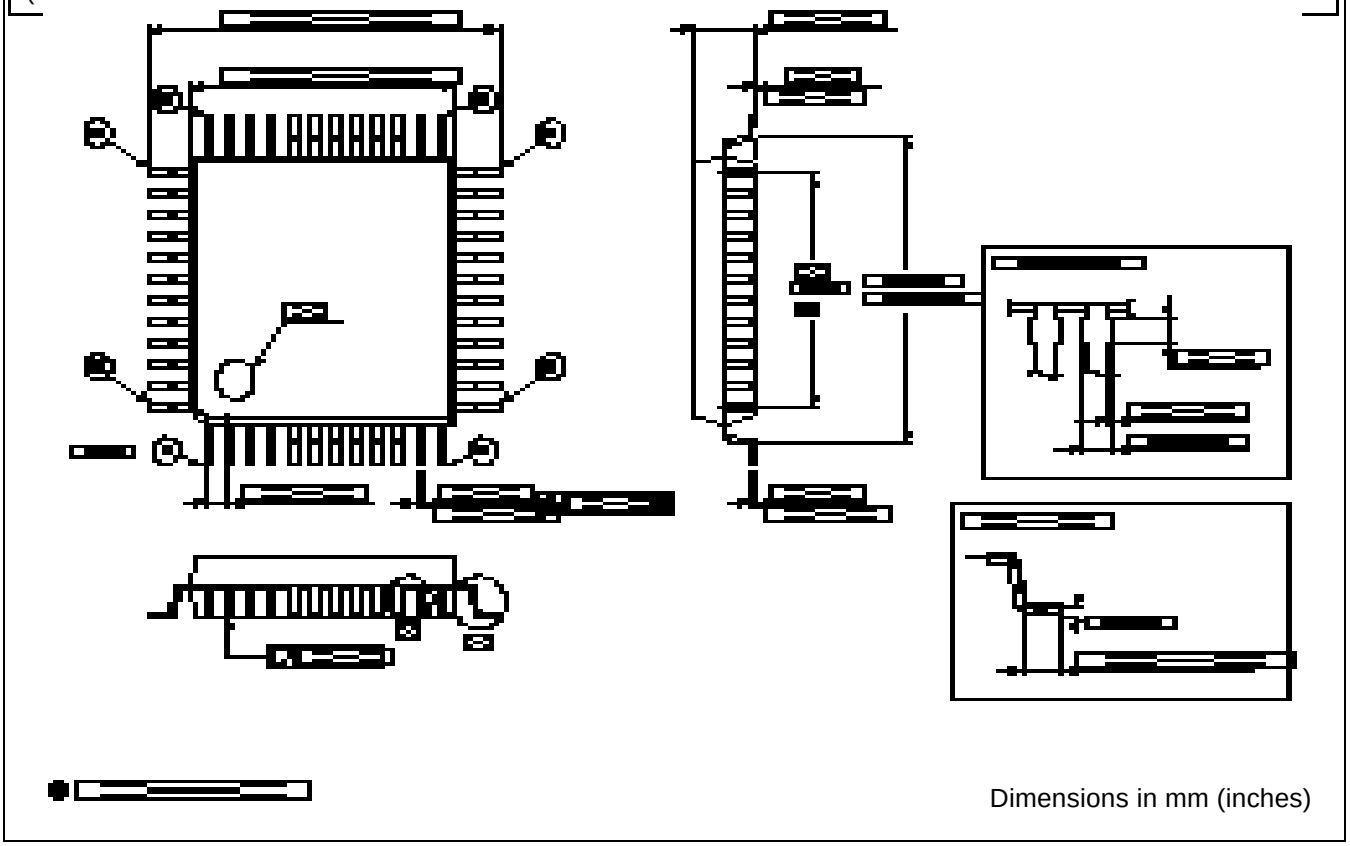
Mnemonic	#	Operation	TL	TH	AH	N	Z	V	C	OP code
PUSHW A	1	(SP) ← (SP) – 2, ((SP)) ← (A)	—	—	—	—	—	—	—	40
POPW A	1	(A) ← ((SP)), (SP) ← (SP) + 2	—	—	—	—	—	—	—	50
PUSHW IX	1	(SP) ← (SP) – 2, ((SP)) ← (IX)	—	—	—	—	—	—	—	41
POPW IX	1	(IX) ← ((SP)), (SP) ← (SP) + 2	—	—	—	—	—	—	—	51
NOP	1	No operation	—	—	—	—	—	—	—	00
CLRB	1	(dir: b) ← 0	—	—	—	—	—	—	—	80 to 87
SETB	1	(dir: b) ← 1	—	—	—	—	—	—	—	90 to 97
CLRI	1	I ← 0	—	—	—	—	—	—	—	81
SETI	1	I ← 1	—	—	—	—	—	—	—	91

H / L	0	1	2	3	4	5	6	7	8	9	A	B	C	D
0	NOP	MULU A	ROLC A	RORC A	MOV A,#d8	MOV A,dir	MOV A,@IX +d	MOV A,@EP	MOV A,R0	MOV A,R1	MOV A,R2	MOV A,R3	MOV A,R4	MOV A,R5
1	MOVW A,PS	DIVU A	INCW A	DECW A	MOVW A,SP	MOVW A,PC	MOVW A,@IX +d	MOVW A,@EP	MOVW A,R0	MOVW A,R1	MOVW A,R2	MOVW A,R3	MOVW A,R4	MOVW A,R5
2	MOVW PS,A	ANDW A	ORW A	XORW A	MOVW A,#d16	MOVW A,dir	MOVW A,@IX +d	MOVW A,@EP	MOVW A,R0	MOVW A,R1	MOVW A,R2	MOVW A,R3	MOVW A,R4	MOVW A,R5
3	MOVW SP,A	CALL addr16	SUBC A	SUBC W,A	SUBC A,#d8	SUBC A,dir	SUBC A,@IX +d	SUBC A,@EP	SUBC A,R0	SUBC A,R1	SUBC A,R2	SUBC A,R3	SUBC A,R4	SUBC A,R5
4	PUSHW A	JMP addr16	ADDC A	ADDC W,A	ADDC A,#d8	ADDC A,dir	ADDC A,@IX +d	ADDC A,@EP	ADDC A,R0	ADDC A,R1	ADDC A,R2	ADDC A,R3	ADDC A,R4	ADDC A,R5
5	MOVW IX,A	RET	CMP A	CMPW A	CMP A,#d8	CMP A,dir	CMP A,@IX +d	CMP A,@EP	CMP A,R0	CMP A,R1	CMP A,R2	CMP A,R3	CMP A,R4	CMP A,R5
6	MOVW A,IX	RETI	AND A	ANDW A	AND A,#d8	AND A,dir	AND A,@IX +d	AND A,@EP	AND A,R0	AND A,R1	AND A,R2	AND A,R3	AND A,R4	AND A,R5
7	PUSHW IX	JMP @A	OR A	ORW A	OR A,#d8	OR A,dir	OR A,@IX +d	OR A,@EP	OR A,R0	OR A,R1	OR A,R2	OR A,R3	OR A,R4	OR A,R5
8	POPW IX	MOV ext,A	XOR A	XORW A	XOR A,#d8	XOR A,dir	XOR A,@IX +d	XOR A,@EP	XOR A,R0	XOR A,R1	XOR A,R2	XOR A,R3	XOR A,R4	XOR A,R5
9	MOVW SP,IX	MOV A,ext	MOV A	MOVW A	MOV A,#d8	MOV A,dir	MOV A,@IX +d	MOV A,@EP	MOV A,R0	MOV A,R1	MOV A,R2	MOV A,R3	MOV A,R4	MOV A,R5
A	PUSH A	MOV @A,T	XCH A,T	XCHW A,T	MOV dir,A	MOV @IX +d,A	MOV @EP,A	MOV R0,A	MOV R1,A	MOV R2,A	MOV R3,A	MOV R4,A	MOV R5,A	
B	POP A	MOV T,@A	CLRB dir: 0	CLRB dir: 1	CLRB dir: 2	CLRB dir: 3	CLRB dir: 4	CLRB dir: 5	CLRB dir: 6	CLRB dir: 7	SETB dir: 0	SETB dir: 1	SETB dir: 2	SETB dir: 3	SETB dir: 4	SETB dir: 5
C	PUSH IX	MOVW PS,A	BBC dir: 0,rel	BBC dir: 1,rel	BBC dir: 2,rel	BBC dir: 3,rel	BBC dir: 4,rel	BBC dir: 5,rel	BBC dir: 6,rel	BBC dir: 7,rel	BBS dir: 0,rel	BBS dir: 1,rel	BBS dir: 2,rel	BBS dir: 3,rel	BBS dir: 4,rel	BBS dir: 5,rel
D	POP IX	MOVW A,PS	INCW SP	DECW SP	MOVW SP,#d16	MOVW dir,A	MOVW A,@IX +d	MOVW A,@EP	MOVW A,R0	MOVW A,R1	MOVW A,R2	MOVW A,R3	MOVW A,R4	MOVW A,R5		
E	MOVW A,SP	MOVW IX,A	MOVW A,IX	XCHW A,IX	MOVW EP,#d8	MOVW EP,A	MOVW @IX +d,A	MOVW @EP,A	MOVW R0,A	MOVW R1,A	MOVW R2,A	MOVW R3,A	MOVW R4,A	MOVW R5,A		
F	MOVW SP,#d16	CALLV #1	CALLV #2	CALLV #3	CALLV #4	CALLV #5	CALLV #6	CALLV #7	BNC rel	BC rel	BP rel	BN rel	BNZ rel	BZ rel		

■ INSTRUCTION MAP

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89863PMC-XXX (XXX = ROM No.)	48-pin Plastic QFP (FPT-48P-M04)	



Dimensions in mm (inches)

■ [illegible]ENSIONS

MEMO

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