FUJITSU

Corrections of Datasheet

MB90595/595G -

DS90595_add_V100

Addendum, MB90595 Datasheet (DS07-13705-5E)

This is the Addendum for the Datasheet DS07-13705-4E of the MB90595/595G microcontroller series. It describes all known discrepancies of the MB90595/595G microcontroller series datasheet.

Ref. Number	Date	Version No.	Chapter/Page	Description/Correction
(Text Link)	dd.mm.yy			

DS90595001	05.06.01	1.00	AC Characteristics	Table Clock timing : External clock range added
DS90595002	05.06.01	1.00	Handling Devices	Ports behaviour during Power on

AC Characteristics:

Table 1 is incorrect, see correction below:

(1) Clock Timing:

Parameter	Symbol	Pin	Value			Units	Remarks
			Min.	Typ.	Max.		
Oscillation frequency	f_c	X0,X1	3	--	5	MHz	When using oscillation circuit
Oscillation cycle time	t_{CYL}	X0,X1	200	--	333	ns	When using oscillation circuit
External clock frequency	f_c	X0,X1	3	--	16	MHz	When using external clock
External clock cycle time	t_{CYL}	X0,X1	62.5	--	333	ns	When using external clock
Input clock pulse width	P_{WH}, P_{WL}	X0	10	--	--	ns	Duty ratio is about 30 to 70%
Input clock rise and fall time	t_{CR}, t_{CF}	X0	--	--	5	ns	When using external clock
Machine clock frequency	f_{CP}	--	1.5	--	16	MHz	
Machine clock cycle	t_{CP}	--	62.5	--	666	ns	
Flash Read cycle time	t_{CYCL}	--	--	$2*t_{CP}$	--	ns	When Flash is accessed by CPU

*: Frequency Deviation indicates the maximum Frequency difference from the target frequency when using a multiplied clock

Power-On Reset

Output "unknown value" , when the power supply Is turned on If F^2MC-16LX is used. (Note)

1.Device covered

MB90V595, MB90V595G, MB90598, MB90F598, MB90F598G

2. Note:

During testing it has been found that some port pins may enter an undefined state during power on. By asserting RSTx during the power on reset (2^{17} cycles of main clock) port pins can be forced to high impedance.

1. The following Ports will output a High Impedance (Hi-z) at the terminal when the power supply is turned on when PONR and RSTX = 1 (RSTx not asserted):

P20 – P45, P50 – P67, P90 – P95

2. The following ports can be forced to high impedance state (Hi-z) during PONR if RSTX is asserted during power on (2^{17} cycles of main clock) or with the End of POMR and the Start of the internal clock

P00 – P03, P16 – P17, P46 – P47, P70 – P87

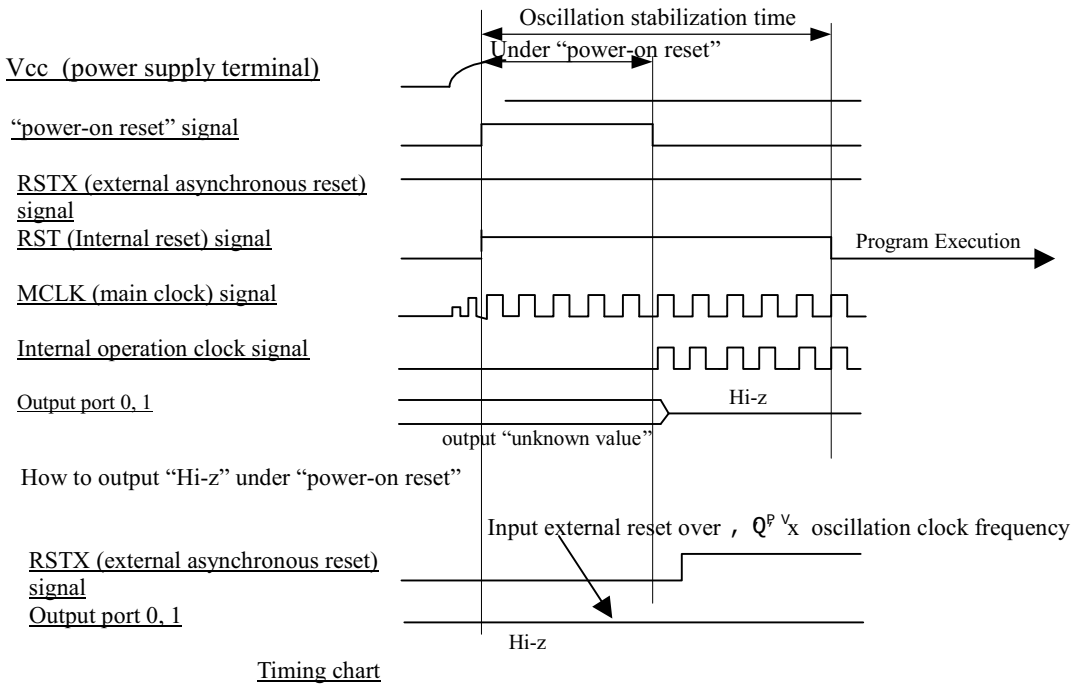
3. The following Ports will output an High-Z with the End of PONR and the Start of internal clocks. RSTx does not force the pins to High-Z during power on.

P04 – P15

Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)

- PONR: Power on Reset
- RSTX: Reset input pin

The following diagram shows the timing chart in detail.



Under “power-on reset” 2^{17} x oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation 2^{18} x oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz)