

# 16-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90595/595G Series

### MB90598/598G/F598/F598G/V595/V595G

#### ■ DESCRIPTION

The MB90595/595G series with FULL-CAN\*1 interface and FLASH ROM is especially designed for automotive and industrial applications. Its main features are two on board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The instruction set of F<sup>2</sup>MC-16LX CPU core inherits an AT architecture of the F<sup>2</sup>MC\*2 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

The MB90595/595G series has peripheral resources of 8/10-bit A/D converters, UART (SCI), extended I/O serial interface, 8/16-bit PPG timer, I/O timer (input capture (ICU), output compare (OCU)) and stepping motor controller.

\*1: Controller Area Network (CAN) - License of Robert Bosch GmbH

\*2: F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller.

#### ■ FEATURES

- Clock

Embedded PLL clock multiplication circuit

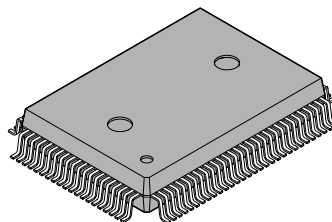
Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).

Minimum instruction execution time: 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V<sub>CC</sub> of 5.0 V)

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#### ■ PACKAGE

100-pin Plastic QFP



(FPT-100P-M06)

# MB90595/595G Series

(Continued)

- Instruction set to optimize controller applications
  - Rich data types (bit, byte, word, long word)
  - Rich addressing mode (23 types)
  - Enhanced signed multiplication/division instruction and RETI instruction functions
  - Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
  - Adoption of system stack pointer
  - Enhanced pointer indirect instructions
  - Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed: 4-byte instruction queue
- Enhanced interrupt function: 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  - Extended intelligent I/O service function (EI<sup>2</sup>OS): Up to 10 channels
- Embedded ROM size and types
  - Mask ROM: 128 Kbytes
  - Flash ROM: 128 Kbytes
  - Embedded RAM size: 4 Kbytes (MB90V595/595G : 6 Kbytes)
- Flash ROM
  - Supports automatic programming, Embedded Algorithm ™\*
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the algorithm
  - Hard-wired reset vector available in order to point to a fixed boot sector
  - Erase can be performed on each block
  - Block protection with external programming voltage
- Low-power consumption (stand-by) mode
  - Sleep mode (mode in which CPU operating clock is stopped)
  - Stop mode (mode in which oscillation is stopped)
  - CPU intermittent operation mode
  - Hardware stand-by mode
- Process: 0.5 μm CMOS technology
- I/O port
  - General-purpose I/O ports: 78 ports
  - Push-pull output and Schmitt trigger input.
  - Programmable on each bit as I/O or signal for peripherals.
- Timer
  - Watchdog timer: 1 channel
  - 8/16-bit PPG timer: 8/16-bit × 6 channels
  - 16-bit re-load timer: 2 channels
- 16-bit I/O timer
  - Input capture: 4 channels
  - Output compare: 4 channels
- Extended I/O serial interface: 1 channel
- UART0
  - With full-duplex double buffer (8-bit length)
  - Clock asynchronous or clock synchronized (with start/stop bit) transmission can be selectively used.

- UART1 (SCI)  
With full-duplex double buffer (8-bit length)  
Clock asynchronous or clock synchronized serial transmission (I/O extended transmission) can be selectively used.
- Stepping motor controller (4 channels)
- External interrupt circuit (8 channels)  
A module for starting an extended intelligent I/O service (EI<sup>2</sup>OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module: Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)  
8/10-bit resolution can be selectively used.  
Starting by an external trigger input.
- FULL-CAN interface: 1 channel  
Conforming to Version 2.0 Part A and Part B  
Flexible message buffering (mailbox and FIFO buffering can be mixed)
- 18-bit Time-base counter
- External bus interface: Maximum address space 16 Mbytes

\*: Embedded Algorithm is a trademark of Advanced Micro Devices Inc.

# MB90595/595G Series

## ■ PRODUCT LINEUP

| Features                          |                        | MB90598<br>MB90598G (under development)   | MB90F598/F598G                                      | MB90V595/V595G     |
|-----------------------------------|------------------------|---|---|--------------------|
| Classification                    |                        | Mask ROM product  | Flash ROM product                                   | Evaluation product |
| ROM size                          |                        | 128 Kbytes  | 128 Kbytes<br>Boot block<br>Hard-wired reset vector | None               |
| RAM size                          |                        | 4 Kbytes  | 4 Kbytes  | 6 Kbytes           |
| Emulator-specific power supply *1 |                        | —   |   | None               |
| CPU functions                     |                        | The number of instructions: 351<br>Instruction bit length: 8 bits, 16 bits<br>Instruction length: 1 byte to 7 bytes<br>Data bit length: 1 bit, 8 bits, 16 bits<br>Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz)<br>Interrupt processing time: 1.5 μs<br>(at machine clock frequency of 16 MHz, minimum value)  |   |                    |
| UART0                             |                        | Clock synchronized transmission (500 K/1 M/2 Mbps)<br>Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz)<br>Transmission can be performed by bi-directional serial transmission or by master/ slave connection.   |   |                    |
| UART1(SCI)                        |                        | Clock synchronized transmission (62.5 K/125 K/250 K/500 K/1 Mbps)<br>Clock asynchronized transmission (1202/2404/4808/9615/31250 bps)<br>Transmission can be performed by bi-directional serial transmission or by master/ slave connection.  |   |                    |
| 8/10-bit A/D converter            |                        | Conversion precision: 8/10-bit can be selectively used.<br>Number of inputs: 8<br>One-shot conversion mode (converts selected channel once only)<br>Scan conversion mode (converts two or more successive channels and can program up to 8 channels)<br>Continuous conversion mode (converts selected channel continuously)<br>Stop conversion mode (converts selected channel and stop operation repeatedly) |   |                    |
| 8/16-bit PPG timers (6 channels)  |                        | Number of channels: 6 (8/16-bit × 6 channels)<br>PPG operation of 8-bit or 16-bit<br>A pulse wave of given intervals and given duty ratios can be output.<br>Pulse interval: $f_{sys}$ , $f_{sys}/2^1$ , $f_{sys}/2^2$ , $f_{sys}/2^3$ , $f_{sys}/2^4$ ( $f_{sys}$ = system clock frequency )<br>128μs ( $f_{osc}$ = 4MHz : oscillation clock frequency)  |   |                    |
| 16-bit Reload timer               |                        | Number of channels: 2<br>Operation clock frequency: $f_{sys}/2^1$ , $f_{sys}/2^3$ , $f_{sys}/2^5$ ( $f_{sys}$ = System clock frequency)<br>Supports External Event Count function   |   |                    |
| 16-bit I/O timer                  | 16-bit Output compares | Number of channels: 4<br>Pin input factor: A match signal of compare register   |   |                    |
|                                   | Input captures         | Number of channels: 4<br>Rewriting a register value upon a pin input (rising, falling, or both edges)   |   |                    |

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# MB90595/595G Series

(Continued)

| Features                                  | MB90598<br>MB90598G (under development)   | MB90F598/F598G | MB90V595/V595G |
|---|---|----------------|----------------|
| CAN Interface                             | Number of channels: 1<br>Conforms to CAN Specification Version 2.0 Part A and B<br>Automatic re-transmission in case of error<br>Automatic transmission responding to Remote Frame<br>Prioritized 16 message buffers for data and ID's<br>Supports multiple messages<br>Flexible configuration of acceptance filtering:<br>Full bit compare / Full bit mask / Two partial bit masks<br>Supports up to 1Mbps<br>CAN bit timing setting:<br>MB90xxx:TSEG2 $\geq$ RSJW+2TQ<br>MB90xxxG:TSEG2 $\geq$ RSJW |                |                |
| Stepping motor controller<br>(4 channels) | Four high current outputs for each channel<br>Synchronized two 8-bit PWM's for each channel   |                |                |
| External interrupt circuit                | Number of inputs: 8<br>Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.   |                |                |
| Serial IO                                 | Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz)<br>LSB first/MSB first  |                |                |
| Watchdog timer                            | Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms<br>(at oscillation of 4 MHz, minimum value)   |                |                |
| Flash Memory                              | Supports automatic programming, Embedded Algorithm™ and Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory<br>Boot block configuration<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Writer from Minato Electronics Inc.   |                |                |
| Low-power consumption<br>(stand-by) mode  | Sleep/stop/CPU intermittent operation/clock timer/hardware stand-by   |                |                |
| Process                                   | CMOS  |                |                |
| Power supply voltage for operation*2      | +5 V $\pm$ 10 %   |                |                |
| Package                                   | QFP-100   |                | PGA-256        |

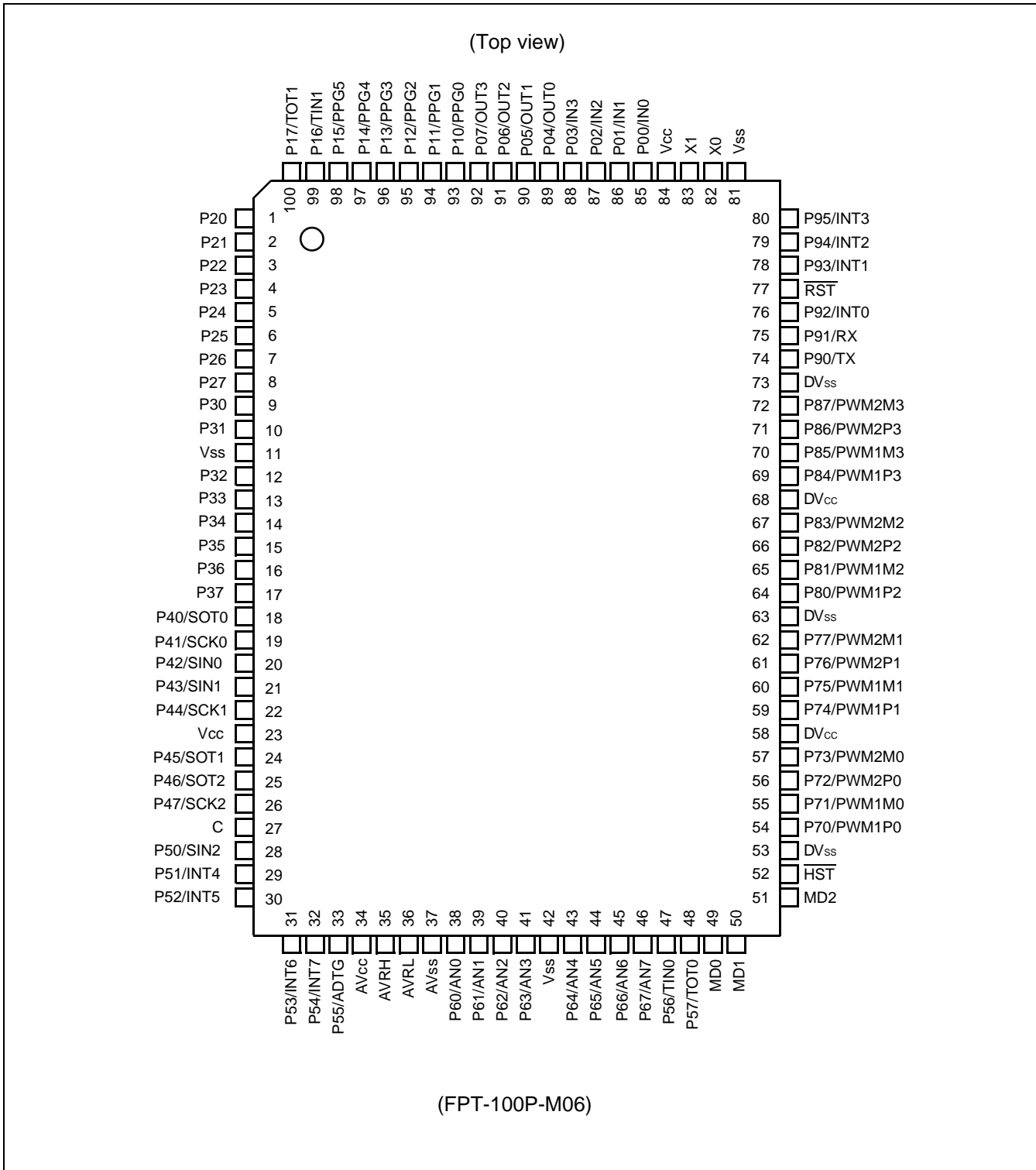
\*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.

Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

\*2: Varies with conditions such as the operating frequency. (See section "■ ELECTRICAL CHARACTERISTICS.")

# MB90595/595G Series

## PIN ASSIGNMENT



## ■ PIN DESCRIPTION

| Pin no.  | Pin name                | Circuit type | Function                                      |
|----------|-------------------------|--------------|---|
| 82       | X0                      | A            | Oscillator pin                                |
| 83       | X1                      |              |   |
| 77       | $\overline{\text{RST}}$ | B            | Reset input                                   |
| 52       | $\overline{\text{HST}}$ | C            | Hardware standby input                        |
| 85 to 88 | P00 to P03              | G            | General purpose IO                            |
|          | IN0 to IN3              |              | Inputs for the Input Captures                 |
| 89 to 92 | P04 to P07              | G            | General purpose IO                            |
|          | OUT0 to OUT3            |              | Outputs for the Output Compares.              |
| 93 to 98 | P10 to P15              | D            | General purpose IO                            |
|          | PPG0 to PPG5            |              | Outputs for the Programmable Pulse Generators |
| 99       | P16                     | D            | General purpose IO                            |
|          | TIN1                    |              | TIN input for the 16-bit Reload Timer 1       |
| 100      | P17                     | D            | General purpose IO                            |
|          | TOT1                    |              | TOT output for the 16-bit Reload Timer 1      |
| 1 to 8   | P20 to P27              | G            | General purpose IO                            |
| 9 to 10  | P30 to P31              | G            | General purpose IO                            |
| 12 to 16 | P32 to P36              | G            | General purpose IO                            |
| 17       | P37                     | D            | General purpose IO                            |
| 18       | P40                     | G            | General purpose IO                            |
|          | SOT0                    |              | SOT output for UART 0                         |
| 19       | P41                     | G            | General purpose IO                            |
|          | SCK0                    |              | SCK input/output for UART 0                   |
| 20       | P42                     | G            | General purpose IO                            |
|          | SIN0                    |              | SIN input for UART 0                          |
| 21       | P43                     | G            | General purpose IO                            |
|          | SIN1                    |              | SIN input for UART 1                          |
| 22       | P44                     | G            | General purpose IO                            |
|          | SCK1                    |              | SCK input/output for UART 1                   |
| 24       | P45                     | G            | General purpose IO                            |
|          | SOT1                    |              | SOT output for UART 1                         |
| 25       | P46                     | G            | General purpose IO                            |
|          | SOT2                    |              | SOT output for the Serial IO                  |
| 26       | P47                     | G            | General purpose IO                            |
|          | SCK2                    |              | SCK input/output for the Serial IO            |

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# MB90595/595G Series

| Pin no.  | Pin name                             | Circuit type | Function  |
|----------|--------------------------------------|--------------|---|
| 28       | P50                                  | D            | General purpose IO                                  |
|          | SIN2                                 |              | SIN Input for the Serial IO                         |
| 29 to 32 | P51 to P54                           | D            | General purpose IO                                  |
|          | INT4 to INT7                         |              | External interrupt input for INT4 to INT7           |
| 33       | P55                                  | D            | General purpose IO                                  |
|          | ADTG                                 |              | Input for the external trigger of the A/D Converter |
| 38 to 41 | P60 to P63                           | E            | General purpose IO                                  |
|          | AN0 to AN3                           |              | Inputs for the A/D Converter                        |
| 43 to 46 | P64 to P67                           | E            | General purpose IO                                  |
|          | AN4 to AN7                           |              | Inputs for the A/D Converter                        |
| 47       | P56                                  | D            | General purpose IO                                  |
|          | TIN0                                 |              | TIN input for the 16-bit Reload Timer 0             |
| 48       | P57                                  | D            | General purpose IO                                  |
|          | TOT0                                 |              | TOT output for the 16-bit Reload Timer 0            |
| 54 to 57 | P70 to P73                           | F            | General purpose IO                                  |
|          | PWM1P0<br>PWM1M0<br>PWM2P0<br>PWM2M0 |              | Output for Stepper Motor Controller channel 0       |
| 59 to 62 | P74 to P77                           | F            | General purpose IO                                  |
|          | PWM1P1<br>PWM1M1<br>PWM2P1<br>PWM2M1 |              | Output for Stepper Motor Controller channel 1       |
| 64 to 67 | P80 to P83                           | F            | General purpose IO                                  |
|          | PWM1P2<br>PWM1M2<br>PWM2P2<br>PWM2M2 |              | Output for Stepper Motor Controller channel 2       |
| 69 to 72 | P84 to P87                           | F            | General purpose IO                                  |
|          | PWM1P3<br>PWM1M3<br>PWM2P3<br>PWM2M3 |              | Output for Stepper Motor Controller channel 3       |
| 74       | P90                                  | D            | General purpose IO                                  |
|          | TX                                   |              | TX output for CAN Interface                         |
| 75       | P91                                  | D            | General purpose IO                                  |
|          | RX                                   |              | RX input for CAN Interface                          |

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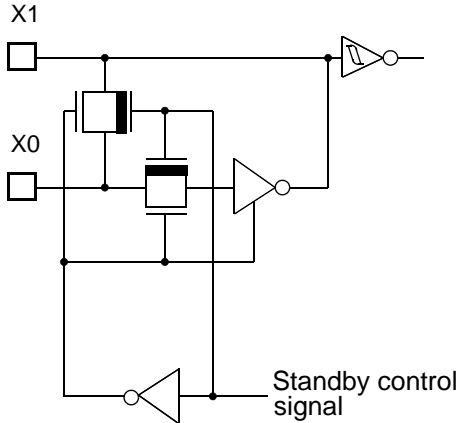
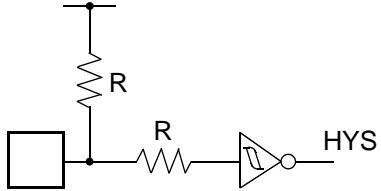
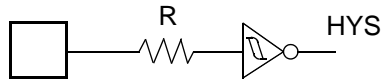
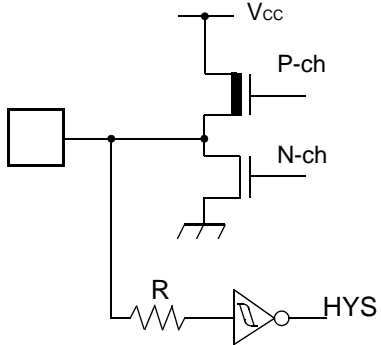
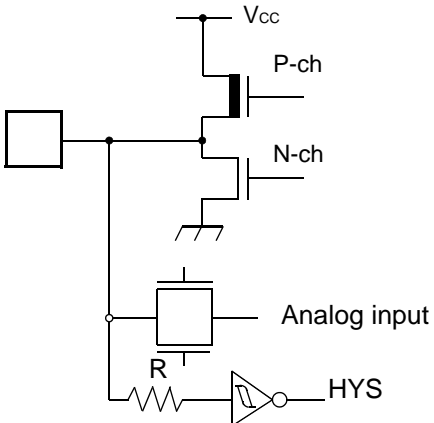
# MB90595/595G Series

(Continued)

| Pin no.    | Pin name         | Circuit type | Function  |
|------------|------------------|--------------|---|
| 76         | P92              | D            | General purpose IO  |
|            | INT0             |              | External interrupt input for INT0   |
| 78 to 80   | P93 to P95       | D            | General purpose IO  |
|            | INT1 to INT3     |              | External interrupt input for INT1 to INT3   |
| 58, 68     | DV <sub>CC</sub> | —            | Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)                          |
| 53, 63, 73 | DV <sub>SS</sub> | —            | Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)                                |
| 34         | AV <sub>CC</sub> | Power supply | Dedicated power supply pin for the A/D Converter  |
| 37         | AV <sub>SS</sub> | Power supply | Dedicated ground pin for the A/D Converter  |
| 35         | AVRH             | Power supply | Upper reference voltage input for the A/D Converter   |
| 36         | AVRL             | Power supply | Lower reference voltage input for the A/D Converter   |
| 49, 50     | MD0<br>MD1       | C            | Operating mode selection input pins. These pins should be connected to V <sub>CC</sub> or V <sub>SS</sub> . |
| 51         | MD2              | H            | Operating mode selection input pin. This pin should be connected to V <sub>CC</sub> or V <sub>SS</sub> .    |
| 27         | C                | —            | External capacitor pin. A capacitor of 0.1μF should be connected to this pin and V <sub>SS</sub> .          |
| 23, 84     | V <sub>CC</sub>  | Power supply | Power supply pins (5.0 V).  |
| 11, 42, 81 | V <sub>SS</sub>  | Power supply | Ground pins (0.0 V).  |

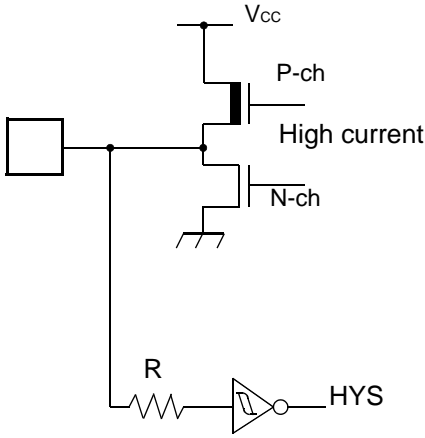
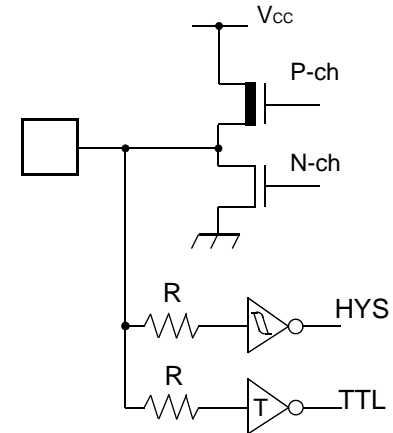
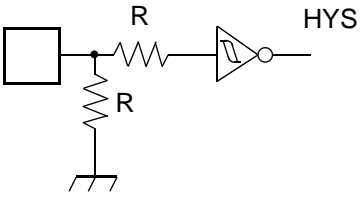
# MB90595/595G Series

## I/O CIRCUIT TYPE

| Circuit Type | Circuit   | Remarks  |
|--------------|---|--|
| A            |    | <ul style="list-style-type: none"> <li>Oscillation feedback resistor: 1 MΩ approx.</li> </ul>                      |
| B            |   | <ul style="list-style-type: none"> <li>Hysteresis input with pull-up Resistor: 50 kΩ approx.</li> </ul>            |
| C            |  | <ul style="list-style-type: none"> <li>Hysteresis input</li> </ul>   |
| D            |  | <ul style="list-style-type: none"> <li>CMOS output</li> <li>CMOS Hysteresis input</li> </ul>                       |
| E            |  | <ul style="list-style-type: none"> <li>CMOS output</li> <li>CMOS Hysteresis input</li> <li>Analog input</li> </ul> |

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# MB90595/595G Series

| Circuit Type | Circuit   | Remarks  |
|--------------|---|--|
| F            |    | <ul style="list-style-type: none"> <li>• CMOS high current output</li> <li>• CMOS Hysteresis input</li> </ul>  |
| G            |   | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS Hysteresis input</li> <li>• TTL input<br/>(MB90F598/F598G, only in Flash mode)</li> </ul> |
| H            |  | <ul style="list-style-type: none"> <li>• Hysteresis input<br/>Pull-down Resistor: 50 <math>\Omega</math> approx.<br/>(except MB90F598/F598G)</li> </ul>        |

# MB90595/595G Series

## ■ HANDLING DEVICES

### (1) Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding  $V_{CC}$  or an voltage below  $V_{SS}$  is applied to input or output pins or a voltage exceeding the rating is applied across  $V_{CC}$  and  $V_{SS}$ .

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage ( $AV_{CC}$ ,  $AVRH$ ,  $DV_{CC}$ ) and analog input voltages not exceed the digital voltage ( $V_{CC}$ ).

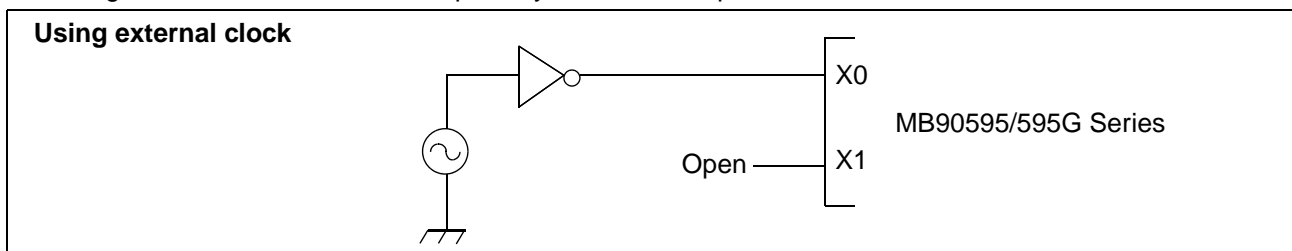
### (2) Treatment of Unused Pins

Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 k $\Omega$  resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

### (3) Using external clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

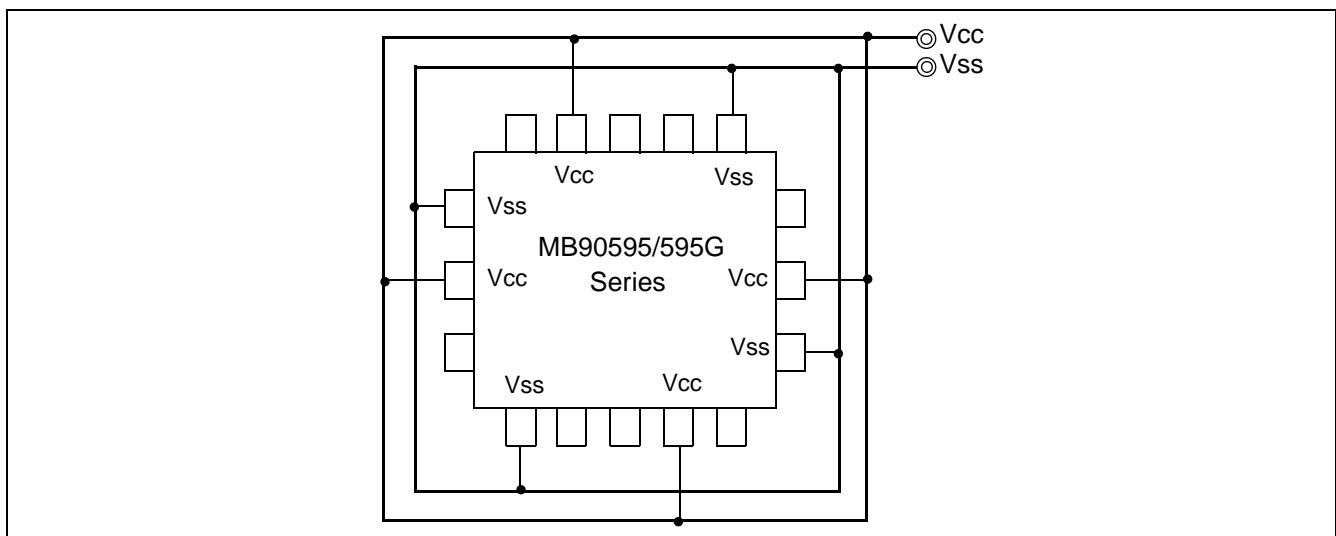


### (4) Power supply pins ( $V_{CC}/V_{SS}$ )

In products with multiple  $V_{CC}$  or  $V_{SS}$  pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating (See the figure below.)

Make sure to connect  $V_{CC}$  and  $V_{SS}$  pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1  $\mu\text{F}$  between  $V_{CC}$  and  $V_{SS}$  pins near the device.



## (5) Pull-up/down resistors

The MB90595 Series does not support internal pull-up/down resistors. Use external components where needed.

## (6) Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

## (7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV<sub>CC</sub>, AVR<sub>H</sub>, AVR<sub>L</sub>) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V<sub>CC</sub>).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVR<sub>H</sub> or AV<sub>CC</sub> (turning on/off the analog and digital power supplies simultaneously is acceptable).

## (8) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to AV<sub>CC</sub> = V<sub>CC</sub>, AV<sub>SS</sub> = AVR<sub>H</sub> = DV<sub>CC</sub> = V<sub>SS</sub>.

## (9) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

## (10) Notes on Energization

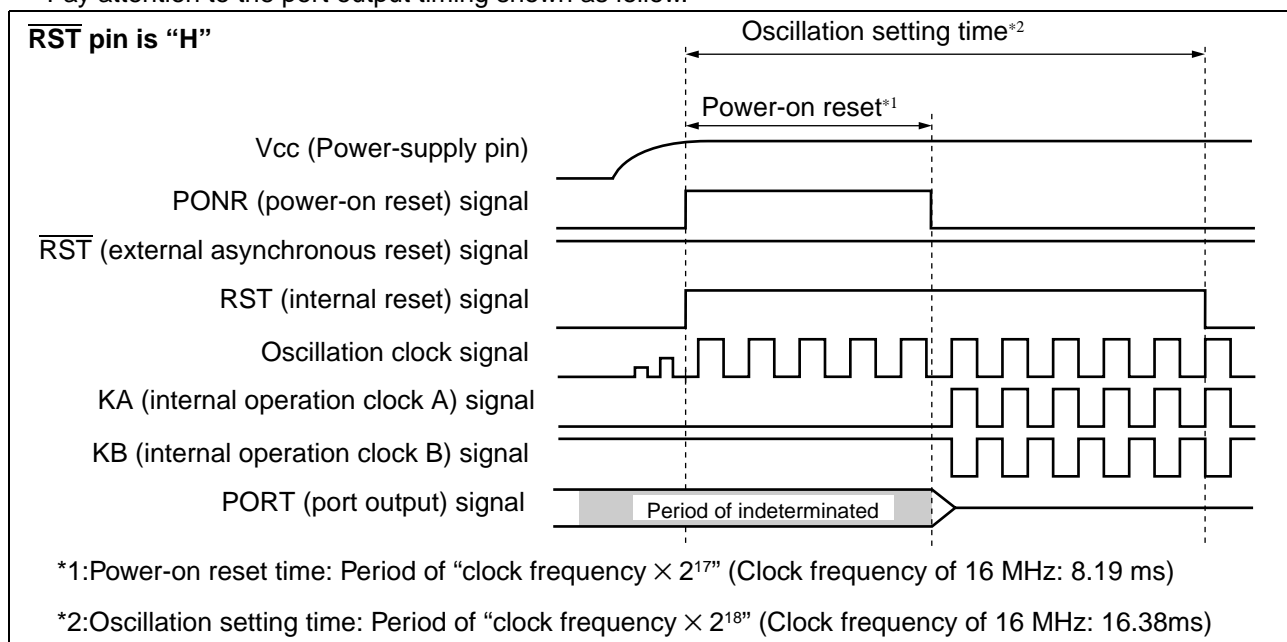
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V).

## (11) Indeterminate outputs from ports 0 and 1 (MB90598/F598/V595/V595G only)

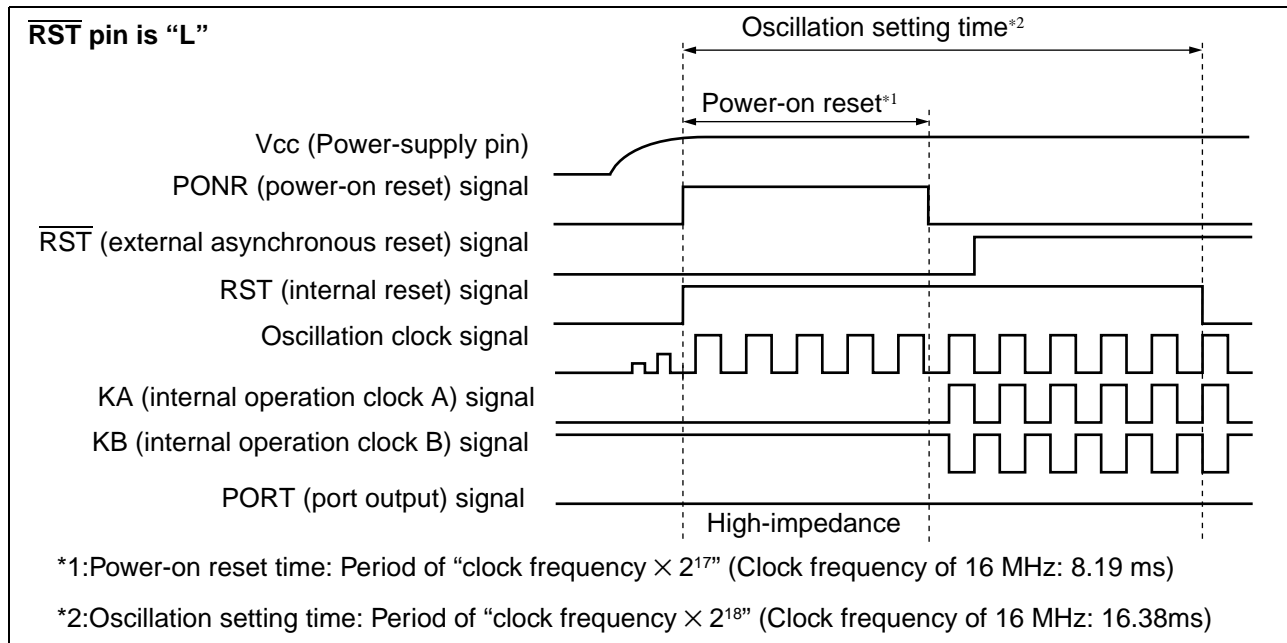
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If  $\overline{\text{RST}}$  pin is "H", the outputs become indeterminate.
- If  $\overline{\text{RST}}$  pin is "L", the outputs become high-impedance.

Pay attention to the port output timing shown as follow.



# MB90595/595G Series



## (12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

## (13) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

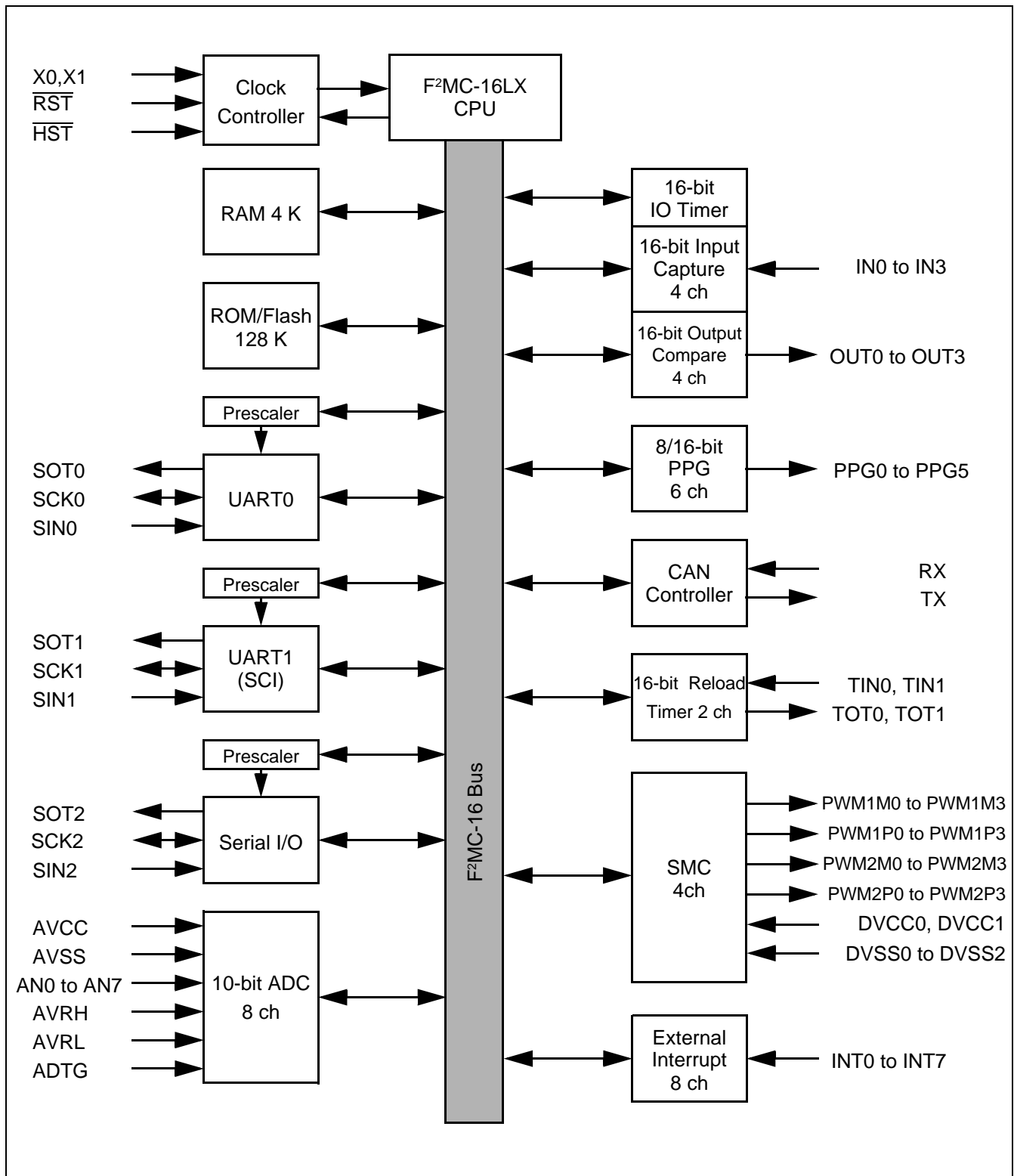
In the signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00H".

If the values of the corresponding bank register (DTB, ADB, USB, SSB) are set to other than "00H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

## (14) Using REALOS

The use of EI<sup>2</sup>OS is not possible with the REALOS real time operating system.

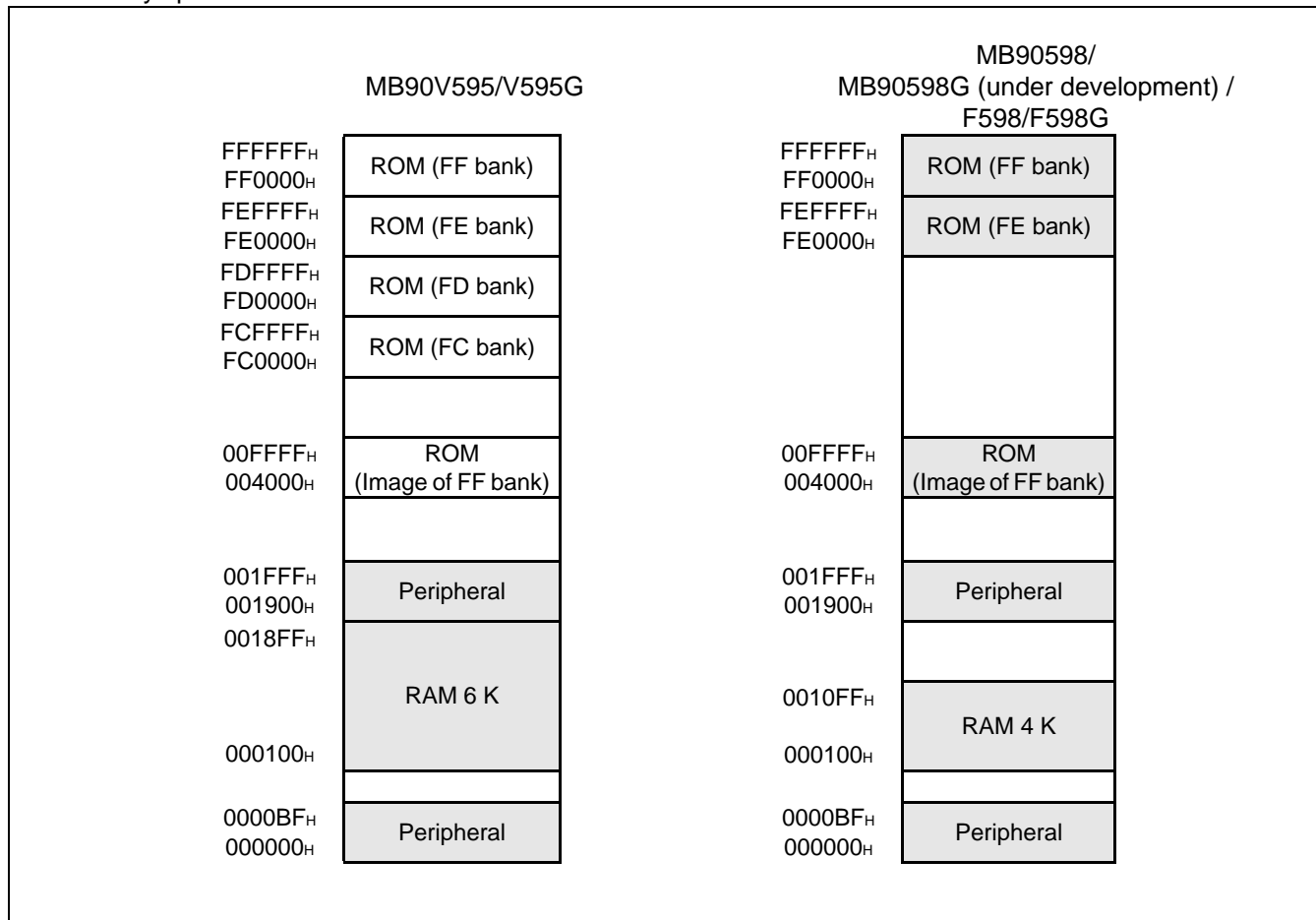
## ■ BLOCK DIAGRAM



# MB90595/595G Series

## ■ MEMORY SPACE

The memory space of the MB90595 Series is shown below



Memory space map

Note: The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating "far".  
For example, if an attempt has been made to access 00C000<sub>H</sub>, the contents of the ROM at FFC000<sub>H</sub> are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000<sub>H</sub> to FFFFFFF<sub>H</sub> looks, therefore, as if it were the image for 004000<sub>H</sub> to 00FFFF<sub>H</sub>. Thus, it is recommended that the ROM data table be stored in the area of FF4000<sub>H</sub> to FFFFFFF<sub>H</sub>.



# MB90595/595G Series

## ■ I/O MAP

| Address    | Register                            | Abbreviation    | Access | Peripheral  | Initial value                |
|------------|-------------------------------------|-----------------|--------|-------------|------------------------------|
| 00H        | Port 0 Data Register                | PDR0            | R/W    | Port 0      | XXXXXXXX <sub>B</sub>        |
| 01H        | Port 1 Data Register                | PDR1            | R/W    | Port 1      | XXXXXXXX <sub>B</sub>        |
| 02H        | Port 2 Data Register                | PDR2            | R/W    | Port 2      | XXXXXXXX <sub>B</sub>        |
| 03H        | Port 3 Data Register                | PDR3            | R/W    | Port 3      | XXXXXXXX <sub>B</sub>        |
| 04H        | Port 4 Data Register                | PDR4            | R/W    | Port 4      | XXXXXXXX <sub>B</sub>        |
| 05H        | Port 5 Data Register                | PDR5            | R/W    | Port 5      | XXXXXXXX <sub>B</sub>        |
| 06H        | Port 6 Data Register                | PDR6            | R/W    | Port 6      | XXXXXXXX <sub>B</sub>        |
| 07H        | Port 7 Data Register                | PDR7            | R/W    | Port 7      | XXXXXXXX <sub>B</sub>        |
| 08H        | Port 8 Data Register                | PDR8            | R/W    | Port 8      | XXXXXXXX <sub>B</sub>        |
| 09H        | Port 9 Data Register                | PDR9            | R/W    | Port 9      | __ XXXXXX <sub>B</sub>       |
| 0AH to 0FH | Reserved                            |                 |        |             |                              |
| 10H        | Port 0 Direction Register           | DDR0            | R/W    | Port 0      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 11H        | Port 1 Direction Register           | DDR1            | R/W    | Port 1      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 12H        | Port 2 Direction Register           | DDR2            | R/W    | Port 2      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 13H        | Port 3 Direction Register           | DDR3            | R/W    | Port 3      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 14H        | Port 4 Direction Register           | DDR4            | R/W    | Port 4      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 15H        | Port 5 Direction Register           | DDR5            | R/W    | Port 5      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 16H        | Port 6 Direction Register           | DDR6            | R/W    | Port 6      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 17H        | Port 7 Direction Register           | DDR7            | R/W    | Port 7      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 18H        | Port 8 Direction Register           | DDR8            | R/W    | Port 8      | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 19H        | Port 9 Direction Register           | DDR9            | R/W    | Port 9      | __ 0 0 0 0 0 0 <sub>B</sub>  |
| 1AH        | Reserved                            |                 |        |             |                              |
| 1BH        | Analog Input Enable Register        | ADER            | R/W    | Port 6, A/D | 1 1 1 1 1 1 1 1 <sub>B</sub> |
| 1CH to 1FH | Reserved                            |                 |        |             |                              |
| 20H        | Serial Mode Control Register 0      | UMC0            | R/W    | UART0       | 0 0 0 0 0 1 0 0 <sub>B</sub> |
| 21H        | Serial status Register 0            | USR0            | R/W    |             | 0 0 0 1 0 0 0 0 <sub>B</sub> |
| 22H        | Serial Input/Output Data Register 0 | UIDR0/<br>UODR0 | R/W    |             | XXXXXXXX <sub>B</sub>        |
| 23H        | Rate and Data Register 0            | URD0            | R/W    |             | 0 0 0 0 0 0 0 X <sub>B</sub> |
| 24H        | Serial Mode Register 1              | SMR1            | R/W    | UART1       | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 25H        | Serial Control Register 1           | SCR1            | R/W    |             | 0 0 0 0 0 1 0 0 <sub>B</sub> |
| 26H        | Serial Input/Output Data Register 1 | SIDR1/<br>SODR1 | R/W    |             | XXXXXXXX <sub>B</sub>        |
| 27H        | Serial Status Register 1            | SSR1            | R/W    |             | 0 0 0 0 1 _ 0 0 <sub>B</sub> |
| 28H        | UART1 Prescaler Control Register    | U1CDR           | R/W    |             | 0 _ _ _ 1 1 1 1 <sub>B</sub> |

(Continued)

# MB90595/595G Series

| Address    | Register                                  | Abbreviation | Access | Peripheral                                      | Initial value                |
|------------|---|--------------|--------|---|------------------------------|
| 29H to 2AH | Reserved                                  |              |        |   |                              |
| 2BH        | Serial IO Prescaler                       | SCDCR        | R/W    | Serial IO                                       | 0 ___ 1 1 1 1 <sub>B</sub>   |
| 2CH        | Serial Mode Control Register (low-order)  | SMCS         | R/W    |   | ___ 0 0 0 0 <sub>B</sub>     |
| 2DH        | Serial Mode Control Register (high-order) | SMCS         | R/W    |   | 0 0 0 0 0 1 0 <sub>B</sub>   |
| 2EH        | Serial Data Register                      | SDR          | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 2FH        | Edge Selector                             | SES          | R/W    |   | ___ 0 <sub>B</sub>           |
| 30H        | External Interrupt Enable Register        | ENIR         | R/W    | External Interrupt                              | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 31H        | External Interrupt Request Register       | EIRR         | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 32H        | External Interrupt Level Register         | ELVR         | R/W    |   | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 33H        | External Interrupt Level Register         | ELVR         | R/W    |   | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 34H        | A/D Control Status Register 0             | ADCS0        | R/W    | A/D Converter                                   | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 35H        | A/D Control Status Register 1             | ADCS1        | R/W    |   | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 36H        | A/D Data Register 0                       | ADCR0        | R      |   | XXXXXXXX <sub>B</sub>        |
| 37H        | A/D Data Register 1                       | ADCR1        | R/W    |   | 0 0 0 0 1 _ XX <sub>B</sub>  |
| 38H        | PPG0 Operation Mode Control Register      | PPGC0        | R/W    | 16-bit Program-<br>mable Pulse<br>Generator 0/1 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 39H        | PPG1 Operation Mode Control Register      | PPGC1        | R/W    |   | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 3AH        | PPG0, 1 Output Pin Control Register       | PPG01        | R/W    |   | 0 0 0 0 0 0 _ _ <sub>B</sub> |
| 3BH        | Reserved                                  |              |        |   |                              |
| 3CH        | PPG2 Operation Mode Control Register      | PPGC2        | R/W    | 16-bit Program-<br>mable Pulse<br>Generator 2/3 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 3DH        | PPG3 Operation Mode Control Register      | PPGC3        | R/W    |   | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 3EH        | PPG2, 3 Output Pin Control Register       | PPG23        | R/W    |   | 0 0 0 0 0 0 _ _ <sub>B</sub> |
| 3FH        | Reserved                                  |              |        |   |                              |
| 40H        | PPG4 Operation Mode Control Register      | PPGC4        | R/W    | 16-bit Program-<br>mable Pulse<br>Generator 4/5 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 41H        | PPG5 Operation Mode Control Register      | PPGC5        | R/W    |   | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 42H        | PPG4, 5 Output Pin Control Register       | PPG45        | R/W    |   | 0 0 0 0 0 0 _ _ <sub>B</sub> |
| 43H        | Reserved                                  |              |        |   |                              |
| 44H        | PPG6 Operation Mode Control Register      | PPGC6        | R/W    | 16-bit Program-<br>mable Pulse<br>Generator 6/7 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 45H        | PPG7 Operation Mode Control Register      | PPGC7        | R/W    |   | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 46H        | PPG6, 7 Output Pin Control Register       | PPG67        | R/W    |   | 0 0 0 0 0 0 _ _ <sub>B</sub> |
| 47H        | Reserved                                  |              |        |   |                              |
| 48H        | PPG8 Operation Mode Control Register      | PPGC8        | R/W    | 16-bit Program-<br>mable Pulse<br>Generator 8/9 | 0 _ 0 0 0 _ _ 1 <sub>B</sub> |
| 49H        | PPG9 Operation Mode Control Register      | PPGC9        | R/W    |   | 0 _ 0 0 0 0 0 1 <sub>B</sub> |
| 4AH        | PPG8, 9 Output Pin Control Register       | PPG89        | R/W    |   | 0 0 0 0 0 0 _ _ <sub>B</sub> |
| 4BH        | Reserved                                  |              |        |   |                              |

(Continued)

# MB90595/595G Series

| Address                            | Register                                  | Abbreviation    | Access | Peripheral                              | Initial value              |
|------------------------------------|---|-----------------|--------|---|----------------------------|
| 4C <sub>H</sub>                    | PPGA Operation Mode Control Register      | PPGCA           | R/W    | 16-bit Programmable Pulse Generator A/B | 0_000__1 <sub>B</sub>      |
| 4D <sub>H</sub>                    | PPGB Operation Mode Control Register      | PPGCB           | R/W    |   | 0_000001 <sub>B</sub>      |
| 4E <sub>H</sub>                    | PPGA, B Output Pin Control Register       | PPGAB           | R/W    |   | 000000__ <sub>B</sub>      |
| 4F <sub>H</sub>                    | Reserved                                  |                 |        |   |                            |
| 50 <sub>H</sub>                    | Timer Control Status Register 0           | TMCSR0          | R/W    | 16-bit Reload Timer 0                   | 00000000 <sub>B</sub>      |
| 51 <sub>H</sub>                    | Timer Control Status Register 0           | TMCSR0          | R/W    |   | __ __ __ 0000 <sub>B</sub> |
| 52 <sub>H</sub>                    | Timer 0/Reload Register 0                 | TMR0/<br>TMRLR0 | R/W    |   | XXXXXXXX <sub>B</sub>      |
| 53 <sub>H</sub>                    | Timer 0/Reload Register 0                 | TMR0/<br>TMRLR0 | R/W    |   | XXXXXXXX <sub>B</sub>      |
| 54 <sub>H</sub>                    | Timer Control Status Register 1           | TMCSR1          | R/W    | 16-bit Reload Timer 1                   | 00000000 <sub>B</sub>      |
| 55 <sub>H</sub>                    | Timer Control Status Register 1           | TMCSR1          | R/W    |   | __ __ __ 0000 <sub>B</sub> |
| 56 <sub>H</sub>                    | Timer Register 1/Reload Register 1        | TMR1/<br>TMRLR1 | R/W    |   | XXXXXXXX <sub>B</sub>      |
| 57 <sub>H</sub>                    | Timer Register 1/Reload Register 1        | TMR1/<br>TMRLR1 | R/W    |   | XXXXXXXX <sub>B</sub>      |
| 58 <sub>H</sub>                    | Output Compare Control Status Register 0  | OCS0            | R/W    | Output Compare 0/1                      | 0000__00 <sub>B</sub>      |
| 59 <sub>H</sub>                    | Output Compare Control Status Register 1  | OCS1            | R/W    |   | __ __ 00000 <sub>B</sub>   |
| 5A <sub>H</sub>                    | Output Compare Control Status Register 2  | OCS2            | R/W    | Output Compare 2/3                      | 0000__00 <sub>B</sub>      |
| 5B <sub>H</sub>                    | Output Compare Control Status Register 3  | OCS3            | R/W    |   | __ __ 00000 <sub>B</sub>   |
| 5C <sub>H</sub>                    | Input Capture Control Status Register 0/1 | ICS01           | R/W    | Input Capture 0/1                       | 00000000 <sub>B</sub>      |
| 5D <sub>H</sub>                    | Input Capture Control Status Register 2/3 | ICS23           | R/W    | Input Capture 2/3                       | 00000000 <sub>B</sub>      |
| 5E <sub>H</sub>                    | PWM Control Register 0                    | PWC0            | R/W    | Stepping Motor Controller 0             | 00000__0 <sub>B</sub>      |
| 5F <sub>H</sub>                    | Reserved                                  |                 |        |   |                            |
| 60 <sub>H</sub>                    | PWM Control Register 1                    | PWC1            | R/W    | Stepping Motor Controller 1             | 00000__0 <sub>B</sub>      |
| 61 <sub>H</sub>                    | Reserved                                  |                 |        |   |                            |
| 62 <sub>H</sub>                    | PWM Control Register 2                    | PWC2            | R/W    | Stepping Motor Controller 2             | 00000__0 <sub>B</sub>      |
| 63 <sub>H</sub>                    | Reserved                                  |                 |        |   |                            |
| 64 <sub>H</sub>                    | PWM Control Register 3                    | PWC3            | R/W    | Stepping Motor Controller 3             | 00000__0 <sub>B</sub>      |
| 65 <sub>H</sub>                    | Reserved                                  |                 |        |   |                            |
| 66 <sub>H</sub>                    | Timer Data Register (low-order)           | TCDT            | R/W    | IO Timer                                | 00000000 <sub>B</sub>      |
| 67 <sub>H</sub>                    | Timer Data Register (high-order)          | TCDT            | R/W    |   | 00000000 <sub>B</sub>      |
| 68 <sub>H</sub>                    | Timer Control Status Register             | TCCS            | R/W    |   | 00000000 <sub>B</sub>      |
| 69 <sub>H</sub> to 6E <sub>H</sub> | Reserved                                  |                 |        |   |                            |

(Continued)

# MB90595/595G Series

| Address    | Register   | Abbreviation | Access | Peripheral                       | Initial value                |
|------------|--|--------------|--------|----------------------------------|------------------------------|
| 6FH        | ROM Mirror Function Selection Register   | ROMM         | R/W    | ROM Mirror                       | _____1 <sub>B</sub>          |
| 70H        | PWM1 Compare Register 0  | PWC10        | R/W    | Stepping Motor Controller 0      | XXXXXXXX <sub>B</sub>        |
| 71H        | PWM2 Compare Register 0  | PWC20        | R/W    |                                  | XXXXXXXX <sub>B</sub>        |
| 72H        | PWM1 Select Register 0   | PWS10        | R/W    |                                  | _ _ 0 0 0 0 0 0 <sub>B</sub> |
| 73H        | PWM2 Select Register 0   | PWS20        | R/W    |                                  | _ 0 0 0 0 0 0 <sub>B</sub>   |
| 74H        | PWM1 Compare Register 1  | PWC11        | R/W    | Stepping Motor Controller 1      | XXXXXXXX <sub>B</sub>        |
| 75H        | PWM2 Compare Register 1  | PWC21        | R/W    |                                  | XXXXXXXX <sub>B</sub>        |
| 76H        | PWM1 Select Register 1   | PWS11        | R/W    |                                  | _ _ 0 0 0 0 0 0 <sub>B</sub> |
| 77H        | PWM2 Select Register 1   | PWS21        | R/W    |                                  | _ 0 0 0 0 0 0 <sub>B</sub>   |
| 78H        | PWM1 Compare Register 2  | PWC12        | R/W    | Stepping Motor Controller 2      | XXXXXXXX <sub>B</sub>        |
| 79H        | PWM2 Compare Register 2  | PWC22        | R/W    |                                  | XXXXXXXX <sub>B</sub>        |
| 7AH        | PWM1 Select Register 2   | PWS12        | R/W    |                                  | _ _ 0 0 0 0 0 0 <sub>B</sub> |
| 7BH        | PWM2 Select Register 2   | PWS22        | R/W    |                                  | _ 0 0 0 0 0 0 <sub>B</sub>   |
| 7CH        | PWM1 Compare Register 3  | PWC13        | R/W    | Stepping Motor Controller 3      | XXXXXXXX <sub>B</sub>        |
| 7DH        | PWM2 Compare Register 3  | PWC23        | R/W    |                                  | XXXXXXXX <sub>B</sub>        |
| 7EH        | PWM1 Select Register 3   | PWS13        | R/W    |                                  | _ _ 0 0 0 0 0 0 <sub>B</sub> |
| 7FH        | PWM2 Select Register 3   | PWS23        | R/W    |                                  | _ 0 0 0 0 0 0 <sub>B</sub>   |
| 80H to 8FH | CAN Controller. Refer to section about CAN Controller                          |              |        |                                  |                              |
| 90H to 9DH | Reserved   |              |        |                                  |                              |
| 9EH        | Program Address Detection Control Status Register                              | PACSR        | R/W    | Address Match Detection Function | 0 0 0 0 0 0 0 0 <sub>B</sub> |
| 9FH        | Delayed Interrupt/Request Register   | DIRR         | R/W    | Delayed Interrupt                | _____0 <sub>B</sub>          |
| A0H        | Low-Power Mode Control Register  | LPMCR        | R/W    | Low Power Controller             | 0 0 0 1 1 0 0 0 <sub>B</sub> |
| A1H        | Clock Selection Register   | CKSCR        | R/W    | Low Power Controller             | 1 1 1 1 1 1 0 0 <sub>B</sub> |
| A2H to A7H | Reserved   |              |        |                                  |                              |
| A8H        | Watchdog Timer Control Register  | WDTC         | R/W    | Watchdog Timer                   | XXXXX 1 1 1 <sub>B</sub>     |
| A9H        | Time Base Timer Control Register   | TBTC         | R/W    | Time Base Timer                  | 1 _ _ 0 0 1 0 0 <sub>B</sub> |
| AAH to ADH | Reserved   |              |        |                                  |                              |
| AEH        | Flash Memory Control Status Register (MB90F598/F598G only. Otherwise reserved) | FMCS         | R/W    | Flash Memory                     | 0 0 0 X 0 0 0 0 <sub>B</sub> |
| AFH        | Reserved   |              |        |                                  |                              |

(Continued)

# MB90595/595G Series

| Address                            | Register                      | Abbreviation | Access | Peripheral                              | Initial value                |
|------------------------------------|-------------------------------|--------------|--------|---|------------------------------|
| B0 <sub>H</sub>                    | Interrupt Control Register 00 | ICR00        | R/W    | Interrupt controller                    | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B1 <sub>H</sub>                    | Interrupt Control Register 01 | ICR01        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B2 <sub>H</sub>                    | Interrupt Control Register 02 | ICR02        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B3 <sub>H</sub>                    | Interrupt Control Register 03 | ICR03        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B4 <sub>H</sub>                    | Interrupt Control Register 04 | ICR04        | R/W    | Interrupt controller                    | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B5 <sub>H</sub>                    | Interrupt Control Register 05 | ICR05        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B6 <sub>H</sub>                    | Interrupt Control Register 06 | ICR06        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B7 <sub>H</sub>                    | Interrupt Control Register 07 | ICR07        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B8 <sub>H</sub>                    | Interrupt Control Register 08 | ICR08        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| B9 <sub>H</sub>                    | Interrupt Control Register 09 | ICR09        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BA <sub>H</sub>                    | Interrupt Control Register 10 | ICR10        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BB <sub>H</sub>                    | Interrupt Control Register 11 | ICR11        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BC <sub>H</sub>                    | Interrupt Control Register 12 | ICR12        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BD <sub>H</sub>                    | Interrupt Control Register 13 | ICR13        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BE <sub>H</sub>                    | Interrupt Control Register 14 | ICR14        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| BF <sub>H</sub>                    | Interrupt Control Register 15 | ICR15        | R/W    |   | 0 0 0 0 0 1 1 1 <sub>B</sub> |
| C0 <sub>H</sub> to FF <sub>H</sub> | Reserved                      |              |        |   |                              |
| 1900 <sub>H</sub>                  | Reload Register L             | PRL0         | R/W    | 16-bit Programmable Pulse Generator 0/1 | XXXXXXXX <sub>B</sub>        |
| 1901 <sub>H</sub>                  | Reload Register H             | PRLH0        | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 1902 <sub>H</sub>                  | Reload Register L             | PRL1         | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 1903 <sub>H</sub>                  | Reload Register H             | PRLH1        | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 1904 <sub>H</sub>                  | Reload Register L             | PRL2         | R/W    | 16-bit Programmable Pulse Generator 2/3 | XXXXXXXX <sub>B</sub>        |
| 1905 <sub>H</sub>                  | Reload Register H             | PRLH2        | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 1906 <sub>H</sub>                  | Reload Register L             | PRL3         | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 1907 <sub>H</sub>                  | Reload Register H             | PRLH3        | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 1908 <sub>H</sub>                  | Reload Register L             | PRL4         | R/W    | 16-bit Programmable Pulse Generator 4/5 | XXXXXXXX <sub>B</sub>        |
| 1909 <sub>H</sub>                  | Reload Register H             | PRLH4        | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 190A <sub>H</sub>                  | Reload Register L             | PRL5         | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 190B <sub>H</sub>                  | Reload Register H             | PRLH5        | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 190C <sub>H</sub>                  | Reload Register L             | PRL6         | R/W    | 16-bit Programmable Pulse Generator 6/7 | XXXXXXXX <sub>B</sub>        |
| 190D <sub>H</sub>                  | Reload Register H             | PRLH6        | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 190E <sub>H</sub>                  | Reload Register L             | PRL7         | R/W    |   | XXXXXXXX <sub>B</sub>        |
| 190F <sub>H</sub>                  | Reload Register H             | PRLH7        | R/W    |   | XXXXXXXX <sub>B</sub>        |

(Continued)

# MB90595/595G Series

(Continued)

| Address                                | Register                               | Abbreviation | Access | Peripheral                              | Initial value         |
|--|--|--------------|--------|---|-----------------------|
| 1910 <sub>H</sub>                      | Reload Register L                      | PRL8         | R/W    | 16-bit Programmable Pulse Generator 8/9 | XXXXXXXX <sub>B</sub> |
| 1911 <sub>H</sub>                      | Reload Register H                      | PRLH8        | R/W    |   | XXXXXXXX <sub>B</sub> |
| 1912 <sub>H</sub>                      | Reload Register L                      | PRL9         | R/W    |   | XXXXXXXX <sub>B</sub> |
| 1913 <sub>H</sub>                      | Reload Register H                      | PRLH9        | R/W    |   | XXXXXXXX <sub>B</sub> |
| 1914 <sub>H</sub>                      | Reload Register L                      | PRLLA        | R/W    | 16-bit Programmable Pulse Generator A/B | XXXXXXXX <sub>B</sub> |
| 1915 <sub>H</sub>                      | Reload Register H                      | PRLHA        | R/W    |   | XXXXXXXX <sub>B</sub> |
| 1916 <sub>H</sub>                      | Reload Register L                      | PRLLB        | R/W    | 16-bit Programmable Pulse Generator A/B | XXXXXXXX <sub>B</sub> |
| 1917 <sub>H</sub>                      | Reload Register H                      | PRLHB        | R/W    |   | XXXXXXXX <sub>B</sub> |
| 1918 <sub>H</sub> to 191F <sub>H</sub> | Reserved                               |              |        |   |                       |
| 1920 <sub>H</sub>                      | Input Capture Register 0 (low-order)   | IPCP0        | R      | Input Capture 0/1                       | XXXXXXXX <sub>B</sub> |
| 1921 <sub>H</sub>                      | Input Capture Register 0 (high-order)  | IPCP0        | R      |   | XXXXXXXX <sub>B</sub> |
| 1922 <sub>H</sub>                      | Input Capture Register 1 (low-order)   | IPCP1        | R      |   | XXXXXXXX <sub>B</sub> |
| 1923 <sub>H</sub>                      | Input Capture Register 1 (high-order)  | IPCP1        | R      |   | XXXXXXXX <sub>B</sub> |
| 1924 <sub>H</sub>                      | Input Capture Register 2 (low-order)   | IPCP2        | R      | Input Capture 2/3                       | XXXXXXXX <sub>B</sub> |
| 1925 <sub>H</sub>                      | Input Capture Register 2 (high-order)  | IPCP2        | R      |   | XXXXXXXX <sub>B</sub> |
| 1926 <sub>H</sub>                      | Input Capture Register 3 (low-order)   | IPCP3        | R      |   | XXXXXXXX <sub>B</sub> |
| 1927 <sub>H</sub>                      | Input Capture Register 3 (high-order)  | IPCP3        | R      |   | XXXXXXXX <sub>B</sub> |
| 1928 <sub>H</sub>                      | Output Compare Register 0 (low-order)  | OCCP0        | R/W    | Output Compare 0/1                      | XXXXXXXX <sub>B</sub> |
| 1929 <sub>H</sub>                      | Output Compare Register 0 (high-order) | OCCP0        | R/W    |   | XXXXXXXX <sub>B</sub> |
| 192A <sub>H</sub>                      | Output Compare Register 1 (low-order)  | OCCP1        | R/W    |   | XXXXXXXX <sub>B</sub> |
| 192B <sub>H</sub>                      | Output Compare Register 1 (high-order) | OCCP1        | R/W    |   | XXXXXXXX <sub>B</sub> |

(Continued)

# MB90595/595G Series

(Continued)

| Address                                | Register  | Abbreviation | Access | Peripheral                       | Initial value         |
|--|---|--------------|--------|----------------------------------|-----------------------|
| 192C <sub>H</sub>                      | Output Compare Register 2 (low-order)                 | OCCP2        | R/W    | Output Compare 2/3               | XXXXXXXX <sub>B</sub> |
| 192D <sub>H</sub>                      | Output Compare Register 2 (high-order)                | OCCP2        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 192E <sub>H</sub>                      | Output Compare Register 3 (low-order)                 | OCCP3        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 192F <sub>H</sub>                      | Output Compare Register 3 (high-order)                | OCCP3        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 1930 <sub>H</sub> to 19FF <sub>H</sub> | Reserved  |              |        |                                  |                       |
| 1A00 <sub>H</sub> to 1AFF <sub>H</sub> | CAN Controller. Refer to section about CAN Controller |              |        |                                  |                       |
| 1B00 <sub>H</sub> to 1BFF <sub>H</sub> | CAN Controller. Refer to section about CAN Controller |              |        |                                  |                       |
| 1C00 <sub>H</sub> to 1EFF <sub>H</sub> | Reserved  |              |        |                                  |                       |
| 1FF0 <sub>H</sub>                      | Program Address Detection Register 0 (low-order)      | PADR0        | R/W    | Address Match Detection Function | XXXXXXXX <sub>B</sub> |
| 1FF1 <sub>H</sub>                      | Program Address Detection Register 0 (middle-order)   |              |        |                                  | XXXXXXXX <sub>B</sub> |
| 1FF2 <sub>H</sub>                      | Program Address Detection Register 0 (high-order)     |              |        |                                  | XXXXXXXX <sub>B</sub> |
| 1FF3 <sub>H</sub>                      | Program Address Detection Register 1 (low-order)      | PADR1        | R/W    |                                  | XXXXXXXX <sub>B</sub> |
| 1FF4 <sub>H</sub>                      | Program Address Detection Register 1 (middle-order)   |              |        |                                  | XXXXXXXX <sub>B</sub> |
| 1FF5 <sub>H</sub>                      | Program Address Detection Register 1 (high-order)     |              |        |                                  | XXXXXXXX <sub>B</sub> |
| 1FF6 <sub>H</sub> to 1FFF <sub>H</sub> | Reserved  |              |        |                                  |                       |

Note: Initial value of “\_” represents unused bit; “X” represents unknown value.

Addresses in the range 0000<sub>H</sub> to 00FF<sub>H</sub>, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading “X”, and any write access should not be performed.

# MB90595/595G Series

## ■ CAN CONTROLLER

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbit/s to 2 Mbit/s (when input clock is at 16 MHz)

**List of Control Registers**

| Address             | Register                          | Abbreviation | Access | Initial Value                   |
|---------------------|-----------------------------------|--------------|--------|---------------------------------|
| 000080 <sub>H</sub> | Message buffer valid register     | BVALR        | R/W    | 00000000 00000000 <sub>B</sub>  |
| 000081 <sub>H</sub> |                                   |              |        |                                 |
| 000082 <sub>H</sub> | Transmit request register         | TREQR        | R/W    | 00000000 00000000 <sub>B</sub>  |
| 000083 <sub>H</sub> |                                   |              |        |                                 |
| 000084 <sub>H</sub> | Transmit cancel register          | TCANR        | W      | 00000000 00000000 <sub>B</sub>  |
| 000085 <sub>H</sub> |                                   |              |        |                                 |
| 000086 <sub>H</sub> | Transmit complete register        | TCR          | R/W    | 00000000 00000000 <sub>B</sub>  |
| 000087 <sub>H</sub> |                                   |              |        |                                 |
| 000088 <sub>H</sub> | Receive complete register         | RCR          | R/W    | 00000000 00000000 <sub>B</sub>  |
| 000089 <sub>H</sub> |                                   |              |        |                                 |
| 00008A <sub>H</sub> | Remote request receiving register | RRTRR        | R/W    | 00000000 00000000 <sub>B</sub>  |
| 00008B <sub>H</sub> |                                   |              |        |                                 |
| 00008C <sub>H</sub> | Receive overrun register          | ROVRR        | R/W    | 00000000 00000000 <sub>B</sub>  |
| 00008D <sub>H</sub> |                                   |              |        |                                 |
| 00008E <sub>H</sub> | Receive interrupt enable register | RIER         | R/W    | 00000000 00000000 <sub>B</sub>  |
| 00008F <sub>H</sub> |                                   |              |        |                                 |
| 001B00 <sub>H</sub> | Control status register           | CSR          | R/W, R | 00---000 0----0-1 <sub>B</sub>  |
| 001B01 <sub>H</sub> |                                   |              |        |                                 |
| 001B02 <sub>H</sub> | Last event indicator register     | LEIR         | R/W    | ----- 000-0000 <sub>B</sub>     |
| 001B03 <sub>H</sub> |                                   |              |        |                                 |
| 001B04 <sub>H</sub> | Receive/transmit error counter    | RTEC         | R      | 00000000 00000000 <sub>B</sub>  |
| 001B05 <sub>H</sub> |                                   |              |        |                                 |
| 001B06 <sub>H</sub> | Bit timing register               | BTR          | R/W    | -11111111 11111111 <sub>B</sub> |
| 001B07 <sub>H</sub> |                                   |              |        |                                 |

(Continued)



# MB90595/595G Series

(Continued)

| Address | Register                              | Abbreviation | Access | Initial Value      |
|---------|---------------------------------------|--------------|--------|--------------------|
| 001B08H | IDE register                          | IDER         | R/W    | XXXXXXXX XXXXXXXXB |
| 001B09H |                                       |              |        |                    |
| 001B0AH | Transmit RTR register                 | TRTRR        | R/W    | 00000000 00000000B |
| 001B0BH |                                       |              |        |                    |
| 001B0CH | Remote frame receive waiting register | RFWTR        | R/W    | XXXXXXXX XXXXXXXXB |
| 001B0DH |                                       |              |        |                    |
| 001B0EH | Transmit interrupt enable register    | TIER         | R/W    | 00000000 00000000B |
| 001B0FH |                                       |              |        |                    |
| 001B10H | Acceptance mask select register       | AMSR         | R/W    | XXXXXXXX XXXXXXXXB |
| 001B11H |                                       |              |        | XXXXXXXX XXXXXXXXB |
| 001B12H |                                       |              |        | XXXXXXXX XXXXXXXXB |
| 001B13H |                                       |              |        | XXXXXXXX XXXXXXXXB |
| 001B14H | Acceptance mask register 0            | AMR0         | R/W    | XXXXXXXX XXXXXXXXB |
| 001B15H |                                       |              |        | XXXXX--- XXXXXXXXB |
| 001B16H |                                       |              |        | XXXXX--- XXXXXXXXB |
| 001B17H |                                       |              |        | XXXXX--- XXXXXXXXB |
| 001B18H | Acceptance mask register 1            | AMR1         | R/W    | XXXXXXXX XXXXXXXXB |
| 001B19H |                                       |              |        | XXXXX--- XXXXXXXXB |
| 001B1AH |                                       |              |        | XXXXX--- XXXXXXXXB |
| 001B1BH |                                       |              |        | XXXXX--- XXXXXXXXB |

# MB90595/595G Series

List of Message Buffers (ID Registers)

| Address                  | Register            | Abbreviation | Access | Initial Value  |
|--------------------------|---------------------|--------------|--------|--|
| 001A00H<br>to<br>001A1FH | General-purpose RAM | --           | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001A20H                  | ID register 0       | IDR0         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub>                       |
| 001A21H                  |                     |              |        | XXXXX--- XXXXXXXX <sub>B</sub>                       |
| 001A22H                  |                     |              |        |  |
| 001A23H                  |                     |              |        |  |
| 001A24H                  | ID register 1       | IDR1         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub>                       |
| 001A25H                  |                     |              |        | XXXXX--- XXXXXXXX <sub>B</sub>                       |
| 001A26H                  |                     |              |        |  |
| 001A27H                  |                     |              |        |  |
| 001A28H                  | ID register 2       | IDR2         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub>                       |
| 001A29H                  |                     |              |        | XXXXX--- XXXXXXXX <sub>B</sub>                       |
| 001A2AH                  |                     |              |        |  |
| 001A2BH                  |                     |              |        |  |
| 001A2CH                  | ID register 3       | IDR3         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub>                       |
| 001A2DH                  |                     |              |        | XXXXX--- XXXXXXXX <sub>B</sub>                       |
| 001A2EH                  |                     |              |        |  |
| 001A2FH                  |                     |              |        |  |
| 001A30H                  | ID register 4       | IDR4         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub>                       |
| 001A31H                  |                     |              |        | XXXXX--- XXXXXXXX <sub>B</sub>                       |
| 001A32H                  |                     |              |        |  |
| 001A33H                  |                     |              |        |  |
| 001A34H                  | ID register 5       | IDR5         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub>                       |
| 001A35H                  |                     |              |        | XXXXX--- XXXXXXXX <sub>B</sub>                       |
| 001A36H                  |                     |              |        |  |
| 001A37H                  |                     |              |        |  |
| 001A38H                  | ID register 6       | IDR6         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub>                       |
| 001A39H                  |                     |              |        | XXXXX--- XXXXXXXX <sub>B</sub>                       |
| 001A3AH                  |                     |              |        |  |
| 001A3BH                  |                     |              |        |  |
| 001A3CH                  | ID register 7       | IDR7         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub>                       |
| 001A3DH                  |                     |              |        | XXXXX--- XXXXXXXX <sub>B</sub>                       |
| 001A3EH                  |                     |              |        |  |
| 001A3FH                  |                     |              |        |  |

(Continued)

# MB90595/595G Series

(Continued)

| Address             | Register       | Abbreviation | Access | Initial Value                  |
|---------------------|----------------|--------------|--------|--------------------------------|
| 001A40 <sub>H</sub> | ID register 8  | IDR8         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A41 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A42 <sub>H</sub> |                |              |        |                                |
| 001A43 <sub>H</sub> |                |              |        |                                |
| 001A44 <sub>H</sub> | ID register 9  | IDR9         | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A45 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A46 <sub>H</sub> |                |              |        |                                |
| 001A47 <sub>H</sub> |                |              |        |                                |
| 001A48 <sub>H</sub> | ID register 10 | IDR10        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A49 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A4A <sub>H</sub> |                |              |        |                                |
| 001A4B <sub>H</sub> |                |              |        |                                |
| 001A4C <sub>H</sub> | ID register 11 | IDR11        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A4D <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A4E <sub>H</sub> |                |              |        |                                |
| 001A4F <sub>H</sub> |                |              |        |                                |
| 001A50 <sub>H</sub> | ID register 12 | IDR12        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A51 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A52 <sub>H</sub> |                |              |        |                                |
| 001A53 <sub>H</sub> |                |              |        |                                |
| 001A54 <sub>H</sub> | ID register 13 | IDR13        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A55 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A56 <sub>H</sub> |                |              |        |                                |
| 001A57 <sub>H</sub> |                |              |        |                                |
| 001A58 <sub>H</sub> | ID register 14 | IDR14        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A59 <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A5A <sub>H</sub> |                |              |        |                                |
| 001A5B <sub>H</sub> |                |              |        |                                |
| 001A5C <sub>H</sub> | ID register 15 | IDR15        | R/W    | XXXXXXXX XXXXXXXX <sub>B</sub> |
| 001A5D <sub>H</sub> |                |              |        | XXXXX--- XXXXXXXX <sub>B</sub> |
| 001A5E <sub>H</sub> |                |              |        |                                |
| 001A5F <sub>H</sub> |                |              |        |                                |

# MB90595/595G Series

List of Message Buffers (DLC Registers and Data Registers)

| Address  | Register                  | Abbreviation | Access | Initial Value  |
|--|---------------------------|--------------|--------|--|
| 001A60 <sub>H</sub>                              | DLC register 0            | DLCR0        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A61 <sub>H</sub>                              |                           |              |        |  |
| 001A62 <sub>H</sub>                              | DLC register 1            | DLCR1        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A63 <sub>H</sub>                              |                           |              |        |  |
| 001A64 <sub>H</sub>                              | DLC register 2            | DLCR2        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A65 <sub>H</sub>                              |                           |              |        |  |
| 001A66 <sub>H</sub>                              | DLC register 3            | DLCR3        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A67 <sub>H</sub>                              |                           |              |        |  |
| 001A68 <sub>H</sub>                              | DLC register 4            | DLCR4        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A69 <sub>H</sub>                              |                           |              |        |  |
| 001A6A <sub>H</sub>                              | DLC register 5            | DLCR5        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A6B <sub>H</sub>                              |                           |              |        |  |
| 001A6C <sub>H</sub>                              | DLC register 6            | DLCR6        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A6D <sub>H</sub>                              |                           |              |        |  |
| 001A6E <sub>H</sub>                              | DLC register 7            | DLCR7        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A6F <sub>H</sub>                              |                           |              |        |  |
| 001A70 <sub>H</sub>                              | DLC register 8            | DLCR8        | R/W    | ----XXXX   |
| 001A71 <sub>H</sub>                              |                           |              |        |  |
| 001A72 <sub>H</sub>                              | DLC register 9            | DLCR9        | R/W    | ----XXXX <sub>B</sub>                                |
| 001A73 <sub>H</sub>                              |                           |              |        |  |
| 001A74 <sub>H</sub>                              | DLC register 10           | DLCR10       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A75 <sub>H</sub>                              |                           |              |        |  |
| 001A76 <sub>H</sub>                              | DLC register 11           | DLCR11       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A77 <sub>H</sub>                              |                           |              |        |  |
| 001A78 <sub>H</sub>                              | DLC register 12           | DLCR12       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A79 <sub>H</sub>                              |                           |              |        |  |
| 001A7A <sub>H</sub>                              | DLC register 13           | DLCR13       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A7B <sub>H</sub>                              |                           |              |        |  |
| 001A7C <sub>H</sub>                              | DLC register 14           | DLCR14       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A7D <sub>H</sub>                              |                           |              |        |  |
| 001A7E <sub>H</sub>                              | DLC register 15           | DLCR15       | R/W    | ----XXXX <sub>B</sub>                                |
| 001A7F <sub>H</sub>                              |                           |              |        |  |
| 001A80 <sub>H</sub><br>to<br>001A87 <sub>H</sub> | Data register 0 (8 bytes) | DTR0         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |

(Continued)

# MB90595/595G Series

(Continued)

| Address  | Register                   | Abbreviation | Access | Initial Value  |
|--|----------------------------|--------------|--------|--|
| 001A88 <sub>H</sub><br>to<br>001A8F <sub>H</sub> | Data register 1 (8 bytes)  | DTR1         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001A90 <sub>H</sub><br>to<br>001A97 <sub>H</sub> | Data register 2 (8 bytes)  | DTR2         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001A98 <sub>H</sub><br>to<br>001A9F <sub>H</sub> | Data register 3 (8 bytes)  | DTR3         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AA0 <sub>H</sub><br>to<br>001AA7 <sub>H</sub> | Data register 4 (8 bytes)  | DTR4         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AA8 <sub>H</sub><br>to<br>001AAF <sub>H</sub> | Data register 5 (8 bytes)  | DTR5         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AB0 <sub>H</sub><br>to<br>001AB7 <sub>H</sub> | Data register 6 (8 bytes)  | DTR6         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AB8 <sub>H</sub><br>to<br>001ABF <sub>H</sub> | Data register 7 (8 bytes)  | DTR7         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AC0 <sub>H</sub><br>to<br>001AC7 <sub>H</sub> | Data register 8 (8 bytes)  | DTR8         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AC8 <sub>H</sub><br>to<br>001ACF <sub>H</sub> | Data register 9 (8 bytes)  | DTR9         | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AD0 <sub>H</sub><br>to<br>001AD7 <sub>H</sub> | Data register 10 (8 bytes) | DTR10        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AD8 <sub>H</sub><br>to<br>001ADF <sub>H</sub> | Data register 11 (8 bytes) | DTR11        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AE0 <sub>H</sub><br>to<br>001AE7 <sub>H</sub> | Data register 12 (8 bytes) | DTR12        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AE8 <sub>H</sub><br>to<br>001AEF <sub>H</sub> | Data register 13 (8 bytes) | DTR13        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AF0 <sub>H</sub><br>to<br>001AF7 <sub>H</sub> | Data register 14 (8 bytes) | DTR14        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |
| 001AF8 <sub>H</sub><br>to<br>001AFF <sub>H</sub> | Data register 15 (8 bytes) | DTR15        | R/W    | XXXXXXXX <sub>B</sub><br>to<br>XXXXXXXX <sub>B</sub> |

# MB90595/595G Series

## ■ INTERRUPT MAP

| Interrupt source               | EI <sup>2</sup> OS clear | Interrupt vector |                     | Interrupt control register |                     |
|--------------------------------|--------------------------|------------------|---------------------|----------------------------|---------------------|
|                                |                          | Number           | Address             | Number                     | Address             |
| Reset                          | N/A                      | # 08             | FFFFDC <sub>H</sub> | —                          | —                   |
| INT9 instruction               | N/A                      | # 09             | FFFFD8 <sub>H</sub> | —                          | —                   |
| Exception                      | N/A                      | # 10             | FFFFD4 <sub>H</sub> | —                          | —                   |
| CAN RX                         | N/A                      | # 11             | FFFFD0 <sub>H</sub> | ICR00                      | 0000B0 <sub>H</sub> |
| CAN TX/NS                      | N/A                      | # 12             | FFFFCC <sub>H</sub> |                            |                     |
| External Interrupt (INT0/INT1) | *1                       | # 13             | FFFFC8 <sub>H</sub> | ICR01                      | 0000B1 <sub>H</sub> |
| Time Base Timer                | N/A                      | # 14             | FFFFC4 <sub>H</sub> |                            |                     |
| 16-bit Reload Timer 0          | *1                       | # 15             | FFFFC0 <sub>H</sub> | ICR02                      | 0000B2 <sub>H</sub> |
| 8/10-bit A/D Converter         | *1                       | # 16             | FFFFBC <sub>H</sub> |                            |                     |
| I/O Timer                      | N/A                      | # 17             | FFFFB8 <sub>H</sub> | ICR03                      | 0000B3 <sub>H</sub> |
| External Interrupt (INT2/INT3) | *1                       | # 18             | FFFFB4 <sub>H</sub> |                            |                     |
| Serial I/O                     | *1                       | # 19             | FFFFB0 <sub>H</sub> | ICR04                      | 0000B4 <sub>H</sub> |
| External Interrupt (INT4/INT5) | *1                       | # 20             | FFFFAC <sub>H</sub> |                            |                     |
| Input Capture 0                | *1                       | # 21             | FFFFA8 <sub>H</sub> | ICR05                      | 0000B5 <sub>H</sub> |
| 8/16-bit PPG 0/1               | N/A                      | # 22             | FFFFA4 <sub>H</sub> |                            |                     |
| Output Compare 0               | *1                       | # 23             | FFFFA0 <sub>H</sub> | ICR06                      | 0000B6 <sub>H</sub> |
| 8/16-bit PPG 2/3               | N/A                      | # 24             | FFFF9C <sub>H</sub> |                            |                     |
| External Interrupt (INT6/INT7) | *1                       | # 25             | FFFF98 <sub>H</sub> | ICR07                      | 0000B7 <sub>H</sub> |
| Input Capture 1                | *1                       | # 26             | FFFF94 <sub>H</sub> |                            |                     |
| 8/16-bit PPG 4/5               | N/A                      | # 27             | FFFF90 <sub>H</sub> | ICR08                      | 0000B8 <sub>H</sub> |
| Output Compare 1               | *1                       | # 28             | FFFF8C <sub>H</sub> |                            |                     |
| 8/16-bit PPG 6/7               | N/A                      | # 29             | FFFF88 <sub>H</sub> | ICR09                      | 0000B9 <sub>H</sub> |
| Input Capture 2                | *1                       | # 30             | FFFF84 <sub>H</sub> |                            |                     |
| 8/16-bit PPG 8/9               | N/A                      | # 31             | FFFF80 <sub>H</sub> | ICR10                      | 0000BA <sub>H</sub> |
| Output Compare 2               | *1                       | # 32             | FFFF7C <sub>H</sub> |                            |                     |
| Input Capture 3                | *1                       | # 33             | FFFF78 <sub>H</sub> | ICR11                      | 0000BB <sub>H</sub> |
| 8/16-bit PPG A/B               | N/A                      | # 34             | FFFF74 <sub>H</sub> |                            |                     |
| Output Compare 3               | *1                       | # 35             | FFFF70 <sub>H</sub> | ICR12                      | 0000BC <sub>H</sub> |
| 16-bit Reload Timer 1          | *1                       | # 36             | FFFF6C <sub>H</sub> |                            |                     |
| UART 0 RX                      | *2                       | # 37             | FFFF68 <sub>H</sub> | ICR13                      | 0000BD <sub>H</sub> |
| UART 0 TX                      | *1                       | # 38             | FFFF64 <sub>H</sub> |                            |                     |
| UART 1 RX                      | *2                       | # 39             | FFFF60 <sub>H</sub> | ICR14                      | 0000BE <sub>H</sub> |
| UART 1 TX                      | *1                       | # 40             | FFFF5C <sub>H</sub> |                            |                     |
| Flash Memory                   | N/A                      | # 41             | FFFF58 <sub>H</sub> | ICR15                      | 0000BF <sub>H</sub> |
| Delayed interrupt              | N/A                      | # 42             | FFFF54 <sub>H</sub> |                            |                     |

\*1: The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal.

\*2: The interrupt request flag is cleared by the EI<sup>2</sup>OS interrupt clear signal. A stop request is available.

N/A: The interrupt request flag is not cleared by the EI<sup>2</sup>OS interrupt clear signal.

Notes: • For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI<sup>2</sup>OS interrupt clear signal.

- At the end of EI<sup>2</sup>OS, the EI<sup>2</sup>OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI<sup>2</sup>OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI<sup>2</sup>OS clear signal caused by the first event. So it is recommended not to use the EI<sup>2</sup>OS for this interrupt number.
- If EI<sup>2</sup>OS is enabled, EI<sup>2</sup>OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI<sup>2</sup>OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI<sup>2</sup>OS, the other interrupt should be disabled.

# MB90595/595G Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                             | Symbol           | Rating         |                | Unit | Remarks                                       |
|---------------------------------------|------------------|----------------|----------------|------|---|
|                                       |                  | Min.           | Max.           |      |   |
| Power supply voltage                  | $V_{CC}$         | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    |   |
|                                       | $AV_{CC}$        | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | $V_{CC} = AV_{CC}$ *1                         |
|                                       | $AVRH, AVRL$     | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | $AV_{CC} \geq AVRH/L,$<br>$AVRH \geq AVRL$ *1 |
|                                       | $DV_{CC}$        | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | $V_{CC} \geq DV_{CC}$                         |
| Input voltage                         | $V_I$            | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | *2  |
| Output voltage                        | $V_O$            | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | *2  |
| Clamp Current                         | $I_{CLAMP}$      | -2.0           | 2.0            | mA   |   |
| "L" level Max. output current         | $I_{OL1}$        | —              | 15             | mA   | Normal output *3                              |
| "L" level Avg. output current         | $I_{OLAV1}$      | —              | 4              | mA   | Normal output, average value *4               |
| "L" level Max. output current         | $I_{OL2}$        | —              | 40             | mA   | High current output *3                        |
| "L" level Avg. output current         | $I_{OLAV2}$      | —              | 30             | mA   | High current output, average value *4         |
| "L" level Max. overall output current | $\sum I_{OL1}$   | —              | 100            | mA   | Total normal output                           |
| "L" level Max. overall output current | $\sum I_{OL2}$   | —              | 330            | mA   | Total high current output                     |
| "L" level Avg. overall output current | $\sum I_{OLAV1}$ | —              | 50             | mA   | Total normal output, average value *5         |
| "L" level Avg. overall output current | $\sum I_{OLAV2}$ | —              | 250            | mA   | Total high current output, average value *5   |
| "H" level Max. output current         | $I_{OH1}$        | —              | -15            | mA   | Normal output *3                              |
| "H" level Avg. output current         | $I_{OHAV1}$      | —              | -4             | mA   | Normal output, average value *4               |
| "H" level Max. output current         | $I_{OH2}$        | —              | -40            | mA   | High current output *3                        |
| "H" level Avg. output current         | $I_{OHAV2}$      | —              | -30            | mA   | High current output, average value *4         |
| "H" level Max. overall output current | $\sum I_{OH1}$   | —              | -100           | mA   | Total normal output                           |
| "H" level Max. overall output current | $\sum I_{OH2}$   | —              | -330           | mA   | Total high current output                     |
| "H" level Avg. overall output current | $\sum I_{OHAV1}$ | —              | -50            | mA   | Total normal output, average value *5         |
| "H" level Avg. overall output current | $\sum I_{OHAV2}$ | —              | -250           | mA   | Total high current output, average value *5   |
| Power consumption                     | $P_D$            | —              | 500            | mW   | MB90F598/F598G                                |
|                                       |                  | —              | 400            | mW   | MB90598/<br>MB90598G (under development)      |
| Operating temperature                 | $T_A$            | -40            | +85            | °C   |   |
| Storage temperature                   | $T_{STG}$        | -55            | +150           | °C   |   |

\*1:  $AV_{CC}$ ,  $AVRH$  and  $AVRL$  does not exceed  $V_{CC}$  and  $AVRL$  does not exceed  $AVRH$ .

\*2:  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3V$ .  $V_I$  should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_I$  rating.

\*3: The maximum output current is a peak value for a corresponding pin.

\*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

\*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



## 2. Recommended Conditions

( $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter             | Symbol    | Value |      |      | Unit               | Remarks                         |
|-----------------------|-----------|-------|------|------|--------------------|---------------------------------|
|                       |           | Min.  | Typ. | Max. |                    |                                 |
| Power supply voltage  | $V_{CC}$  | 4.5   | 5.0  | 5.5  | V                  | Under normal operation          |
|                       | $AV_{CC}$ | 3.0   | —    | 5.5  | V                  | Maintains RAM data in stop mode |
| Smooth capacitor      | $C_S$     | 0.022 | 0.1  | 1.0  | $\mu\text{F}$      | *                               |
| Operating temperature | $T_A$     | -40   | —    | +85  | $^{\circ}\text{C}$ |                                 |

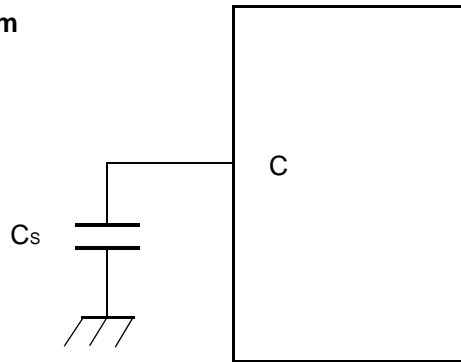
\*: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the  $V_{CC}$  pin must have a capacitance value higher than  $C_S$ .

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### • C Pin Connection Diagram



# MB90595/595G Series

## 3. DC Characteristics

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter               | Symbol     | Pin name                      | Condition  | Value          |               |                | Unit          | Remarks                             |
|-------------------------|------------|-------------------------------|--|----------------|---------------|----------------|---------------|-------------------------------------|
|                         |            |                               |  | Min.           | Typ.          | Max.           |               |                                     |
| Input H voltage         | $V_{IHS}$  | CMOS hysteresis input pin     | —  | $0.8 V_{CC}$   | —             | $V_{CC} + 0.3$ | V             |                                     |
|                         | $V_{IHM}$  | MD input pin                  | —  | $V_{CC} - 0.3$ | —             | $V_{CC} + 0.3$ | V             |                                     |
| Input L voltage         | $V_{ILS}$  | CMOS hysteresis input pin     | —  | $V_{SS} - 0.3$ | —             | $0.2 V_{CC}$   | V             |                                     |
|                         | $V_{ILM}$  | MD input pin                  | —  | $V_{SS} - 0.3$ | —             | $V_{SS} + 0.3$ | V             |                                     |
| Output H voltage        | $V_{OH1}$  | Output pins except P70 to P87 | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OH1} = -4.0\text{ mA}$  | $V_{CC} - 0.5$ | —             | —              | V             |                                     |
| Output H voltage        | $V_{OH2}$  | P70 to P87                    | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OH2} = -30.0\text{ mA}$   | $V_{CC} - 0.5$ | —             | —              | V             |                                     |
| Output L voltage        | $V_{OL1}$  | Output pins except P70 to P87 | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OL1} = 4.0\text{ mA}$   | —              | —             | 0.4            | V             |                                     |
| Output L voltage        | $V_{OL2}$  | P70 to P87                    | $V_{CC} = 4.5\text{ V}$ ,<br>$I_{OL2} = 30.0\text{ mA}$  | —              | —             | 0.5            | V             |                                     |
| Input leak current      | $I_{IL}$   |                               | $V_{CC} = 5.5\text{ V}$ ,<br>$V_{SS} < V_i < V_{CC}$   | -5             | —             | 5              | $\mu\text{A}$ |                                     |
| Power supply current *1 | $I_{CC}$   | $V_{CC}$                      | $V_{CC} = 5.0\text{ V} \pm 10\%$ ,<br>Internal frequency:<br>16 MHz,<br>At normal operating          | —              | 35            | 60             | $\text{mA}$   | MB90598,<br>MB90598G*2              |
|                         |            |                               |  | —              | 50            | 90             | $\text{mA}$   | MB90F598                            |
|                         |            |                               |  | —              | 40            | 60             | $\text{mA}$   | MB90F598G                           |
|                         | $I_{CCS}$  |                               | $V_{CC} = 5.0\text{ V} \pm 10\%$ ,<br>Internal frequency:<br>16 MHz,<br>At sleep                     | —              | 11            | 18             | $\text{mA}$   |                                     |
|                         | $I_{CTS}$  |                               | $V_{CC} = 5.0\text{ V} \pm 1\%$ ,<br>Internal frequency:<br>2 MHz,<br>At timer mode                  | —              | 0.3           | 0.6            | $\text{mA}$   |                                     |
|                         | $I_{CCH}$  |                               | $V_{CC} = 5.0\text{ V} \pm 10\%$ ,<br>At stop, $T_A = 25\text{ }^\circ\text{C}$                      | —              | —             | 20             | $\mu\text{A}$ |                                     |
|                         | $I_{CCH2}$ |                               | $V_{CC} = 5.0\text{ V} \pm 10\%$ ,<br>At Hardware stand-by mode,<br>$T_A = 25\text{ }^\circ\text{C}$ | —              | —             | 20             | $\mu\text{A}$ | MB90598,<br>MB90598G*2,<br>MB90F598 |
| —                       |            | 50                            |  | 100            | $\mu\text{A}$ | MB90F598G      |               |                                     |

(Continued)

# MB90595/595G Series

(Continued)

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter      | Symbol          | Pin name   | Condition | Value |      |      | Unit | Remarks |
|----------------|-----------------|--|-----------|-------|------|------|------|---------|
|                |                 |  |           | Min.  | Typ. | Max. |      |         |
| Input capacity | C <sub>IN</sub> | Other than C, AV <sub>CC</sub> , AV <sub>SS</sub> , AVRH, AVRL, V <sub>CC</sub> , V <sub>SS</sub> , DV <sub>CC</sub> , DV <sub>SS</sub> , P70 to P87 | —         | —     | 5    | 15   | pF   |         |
|                |                 | P70 to P87   | —         | —     | 15   | 30   | pF   |         |

\*1: Current values are tentative and subject to change without notice according to improvements in the characteristics. The power supply current testing conditions are when using the external clock.

\*2: Under development

# MB90595/595G Series

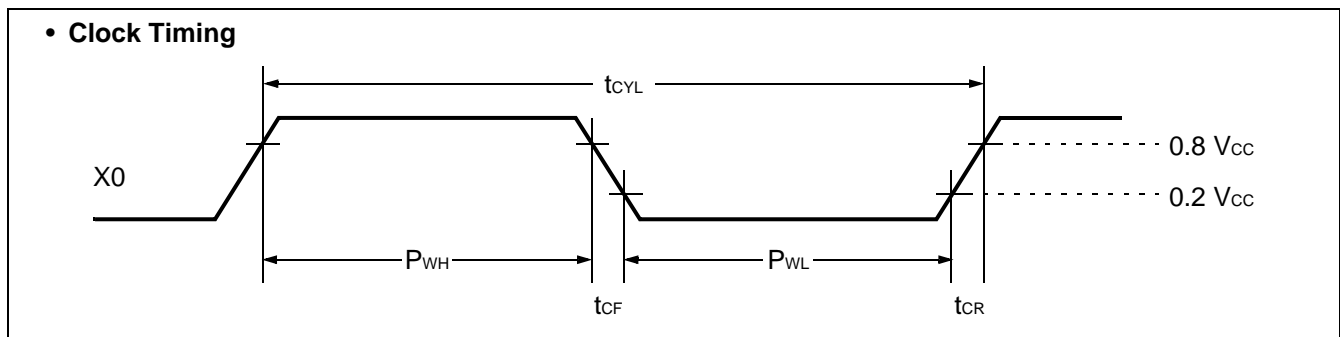
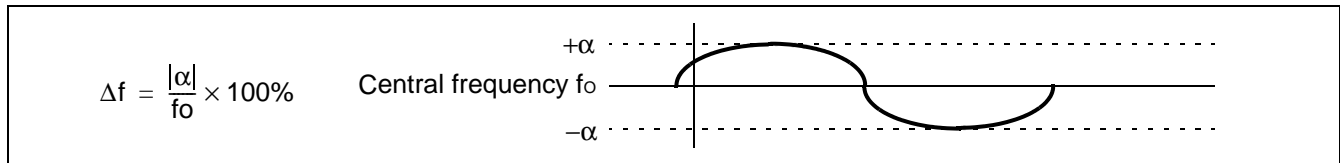
## 4. AC Characteristics

### (1) Clock Timing

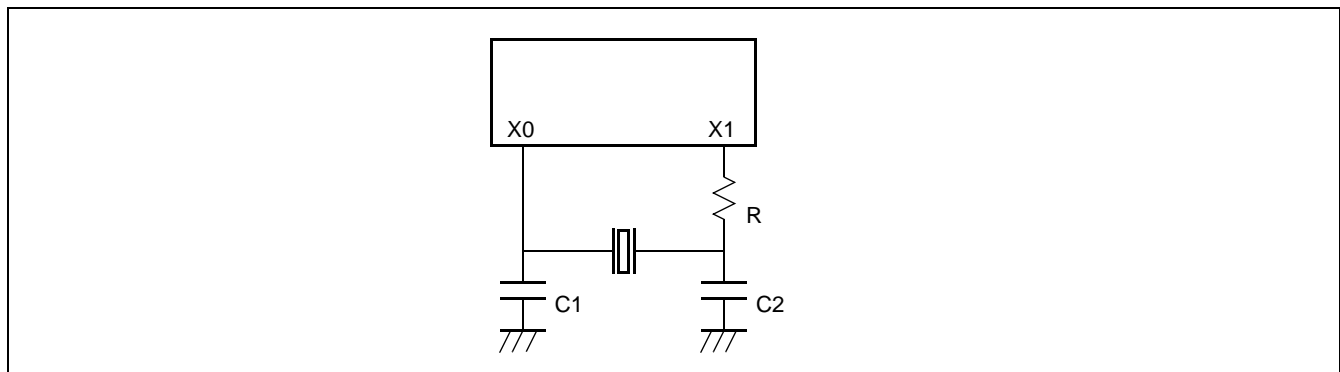
( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter                      | Symbol           | Pin name | Value |      |      | Unit | Remarks                           |
|--------------------------------|------------------|----------|-------|------|------|------|-----------------------------------|
|                                |                  |          | Min.  | Typ. | Max. |      |                                   |
| Oscillation frequency          | $f_c$            | X0, X1   | 3     | —    | 5    | MHz  | When using an oscillation circuit |
|                                |                  |          | 3     | —    | 16   | MHz  | When using an external clock      |
| Oscillation cycle time         | $t_{CYL}$        | X0, X1   | 200   | —    | 333  | ns   | When using an oscillation circuit |
|                                |                  |          | 62.5  | —    | 333  | ns   | When using an external clock      |
| Frequency deviation with PLL * | $\Delta f$       | —        | —     | —    | 5    | %    |                                   |
| Input clock pulse width        | $P_{WH}, P_{WL}$ | X0       | 10    | —    | —    | ns   | Duty ratio is about 30 to 70%.    |
| Input clock rise and fall time | $t_{CR}, t_{CF}$ | X0       | —     | —    | 5    | ns   | When using external clock         |
| Machine clock frequency        | $f_{CP}$         | —        | 1.5   | —    | 16   | MHz  |                                   |
| Machine clock cycle time       | $t_{CP}$         | —        | 62.5  | —    | 666  | ns   |                                   |

\*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

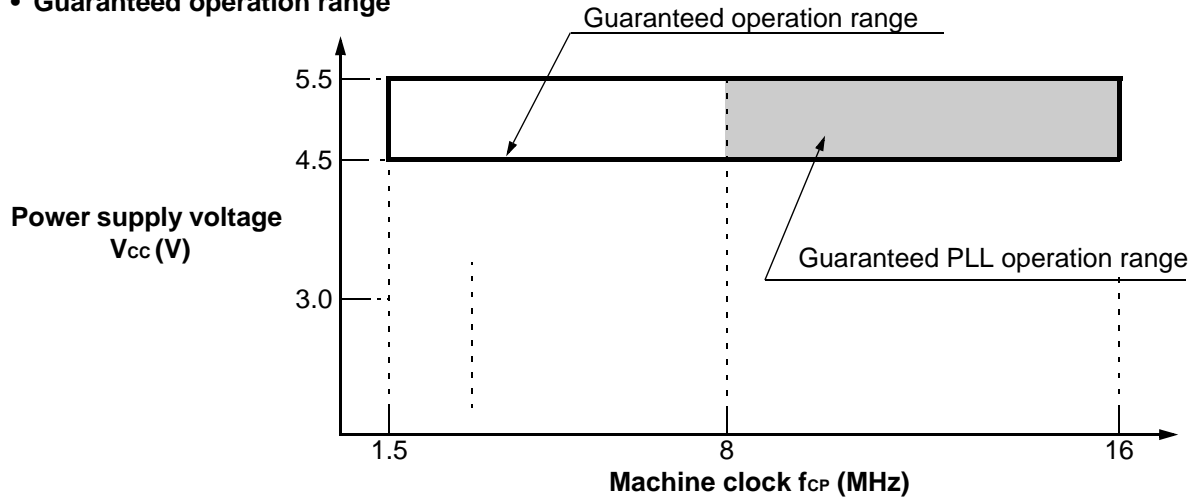


Example of Oscillation circuit

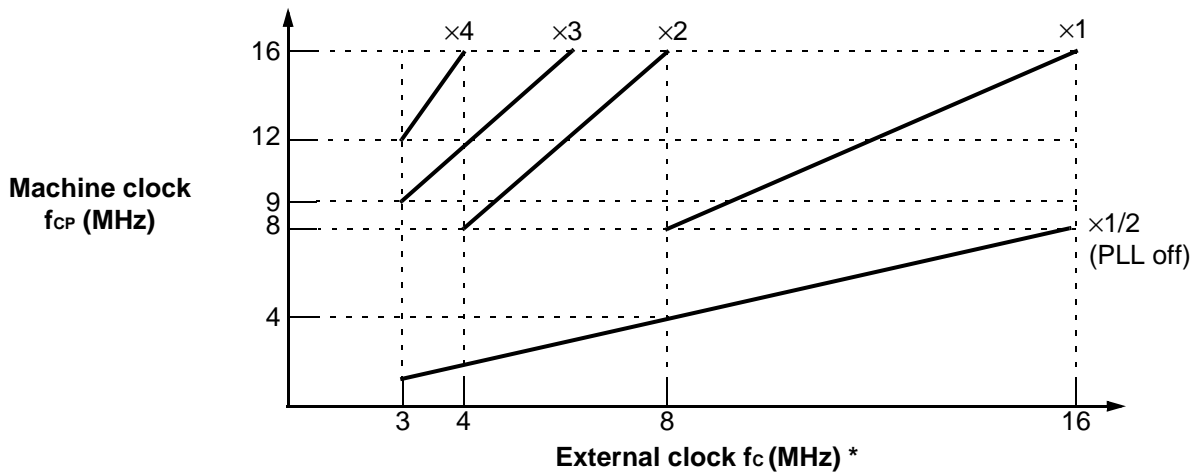


# MB90595/595G Series

- **Guaranteed operation range**



- **External clock frequency and machine clock frequency**

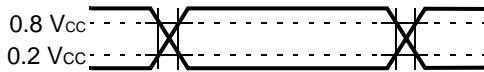


\*: When using the oscillation circuit, the maximum oscillation clock frequency is 5 MHz.

AC characteristics are set to the measured reference voltage values below.

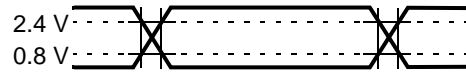
- **Input signal waveform**

**Hysteresis Input Pin**



- **Output signal waveform**

**Output Pin**



# MB90595/595G Series

## (2) Reset and Hardware Standby Input

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

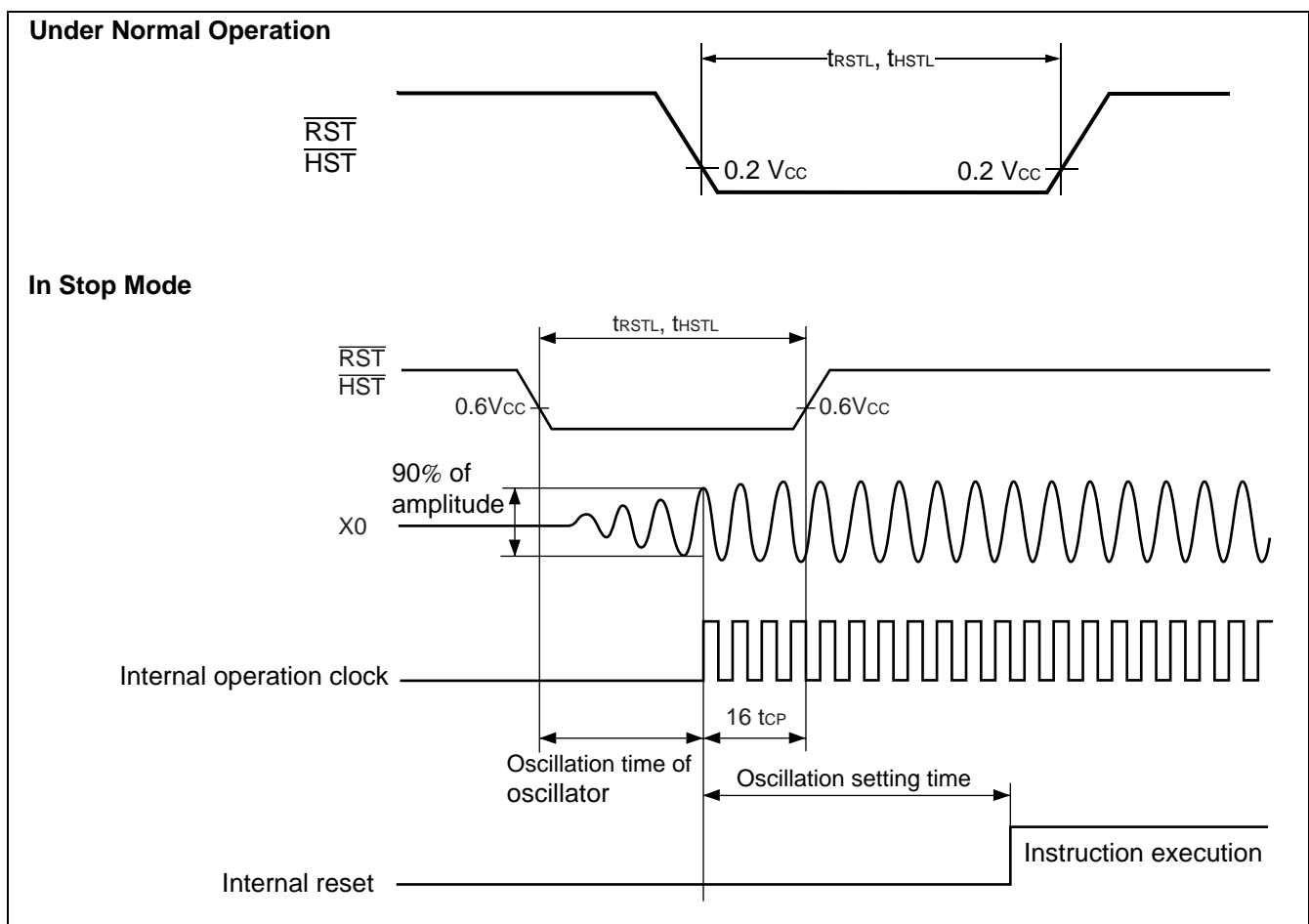
| Parameter                   | Symbol     | Pin name         | Value   |      | Unit | Remarks                |
|-----------------------------|------------|------------------|---|------|------|------------------------|
|                             |            |                  | Min.  | Max. |      |                        |
| Reset input time            | $t_{RSTL}$ | $\overline{RST}$ | $16 t_{CP}^{*1}$  | —    | ns   | Under normal operation |
|                             |            |                  | Oscillation time of oscillator <sup>*2</sup> + $16 t_{CP}^{*1}$ | —    | ms   | In stop mode           |
| Hardware standby input time | $t_{HSTL}$ | $\overline{HST}$ | $16 t_{CP}^{*1}$  | —    | ns   | Under normal operation |
|                             |            |                  | Oscillation time of oscillator <sup>*2</sup> + $16 t_{CP}^{*1}$ | —    | ms   | In stop mode           |

\*1: " $t_{CP}$ " represents one cycle time of the machine clock.

No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

\*2: Oscillation time of oscillator is time that the amplitude reached the 90%.

In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR / ceramic oscillator, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. In the external clock, the oscillation time is 0 ms.



## (3)Power On Reset

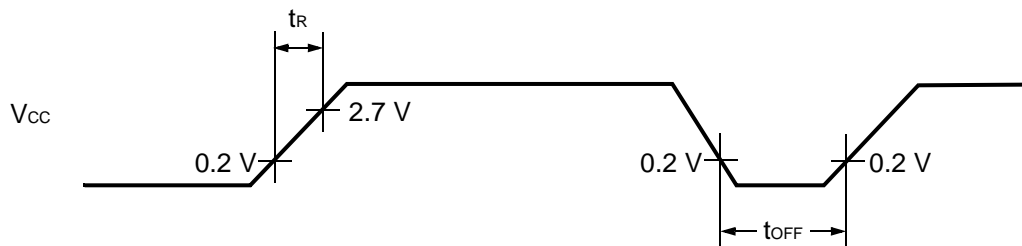
( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter          | Symbol    | Pin name | Condition | Value |      | Unit | Remarks                     |
|--------------------|-----------|----------|-----------|-------|------|------|-----------------------------|
|                    |           |          |           | Min.  | Max. |      |                             |
| Power on rise time | $t_R$     | $V_{CC}$ | —         | 0.05  | 30   | ms   | *                           |
| Power off time     | $t_{OFF}$ | $V_{CC}$ |           | 50    | —    | ms   | Due to repetitive operation |

\*:  $V_{CC}$  must be kept lower than 0.2 V before power-on.

Notes: • The above values are used for creating a power-on reset.

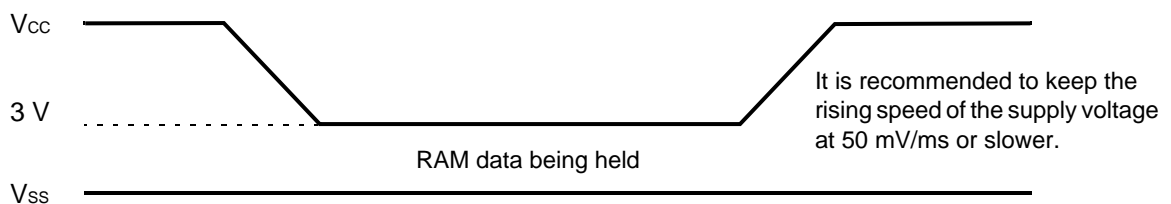
- Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.

To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.

In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



# MB90595/595G Series

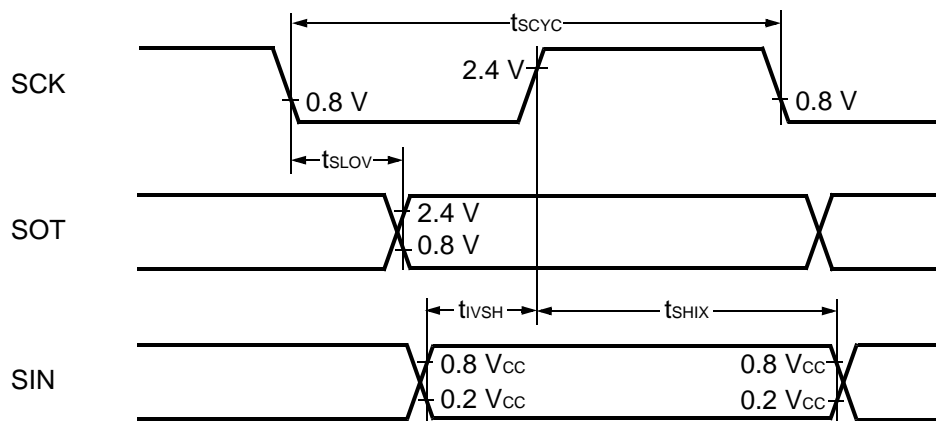
## (4) UART0/1, Serial I/O Timing

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter                    | Symbol     | Pin name                   | Condition  | Value      |      | Unit | Remarks |
|------------------------------|------------|----------------------------|--|------------|------|------|---------|
|                              |            |                            |  | Min.       | Max. |      |         |
| Serial clock cycle time      | $t_{SCYC}$ | SCK0 to SCK2               | Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ . | $8 t_{CP}$ | —    | ns   |         |
| SCK ↓ ⇒ SOT delay time       | $t_{SLOV}$ | SCK0 to SCK2, SOT0 to SOT2 |  | -80        | 80   | ns   |         |
| Valid SIN ⇒ SCK ↑            | $t_{VSH}$  | SCK0 to SCK2, SIN0 to SIN2 |  | 100        | —    | ns   |         |
| SCK ↑ ⇒ Valid SIN hold time  | $t_{SHIX}$ | SCK0 to SCK2, SIN0 to SIN2 |  | 60         | —    | ns   |         |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK0 to SCK2               | External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ . | $4 t_{CP}$ | —    | ns   |         |
| Serial clock "L" pulse width | $t_{LSLH}$ | SCK0 to SCK2               |  | $4 t_{CP}$ | —    | ns   |         |
| SCK ↓ ⇒ SOT delay time       | $t_{SLOV}$ | SCK0 to SCK2, SOT0 to SOT2 |  | —          | 150  | ns   |         |
| Valid SIN ⇒ SCK ↑            | $t_{VSH}$  | SCK0 to SCK2, SIN0 to SIN2 |  | 60         | —    | ns   |         |
| SCK ↑ ⇒ Valid SIN hold time  | $t_{SHIX}$ | SCK0 to SCK2, SIN0 to SIN2 |  | 60         | —    | ns   |         |

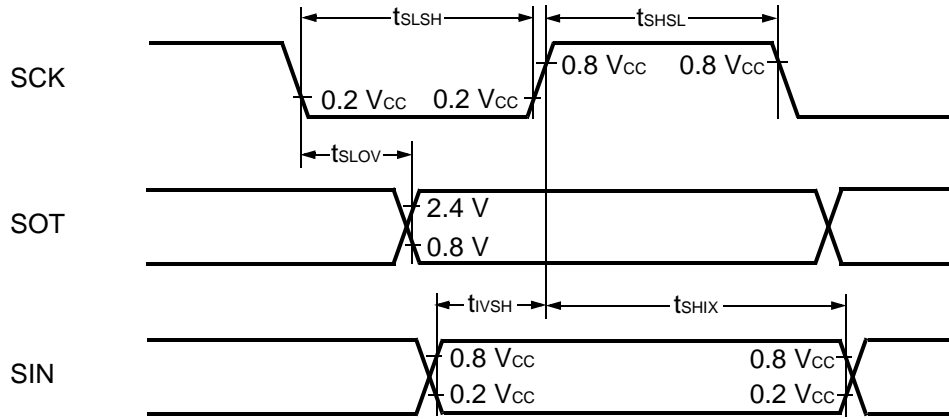
- Notes:
- AC characteristic in CLK synchronized mode.
  - $C_L$  is load capacity value of pins when testing.
  - $t_{CP}$  is the machine cycle (Unit: ns).

### • Internal Shift Clock Mode





• External Shift Clock Mode

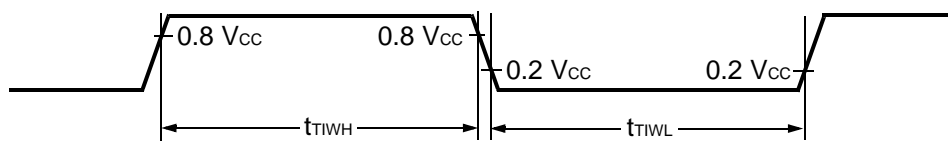


(5) Timer Input Timing

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter         | Symbol     | Pin name   | Condition | Value      |      | Unit | Remarks |
|-------------------|------------|------------|-----------|------------|------|------|---------|
|                   |            |            |           | Min.       | Max. |      |         |
| Input pulse width | $t_{TIWH}$ | TIN0, TIN1 | —         | $4 t_{CP}$ | —    | ns   |         |
|                   | $t_{TIWL}$ | IN0 to IN3 |           |            |      |      |         |

• Timer Input Timing



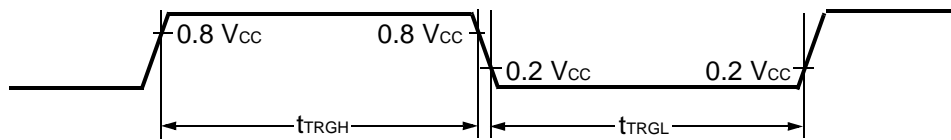
# MB90595/595G Series

## (6) Trigger Input Timing

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter         | Symbol     | Pin name   | Condition | Value      |      | Unit          | Remarks                |
|-------------------|------------|------------|-----------|------------|------|---------------|------------------------|
|                   |            |            |           | Min.       | Max. |               |                        |
| Input pulse width | $t_{TRGH}$ | INT0 to    | —         | $5 t_{CP}$ | —    | ns            | Under normal operation |
|                   | $t_{TRGL}$ | INT7, ADTG |           | 1          | —    | $\mu\text{s}$ | In stop mode           |

### • Trigger Input Timing



## (7) Slew Rate High Current Outputs (MB90598, MB90598G, MB90F598G only)

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter             | Symbol               | Pin name                            | Condition | Value |      |      | Unit | Remarks |
|-----------------------|----------------------|-------------------------------------|-----------|-------|------|------|------|---------|
|                       |                      |                                     |           | Min.  | Typ. | Max. |      |         |
| Output Rise/Fall time | $t_{R2}$<br>$t_{F2}$ | Port P70 to P77,<br>Port P80 to P87 | —         | 15    | 40   | 150  | ns   |         |

### • Slew Rate Output Timing



$$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$$

$$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$$

# MB90595/595G Series

## 5. A/D Converter

( $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $3.0\text{ V} \leq AVR_H - AVR_L$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter                     | Symbol    | Pin name   | Value         |               |               | Unit          | Remarks   |
|-------------------------------|-----------|------------|---------------|---------------|---------------|---------------|---|
|                               |           |            | Min.          | Typ.          | Max.          |               |   |
| Resolution                    | —         | —          | —             | —             | 10            | bit           |   |
| Conversion error              | —         | —          | —             | —             | $\pm 5.0$     | LSB           |   |
| Nonlinearity error            | —         | —          | —             | —             | $\pm 2.5$     | LSB           |   |
| Differential linearity error  | —         | —          | —             | —             | $\pm 1.9$     | LSB           |   |
| Zero transition voltage       | $V_{OT}$  | AN0 to AN7 | $AVR_L - 3.5$ | $AVR_L + 0.5$ | $AVR_L + 4.5$ | mV            |   |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | $AVR_H - 6.5$ | $AVR_H - 1.5$ | $AVR_H + 1.5$ | mV            |   |
| Conversion time               | —         | —          | —             | $352t_{CP}$   | —             | ns            |   |
| Sampling time                 | —         | —          | —             | $64t_{CP}$    | —             | ns            |   |
| Analog port input current     | $I_{AIN}$ | AN0 to AN7 | -10           | —             | 10            | $\mu\text{A}$ |   |
| Analog input voltage range    | $V_{AIN}$ | AN0 to AN7 | $AVR_L$       | —             | $AVR_H$       | V             |   |
| Reference voltage range       | —         | $AVR_H$    | $AVR_L + 2.7$ | —             | $AV_{CC}$     | V             |   |
|                               | —         | $AVR_L$    | 0             | —             | $AVR_H - 2.7$ | V             |   |
| Power supply current          | $I_A$     | $AV_{CC}$  | —             | 5             | —             | mA            |   |
|                               | $I_{AH}$  | $AV_{CC}$  | —             | —             | 5             | $\mu\text{A}$ | *1  |
| Reference voltage current     | $I_R$     | $AVR_H$    | —             | 400           | 600           | $\mu\text{A}$ | MB90V595,<br>MB90V595G,<br>MB90F598,<br>MB90F598G |
|                               |           |            | —             | 140           | 600           | $\mu\text{A}$ | MB90598,<br>MB90598G*2                            |
|                               | $I_{RH}$  | $AVR_H$    | —             | —             | 5             | $\mu\text{A}$ | *1  |
| Offset between input channels | —         | AN0 to AN7 | —             | —             | 4             | LSB           |   |

\*1: When not operating A/D converter, this is the current ( $V_{CC} = AV_{CC} = AVR_H = 5.0\text{ V}$ ) when the CPU is stopped.

\*2: Under development

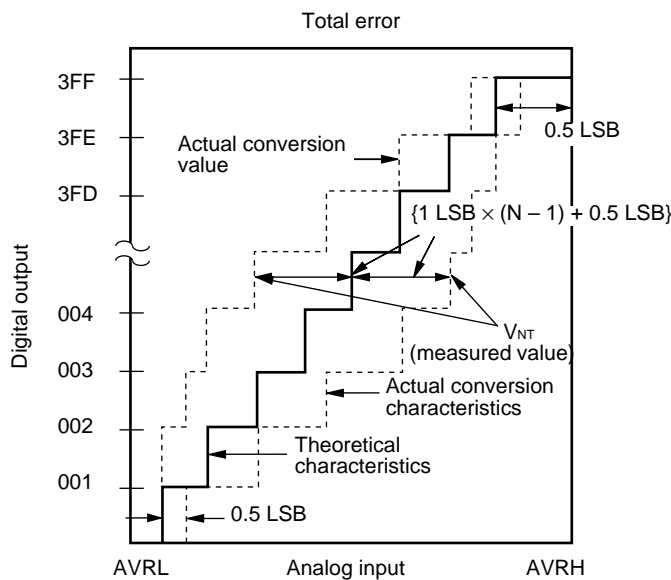
## 6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVRH - AVRL}{1024} \text{ [V]}$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

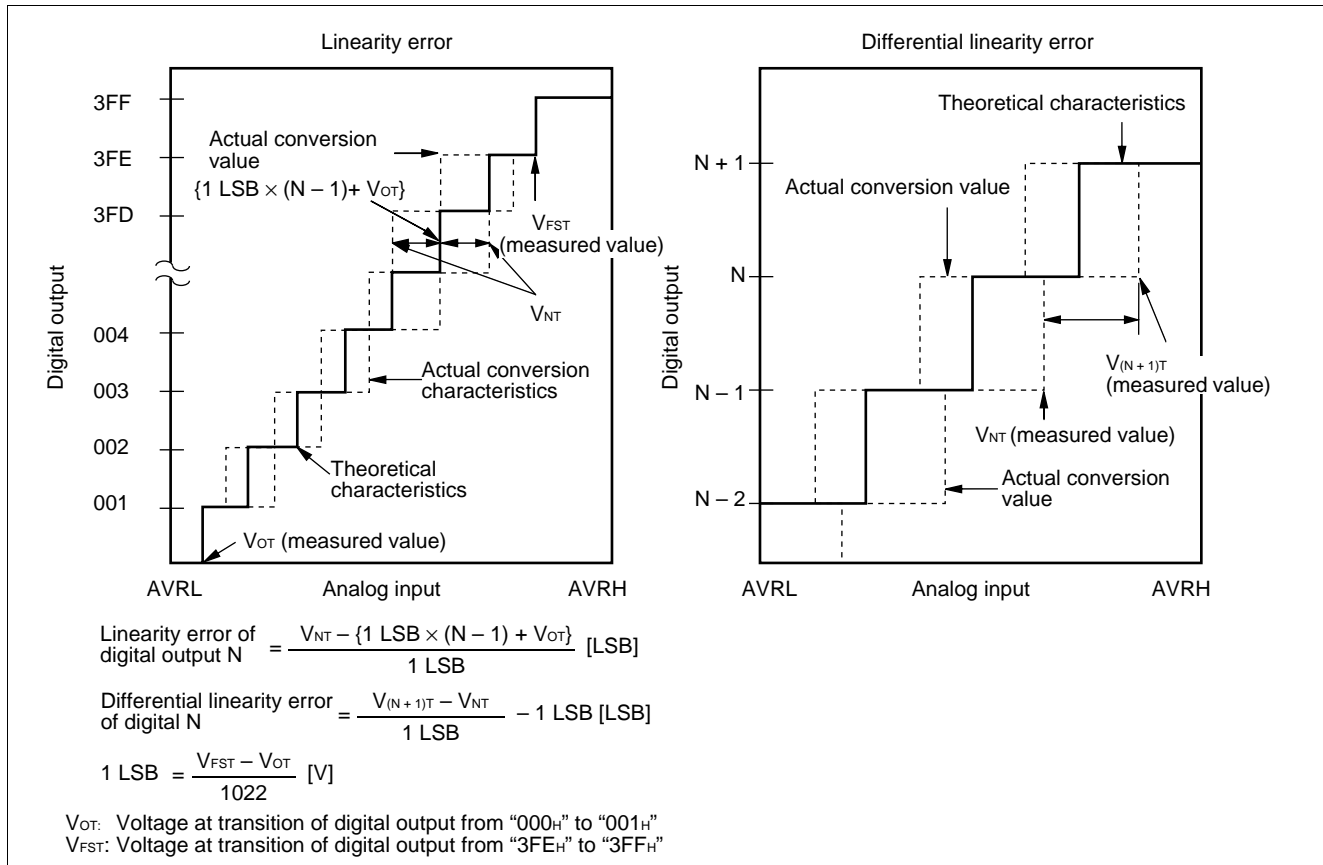
$$V_{0T} (\text{Theoretical value}) = AVRL + 0.5 \text{ LSB [V]}$$

$V_{NT}$ : Voltage at a transition of digital output from (N - 1) to N

$$V_{FST} (\text{Theoretical value}) = AVRH - 1.5 \text{ LSB [V]}$$

(Continued)

(Continued)



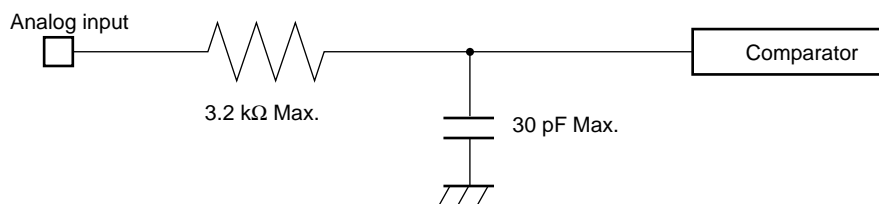
## 7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @ machine clock of 16 MHz).

### • Equipment of analog input circuit model



### • Error

The smaller the  $|AVRH - AVRL|$ , the greater the error would become relatively.

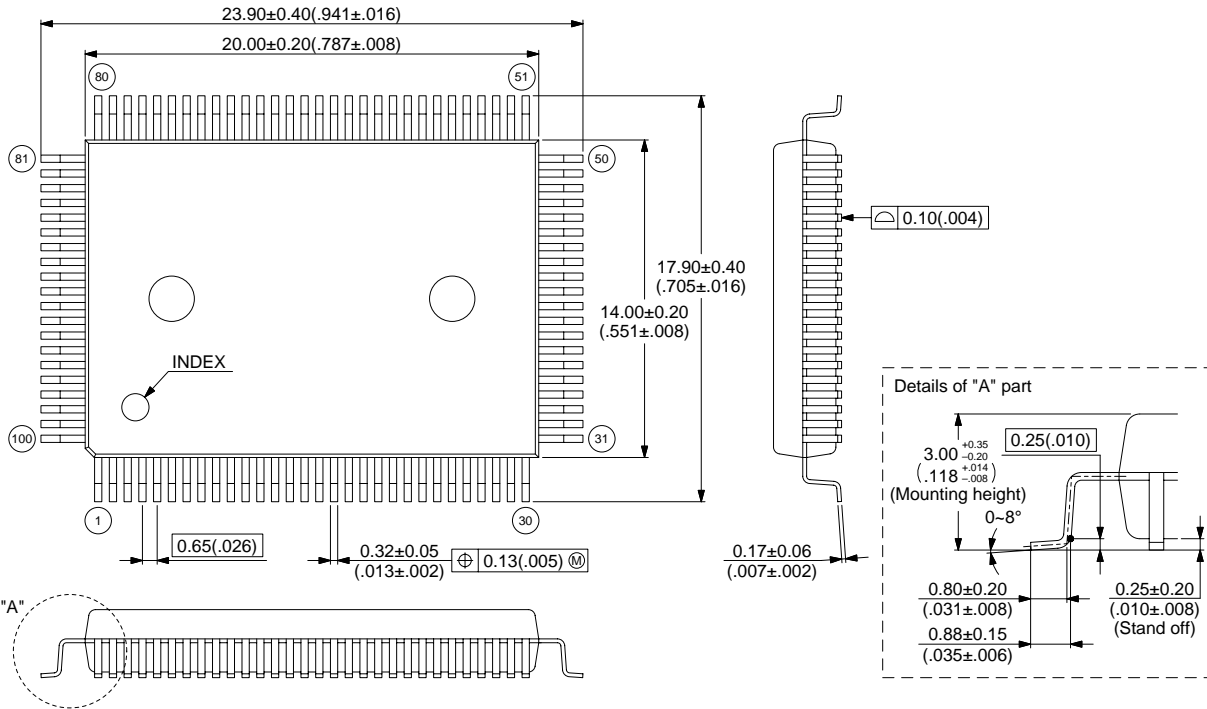
# MB90595/595G Series

## ■ ORDERING INFORMATION

| Part number  | Package                               | Remarks        |
|--|---------------------------------------|----------------|
| MB90598PF<br>MB90598GPF (under development)<br>MB90F598PF<br>MB90F598GPF | 100-pin Plastic QFP<br>(FPT-100P-M06) |                |
| MB90V595CR<br>MB90V595GCR  | 256-pin Ceramic PGA<br>(PGA-256C-A01) | For evaluation |

## ■ PACKAGE DIMENSION

100-pin plastic QFP  
(FPT-100P-M06)



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Dimensions in mm (inches)

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