FUJITSU SEMICONDUCTOR

FR50
32-BIT MICROCONTROLLER
MB91F369G
Data sheet

Release 2.1 20-Jun-2001
Fujitsu Ref. AEQ32046

FUJITSU MICROELECTRONICS EUROPE GmbH
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FUJITSU

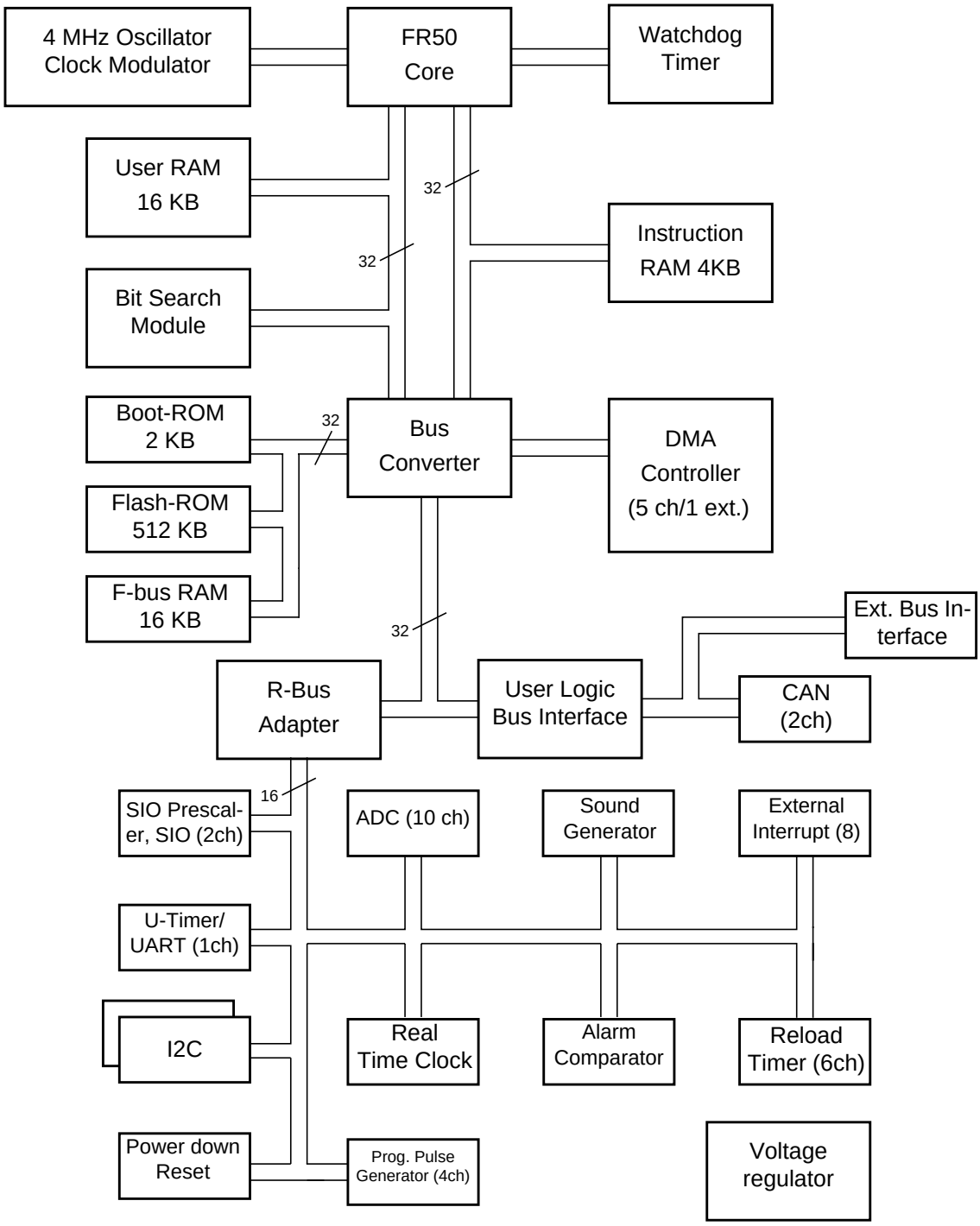
Revision History

Revision	Date	Name	Item
1.0	2000-10-16	Br+kg	First Release
1.1	2000-11-06	Br+kg	Add "old" I^2C module. Add Sound Generator.
1.2	2000-11-12	Br+kg	Replace DAC Pins by two ch. ADC input Flip I2C and Sound Generator in order to get Port M bits in correct orde.r
1.3	2001-01-16	kg	Remove unused ports from pin map.
1.4	2001-02-09	kg	Remove ports from memory map.
1.5	2001-02-12	kg	Add ADRSWAP to core function list and to F362MD chapter. Insert new cell type for MON-CLK pin.
1.6	2001-03-01	kg	New package.
1.7	2001-03-13	Br+kg	Add chapter for power consumption.
1.8	2001-04-11	Br	Add info about power routing in chapter 1.6 add info for bit 14 of F362MD, remove typos found in review on 28-Mar-01
1.9	2001-05-21	kg	Memory Map: Change naming of I2C registers consitently with HW-manual. Correct register bits for PFRs and DDRs
2.0	2001-06-08	Br	Correct Vil value for "automotive" inputs
2.1	2001-06-20	Br	Correct formula for calculation of current consumption

Table of Contents

1 MB91F369G Overview

1.1 MB91F369G Block Structure



1.2 Core Functionality

Function	Feature	Remarks
FR50 Core	32-bit Fujitsu RISC Core FR30 software compatible	
Clock module (clock control, clock divider, PLLs)	Setting of frequencies for CPU and peripherals (see MB91V360) Low power consumption modes: RTC mode: only the **R**eal **T**ime **C**lock and the oscillator are active (= STOP mode and bit 0 of STCR is set to 0) STOP mode: all internal circuits and the oscillation circuits are halted	initial value for oscillation stabilization time in mode MD="000": 32 ms at 4 MHz oscillation clock. Time starts after release of INITX
Watchdog	adjustable watchdog timer interval (between 2^{20} and 2^{26} system clock cycles)	
Instruction RAM 4 kB	RAM for instructions	see remark below table
User RAM 16 kB	RAM for user data	see remark below table
F-bus RAM 16 kB	RAM for data and code	see remark below table
Flash Memory FB35 512 kB	sector architecture: sector 0: 64 kB | sector 7: 64 kB sector 1: 64 kB | sector 8: 64 kB sector 2: 64 kB | sector 9: 64 kB sector 3: 32 kB | sector 10: 32 kB sector 4: 8 kB | sector 11: 8 kB sector 5: 8 kB | sector 12: 8 kB sector 6: 16 kB | sector 13: 16 kB | | V V 16 bit 16 bit write access is 16 bit wide, read access can be 16 or 32 bit wide	Minimum 10000 program/erase cycles Minimum 10 years data retention Net read cycle time to the memory: 40 ns. For overall access time see MB91360 Hardware Manual. located on F-Bus The last two addresses of this flash memory 0FFFF8H and 0FFFFCH overlap with the fixed reset and fixed mode vectors. Writing to these addresses is not possible.
Boot ROM 2 kB		
DMA	5 channels (1 channel external) up to 16 DMA sources can be used transfer modes: single/block, burst, continuous	
32 bit demultiplexed External Bus Interface	32 bit data, 21 bit address (extensible to 24 bit), up to 7 CS, CLK	can be set to HiZ by software: (refer to feature "Mode Register")

Interrupt Controller	8 external interrupt channels, 38 internal interrupts, 16 programmable priority levels	
Bit Search Module	Searches a word for the position of the first “1” and “0” change bit, starting from the MSB. Performs the search in 1 cycle.	
Fixed Reset Vector	Hardwired reset and mode vector	code starts at 0F:4000$_H$
Voltage Regulator	Generates internal voltage of 3.3 V	

Remark:

Set bit 9 (SYNCR) of TBCR to 1 to enable the synchronization of the reset signal; a reset will be generated only after all bus accesses have been done. This avoids that erroneous data are written into the RAMs during reset.

1.3 Features

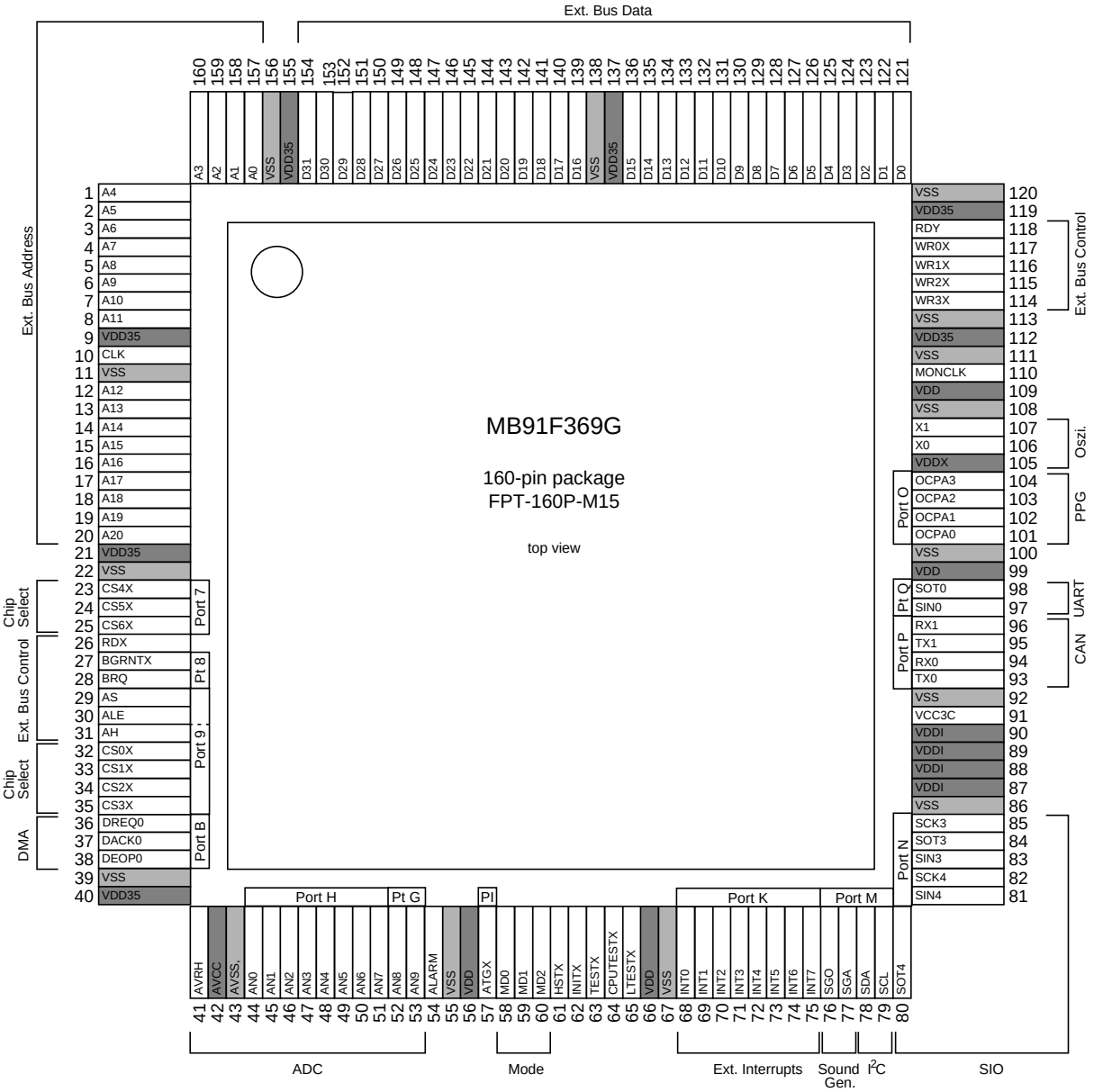
Function	Feature	Remarks
PPG for dimmer (4 channels)	16-bit PWM Timer 16 bit down counter, cycle and duty setting registers interrupt at triggering, cycle or duty match can be triggered by software or reload timer PWM operation and one-shot operation Clock disable internal prescaler allows $f_{RES}/1$, $f_{RES}/4$, $f_{RES}/16$, $f_{RES}/64$ as counter clock	 required frequencies are 90-300 Hz
ADC (10 channels)	successive approximation, internal sample and hold circuit 10-bit resolution, 5 V operation, (conversion time: 178 cycles of CLKP) program selectable analogue input channels: single conversion mode continuous conversion mode stop conversion mode interrupt at the end of a conversion can be used to activate DMA transfer activation by software, external trigger or reload timer can be selected Prescaling is done internally Clock disable	Maximum allowed frequency for digital part of ADC is 32 MHz
Basic Interval Timer (6 channels)	16-bit reload timer, includes clock prescaler ($f_{RES}/2^1$, $f_{RES}/2^3$, $f_{RES}/2^5$)	

CAN (2 channels)	conforms to CAN specification version 2.0 A and B automatic re-transmission in case of error automatic transmission responding to remote frame prioritized 16 message buffers for data and IDs supports multiple messages flexible configuration of acceptance filtering: full bit compare / full bit mask / two partial bit masks supports up to 1 Mb/s Clock Disable	
External Interrupt (8 channels)	can be programmed to be edge sensitive or level sensitive interrupt mask and request pending bits per channel	
Mode Register (F362MD)	Special Mode Register, controls - the I2C module selection, - the Address pin mapping, - the external bus disable mode	Address: $0001FE_H$ Bit 8: New I^2C select Bit 10-13: Ext.Bus high-Z control Bit 15: Address pin mapping
I^2C-1 for standard mode	master or slave transmission arbitration function clock synchronization function slave address and general call address detect function transfer direction detect function start condition repeat generation and detection function bus error detect function compatible to I^2C standard mode specification (operation up to 100 kHz, 7 bit addressing) includes clock divider functionality Clock disable	Only I^2C-1 or I^2C-2 can be used, not both in parallel. Bit 0 of F362MD will be used to decide which module is connected to the SCL and SDA pads. By default it is I^2C-1.

I^2C for standard and fast mode	master or slave transmission arbitration function clock synchronization function slave address and general call address detect function transfer direction detect function start condition repeat generation and detection function bus error detect function compatible to I^2C standard and fast mode specification (operation up to 400 kHz, 10 bit addressing) includes clock divider functionality Clock disable	SCL and SDA lines include optional noise filter. The noise filter allows the suppression of spikes in the range of 1 to 1.5 cycles of CLKP. Communication on the I2C bus between other connected devices is not possible if MB91F369G is switched off.
Alarm Comparator (OV/UV detection)	monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds status is readable, interrupts can be masked separately Clock disable	uses external 4:1 voltage divider
Sound Generator (Buzzer)	8-bit PWM signal is mixed with tone frequency from 8-bit reload counter PWM clock by internal prescaler: $f_{RES}/1$, $f_{RES}/2$, $f_{RES}/4$, $f_{RES}/8$ tone frequency: PWM frequency / 2 / (reload value + 1) Clock disable	Target frequency to be programmable in the range of 300 Hz to 5 kHz $f_{RES}/1$ and a reload value of 5 result in 5.2 kHz at f_{RES} = 16MHz, $f_{RES}/4$ and a reload value of 25 result in 300.48 Hz @ f_{RES} = 16MHz
Power down reset	monitors Vdd and generates a reset if Vdd is less than a defined threshold voltage	is disabled in RTC and STOP mode
Serial IO SIO Synchronous Serial Interface (2 channels) + SIO-Prescaler (2 channels)	Serial IO transfer can be started from MSB or LSB supports internal clock synchronized transfer and external clock synchronized transfer prescaler for shift clock allows: $f_{RES}/3$, $f_{RES}/4$, $f_{RES}/5$, $f_{RES}/6$, $f_{RES}/7$, $f_{RES}/8$ Clock disable	supports positive and negative clock edge synchronization

UART (1 channel)	serial I/O port for performing asynchronous (start-stop synchronization) communication full duplex, double buffering supports multi-processor mode variable data length (7/8 bit) 1 or 2 stop bits error detection function (parity, framing, overrun) interrupt function NRZ type transfer format baud rate generated by U-Timer 16-bit timer to generate the required UART clock: $f_{RES}/2^5,\ldots,\sim f_{RES}/2^{21}$ (asynchr. mode) Clock disable	polarity of the port signals for receive and transmit is programmable
U-Timer (1 per UART)		
Real Time Clock (RTC) (Watch Timer)	facility to correct oscillation deviation read/write accessible second/minute/hour registers can signal interrupts every second/minute/hour/day internal clock divider and prescaler provide exact 1s clock based on the 4 MHz input Clock disable	prescaler value for 4 MHz is $1E847F_H$
Clock modulator	See chapter 7.5	

1.4 Pin Assignment



1.5 I/O Pins and Their Functions

Pin No.	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
1	A4	I/O		Q	Ext. Bus Address Bit 4
2	A5	I/O		Q	Ext. Bus Address Bit 5
3	A6	I/O		Q	Ext. Bus Address Bit 6
4	A7	I/O		Q	Ext. Bus Address Bit 7
5	A8	I/O		Q	Ext. Bus Address Bit 8
6	A9	I/O		Q	Ext. Bus Address Bit 9
7	A10	I/O		Q	Ext. Bus Address Bit 10
8	A11	I/O		Q	Ext. Bus Address Bit 11
9	VDD35				separated Ext.Bus VDD, 3.3 or 5.0 V
10	CLK	I/O		A	Ext. Bus CLock
11	VSS				
12	A12	I/O		Q	Ext. Bus Address Bit 12
13	A13	I/O		Q	Ext. Bus Address Bit 13
14	A14	I/O		Q	Ext. Bus Address Bit 14
15	A15	I/O		Q	Ext. Bus Address Bit 15
16	A16	I/O		Q	Ext. Bus Address Bit 16
17	A17	I/O		Q	Ext. Bus Address Bit 17
18	A18	I/O		Q	Ext. Bus Address Bit 18
19	A19	I/O		Q	Ext. Bus Address Bit 19
20	A20	I/O		Q	Ext. Bus Address Bit 20
21	VDD35				separated Ext.Bus VDD, 3.3 or 5.0 V
22	VSS				
23	CS4X	I/O	P74	A	Chip Select 4
24	CS5X	I/O	P75	A	Chip Select 5
25	CS6X	I/O	P76	A	Chip Select 6
26	RDX	I/O		S	Ext. Bus Control
27	BGRNTX	I/O	P81	A	Ext. Bus Control
28	BRQ	I/O	P82	A	Ext. Bus Control

Pin No.	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
29	AS	I/O	P90	A	Ext. Bus Control
30	ALE	I/O	P91	A	Ext. Bus Control
31	AH	I/O	P93	A	Ext. Bus Control Signal
32	CS0X	I/O	P94	A	Chip select 0
33	CS1X	I/O	P95	A	Chip Select 1
34	CS2X	I/O	P96	A	Chip Select 2
35	CS3X	I/O	P97	A	Chip Select 3
36	DREQ0	I/O	PB0	A	DMA Request 0
37	DACK0	I/O	PB1	A	DMA Acknowledge 0
38	DEOP0	I/O	PB2	A	DMA EOP 0
39	VSS				
40	VDD35				separated Ext.Bus VDD, 3.3 or 5.0 V
41	AVRH			R	Analog Reference High
42	AVCC				Analog VCC
43	AVSS, AVRL				Analog VSS, Analog Reference Low
44	AN0	I/O	PH0	B	ADC Input 0
45	AN1	I/O	PH1	B	ADC Input 1
46	AN2	I/O	PH2	B	ADC Input 2
47	AN3	I/O	PH3	B	ADC Input 3
48	AN4	I/O	PH4	B	ADC Input 4
49	AN5	I/O	PH5	B	ADC Input 5
50	AN6	I/O	PH6	B	ADC Input 6
51	AN7	I/O	PH7	B	ADC Input 7
52	AN8	I/O	PG0	B	ADC Input 8
53	AN9	I/O	PG1	B	ADC Input 9
54	ALARM	I		D	Alarm Comparator Input
55	VSS				
56	VDD				
57	ATGX	I/O	PI3	A	ADC Trigger Input

Pin No.	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
58	MD0	I		T	Mode Pin 0
59	MD1	I		T	Mode Pin 1
60	MD2	I		T	Mode Pin 2
61	HSTX	I		E	Hardware Standby
62	INITX	I		U	Initial Pin
63	TESTX	I		E	Test Input (should be connected to VDD)
64	CPUTESTX	I		E	Test Input (should be connected to VDD)
65	LTESTX	I		E	Test Input (should be connected to VDD)
66	VDD				
67	VSS				
68	INT0	I/O	PK0	A	Ext. Interrupt 0
69	INT1	I/O	PK1	A	Ext. Interrupt 1
70	INT2	I/O	PK2	A	Ext. Interrupt 2
71	INT3	I/O	PK3	A	Ext. Interrupt 3
72	INT4	I/O	PK4	A	Ext. Interrupt 4
73	INT5	I/O	PK5	A	Ext. Interrupt 5
74	INT6	I/O	PK6	A	Ext. Interrupt 6
75	INT7	I/O	PK7	A	Ext. Interrupt 7
76	SGO	I/O	PM0	A	Sound Generator SGO
77	SGA	I/O	PM1	A	Sound Generator SGA
78	SDA	I/O	PM2	Y	I2C SDA
79	SCL	I/O	PM3	Y	I2C SCL
80	SOT4	I/O	PN0	A	SIO Output
81	SIN4	I/O	PN1	A	SIO Input
82	SCK4	I/O	PN2	A	SIO Clock
83	SIN3	I/O	PN3	A	SIO Input
84	SOT3	I/O	PN4	A	SIO Output
85	SCK3	I/O	PN5	A	SIO Clock
86	VSS				
87	VDDI				Supply voltage for internal regulator

Pin No.	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
88	VDDI				Supply voltage for internal regulator
89	VDDI				Supply voltage for internal regulator
90	VDDI				Supply voltage for internal regulator
91	VCC3C				Capacitor pin for internal regulator
92	VSS				
93	TX0	I/O	PP0	Q	CAN 0 TX
94	RX0	I/O	PP1	Q	CAN 0 RX
95	TX1	I/O	PP2	Q	CAN 1 TX
96	RX1	I/O	PP3	Q	CAN 1 RX
97	SIN0	I/O	PQ0	A	UART 0 Input
98	SOT0	I/O	PQ1	A	UART 0 Output
99	VDD				
100	VSS				
101	OCPA0	I/O	PO0	A	PPG Output
102	OCPA1	I/O	PO1	A	PPG Output
103	OCPA2	I/O	PO2	A	PPG Output
104	OCPA3	I/O	PO3	A	PPG Output
105	VDDX				
106	X0			H	4 MHz Oscillator Pin
107	X1			H	4 MHz Oscillator Pin
108	VSS				
109	VDD				
110	MONCLK	O		Q1	System Clock Output
111	VSS				
112	VDD35				separated Ext.Bus VDD, 3.3 or 5.0 V
113	VSS				
114	WR3X	I/O		S	Ext. Bus Control
115	WR2X	I/O		S	Ext. Bus Control
116	WR1X	I/O		S	Ext. Bus Control
117	WR0X	I/O		S	Ext. Bus Control

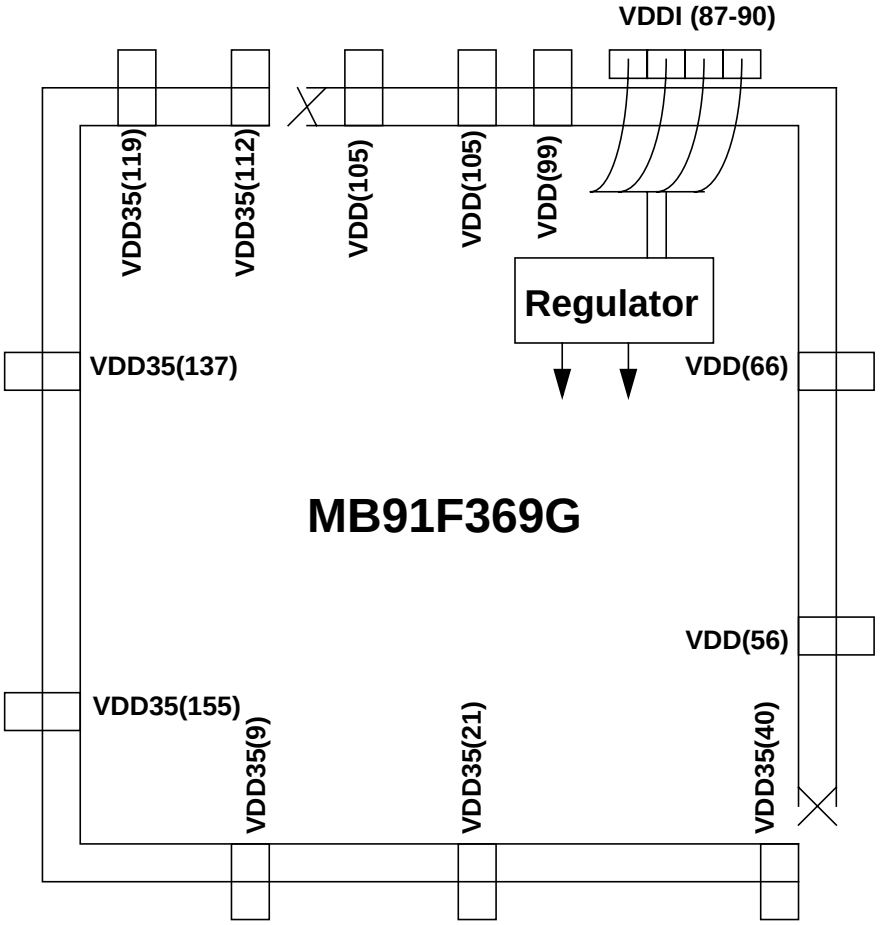
Pin No.	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
118	RDY	I/O		S	Ext. Bus Control
119	VDD35				separated Ext.Bus VDD, 3.3 or 5.0 V
120	VSS				
121	D0	I/O		Q	Ext. Bus Data Bit 0
122	D1	I/O		Q	Ext. Bus Data Bit 1
123	D2	I/O		Q	Ext. Bus Data Bit 2
124	D3	I/O		Q	Ext. Bus Data Bit 3
125	D4	I/O		Q	Ext. Bus Data Bit 4
126	D5	I/O		Q	Ext. Bus Data Bit 5
127	D6	I/O		Q	Ext. Bus Data Bit 6
128	D7	I/O		Q	Ext. Bus Data Bit 7
129	D8	I/O		Q	Ext. Bus Data Bit 8
130	D9	I/O		Q	Ext. Bus Data Bit 9
131	D10	I/O		Q	Ext. Bus Data Bit 10
132	D11	I/O		Q	Ext. Bus Data Bit 11
133	D12	I/O		Q	Ext. Bus Data Bit 12
134	D13	I/O		Q	Ext. Bus Data Bit 13
135	D14	I/O		Q	Ext. Bus Data Bit 14
136	D15	I/O		Q	Ext. Bus Data Bit 15
137	VDD35				separated Ext.Bus VDD, 3.3 or 5.0 V
138	VSS				
139	D16	I/O		Q	Ext. Bus Data Bit 16
140	D17	I/O		Q	Ext. Bus Data Bit 17
141	D18	I/O		Q	Ext. Bus Data Bit 18
142	D19	I/O		Q	Ext. Bus Data Bit 19
143	D20	I/O		Q	Ext. Bus Data Bit 20
144	D21	I/O		Q	Ext. Bus Data Bit 21
145	D22	I/O		Q	Ext. Bus Data Bit 22
146	D23	I/O		Q	Ext. Bus Data Bit 23
147	D24	I/O		Q	Ext. Bus Data Bit 24

Pin No.	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
148	D25	I/O		Q	Ext. Bus Data Bit 25
149	D26	I/O		Q	Ext. Bus Data Bit 26
150	D27	I/O		Q	Ext. Bus Data Bit 27
151	D28	I/O		Q	Ext. Bus Data Bit 28
152	D29	I/O		Q	Ext. Bus Data Bit 29
153	D30	I/O		Q	Ext. Bus Data Bit 30
154	D31	I/O		Q	Ext. Bus Data Bit 31
155	VDD35				separated Ext.Bus VDD, 3.3 or 5.0 V
156	VSS				
157	A0	I/O		Q	Ext. Bus Address Bit 0
158	A1	I/O		Q	Ext. Bus Address Bit 1
159	A2	I/O		Q	Ext. Bus Address Bit 2
160	A3	I/O		Q	Ext. Bus Address Bit 3

If V_{DD} pins 9, 21, 40, 112, 119, 137 and 155 are connected to 3.3 V externally, the external bus interface (pins 1-40 and 112-160) can be operated at 3.3 V levels. .At 3.3 V operation the specifications for $V_{outHIGH}$ and V_{outLOW} given in the chapter about operating conditions are not valid.

Circuit Type	Description
A	I/O, IOH=4 mA / IOL=4 mA, CMOS Automotive Schmitt-Trigger Input, STOP control
B	I/O, IOH=4 mA / IOL=4 mA, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control
C	Analog Output
D	Analog Input
E	CMOS Schmitt-Trigger Input, 50K Pull-up
F	CMOS Schmitt-Trigger Input
H	4 MHz Oscillator Pin
Q	I/O, IOH=4 mA / IOL=4 mA, CMOS Input, STOP control
Q1	O, IOH=8 mA / IOL=8 mA, STOP control
R	AVRH Input
S	I/O, IOH=4 mA / IOL=4 mA, CMOS Input, STOP control, 10K Pull-up Resistor
T	CMOS Input, can withstand V_{ID} for flash programming
U	CMOS Schmitt-Trigger Input, 50K Pull-up, 3.3 V and 5 V inputs to core
Y	I/O, IOH=3mA / IOL=3mA (I2C), CMOS Input, STOP control

1.6 Power routing overview



1.7 Flash Memory Mode of MB91F369G

To enter the flash memory mode set mode pins MD0 to MD2 to “111”. In this mode, the pins correspond to those of the MBM29LV400C standard flash memory as shown in the following table.

MB91F369G				MBM29LV400C
Pin number	**Normal function**	**Flash Memory mode**	**Function in Flash Memory mode**	
58	MD0	HVDA9	High Volt. A9 [c]	A9 (V_{ID})
59	MD1	HVDR5	High Volt. RESET [c]	$\overline{RESET}$ (V_{ID})
60	MD2	HVDOE	High Volt. OE [c]	$\overline{OE}$ (VID)
62	INITX	RSTX	Hardware Reset	$\overline{RESET}$
68	INT0	RY/BYX	Ready/Busy	RY/$\overline{BY}$
69	INT1	CEX	Chip Enable	$\overline{CE}$
70	INT2	TSTX [a]	Flash Test	
71	INT3	BYTEX	switch 8/16 bit mode	$\overline{BYTE}$
72	INT4	WEX	Write Enable	$\overline{WE}$
73	INT5	OEX	Output Enable	$\overline{OE}$
74	INT6	ATDIN[b]	Access Signal ATD	
75	INT7	EQIN[b]	Access Signal EQ	
121 to 136	D0 to D15	AQ19 downto AQ4	Address input	A19 downto A4
139 to 154	D16 to D31	DQ16 to DQ31	Data input/outpu	DQ0 to DQ15
157 to 160	A0 to A3	AQ0 to AQ3	Address input	A0 to A3

a.Pin 70 must be pulled high in Flash Memory Mode.
b.Pins 74 and 75 must be pulled low in Flash Memory Mode
c.Functionality as described in the Data Sheet of MBM29LV400C.

AVRH must be tight to a high level, ALARM to a low level. All other Pins can be left open during Flash Memory Mode.

2 IO-Map

See Appendix A I/O Map on page 34 of this specification.

The addresses shown in this table for CAN registers are based on the settings for CS7 done in the Boot ROM.

3 Interrupt Vector Table

See Appendix B Interrupt Vectors on page 52 of this specification.

4 Power-on sequence

All VDD pins should be connected to the same potential (exception see chapter 1.5). The analogue supply voltage (AVCC) must not be turned on before the digital supply voltage. If the external bus interface is supplied with 3.3 V as described in chapter 1 this voltage also must not be turned on before the 5V digital voltage has been switched on. If the supply voltage to the external bus interface is switched off (it may not be tristate but should be pulled low) it must be made sure that all related signals do not have a voltage higher than this pulled down supply.

Immediately after power on always execute INIT at the INITX pin (input a low level to the INITX pin). Hold this low level at the INITX pin long enough so that after release of the low level at INITX and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. INITX must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

5 Handling of Unused Input Pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be tied to VDD or VSS through resistors. In this case those resistors should be more than 2 KOhm.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

The resistor of more than 2 KOhm is used to limit currents through the protection diodes. In case of voltages at the unused pin of 0.3 V or more below VSS or 0.3 V or more above VDD currents which could cause latch-up will flow through those diodes. It is possible to use one resistor to connect several pins to VDD or VSS. Care should be taken not to connect pins from different supply voltage domains to one resistor.

6 Emulation Device

6.1 Overview

MB91FV360GA can be used as emulation device for MB91F369G .

MB91F369G uses the following resources of this chip:

- Reload Timer 0 - Reload Timer 5
- UART 0 / U-Timer 0
- SIO 0 - SIO 1 and their Prescalers
- I^2C (100 kHz and 400 kHz)
- A/D Converter (channels 0 - 9)
- Sound Generator

- Real Time Clock
- Programmable Pulse Generators: PWM Control 0 and PWM channels 0 - 3
- Power Down Reset
- Alarm Comparator
- CAN 0 - CAN 1
- User RAM 16 kB: address range 03C000 - 03FFFF
- F-Bus RAM 16 kB: address range 040000 - 043FFF
- I-RAM 4 kB: address range 011000 - 011FFF
- Flash Memory 512 kB (on F-Bus): address range 080000 - 0FFFF7

6.2 F369G Mode Register (F362MD)

This register is used to control which pins of the external bus interface are active, where the pins for the

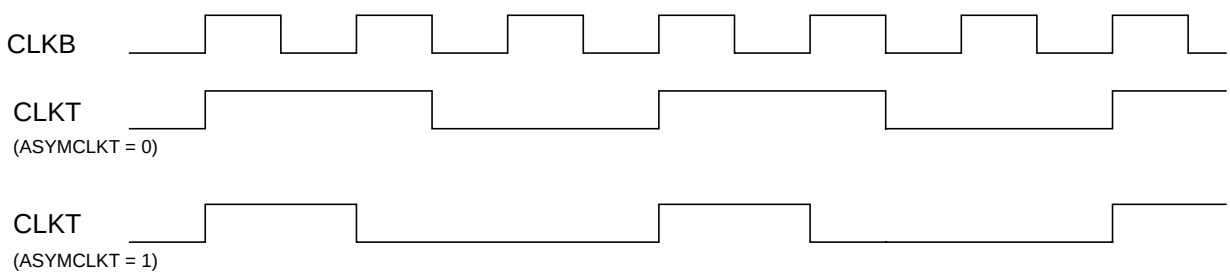
address	bit 15	bit14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
$00001FE_H$	ADR-SWAP	ASYM CLKT	HIZ_D_A	HIZ_ECLK	HIZ_D_23_16	HIZ_D_15_0	----	IICSEL
access	R/W	R/W	R/W	R/W	R/W	R/W		R/W
initial value	0	0	0	0	0	0		0

external DMA channel are located and which I^2C module is used.

Bit 15: ADRSWAP switches between CS signals and address extention to 24 bit:
0: Pin 23 = CS4X, Pin 24 = CS5X, Pin 25 = CS6X
1: Pin 23 = A[21] , Pin 24 = A[22] , Pin25 = A[23]

Bit 14: Bit 14: ASYMCLKT
0: duty cycle for CLKT is 1:1
1: for odd ratios between CLKB and CLKT (1:3, 1:5, ...) the high pulse of CLKT will be shortened by the length of 1 high pulse of CLKB

Example for CLKB:CLKT = 1:3



Bit 13: HIZ_D_A
0: D[31:24], A[20:0], RDX, WR3X, WR2X, WR1X, WR0X outputs enabled
1: D[31:24], A[20:0], RDX, WR3X, WR2X, WR1X, WR0X outputs high-Z

Bit 12: HIZ_ECLK controls the clock output of the external bus:
0: CLK output enabled
1: CLK output high-Z

Bit 11: HIZ_D_23_16

0: D[23:16] outputs enabled
1: D[23:16] outputs high-Z

Bit 10: HIZ_D_15_0

0: D[15:0] outputs enabled
1: D[15:0] outputs high-Z

Bit 9: reserved (unused on MB91F369G), writing to this register has no effect

Bit 8: IICSEL
0: selection of 100 kHz I^2C interface (I^2C-1)
1: selection of 400 kHz I^2C interface (I^2C-2)

6.3 Changes in Boot ROM

The following changes with regard to earlier devices have been implemented in the BOOT ROM of MB91F369G:

- The BOOT pin is NOT checked for a boot condition.
- There is no SELCLK pin to be checked.
- The security vector is valid in the following ranges:
  08 : 0000 - 0F : FFFF
  18 : 0000 - 1F : FFFF
  20 : 0000 - 2F : FFFF

7 Electrical specification

7.1 Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Condition
Digital supply voltage	VDD-VSS	-0.3	6.0	V	
Storage temperature	ϑ_{ST}	-55	125	°C	
Power consumption	P_{TOT}		2500	mW	$\vartheta_{ambient}$ = 25°C
Digital input voltage	V_{IDIG}	-0.3 *	5.8	V	VSS=0V, VDD=5V
Analog input voltage	V_{IA}	-0.3	5.8	V	VSSA=0V, VDDA=5V
Analog supply voltage	VDDA-VSSA	-0.3	5.8	V	VSSA=0V
Analog reference voltage	$V_{REFH/L}$ - VSSA	-0.3	5.8	V	VSSA=0V
Static DC current into digital I/O	$I_{I/ODC}$	-2	2	mA	$\Sigma I_{I/ODC} < I_{SOperation}$

***** Making full use of the allowed static DC current into digital I/Os will lead to lower values here.

7.2 Operating Conditions

Parameter	**Symbol**	**min.**	**typ.**	**max.**	**Unit**	**Condition**
Operating temperature	ϑ_{OP}	-40		85	°C	
Supply voltage						Internal voltage reg.
- Digital supply	VDD-VSS	4.25 [1)]	5	5.25	V	VDD_{CORE}=3.3V
- Analog supply	VDDA-VSSA	4.9	5	5.1	V	VSSA=0V
Current consumption (see note 3)						
-run mode	I_{srun}			see 3)	see 3)	see 3)
-RTC mode	I_{sRTC}		0.5	1.25	mA	fclk=4MHz@ϑ_{op}=25° C
-stop mode	I_{sstop}		10	200	µA	fclk =0 @ϑ_{op}=25°C
RAM data retention voltage	VDD-VSS	3.0			V	
Alarm comparator						
-Threshold voltages						
- overvoltage	V_{TAH}	$^4/_5$ VDDA-5%	$^4/_5$VDDA	$^4/_5$ VDDA+5%	V	(external 4:1 divider)
- undervoltage	V_{TAL}	$^2/_5$ VDDA-5%	$^2/_5$VDDA	$^2/_5$ VDDA+5%	V	
- Switching hysteresis	V_{TAHYS}	12.5	25	50	mV	at V_{TAH}, V_{TAL}
- Alarm sense time	t_{AS}			10	µs	
- Input resistance	R_{in}	5			MΩ	
Power down Reset						
-Threshold voltage	V_{TPOR}	3.5	4.0	4.5	V	
- Switching hysteresis	$V_{TPORHYS}$	20	50	80	mV	
- Reset sense time	t_{RS}			10	µs	

Digital Inputs [2]						
CMOS (Type:Q,S,T,Y)						
- High voltage range	V_{IH}	0.65*VDD		VDD	V	
- Low voltage range	V_{IL}	VSS		0.25*VDD	V	
CMOS Schmitt-Trigger (Types: E, F, U)						
- High voltage range	V_{IH}	0.8*VDD		VDD	V	
- Low voltage range	V_{IL}	VSS		0.2*VDD	V	
CMOS Automotive Schmitt-Trigger (Types: A, B, J, K1, M1)						
- High voltage range	V_{IH}	0.8*VDD		VDD	V	
- Low voltage range	V_{IL}	VSS		0.5*VDD	V	
					V	
- hysteresis voltage			0.5		V	
- Input capacitance	C_{IN}			16	pF	
- Input leakage current	I_{IL}	-1		1	µA	ϑ_{op}=25 C
- Pull up resistor	R_{up1}		50		kΩ	Types: E, U
	R_{up2}		10		kΩ	Type: S
Digital outputs						
- Output "H" voltage	V_{OH}	VDD-0.5		VDD	V	I_{load} = 4mA
- Output "L" voltage	V_{OL}	VSS		VSS+0.4	V	I_{load} = - 4mA
ADC inputs [4]						
- Reference voltage input	V_{REFH}	V_{REFL}+3		VDDA	V	
	V_{REFL}	VSSA		V_{REFH}-3	V	
- Input voltage range	V_{imax}	V_{REFL}		V_{REFH}	V	
	V_{imin}				V	
- Input resistance	R_I			3.6	kΩ	
- Input capacitance	C_I			30	pF	
- Impedance of external output driving the ADC input				4.0	kΩ	@ sampling time of 1.6 µs
- Input leakage current	I_{IL}	-1		1	µA	ϑ_{op}=25 C
PPG						
- Output voltage	$V_{outHIGH}$	VDD-0.5		VDD	V	
	V_{outLOW}	VSS		VSS+0.4	V	
- Output current	I_{out}	4			mA	
I^2C Bus Interface						Open Drain Output
- Output voltage	$V_{outHIGH}$			VDD	V	
	V_{outLOW}	VSS		VSS+0.4	V	I_{outLOW}= 3mA
- Output current	I_{out}	3			mA	
Lock-up time PLL1 (4MHz->16…64MHz)			0.1	1	ms	
ESD Protection (Human body model MIL883-B compliant)	V_{surge}	2			kV	$R_{discharge}$=1.5kΩ $C_{discharge}$= 100pF

1) this is only valid if the integrated power-down reset circuit is switched-off, else a reset can be triggered at voltages less or equal than 4.5 V (see spec items for power-down reset).

2) valid for bidirectional tristate I/O PAD cell.

3) I_{SRUN} : A method how to calculate the application specific total current consumption is provided in chapter 7.2.1.

4) The protection diodes at the analog inputs are connected to the digital supply voltage.

7.2.1 Run Mode Current / Power Consumption

The power dissipation during normal operation is determined by the total power dissipation of the internal logic (P_C), the dissipation from analog modules (P_A) and the power dissipation of the I/O buffers (P_{IO}). Therefore, the overall power consumption P_D will be calculated as a sum of these contributions:

$$P_D = P_C + P_A + P_{IO}$$

Please note that the Stepper Motor Controllers (SMC), which cause a considerable contribution to the power dissipation, are not available in the MB91F369g design.

a) Logic Power Consumption

The following formula can be used to calculate the maximum core current consumption when the PLL is used, depending on the frequency settings for the internal clocks:

I_{CC} = 3.45 mA/MHz • CLKB [MHz] + 2.52 mA/MHz • CLKP [MHz] + 0.72 mA/MHz • CLKT [MHz] + 35.5 mA

If clock modulation is used, the following value must be added to this result:

0.24 mA/MHz • CLKB [MHz]

This results in the following values:

Clock frequency [MHz]			Max. Core Current Consumption [mA]	Logic Power Consumption P_C at 5.25 V [W]	Comments
CLKB	CLKP	CLKT			
64	16	16	308	1.70	No clock modulation possible.
48	24	24	290	1.52	
48	16	16	264	1.40	
32	32	32	257	1.35	
32	16	16	205	1.08	
24	24	24	202	1.06	
24	12	12	163	0.86	
16	16	16	146	0.77	
2	2	2	40	0.21	No PLL, no clock modulation.
0.125	0.125	0.125	30	0.16	No PLL, no clock modulation.

b) Analog Power Consumption

In order to calculate the analog power consumption P_A, the current contributions of the active modules have to be multiplied with the maximum analog supply voltage of 5.1 V.

Module	Maximum Current Consumption	Comment
ADC	7 mA	
Power Down Reset	0.5 mA	
Alarm Comparator	0.5 mA	

c) IO Power Consumption

The power dissipation P_{IO} (at 5.25 V) of the I/O buffers is represented by the sum of the dynamic power dissipation P_{AC} and the static power consumption P_{DC} .

The power dissipation (P_{IO}) (at 5.25 V) of the I/O buffers is represented as the sum of the dynamic power dissipation ($P_{AC5V,}$ P_{AC3V}) and the static power consumption (P_{DC}).

$$P_{IO} = P_{AC5V} * 1.1 + P_{AC3V} *1.2 + P_{DC}$$

The following table lists values for the calculation of P_{AC5V} and P_{AC3V}

Buffer Type	Power Consumption P_{IB} / P_{OB} @ 5V to calculate P_{AC5V}	Power Consumption P_{IB} / P_{OB} @ 3.3V to calculate P_{AC3V}	Unit
Normal Input	12.4	12.4	µW/MHz (C_L in pF)
Bidirectional Input			
4 mA Bidirectional Output	194 + 25 C_L	85.5 + 11 C_L	
4 mA Output			
8 mA Bidirectional Output	353 + 25 C_L	154 + 11 C_L	
8 mA Output			

$$P_{AC} = P_{IB} \bullet In \bullet f \bullet \text{operating rate} + P_{OB} \bullet On \bullet f \bullet \text{operating rate}$$

P_{IB}: Power consumption of input buffers and bidirectional inputs.
P_{OB}: Power consumption of output buffers and bidrectional outputs.
In: Total number of input buffers and bidirectional buffer inputs.
On: Total number of output buffers and bidirectional buffer outputs.
f: System frequency.
operating rate: 1.0 if all buffers are switched simultaneously at system frequency.

P_{DC} is caused by off-chip loads which are drawing static currents.

$$P_{DC} = VO \bullet IO \bullet DC_N$$

VO: Output voltage drop - usually 0.4 V

IO: Output current - usually 4 mA
DC_N: Number of output buffers and bidirectional buffers driving off-chip loads.

7.3 Converter Characteristics

- A/D Converter

Parameter	Symbol	Rating			Unit	Remark
		Minimum	Typical	Maximum		
Resolution				10	Bit	
Conversion error				+/- 5.0	LSB	Overall error
Non-linearity				+/-2.5	LSB	
Differential Non-linearity				+/-1.9	LSB	
Zero Reading voltage	V_{0T}	AVRL -3.5	AVRL+0.5	AVRL+4.5	LSB	
Full scale reading voltage	V_{FST}	AVRH-5.5	AVRH-1.5	AVRH+2.5	LSB	
Input current	IA @ VDDA		3.0	7.0	mA	
Reference voltage current	IR		1.6	2.6	mA	

7.4 Clock Settings

Clock domain	Clock name	Max. frequency setting	Remark
Core	CLKB	64 MHz	under normal operating conditions
		32 MHz	for supply voltage between 4.25 and 3.5 V
Resource bus	CLKP	32 MHz	
Ext. Bus	CLKT	32 MHz	
Clock for CAN	CANCLK	32 MHz	

7.5 Clock modulator settings

The clock modulator is a module to reduce EME (Electromagnetic Emission) problems by spreading the energy of the system over a wide range of the frequency spectrum. In order to allow optimization of system performance versus EME reduction, the modulator is programmable over a wide modulation range.

Clock Modulator	**Input Frequency [MHz]**	**Number of operational settings for Clock Modulator**
OFF	64	-
ON	48	2
ON	40	3
ON	32	8
ON	24	11
ON	16	14

Detailed information about Clock Modulator operation and settings is available from Fujitsu on request.

8 Package

A QFP160 package will be used for MB91F369G (FPT-160P-M15).

The thermal resistance of this package is 16 K/W, if it is used on a multi-layer board with separate power and ground planes.

Thermal resistance [K/W]			
ϑ_{ja} (junction to ambient)			ϑ_{jc} (junction to case)
0 m/s	1 m/s	3 m/s	
16	13	11	2.5

The maximum allowed ambient temperature is 85°C, the maximum allowed junction temperature is 125°C. Under these conditions, the allowed maximum power consumption will be

$$(125^{o}C - 85^{o}C) / 16 (K/W) = 2.5 W.$$

The user has to make sure that the maximum ambient temperature is not exceeded.

For further details about the package, see the Fujitsu Semiconductor Package Data Book.

Appendix A I/O Map

Version 1.3, 2001/05/21

Table A lists the addresses for the registers used by the internal peripheral functions of the MB91F369G.

- How to Read the I/O Map

Address	Register				Block
	+0	+1	+2	+3	
000014_H	PDRG [R/W] XXXXXXXX	PDRH [R/W] XXXXXXXX	PDRI [R/W] ----XXXX	—	Port data register

Read/write attribute
Register initial value after a reset (bit initial values)
"1": initial value "1", "0": initial value "0",
"x": initial value "X" (indeterminate),
"—" indicates non-existent bits
Register name (The register in column 1 is at location 4n, the register in column 2 at 4n+1, and so on.)
Location of far left of register (+0). +1, +2, and +3 each increment the location by one. When performing word access, the register in column 1 is placed at the MSB end of the data.

Precautions:

- Do not use RMW instructions on registers containing write-only (W) bits.

RMW instructions(RMW:read-modify-write)

```
AND   Rj, @Ri      OR    Rj, @Ri      EOR   Rj, @Ri
ANDH  Rj, @Ri      ORH   Rj, @Ri      EORH  Rj, @Ri
ANDB  Rj, @Ri      ORB   Rj, @Ri      EORB  Rj, @Ri
BANDL #u4, @Ri     BORL  #u4, @Ri     BEORL #u4, @Ri
BANDH #u4, @Ri     BORH  #u4, @Ri     BEORH #u4, @Ri
```

- The data in reserved areas and areas marked "—" is indeterminate. Do not use those areas !

Address	Register				Block
	+0	+1	+2	+3	
000000_H	_____				Reserved
000004_H	_____	_____	_____	PDR7 [R/W] -111 - - - -	T-unit Port Data Register
000008_H	PDR8 [R/W] - - - - -XX-	PDR9 [R/W] XXXXX-X1	_____	PDRB [R/W] - - - - - XXX	
$00000C_H$	_____				Reserved
000010_H	PDRG [R/W] - - - - - -XX	PDRH [R/W] XXXXXXXX	PDRI [R/W] - - - - X - - -	_____	R-bus Port Data Register]
000014_H	PDRK [R/W] XXXXXXXX	_____	PDRM [R/W] - - - - XXXX	PDRN [R/W] - - XXXXXX	
000018_H	PDRO [R/W] - - - - XXXX	PDRP [R/W] - - - - XXXX	PDRQ [R/W] - - - - - XX	_____	
$00001C_H$ | $00003C_H$	_____				Reserved
000040_H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000 00000000		Ext int/NMI
000044_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	reserved, writing to this address has no effect	reserved	DLYI/I-unit
000048_H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
$00004C_H$	_____		TMCSR0 [R/W] - - - - 0000 - - - 00000		
000050_H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054_H	_____		TMCSR1 [R/W] - - - - 0000 - - - 00000		
000058_H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
$00005C_H$	_____		TMCSR2 [R/W] - - - - 0000 - - - 00000		
000060_H	SSR0 [R/W] 00001 - 00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00 - - 0 - 0 -	UART0
000064_H	ULS0 [R/W] - - - - 0000	_____	_____	_____	

Address	Register				Block
	+0	+1	+2	+3	
000068_H	UTIM0/UTIMR0 [R/W] 00000000 00000000		DRCL0 [W] - - - - - - - -	UTIMC0 [R/W] 0 - - - 0 - 01	U-TIMER 0
$00006C_H$ | 000080_H	_____				Reserved
000084_H	SMCS0 [R/W] 00000010 - - - - 00-0		SES0 [R/W] - - - - - - 00	SDR0 [R/W] 00000000	SIO 0
000088_H	SMCS1 [R/W] 00000010 - - - - 00 - 0		SES1 [R/W] - - - - - - 00	SDR1 [R/W] 00000000	SIO 1
$00008C_H$	CDCR0 [R/W] 0 - - - 1111	Reserved	CDCR1 [R/W] 0 - - - 1111	Reserved	SIO 0/1 Prescaler
000090_H	_____				Reserved
000094_H	IBCR [R/W] 00000000	IBSR [R] 00000000	IADR [R/W] -XXXXXXX	ICCR [R/W] --0XXXXX	I2C (old)
000098_H	_____	IDAR [R/W] XXXXXXXX	_____	IDBL [R/W] -------0	
$00009C_H$	ADMD [R/W,W] - - - X0000	ADCH [R/W] 00000000	_____	ADCS [R/W,W] 0000 - - 00	A/D Converter
$0000A0_H$	ADCD [R/W] 000000XX XXXXXXXX		_____	ADBL [R/W] - - - - - - - 0	
$0000A4_H$ | $0000E8_H$	_____				Reserved
$0000EC_H$	_____	SGDBL [R/W] - - - - - - - 0	SGCR [R/W] 0 - - - - - 00 000 - - 000		Sound Generator
$0000F0_H$	SGAR [R/W] 00000000	SGFR [R/W] XXXXXXXX	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
$0000F4_H$	_____	WTDBL [R/W] - - - - - - - 0	WTCR [R/W] 00000000 000 - 0000		Real Time Clock (WatchTimer)
$0000F8_H$	_____	WTBR [R/W] - - XXXXXX XXXXXXXX XXXXXXXX			
$0000FC_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	_____	
000100_H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3
000104_H	_____		TMCSR3 [R/W] - - - - XX - - - - - XXXXX		

Address	Register				Block
	+0	+1	+2	+3	
000108_H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4
$00010C_H$	_____		TMCSR4 [R/W] - - - - XX - - - - - XXXXX		
000110_H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5
000114_H	_____		TMCSR5 [R/W] - - - - XX - - - - - XXXXX		
000118_H	GCN10 [R/W] 00110010 00010000		PDBL0 [R/W] - - - 00000	GCN20 [R/W] - - - - 0000	PWM Control 0
$00011C_H$	_____				Reserved
000120_H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PWM0
000124_H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 0000000 -	PCNL0 [R/W] 000000 - 0	
000128_H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PWM1
$00012C_H$	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 0000000 -	PCNL1 [R/W] 000000 - 0	
000130_H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PWM2
000134_H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 0000000 -	PCNL2 [R/W] 000000 - 0	
000138_H	PTMR3 [R] 11111111 11111111		PCSR3 [W] XXXXXXXX XXXXXXXX		PWM3
$00013C_H$	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 0000000 -	PCNL3 [R/W] 000000 - 0	
000140_H | 000160_H	_____				Reserved
000164_H	CMCR [R/W] 11111111 00000000		reserved		Clock Module
000168_H | 000178_H	_____				Reserved
$00017C_H$	_____	PDRCR [R/W] - - - - - 000	_____	_____	Power down reset
000180_H	ACCDBL[R/W] - - - - - - - 0	ACSR [R/W] - - - XXX00	_____	_____	Alarm comparator

Address	Register				Block
	+0	+1	+2	+3	
000184_H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH [R/W] - - - - - - 00	ITBAL [R/W] 00000000	I^2C (new)
000188_H	ITMKH [R/W] 00 - - - - 11	ITMKL [R/W] 11111111	ISMK [R/W] 01111111	ISBA [R/W] - 0000000	(*) old and new I^2C share these bits
$00018C_H$	IDARH [-] 00000000	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	IDBL2(*) [R/W] - - - - - - - 0	
000190_H | $0001F8_H$	_____				Reserved
$0001FC_H$	_____	_____	F362MD [R/W] 00000000	_____	Mode Reg
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H | $00023C_H$	_____				
000240_H	DMACR [R/W] 00--0000 -------- -------- --------				
000244_H | $0003EC_H$	_____				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H	DDRG [R/W] - - - - - - 00	DDRH [R/W] 00000000	DDRI [R/W] - - - - 0 - - -	_____	R-bus Port Direction Register
000404_H	DDRK [R/W] 00000000	_____	DDRM [R/W] - - - - 0000	DDRN [R/W] - - 000000	
000408_H	DDRO [R/W] - - - - 0000	DDRP [R/W] - - - - 0000	DDRQ [R/W] - - - - - - 00	_____	
$00040C_H$	_____	_____	_____	_____	
000410_H	PFRG [R/W] - - - - - - 00	PFRH [R/W] 00000000	PFRI [R/W] - - - - 0 - - -	_____	R-bus Port Function Register
000414_H	PFRK [R/W] 00000000	_____	PFRM [R/W] - - - - 0000	PFRN [R/W] - - 000000	
000418_H	PFRO [R/W] - - - - 0000	PFRP [R/W] - - - - 0000	PFRQ [R/W] - - - - - - 00	_____	
$00041C_H$	_____	_____	_____	_____	
000420_H | $00043C_H$	_____				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control unit
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H | $00047C_H$	_____				
000480_H	RSRR [R/W] 10000000	STCR [R/W] 001100 - 1	TBCR [R/W] X0000X00	CTBR [W] XXXXXXXX	Clock Control unit
000484_H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H | $0005FC_H$	_____				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000600_H	_____	_____	_____	_____	T-unit Port Direction Register
000604_H	_____	_____	_____	DDR7 [R/W] - 000 - - - -	
000608_H	DDR8 [R/W] - - - - - 00 -	DDR9 [R/W] 00000 - 00	_____	DDRB [R/W] - - - - - 000	
$00060C_H$	_____				
000610_H	_____	_____	_____	_____	T-unit Port Function Register (*) P81 function is defined by PFR82.
000614_H	_____	_____	_____	PFR7 [R/W] - 000 - - - -	
000618_H	PFR8 [R/W] - - - - - 0- - (*)	PFR9 [R/W] 11110 - 01	_____	PFRB [R/W] - - - - - 000	
$00061C_H$	_____				
000620_H	_____				
000624_H	_____			PFR27 [R/W] - 111- - - -	
000628_H | $00063F_H$	_____				Reserved
000640_H	ASR0 [W] 00000000 00000000		AMR0 [W] 11111000 11111111		T-unit
000644_H	ASR1 [W] 00000000 00000000		AMR1 [W] 00000000 00000000		
000648_H	ASR2 [W] 00000000 00000000		AMR2 [W] 00000000 00000000		
$00064C_H$	ASR3 [W] 00000000 00000000		AMR3 [W] 00000000 00000000		
000650_H	ASR4 [W] 00000000 00000000		AMR4 [W] 00000000 00000000		
000654_H	ASR5 [W] 00000000 00000000		AMR5 [W] 00000000 00000000		
000658_H	ASR6 [W] 00000000 00000000		AMR6 [W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00065C_H$	ASR7 [W] 00000000 00000000		AMR7 [W] 00000000 00000000		
000660_H	AMD0 [R/W] -00XX111	AMD1 [R/W] -XXXXXXX	AMD2 [R/W] --XXXXXX	AMD3 [R/W] --XXXXXX	
000664_H	AMD4 [R/W] --XXXXXX	AMD5 [R/W] --XXXXXX	AMD6 [R/W] -XXXXXXX	AMD7 [R/W] -XXXXXXX	
000668_H	CSE 11000011	_____	_____	_____	
$00066C_H$	_____		_____		
000670_H	CHE 11111111	_____	_____		
000674_H | $0007F8_H$	_____				Reserved
$0007FC_H$	_____	MODR [W] XXXXXXXX	_____	_____	Mode Register
000800_H | $000FFC_H$	_____				Reserved
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
001028_H | $003FFC_H$	_____				Reserved
004000_H | $006FFF_H$	_____				Reserved
007000_H	FMCS [R/W] 1110X - 00	_____	_____	_____	Flash Memory Control Register
007004_H	FMWT [R/W] -0000011	_____	_____	_____	
007008_H | $00FFFC_H$	_____				Reserved
010000_H | $010FFC_H$	_____				Reserved
011000_H | $011FFC_H$					I-RAM 4 kB
012000_H | $01FFFC_H$	_____				Reserved
020000_H | $03BFFC_H$	_____				Reserved
$03C000_H$ | $03FFFC_H$					User RAM 16 kB (D-Bus)
040000_H | $043FFC_H$					Fast RAM 16 kB (F-Bus)
044000_H | 0FEFFC	_____				Reserved
050000_H | $0507FC_H$					Boot ROM 2 kB (F-Bus)
050800_H | $07FFF4_H$	_____				reserved

Address	Register				Block
	+0	+1	+2	+3	
080000_H | $09FFFC_H$	Sector 0 64 KB		Sector 7 64 KB		Flash Memory 512 K on F-Bus
$0A0000_H$ | 0BFFFC	Sector 1 64 KB		Sector 8 64 KB		
$0C0000_H$ | 0DFFFC	Sector 2 64 KB		Sector 9 64 KB		
$0E0000_H$ | 0EFFFC	Sector 3 32 KB		Sector 10 32 KB		
$0F0000_H$ | $0F3FFC_H$	Sector 4 8 KB		Sector 11 8 KB		
$0F4000_H$ | $0F7FFC_H$	Sector 5 8 KB		Sector 12 8 KB		
$0F8000_H$ | $0FFFF4_H$	Sector 6 16 KB		Sector 13 16 KB		
$0FFFF8_H$	FMV [R] $06\ 00\ 00\ 00_H$				Fixed Reset/Mode Vector
$0FFFFC_H$	FRV [R] $00\ 05\ 00\ 00_H$				
Write operations to addresses $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses the values shown above will be read.					

Address	Register				Block
	+0	+1	+2	+3	
100000_H	BVALR0 [R/W] 00000000 00000000		TREQR0 [R/W] 00000000 00000000		CAN 0
100004_H	TCANR0 [W] 00000000 00000000		TCR0 [R/W] 00000000 00000000		
100008_H	RCR0 [R/W] 00000000 00000000		RRTRR0 [R/W] 00000000 00000000		
$10000C_H$	ROVRR0 [R/W] 00000000 00000000		RIER0 [R/W] 00000000 00000000		
100010_H	CSR0 [R/W] 00000000 00000001		_____	LEIR0 [R/W] 000-0000	
100014_H	RTEC0 [R] 00000000 00000000		BTR0 [R/W] -1111111 11111111		
100018_H	IDER0 [R/W] XXXXXXXX XXXXXXXX		TRTRR0 [R/W] 00000000 00000000		
$10001C_H$	RFWTR0 [R/W] XXXXXXXX XXXXXXXX		TIER0 [R/W] 00000000 00000000		
100020_H	AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100024_H	AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100028_H	AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10002C_H$ | 100048_H	GENERAL PURPOSE RAM [R/W]				
$10004C_H$	IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100050_H	IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100054_H	IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100058_H	IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10005C_H$	IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100060_H	IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100064_H	IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
100068_H	IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 0
$10006C_H$	IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100070_H	IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100074_H	IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100078_H	IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10007C_H$	IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100080_H	IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100084_H	IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100088_H	IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10008C_H$	DLCR00 [R/W] -------- ----XXXX		DLCR10 [R/W] -------- ----XXXX		
100090_H	DLCR20 [R/W] -------- ----XXXX		DLCR30 [R/W] -------- ----XXXX		
100094_H	DLCR40 [R/W] -------- ----XXXX		DLCR50 [R/W] -------- ----XXXX		
100098_H	DLCR60 [R/W] -------- ----XXXX		DLCR70 [R/W] -------- ----XXXX		
$10009C_H$	DLCR80 [R/W] -------- ----XXXX		DLCR90 [R/W] -------- ----XXXX		
$1000A0_H$	DLCR100 [R/W] -------- ----XXXX		DLCR110 [R/W] -------- ----XXXX		
$1000A4_H$	DLCR120 [R/W] -------- ----XXXX		DLCR130 [R/W] -------- ----XXXX		
$1000A8_H$	DLCR140 [R/W] -------- ----XXXX		DLCR150 [R/W] -------- ----XXXX		
$1000AC_H$	DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000B4_H$	DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
$1000BC_H$	DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 0
$1000C4_H$	DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000CC_H$	DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000D4_H$	DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000DC_H$	DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000E4_H$	DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000EC_H$	DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000F4_H$	DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000FC_H$	DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100104_H	DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10010C_H$	DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100114_H	DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10011C_H$	DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100124_H	DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10012C_H$	CREG0 [R/W] 00000000 00000110		_____		

Address	Register				Block
	+0	+1	+2	+3	
100200_H	BVALR1 [R/W] 00000000 00000000		TREQR1 [R/W] 00000000 00000000		CAN 1
100204_H	TCANR1 [W] 00000000 00000000		TCR1 [R/W] 00000000 00000000		
100208_H	RCR1 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
$10020C_H$	ROVRR1 [R/W] 00000000 00000000		RIER1 [R/W] 00000000 00000000		
100210_H	CSR1 [R/W] 00000000 00000001		_____	LEIR1 [R/W] 000-0000	
100214_H	RTEC1 [R] 00000000 00000000		BTR1 [R/W] -1111111 11111111		
100218_H	IDER1 [R/W] XXXXXXXX XXXXXXXX		TRTRR1 [R/W] 00000000 00000000		
$10021C_H$	RFWTR1 [R/W] XXXXXXXX XXXXXXXX		TIER1 [R/W] 00000000 00000000		
100220_H	AMSR1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100224_H	AMR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100228_H	AMR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10022C_H$ | 100248_H	GENERAL PURPOSE RAM [R/W]				
$10024C_H$	IDR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100250_H	IDR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100254_H	IDR21[R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100258_H	IDR31 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX-				
$10025C_H$	IDR41 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100260_H	IDR51 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100264_H	IDR61 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
100268_H	IDR71 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 1
$10026C_H$	IDR81 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100270_H	IDR91 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100274_H	IDR101 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100278_H	IDR111 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10027C_H$	IDR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX---				
100280_H	IDR131 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100284_H	IDR141 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100288_H	IDR151 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10028C_H$	DLCR01 [R/W] -------- ----XXXX		DLCR11 [R/W] -------- ----XXXX		
100290_H	DLCR21 [R/W] -------- ----XXXX		DLCR31 [R/W] -------- ----XXXX		
100294_H	DLCR41 [R/W] -------- ----XXXX		DLCR51 [R/W] -------- ----XXXX		
100298_H	DLCR61 [R/W] -------- ----XXXX		DLCR71 [R/W] -------- ----XXXX		
$10029C_H$	DLCR81[R/W] -------- ----XXXX		DLCR91 [R/W] -------- ----XXXX		
$1002A0_H$	DLCR101 [R/W] -------- ----XXXX		DLCR111 [R/W] -------- ----XXXX		
$1002A4_H$	DLCR121 [R/W] -------- ----XXXX		DLCR131 [R/W] -------- ----XXXX		
$1002A8_H$	DLCR141 [R/W] -------- ----XXXX		DLCR151 [R/W] -------- ----XXXX		
$1002AC_H$	DTR01 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1002B4_H$	DTR11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
$1002BC_H$	DTR21 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 1
$1002C4_H$	DTR31 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1002CC_H$	DTR41 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1002D4_H$	DTR51 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1002DC_H$	DTR61 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1002E4_H$	DTR71 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1002EC_H$	DTR81 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1002F4_H$	DTR91 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1002FC_H$	DTR101 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100304_H	DTR111 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10030C_H$	DTR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100314_H	DTR131 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10031C_H$	DTR141 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
100324_H	DTR151 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10032C_H$	CREG1 [R/W] 00000000 00000110		_____		

Appendix B Interrupt Vectors

This appendix lists the interrupt vector table.

The interrupt vector table lists the interrupt vectors and interrupt control registers assigned to each MB91360 interrupt.

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Reset [*6]	0	00	-	-	0x3FC	0x000FFFFC	
Mode vector [*6]	1	01	-	-	0x3F8	0x000FFFF8	
System reserved	2	02	-	-	0x3F4	0x000FFFF4	
System reserved	3	03	-	-	0x3F0	0x000FFFF0	
System reserved	4	04	-	-	0x3EC	0x000FFFEC	
System reserved	5	05	-	-	0x3E8	0x000FFFE8	
System reserved	6	06	-	-	0x3E4	0x000FFFE4	
Co-processor fault trap [*4]	7	07	-	-	0x3E0	0x000FFFE0	
Co-processor error trap [*4]	8	08	-	-	0x3DC	0x000FFFDC	
INTE instruction [*4]	9	09	-	-	0x3D8	0x000FFFD8	
Instruction break exception [*4]	10	0A	-	-	0x3D4	0x000FFFD4	
Operand break trap [*4]	11	0B	-	-	0x3D0	0x000FFFD0	
Step trace trap [*4]	12	0C	-	-	0x3CC	0x000FFFCC	
NMI interrupt(tool)[*4]	13	0D	-	-	0x3C8	0x000FFFC8	
Undefined instruction exception	14	0E	-	-	0x3C4	0x000FFFC4	
NMI request	15	0F	F_H fixed		0x3C0	0x000FFFC0	
External Interrupt 0	16	10	ICR00	0x440	0x3BC	0x000FFFBC	4
External Interrupt 1	17	11	ICR01	0x441	0x3B8	0x000FFFB8	5
External Interrupt 2	18	12	ICR02	0x442	0x3B4	0x000FFFB4	8
External Interrupt 3	19	13	ICR03	0x443	0x3B0	0x000FFFB0	9

External Interrupt 4	20	14	ICR04	0x444	0x3AC	0x000FFFAC	
External Interrupt 5	21	15	ICR05	0x445	0x3A8	0x000FFFA8	
External Interrupt 6	22	16	ICR06	0x446	0x3A4	0x000FFFA4	
External Interrupt 7	23	17	ICR07	0x447	0x3A0	0x000FFFA0	
Reload Timer 0	24	18	ICR08	0x448	0x39C	0x000FFF9C	6
Reload Timer 1	25	19	ICR09	0x449	0x398	0x000FFF98	7
Reload Timer 2	26	1A	ICR10	0x44A	0x394	0x000FFF94	
CAN 0 RX	27	1B	ICR11	0x44B	0x390	0x000FFF90	
CAN 0 TX/NS	28	1C	ICR12	0x44C	0x38C	0x000FFF8C	
CAN 1 RX	29	1D	ICR13	0x44D	0x388	0x000FFF88	
CAN 1 TX/NS	30	1E	ICR14	0x44E	0x384	0x000FFF84	
CAN 2 RX[5]	31	1F	ICR15	0x44F	0x380	0x000FFF80	
CAN 2 TX/NS[5]	32	20	ICR16	0x450	0x37C	0x000FFF7C	
CAN 3 RX [5]	33	21	ICR17	0x451	0x378	0x000FFF78	
CAN 3 TX/NS [5]	34	22	ICR18	0x452	0x374	0x000FFF74	
PPG 0/1	35	23	ICR19	0x453	0x370	0x000FFF70	
PPG 2/3	36	24	ICR20	0x454	0x36C	0x000FFF6C	
PPG 4/5[5]	37	25	ICR21	0x455	0x368	0x000FFF68	
PPG 6/7[5]	38	26	ICR22	0x456	0x364	0x000FFF64	
Reload Timer 3	39	27	ICR23	0x457	0x360	0x000FFF60	
Reload Timer 4	40	28	ICR24	0x458	0x35C	0x000FFF5C	
Reload Timer 5	41	29	ICR25	0x459	0x358	0x000FFF58	
ICU 0/1[5]	42	2A	ICR26	0x45A	0x354	0x000FFF54	
OCU 0/1[5]	43	2B	ICR27	0x45B	0x350	0x000FFF50	
ICU 2/3[5]	44	2C	ICR28	0x45C	0x34C	0x000FFF4C	
OCU 2/3[5]	45	2D	ICR29	0x45D	0x348	0x000FFF48	
ADC	46	2E	ICR30	0x45E	0x344	0x000FFF44	14
Timebase Overflow	47	2F	ICR31	0x45F	0x340	0x000FFF40	
Free Running Counter 0	48	30	ICR32	0x460	0x33C	0x000FFF3C	
Free Running Counter 1	49	31	ICR33	0x461	0x338	0x000FFF38	
SIO 0	50	32	ICR34	0x462	0x334	0x000FFF34	12

SIO 1	51	33	ICR35	0x463	0x330	0x000FFF30	15
Sound Generator	52	34	ICR36	0x464	0x32C	0x000FFF2C	
UART 0 RX	53	35	ICR37	0x465	0x328	0x000FFF28	0
UART 0 TX	54	36	ICR38	0x466	0x324	0x000FFF24	1
UART 1 RX[5]	55	37	ICR39	0x467	0x320	0x000FFF20	2
UART 1 TX[5]	56	38	ICR40	0x468	0x31C	0x000FFF1C	3
UART 2 RX[5]	57	39	ICR41	0x469	0x318	0x000FFF18	10
UART 2 TX[5]	58	3A	ICR42	0x46A	0x314	0x000FFF14	11
I2C	59	3B	ICR43	0x46B	0x310	0x000FFF10	13
Alarm Comparator	60	3C	ICR44	0x46C	0x30C	0x000FFF0C	
RTC (Watchtimer)	61	3D	ICR45	0x46D	0x308	0x000FFF08	
DMA	62	3E	ICR46	0x46E	0x304	0x000FFF04	
Delayed interrupt activation bit	63	3F	ICR47	0x46F	0x300	0x000FFF00	
System reserved [*3]	64	40	-	-	0x2FC	0x000FFEFC	
System reserved [*3]	65	41	-	-	0x2F8	0x000FFEF8	
Security vector	66	42			0x2F4	0x000FFEF4	
System reserved	67	43	(ICR51)	0x473	0x2F0	0x000FFEF0	
System reserved	68	44	(ICR52)	0x474	0x2EC	0x000FFEEC	
System reserved	69	45	(ICR53)	0x475	0x2E8	0x000FFEE8	
System reserved	70	46	(ICR54)	0x476	0x2E4	0x000FFEE4	
System reserved	71	47	(ICR55)	0x477	0x2E0	0x000FFEE0	
System reserved	72	48	(ICR56)	0x478	0x2DC	0x000FFEDC	
System reserved	73	49	(ICR57)	0x479	0x2D8	0x000FFED8	
System reserved	74	4A	(ICR58)	0x47A	0x2D4	0x000FFED4	
System reserved	75	4B	(ICR59)	0x47B	0x2D0	0x000FFED0	
System reserved	76	4C	(ICR60)	0x47C	0x2CC	0x000FFECC	
System reserved	77	4D	(ICR61)	0x47D	0x2C8	0x000FFEC8	
System reserved	78	4E	(ICR62)	0x47E	0x2C4	0x000FFEC4	
System reserved	79	4F	(ICR63)	0x47F	0x2C0	0x000FFEC0	
Used by the INT instruction.	80 to 255	50 to FF	-	-	0x2BC to 0x000	0x000FFEBC to 0x000FFC00	

*1 The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset.After execution of the internal boot ROM TBR is set to 0_x00FFC00.

*3 Used by REALOS

*4 System reserved

*5 Only available on MB91FV360G

*6 Mode and reset vector cannot be changed, for their contents see IO map

Remarks:

The 1-Kbyte area from the address specified in TBR is the EIT vector area.
Each vector consists of four bytes. The following formula shows the relationship between the vector number and vector address.

$$vctadr = TBR + vctofs$$

$$= TBR + (3FC_H - 4 \times vct)$$

vctadr: Vector address
vctofs: Vector offset
vct : Vector number