FR-DSU3 PGA401P Evaluation Board for the DSU-FR20/30 Emulator Product Specifications

* Some of these specifications are undetermined because of product developments. Specifications may change in the future.
* This Specifications Manual also serves as design specifications.

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1. Application

This manual applies to the product specifications and design specifications for the DSU-FR20/30 Emulator MB2197-01 (called Emulator below) FR-DSU3 PGA401P Evaluation Board (called evaluation board below).
The objective MCU of this product is MB91V360.

2. Composition of the Product

The following shows the composition of the product.

FR-DSU3 PGA401P Evaluation Board (Package Number: MB2197-1XX)

Evaluation Board
Header I/F Cable (Standard: 5 cm) × 2 Pcs.
Header I/F Cable (Long: 20 cm) × 2 Pcs.
Hardware Manual

Note: The Header I/F Cable (Long) is not normally used.

● Parts Sold Separately

• QFP208P Header for the MB2197-110	Package Number: MB2197-1XX
• Evaluation Chip	Package Number: MB91V360
• QFP208PIC Socket	Package Number: NQPACK208SD *
• QFP208PIC Socket Cover	Package Number: HQPACK208SD *
• Emulator for the DSU-FR20/30	Package Number: MB2197-01

In this manual, we call the "MB2197-1XX QFP208P Header" a "Header Board." This product functions as an emulation adapter for the evaluation chip by combining with a Header Board that conforms to the objective MCU.
Refer to the ***QFP208P Header for MB2197-1XX Product Specifications Manual*** for details concerning the Header Board. The QFP208 Header for MB2197-1XX conforms to MB91F361 (QFP-208).

* Attached to the QFP208P Header for MB2197-1XX.

3. Composition of the System

The following shows the composition of the Evaluation Board system.

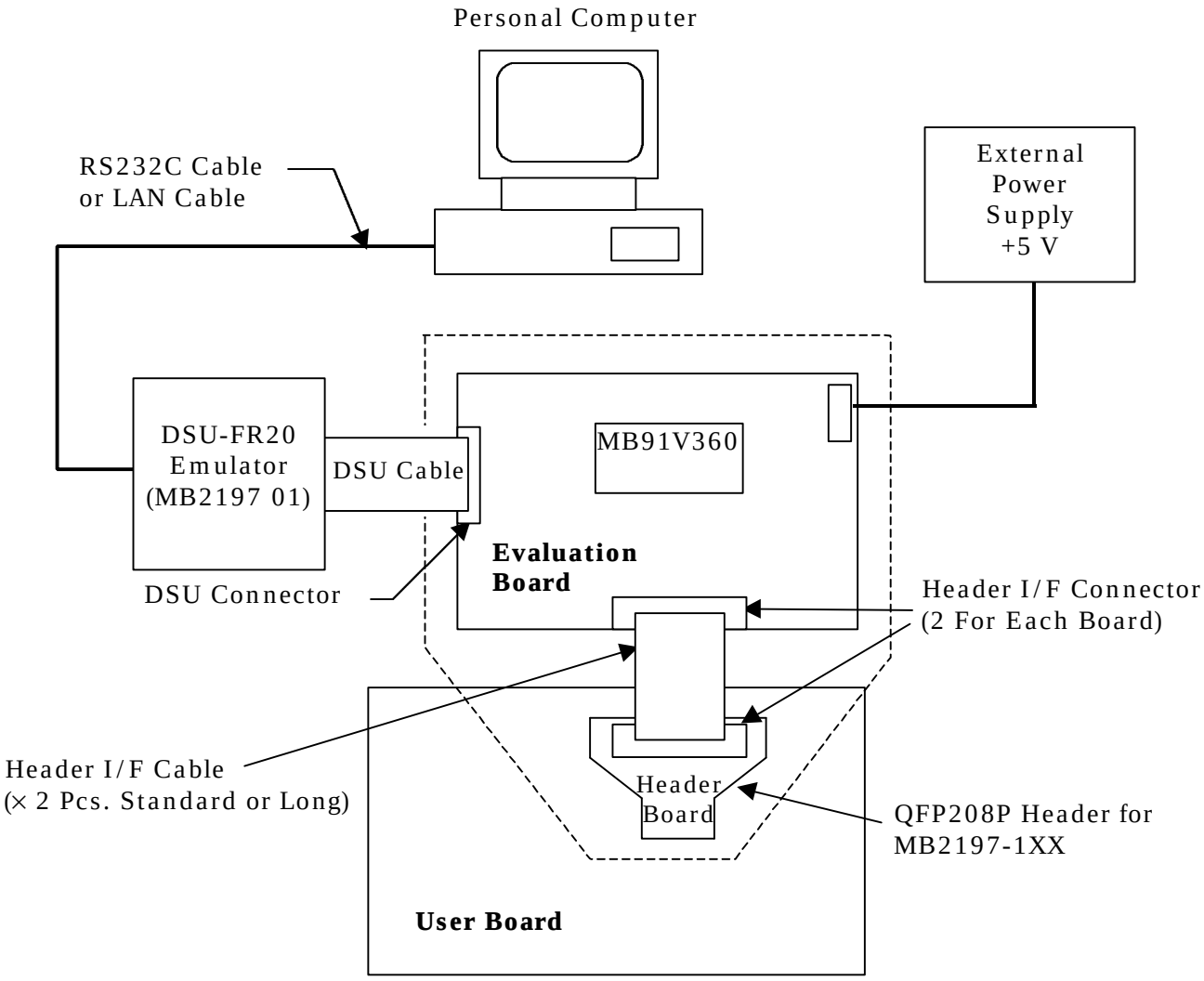


Figure 1 Composition of the System

Notes:
1. Refer to the "***DSU-FR20/30 Emulator MB2197-01 Hardware Manual***" for details concerning the DSU-FR20/30 Emulator.
2. Refer to the "***QFP208P Header for MB2197-1XX Product Specifications Manual***" for details concerning the Header Board.
3. The Header Board is connected to the specified MCU socket on the user board. Refer to the "***Header Board Product Specification Manual***" for details concerning the specific MCU socket.

4. Machine External Appearance

4.1 Machine External Appearance

Figure 2 shows the external appearance of the Evaluation Board. ***Figure 3*** shows the Header I/F Cable connections.

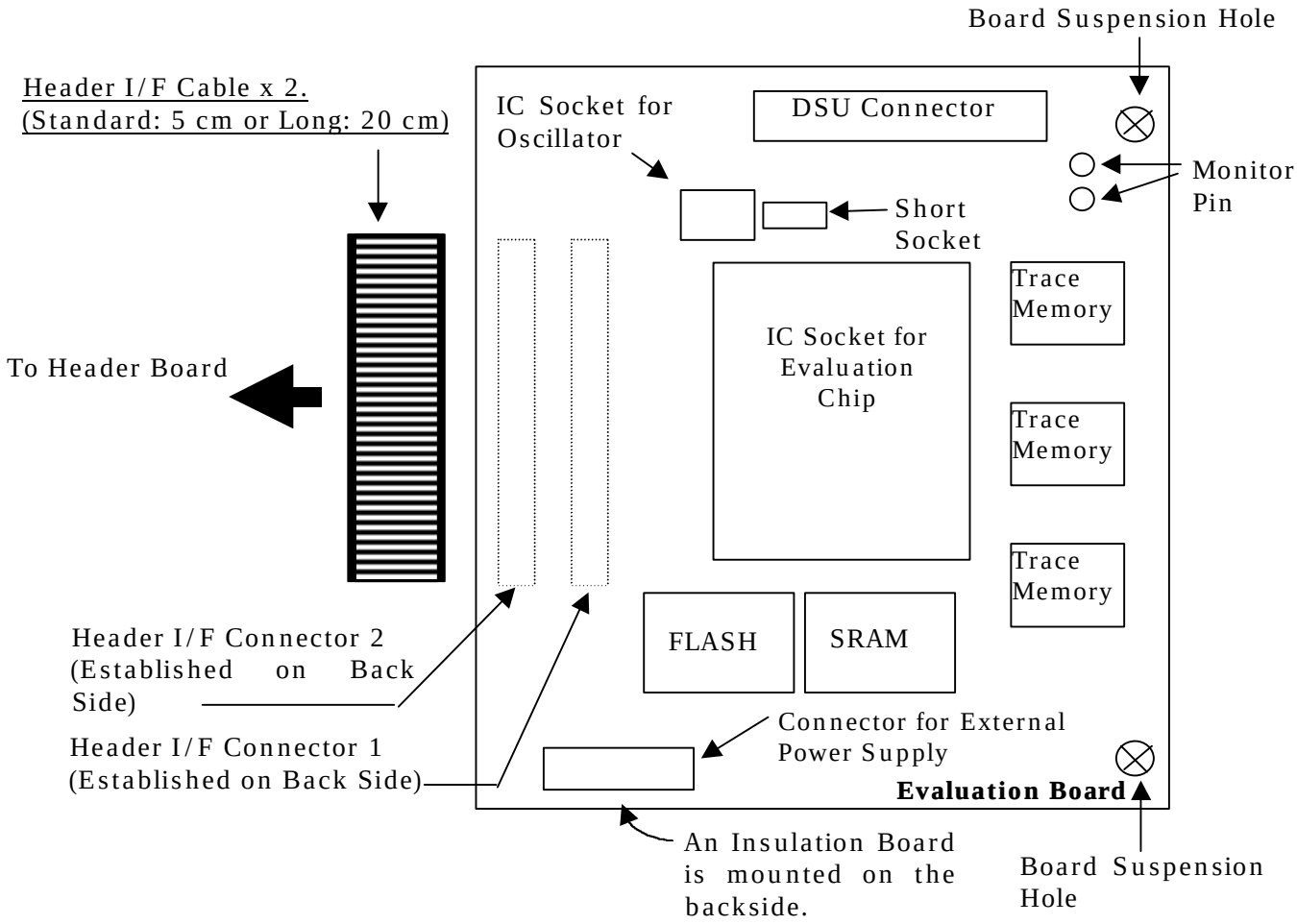


Figure 2 External Appearance of the Evaluation Board

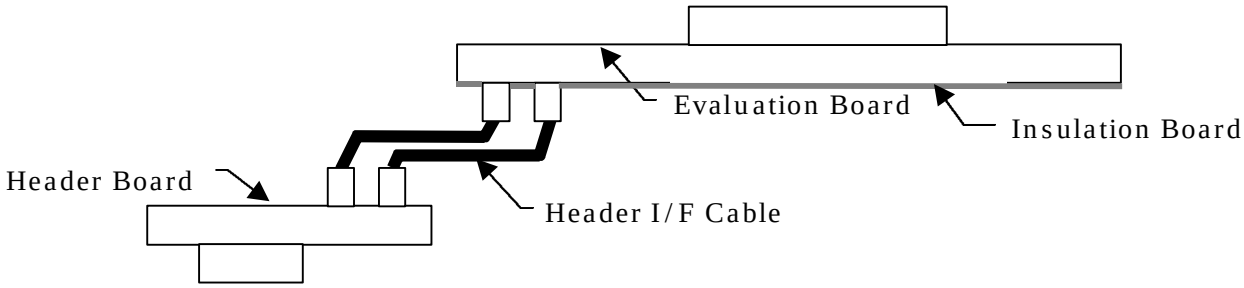


Figure 3 Header I/F Cable Connections

4.2 Usage of the Evaluation Board

Figure 4 and ***Figure 5*** show examples of the usage of the Evaluation Board.

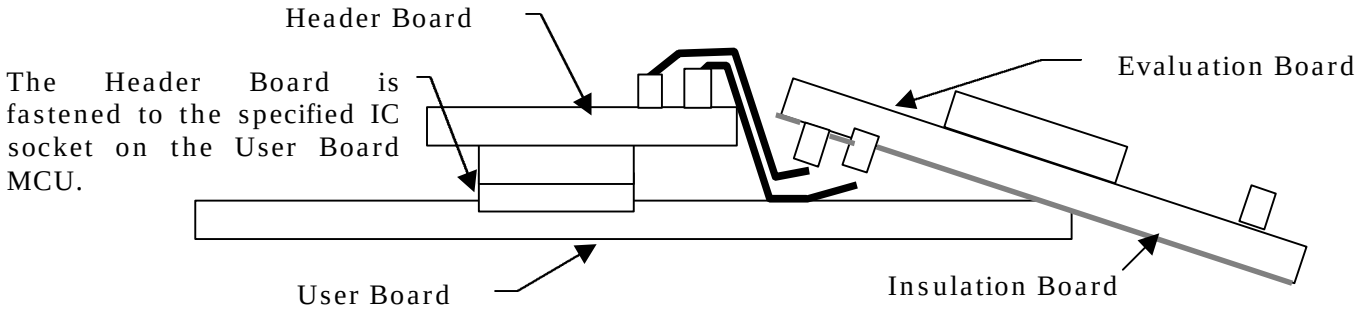


Figure 4 Example 1 of Evaluation Board Usage

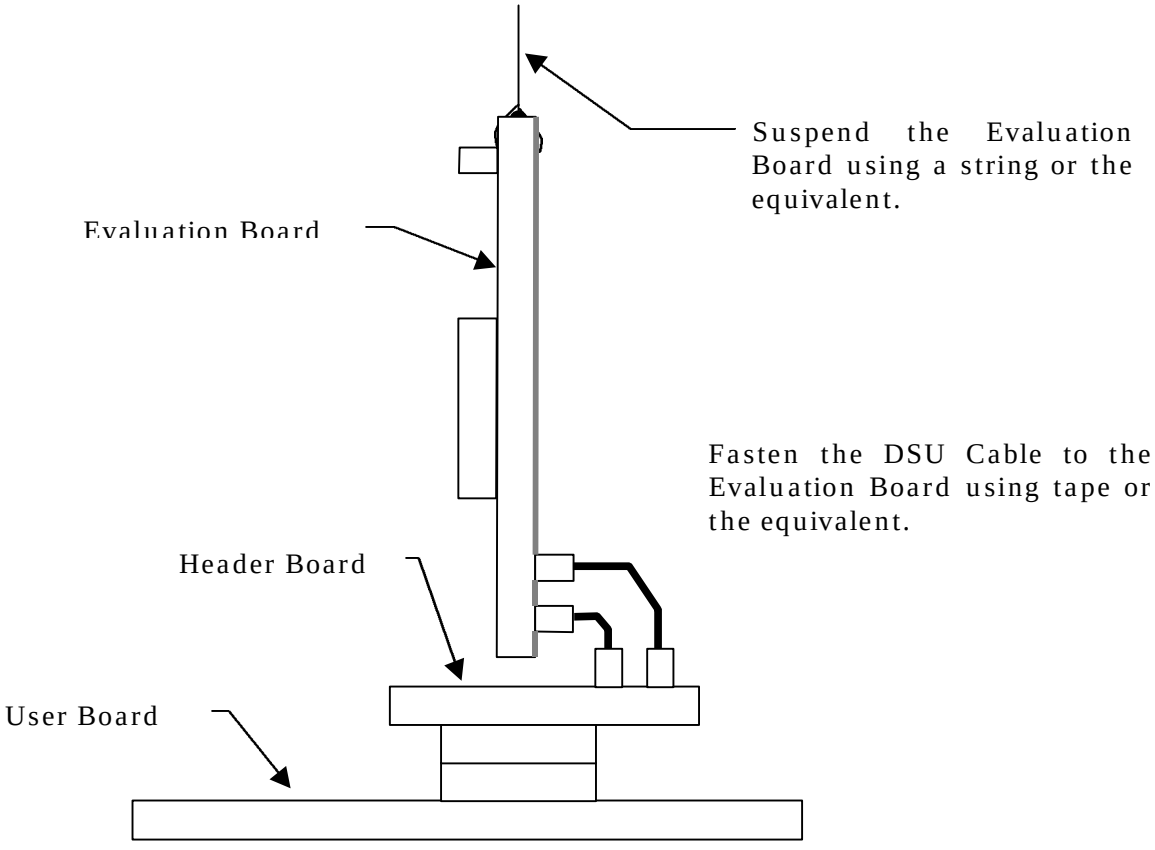


Figure 5 Example 2 of Evaluation Board Usage

5. General Specifications

Table 1 shows the general specifications of the Evaluation Board.

Item		Content	Remarks
Product Name		PGA401P Evaluation Board for FR-DSU3	
Power Supply 1 VCC (Evaluation Chip Power Supply)		5 V (Depends on Evaluation Chip Rating)	*1
Power Supply 2 VCC (Evaluation Board Power Supply)		5 V ± 5% and VCC2 ≥ VCC1 Current Value Not Decided.	*2
Operating Temperature and Storing Temperature		0º to 35ºC (When Operating), -20º to 70ºC (When Stored)	Operating Humidity and Storing Humidity
Operating Temperature and Storing Temperature		30% to 80% (When Operating), 30% to 90% (When Stored)	Operating Humidity and Storing Humidity
External Dimension	Evaluation Board	Evaluation Board	
	Header I/F Cable (Standard)	Cable Length 5 cm	
	Header I/F Cable (Long)	Cable Length 20 cm	
Weight	Evaluation Board	Evaluation Board	

Table 1 General Specifications

*1. This is supplied from the User Board via the Header Board. This is used as the Evaluation Chip VDD Terminal and the Buffer IC Power Supply. We will design so that the product will operate under 3.3 V. That will allow for tentative usage of the MB91V300 which runs under 3.3 V operating specifications. However, we do not guarantee the product will run under 3.3 V at the product level.

*2. This supplies a stable power supply from an external source. This power supply creates the 3.3 V of power (VCC3) for the circuits in the Evaluation Board.

6. Function Specifications

6.1 Function Specifications

Table 2 shows the Evaluation Board function specifications.

Item	Content	Remarks
DSU Connector Header I/F Connector	This is used in conjunction with the QFP208 Header for MB2197-1XX and functions as the MB91V360 adapter.	
Trace Memory	3 SSRAM (64 K words × 32 bit) are mounted onto the board as the Trace Memory for FR-DSU3.	
User Subrogate Memory	FLASH x 2 (256 K word × 32 bit) SRAM x 2 (256 K word × 32 bit) are mounted.	
CLK (2 Systems) Signal Switcher	This uses a Short Plug to switch the CLK (2 System) Signal between the signals from the User Board and the adapter. This uses an oscillator as the power supply of the CLK signal on the User Board to supply the CLK signal from the User Board. You need to connect an oscillator to the oscillator IC socket located on the Evaluation Board to supply the CLK signal from the Evaluation Board.	
CS Signal Switcher	This uses a Short Plug to switch the output destination of the Evaluation Chip CSOX to CS7X signal to the User Board FLASH and SRAM.	
C Pin Control	This uses a Short Plug to add a capacitor to the VCC3/C on the Evaluation Board.	
Low Path Filter	The Low Path Filter is mounted onto the Evaluation Board. This uses a Short Plug to switch to the User Board. An IC Socket is mounted.	
Tracer Power Supply Switcher	The Short Plug switches the Tracer power supply to VCC1 when the VCC1 power supply is 3 V.	

Table 2 Evaluation Board Function Specifications

6.2 Composition of the Main Components

Table 3 shows the composition of the main components.

Item		Content	Remarks
Evaluation Board	Evaluation Chip	Package Number: MB91V360 PGA401 Pin (Fujitsu) × 1	*
	DSU Connector	30 Pin FPC Connector (Right Angle) × 1 Package Number: FH10A-30S-1SH (Hirose Electric)	
	IC Socket	PGA401 Pin IC Socket × 1 Package Number: 2401-1335-00-3302 (Sumitomo 3M)	
	Header I/F Cable Connector	100 Pin SMT Type Connector (Straight) × 2 Package Number: FX2-100P-1.27SVL (Hirose Electric)	
	FLASH	Package Number: MBM29LV400T-10PFTN (Fujitsu) × 2	
	SRAM	Package Number: TC55V16256FT-12 (Toshiba) × 2	
	Buffer IC	Package Number: HD74LVC244AFP (Hitachi) × 3 TC74LVXC3245FS (Toshiba) × 4	
	Trace Memory	Package Number: MT58LC64K32D9LG-11 (Micron)	
	Short Plug	3 Pin Short Plug (3 x 4 Rows) × 6 Package Number: FFC-12NSM1 (Honda Tsushin)	
	IC Socket for CLK	300 MIL 8 Pin IC Socket x 3 Package Number: FCN-064M008-H/3A (Fujitsu)	
	Power Supply Connector	Package Number: ML-70B2P (Sato Parts)	
Header I/F Cable	Cable Header	Header for 100 Pin Socket Type Bracket Cable × 2 Package Number: FX2BA-100S - 1.27 R (Hirose Electric)	

Table 3 Composition of the Main Component

* The Evaluation Chip is sold separately. Also, refer to the Evaluation Chip Data Sheet for details concerning the Evaluation Chip specifications.

6.3 Evaluation Pin Assignment

Refer to the ***MB91V360 Data Sheet*** for details on the Evaluation Pin assignment.

6.4 DSU Connector Pin Assignment

Refer to the ***DSU-FR20/30 Emulation Hardware Manual*** for details on the DSU Connector Pin assignment.

6.5 Header I/F Connector Pin Assignment

Tables 4 and ***5*** show the pin assignments of the Header I/F Connectors 1 and 2. Also, the numbers of the pins in the following tables match the pin numbers in the Connector Data Sheet.

Connector	MB91V360	MB91F361	Pin name	Connector	MB91V360	MB91F361	Pin name
A1			VSS	B1	132	77	ALARM
A2	189	76	DA1	B2	246	75	DA0
A3			AVSS	B3	133	73	AN7
A4	81	72	AN6	B4	247	71	AN5
A5	190	70	AN4	B5	34	69	AN3
A6	134	68	AN2	B6	82	67	AN1
A7	248	66	AN0	B7	300	65	AVRH
A8			AVCC	B8	84	63	DEOP0
A9	135	62	DACK0	B9	193	61	DREQ0
A10	249	60	AN15	B10	85	59	AN14
A11	36	58	AN13	B11	302	57	AN12
A12	303	56	AN11	B12	136	55	AN10
A13	86	54	AN9	B13	37	53	AN8
A14	138	50	CS3X	B14	351	49	CS2X
A15	250	48	CS1X	B15	137	47	CS0X
A16	195	46	AH/BOOT	B16	194	45	CLK
A17	38	44	ALE	B17	87	43	AS
A18	251	42	WR3X	B18	252	41	WR2X
A19	39	40	WR1X	B19	304	39	WR0X
A20	40	38	RDX	B20	88	37	BRQ
A21	139	36	BGRNTX	B21	305	35	RDY
A22	89	34	CS6X	B22	196	33	CS5X
A23	140	32	CS4X	B23	43	31	A20
A24	254	30	A19	B24	142	29	A18
A25	91	28	A17	B25	307	27	A16
A26	199	24	A15	B26	143	23	A14
A27	255	22	A13	B27	44	21	A12
A28	92	20	A11	B28	308	19	A10
A29	356	18	A9	B29	200	17	A8
A30	256	16	A7	B30	309	15	A6
A31	144	14	A5	B31	257	13	A4
A32	357	12	A3	B32	201	11	A2
A33	310	10	A1	B33	202	9	A0
A34	258	8	D31	B34	146	7	D30
A35	203	6	D29	B35	259	5	D28
A36	93	4	D27	B36	147	3	D26
A37	204	2	D25	B37	312	1	D24
A38	260	208	D23	B38	94	207	D22
A39	45	206	D21	B39	205	205	D20
A40	148	204	D19	B40	1	203	D18
A41	95	202	D17	B41	46	201	D16
A42	206	200	D15	B42			VSS
A43			VDD	B43	261	197	D14
A44	47	196	D13	B44	313	195	D12
A45	2	194	D11	B45	149	193	D10
A46	150	192	D9	B46	262	191	D8
A47	48	190	D7	B47	96	189	D6
A48	151	188	D5	B48	207	187	D4
A49	49	186	D3	B49	3	185	D2
A50	263	184	D1	B50	264	183	D0

Table 4 Header I/F Connector 1 Pin Assignment

Connector	MB91V360	MB91F361	Pin name	Connector	MB91V360	MB91F361	Pin name
A1	58	130	SOT4	B1	109	129	SCL
A2	165	128	SDA	B2	221	127	SGA
A3	61	126	SGO	B3	59	125	VCI
A4	325	124	CPO	B4	164	121	X0A
A5	163	122	X1A	B5	29	119	X0
A6	291	120	X1	B6	126	117	SELCLK
A7			VDDX	B7	30	115	INITX
A8	292	116	MONCLK	B8	239	113	MD2
A9	182	114	HSTX	B9	293	111	MD0
A10	31	112	MD1	B10	183	109	OUT3
A11			VSS	B11	128	107	OUT1
A12	78	108	OUT2	B12	32	105	IN3
A13	184	106	OUT0	B13	129	103	IN1
A14	240	104	IN2	B14	294	101	INT7
A15	79	102	IN0	B15	130	99	INT5
A16	185	100	INT6	B16	33	97	INT3
A17	241	98	INT4	B17	295	95	INT1
A18	80	96	INT2	B18			VSS
A19	344	94	INT0	B19	186	91	LED7
A20			VDD	B20	296	89	LED5
A21	242	90	LED6	B21	243	87	LED3
A22	131	88	LED4	B22	187	85	LED1
A23	345	86	LED2	B23	297	83	LTESTX
A24	346	84	LED0	B24	245	81	TESTX
A25	188	82	CPUTESTX	B25			VDD
A26	298	80	ATGX	B26			HVSS
A27			VDD	B27	315	179	PWM2P3
A28	99	180	PWM2M3	B28	153	177	PWM1P3
A29	98	178	PWM1M3	B29	152	175	PWM2M2
A30			HVDD	B30	209	173	PWM1M2
A31	51	174	PWM2P2	B31	52	169	PWM2P1
A32	210	172	PWM1P2	B32	53	167	PWM1P1
A33	7	170	PWM2M1	B33	154	165	PWM2M0
A34	8	168	PWM1M1	B34	211	163	PWM1M0
A35	101	164	PWM2P0	B35			HVSS
A36	9	162	PWM1P0	B36	102	159	VCC3/C
A37	10	160	VDD int.	B37	156	157	SOT2
A38			VSS	B38	103	155	SOT1
A39	212	156	SIN2	B39	157	153	SOT0
A40	55	154	SIN1	B40	269	151	RX2
A41	104	152	SIN0	B41	270	149	RX1
A42	320	150	TX2	B42	215	147	RX0
A43	105	148	TX1	B43			VSS
A44	321	146	TX0	B44	159	143	OCPA7
A45	322	142	OCPA6	B45	160	141	OCPA5
A46	217	140	OCPA4	B46	272	139	OCPA3
A47	106	138	OCPA2	B47	161	137	OCPA1
A48	218	136	OCPA0	B48	107	135	SCK3
A49	57	134	SOT3	B49	219	133	SIN3
A50	12	132	SCK4	B50	108	131	SIN4

Table 5 Header I/F Connector 2 Pin Assignment

6.6 SSRAM Specifications

Table 6 shows the specifications of the SSRAM.

Item	Content	Remarks
Package Number	MT58LC64K32D9LG-11	
Manufacturer	Micron Corporation	
Capacity	64 K Words	
Bus Width	32 bits	
Power Supply Voltage	3.3 V (+10/ -5%)	
Access Time	7 ns	

Table 6 SSRAM Specifications

6.7 FLASH Specifications

Table 7 shows the FLASH specifications.

Item	Content	Content
Package Number	MBM29LV400T-10PFTN	
Manufacturer	Fujitsu	
Capacity	64 K Words	
Bus Width	16 bits	
Power Supply Voltage	3.3 V (+10/ -5%)	
Access Time	100 ns	

Table 7 FLASH Specifications

6.8 SRAM Specifications

Table 8 shows the SRAM specifications.

Item	Content	Content
Package Number	TC55V16256FT-12	
Manufacturer	Toshiba	
Capacity	256 K Words	
Bus Width	16 bits	
Power Supply Voltage	3.3 V (+10/ -5%)	
Access Time	12 ns	

Table 8 SRAM Specifications

7. Detailed Specifications

The values of the resistors, etc. will be determined after function evaluations because some chip specifications have not yet been determined.

7.1 Block Drawing

Figure 7 shows the Block Drawing of the Evaluation Board.

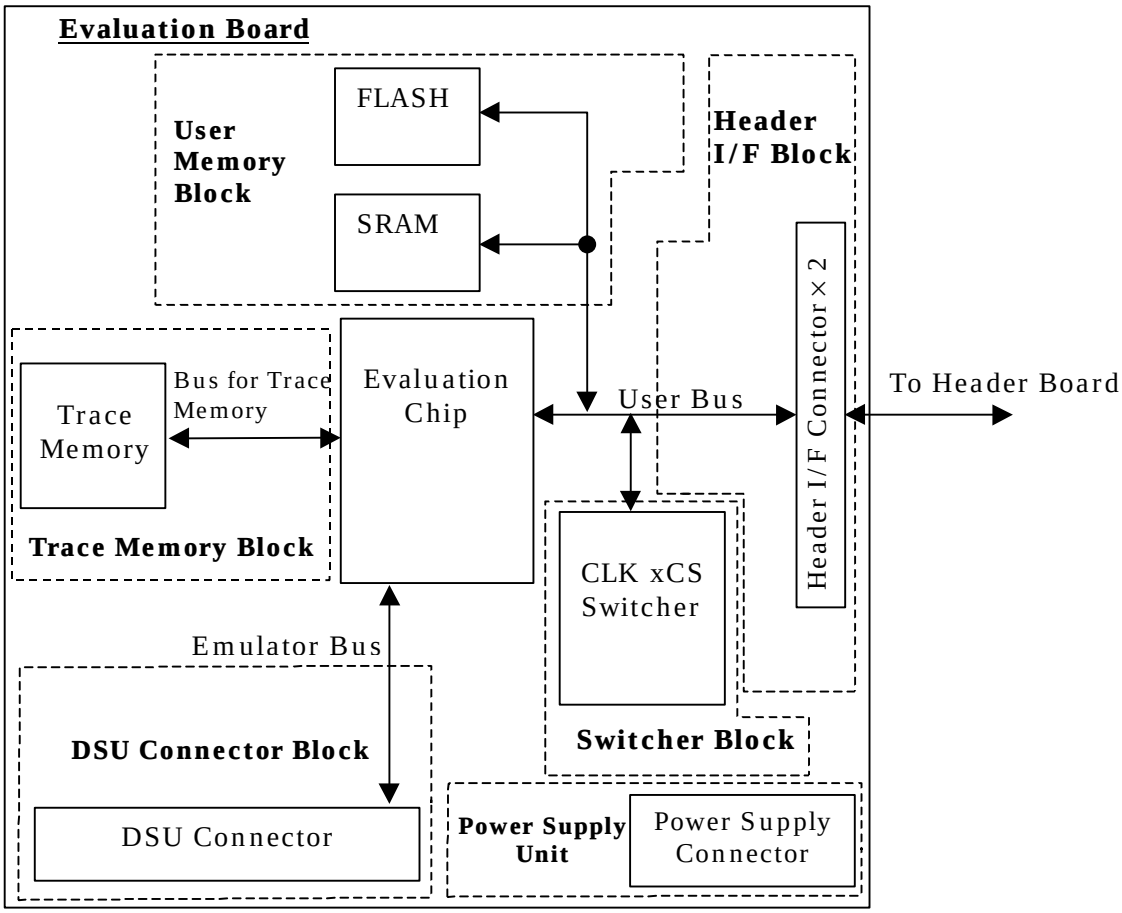


Figure 6. shows the Block Drawing of the Evaluation Board.

The details concerning the Trace Block, User Memory Block, Switcher Block and Evaluation Chip Reset Pin are explained on the following pages.
The DSU Block is wired directly to all Evaluation Chips and Header I/F connector pins, excluding the DSU connector's *RSTIN Pin. See ***7.4*** for details concerning the processing of the *RSTIN Pin.
The Header I/F Block is wired directly to all Evaluation Chips and Header I/F connector pins, excluding the Header I/F Connector's CS0X to CS6X, X0, X1, X0A, X1A and INITX Pins. See ***7.3*** for details concerning the processing of the CS0X to CS6X, X0, X1, X0A, X1A and INITX Pins. See ***7.4*** for details concerning the processing of the INITX Pin.
See ***7.6*** for details concerning the processing of the C Pin and Low Path Filter.

7.2 Trace Memory Block

Figure 7 shows the wiring of the Trace Memory and the Evaluation Chip. (The Trace Memory Power Supply is VCCT.)

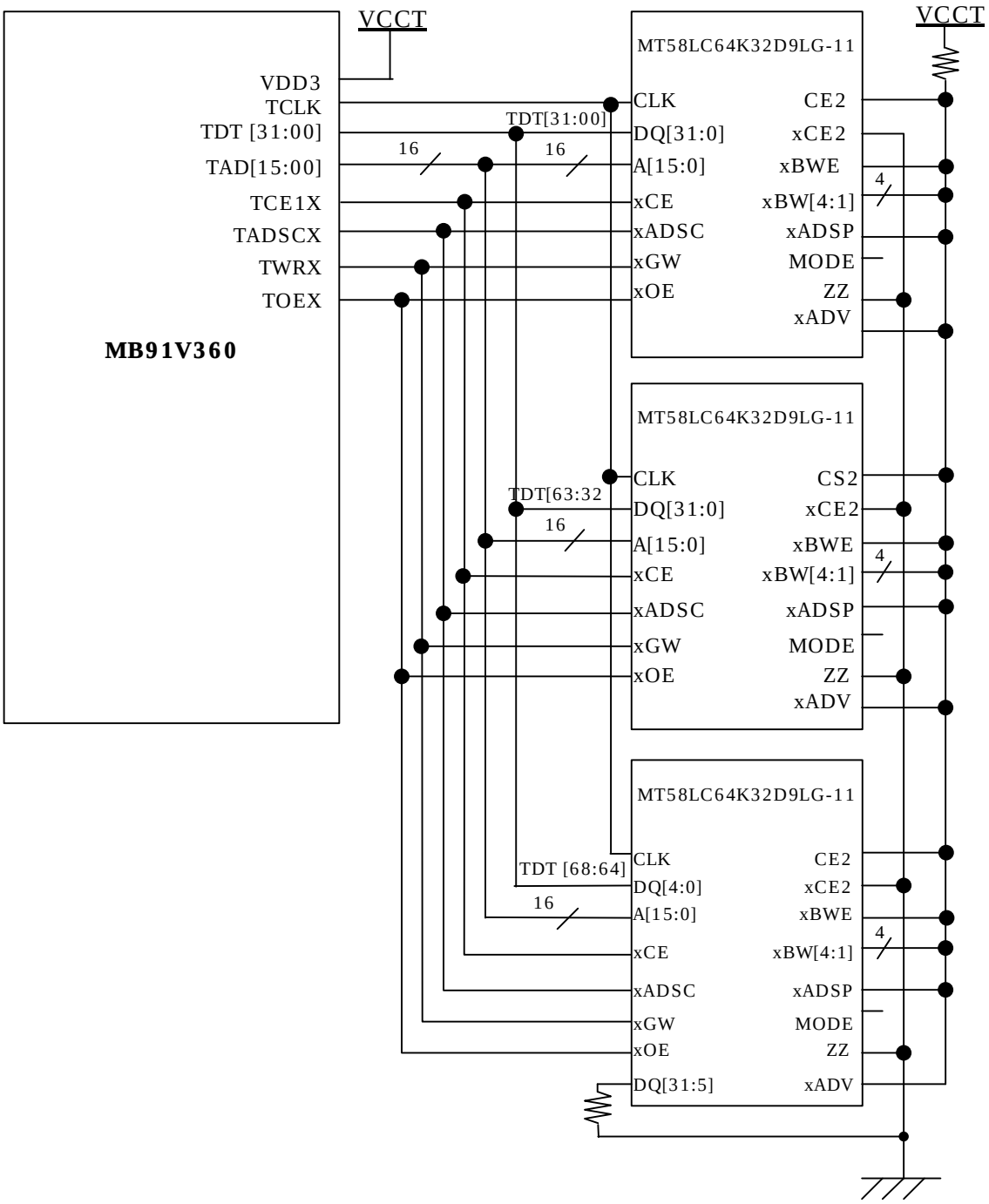


Figure 7 Wiring of the Trace Memory and Evaluation Chip

7.3 User Memory Block

Figure 8 shows the wiring of the User Memory Block. Also, ***Table 9*** and ***Figure 9*** show the functions of the CLK and CS Switcher Blocks.

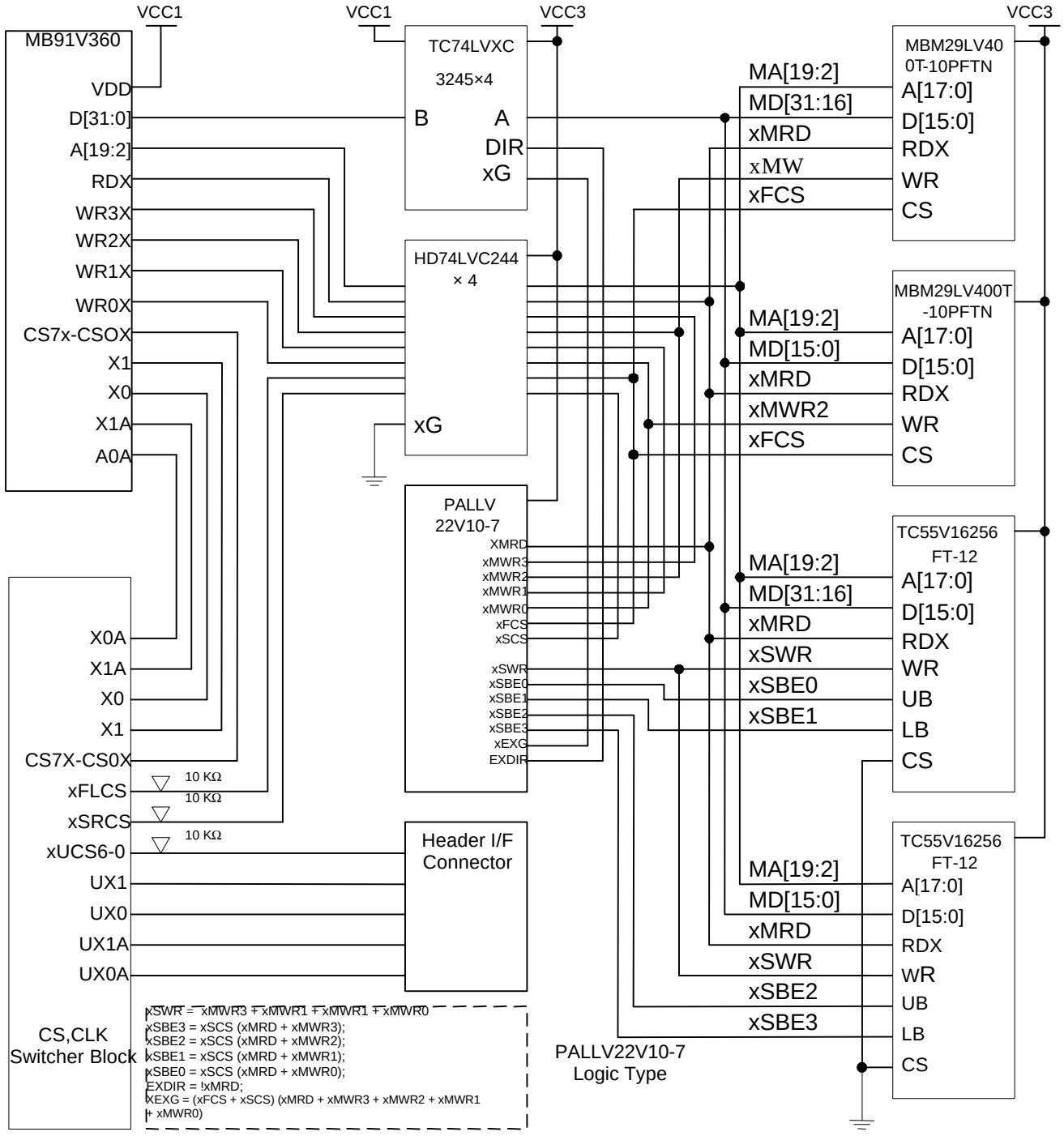


Figure 8 User Memory Block

	Function
	CS Signal Input
	FLASH Chip Select Signal Input
xSRCS	SRAM Chip Select Signal Input
xUCS6 to 0	User Chip Select Input
UX0,UX1	CLK Signal Input from the User Board
UX0A,UX1A	SUBCLK Signal Input from the User Board
X0,X1	The CLK signals from the Evaluation Board and from the User Board are supplied to the Evaluation Chip. Use a Short Plug to switch signals.
X0A,X1A	The SUBCLK signals from the Evaluation Board and from the User Board are supplied to the Evaluation Chip. Use a Short Plug to switch signals.

Table 9 CS and CLK Switcher Block Pin Names and Functions

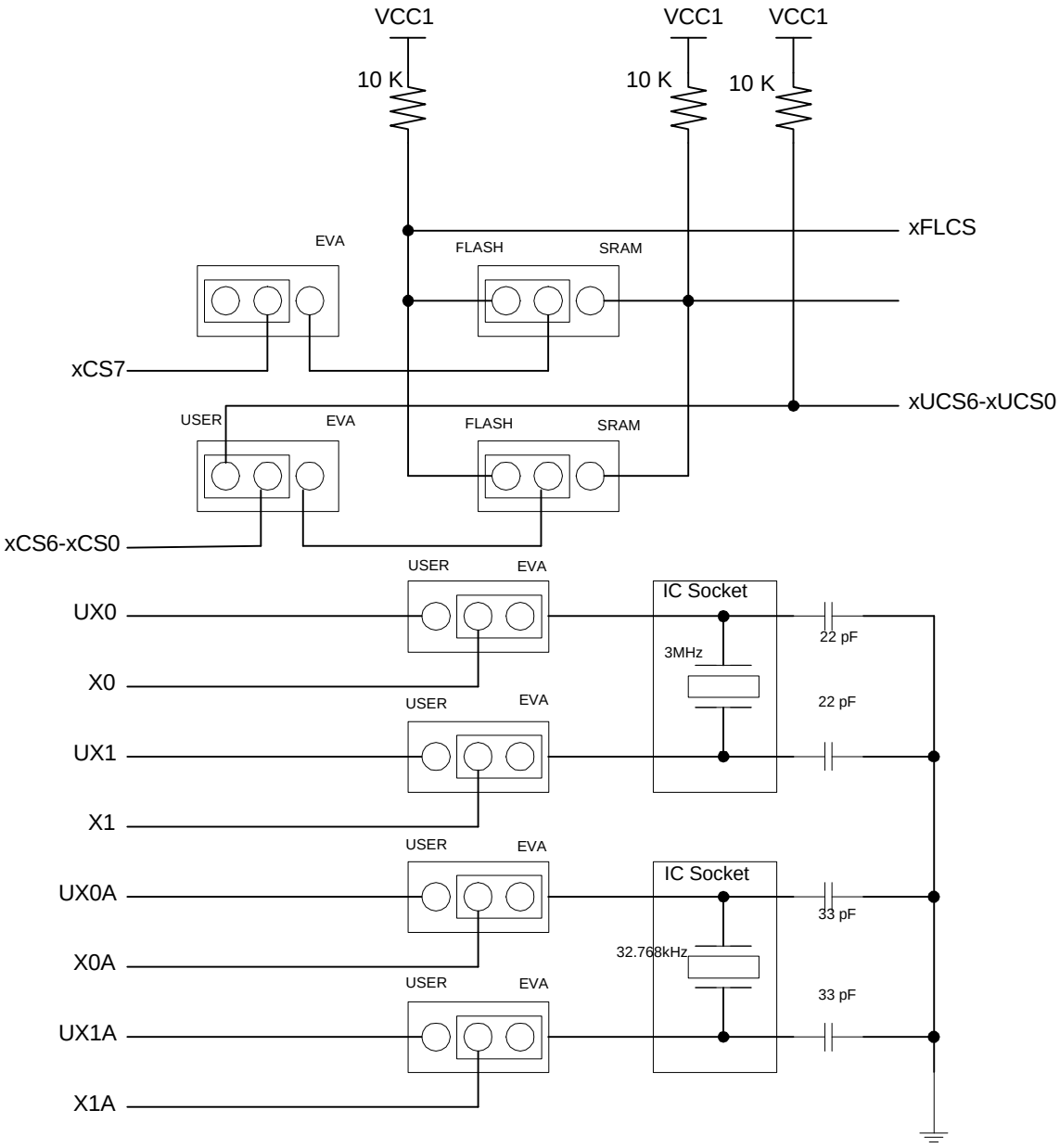


Figure 9 CS and CLK Switcher Block

7.4 Processing of the Reset Pin

Figure 10 shows the processing of the Reset Pin.

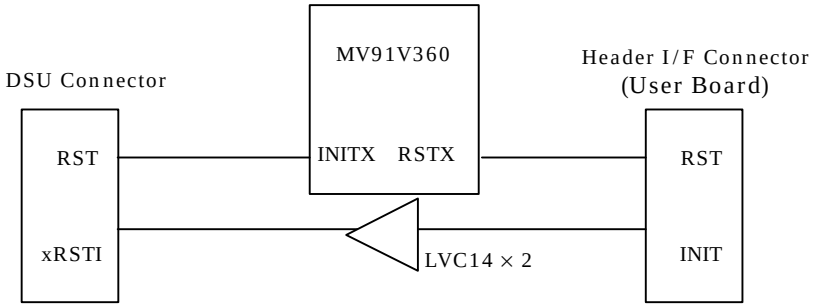


Figure 10 Processing of the Reset Pin

7.5 Power Supply Unit

Figure 11 shows the Power Supply Unit.

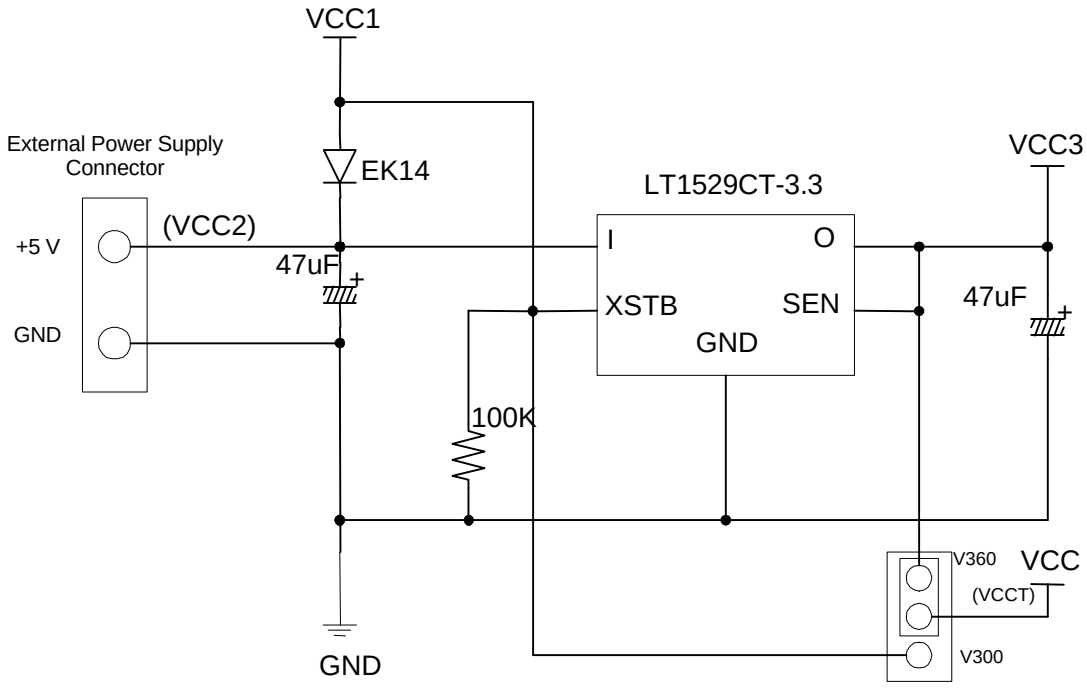


Figure 11 Power Supply Unit

7.6 Other Peripheral Blocks

The following shows the C Pin (VCC3/C) and Low Path Filter (CPO and VCO) circuits.
The Short Plug switches the C Pin ON and OFF.
The Short Plug switches the Low Path Filter between the User Board and the Evaluation Board.

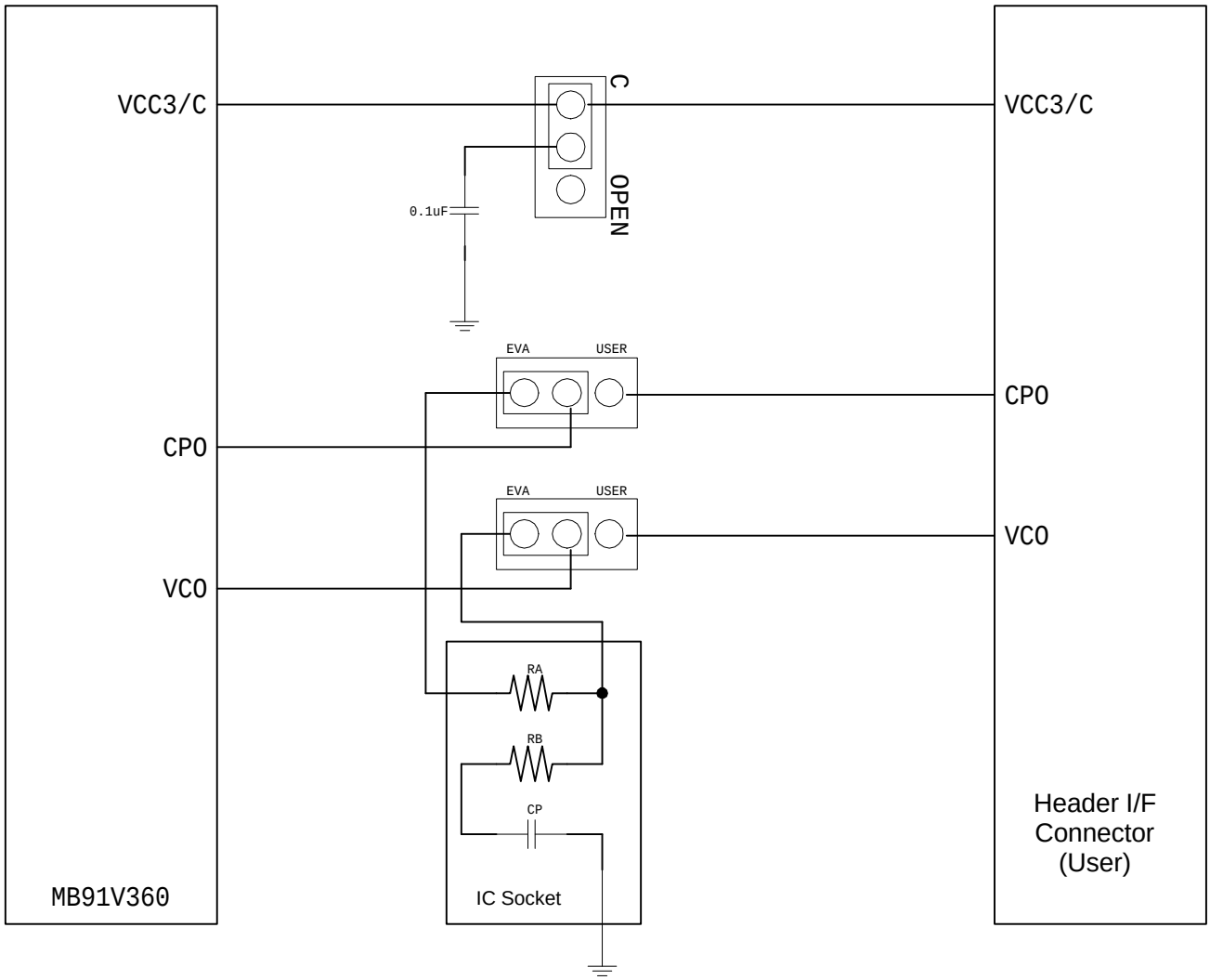


Figure 12 Other Peripheral Blocks

The Low Path Filter is mounted onto the IC Socket and tuning is possible. (When this is not going to be used, the Low Path Filter will not be mounted.)

8. AC Characteristics

Because the AC Specifications have not yet been determined, Fujitsu will rewrite them when MB91V360AC has been disclosed.

8.1 Trace Memory Read Timing

Figure 13 shows the TCLK 64 MHz Trace Memory Read Timing

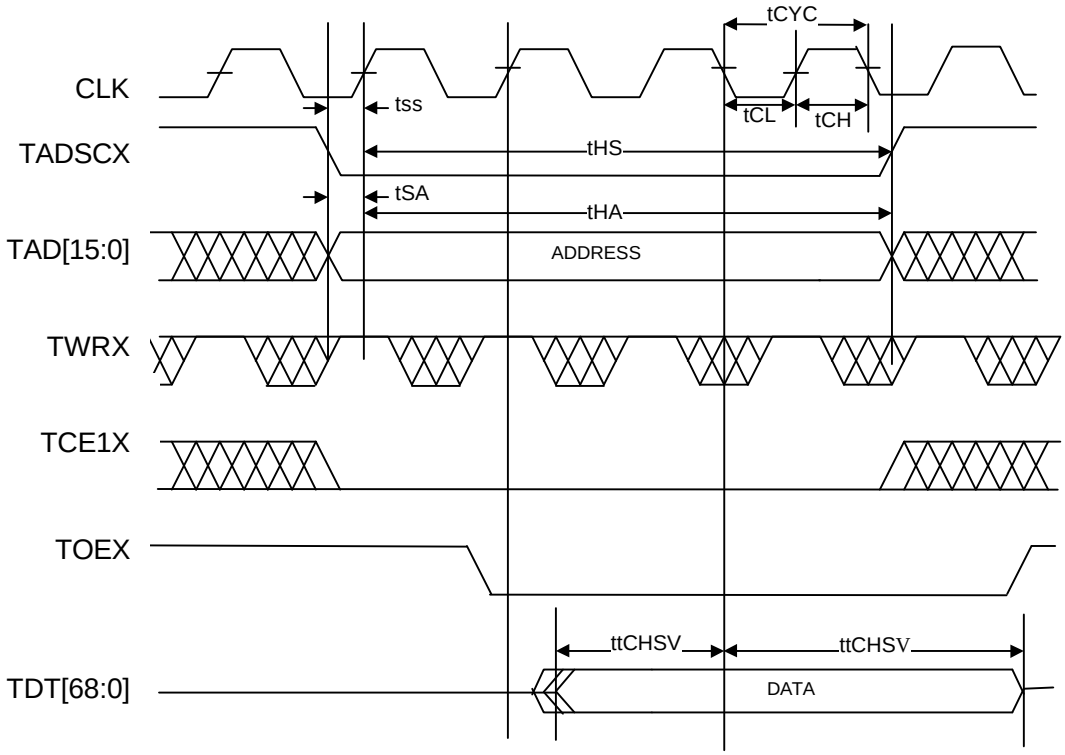


Figure 13 Trace Memory Read Timing

Symbol	Meaning	Value		Calculated Value		Units
		Min	Max	Min	Max	
tCYC	Cycle Time	15	--	15.6	--	ns
tCH	TCLK H Width	5	--	5	--	ns
tCL	TCLK L Width	5	--	5	--	ns
tSA	Address Setup Time	2.5	--	2.8	--	ns
tHA	Address Hold Time	0.5	--	59.6	--	ns
tSS	Address Status Setup Time	2.5	--	2.8	--	ns
tHS	Address Status Hold Time	0.5	--	59.6	--	ns
ttCHSV	Data Setup Time	15	--	17.4	--	ns
ttCHSX	Data Hold Time	0	--	31.2	--	ns

8.2 Trace Memory Write Timing

Figure 14 shows the TCLK 64 MHz Trace Memory Write Timing

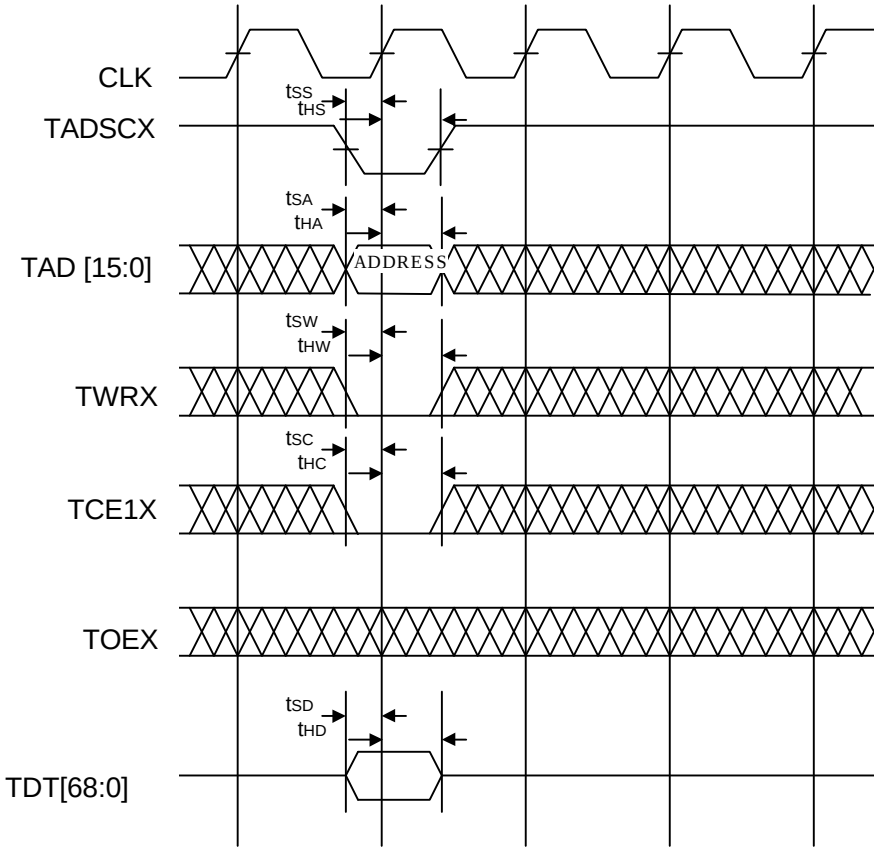
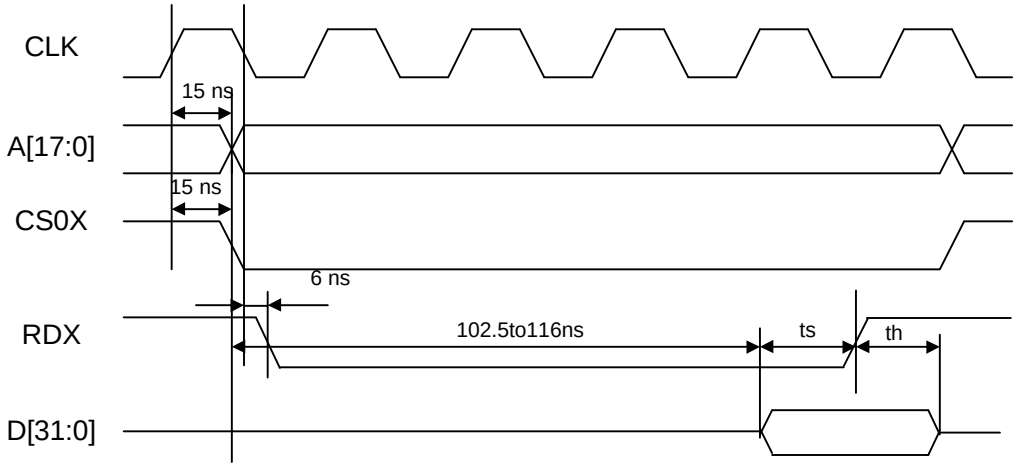


Figure 14 Trace Memory Write Timing

Symbol	Meaning	Meaning		Calculated Value		Units
		Min	Max	Min	Max	
tSA	Address Setup Time	2.5	--	2.8	--	ns
tHA	Address Hold Time	0.5	--	12.8	--	ns
tSS	Address Status Setup Time	2.5	--	2.8	--	ns
tHS	Address Status Hold Time	0.5	--	12.8	--	ns
tSD	Data Setup Time	2.5	--	2.8	--	ns
tHD	Data Hold Time	0.5	--	12.8	--	ns
tSW	TWRX Setup Time	2.5	--	2.8	--	ns
tHW	TWRX Hold Time	0.5	--	12.8	--	ns
tSC	TCE1X Setup Time	2.5	--	2.8	--	ns
tHC	TCE1X Hold Time	0.5	--	12.8	--	ns

8.3 FLASH Read Timing

There are 3 Wait Accesses when read accessing FLASH. (When CLK = 32 kHz) ***Figure 15*** shows the FLASH Read Timing.



Symbol	Meaning	Value		Calculated Value		Units
		min	max	min	max	
ts	Data Setup Time for ↑ R	10	--	17.1	--	ns
th	Data Hold Time for ↑ R	0	--	1	--	ns

Figure 15 FLASH Read Timing

ts, shown in the figure above, changes due to the Clock Frequency (Cycle Time) or the Wait Count. The relationships between the **ts** calculation value, cycle time and the Wait Count are shown below.
ω: Wait Count; τ: Cycle Count

$$(\omega + 1.5)\ \tau + 133.5 = ts \geq 10 \quad \text{.....(1)}$$

Insert the following to complete the above formula.

Block Frequency Count Minimum 11.2 MHz (Cycle Time 89.2 ns):
Minimum 1 Wait
Block Frequency Count Minimum 18.7 MHz (Cycle Time 53.4 ns):
Minimum 2 Waits
Block Frequency Count Minimum 26.2 MHz (Cycle Time 38.1 ns):
Minimum 3 Waits

8.4 FLASH Write Timing

There are 3 Wait Accesses when write accessing FLASH. (When CLK = 32 kHz) ***Figure 16*** shows the FLASH Write Timing.

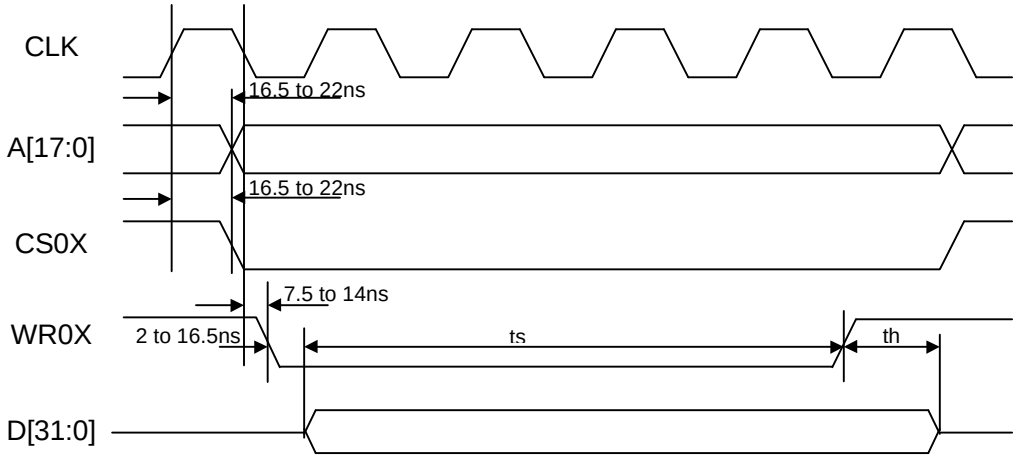


Figure 16 FLASH Write Timing

Symbol	Meaning	Value		Calculated Value		Units
		min	max	min	max	
ts	Data Setup Time for ↑W	50	--	102	--	ns
th	Data Hold Time for ↑W	0	--	1	--	ns

8.5 SRAM Read Timing

There is 1 Wait Access when read accessing the SRAM. ***Figure 17*** shows the SRAM Read Timing.

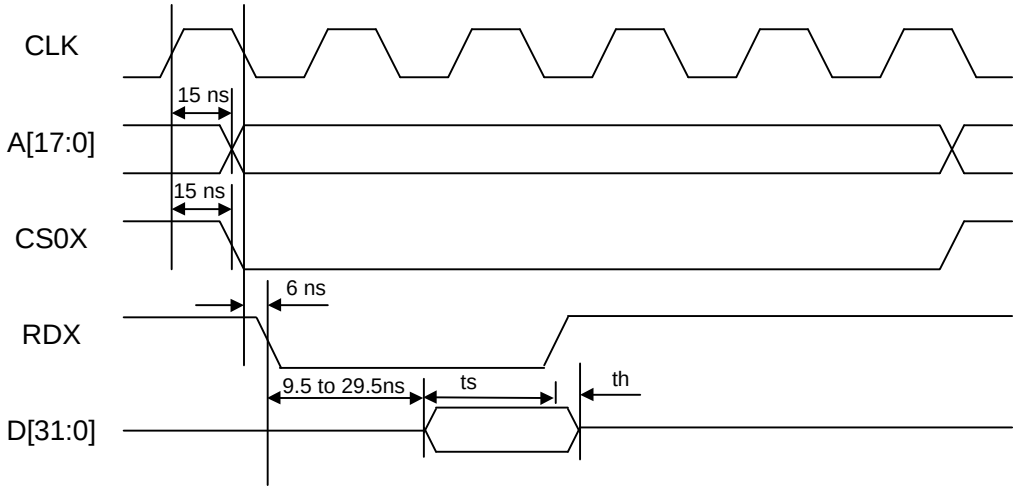


Figure 17 SRAM Read Timing

Symbol	Meaning	Value		Calculated Value		Units
		min	max	min	max	
ts	Data Setup Time for ↑ R	10	--	34.5	--	ns
th	Data Hold Time for ↑ R	0	--	1	--	ns

ts, shown in the figure above, changes due to the Clock Frequency (Cycle Time) or the Wait Count. The relationships between the ts calculation value, cycle time and the Wait Count are shown below.

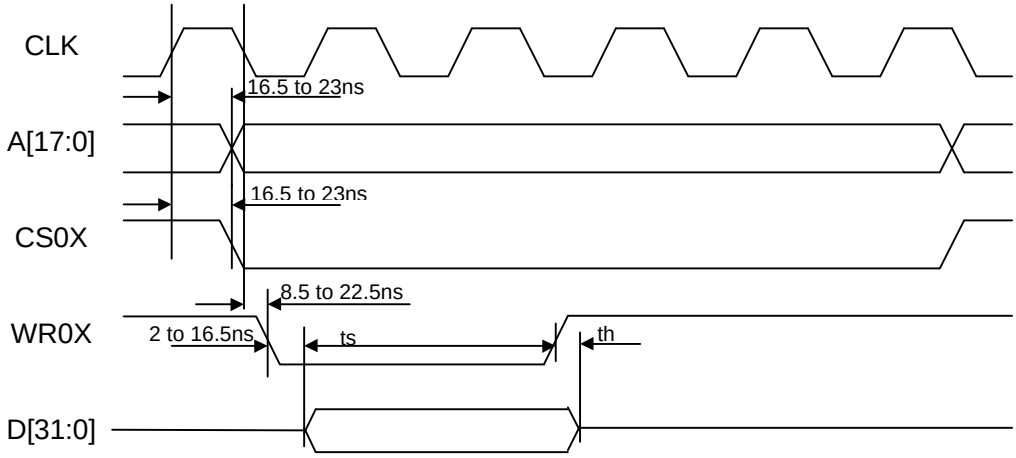
ω: Wait Count; τ: Cycle Count

$$(\omega + 1)\ \tau - 28 = ts \geq 10 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ (1)$$

Insert the following to complete the above formula.
Block Frequency Count Minimum 26.3 MHz (Cycle Time 38 ns):
Minimum 1 Wait

8.6 SRAM Write Timing

There are 1 Wait Accesses when write accessing SRAM.
Figure 18 shows the SRAM Write Timing.



Symbol	Meaning	Value		Calculated Value		Units
		min	max	min	max	
ts	Data Setup Time for ↑ W	7	--	32	--	ns
th	Data Hold Time for ↑ W	0	--	1	--	ns

Figure 18 SRAM Write Timing

9. Control Items

9.1 Power ON and Power OFF Order

The following shows the order for turning ON the system power supply when using the Evaluation Board.

Turn ON the Emulator Power Supply.
Turn ON the Evaluation Board Power Supply (External Power Supply).
Turn ON the User Board Power Supply.

The following shows the order for turning OFF the system power supply when using the Evaluation Board.

Turn OFF the User Board Power Supply.
Turn OFF the Evaluation Board Power Supply (External Power Supply).
Turn OFF the Emulator Power Supply.

9.2 Control Items

The following shows the control items when using the Evaluation Board.

1	IC Socket for Specific MCU
	Sockets must always be mounted for the MCU on the User Board when using an Evaluation Board. Use the specified IC Socket.
2	Resetting the Evaluation Chip.
	The Emulator controls the Evaluation Chip INITX pin. Reset is input from the User System via the Emulator instead of being directly input to the Evaluation Chip. For that reason, reset timing is delayed several clocks by the reset timing of the User System. Also, the Emulator Reset Command resets only the Evaluation Chip. It does not reset the User System.
3	Supplying a CLK Signal from the User Board.
	Use an oscillator to supply power for the CLK signal on the User Board when supplying CLK signals from the User Board to the Evaluation Chip.
4	Using a Header I/F Cable (Long).
	It is possible to use this cable when there the MCU Clock frequency is low or when there is extremely little chance of putting a load on the User Pins. Normally, use the standard cable.
5	Using User Memory
	An External Bus is possible only when there is a 32 Bit Bus width. It is not possible when using 8 or 16 bit widths. However, it is possible to drive the D23-0 when FLASH or SRAM have entered Mode Fetch. Memory will correctly fetch the mode data. All Data Bus are driven regardless of access size when reading both FLASH and SRAM. You can access words or half-words when FLASH is in the Write mode. You can access words, half-words and bytes when SRAM is in the Write mode. Neither FLASH nor SRAM support DMA by an external Bus Master.
6	Selecting Chips
	You cannot use the User Board when you are using the User Board on the Evaluation Board of CS6X to CS0X. Only 1 FLASH and SRAM can be set in the User Memory of CS7X to CS0X.

Table 10 Control Board