MB86290EB01

CREMSON [MB86290A] Evaluation System
Hardware Specifications
December 8 ‘99　(Rev.0.2)

FUJITSU

Overview

This documentation describes the hardware specifications of Cremson Evaluation System "MB86290EB01".

Outline

Figures

Tables

1 Overview

This board system is designed to mainly evaluate the functionality and performance of Fujitsu MB86290A “Cremson” Graphics Display Controller.

2 System Configuration

2.1 Board Configuration

Depending on the needs, this board can be used either by mounting on a PCI slot of ordinary Windows NT PC or by combining with a specific CPU evaluation board (A stand alone configuration). The applicable CPU boards are SH3-EVA BOD (CX06706C-9901, SH3 CPU evaluation board) or SH7750 EVA BOD-02 (CX06710B-9901, SH4 CPU evaluation board) made by Computex, or KZ-V832-01 (V832 evaluation board) made by Kyoto Micro Computers, Co. Ltd. When MB86290EB01 is used with this V832 evaluation board, the dedicated interface adapter board “MB86290EB02” is needed.

When MB86290EB01 is mounted on a PCI slot, the PCI bus bridge device PCI9054 (made by PLX) acts as a local bus master. When MB86290EB01 is combined with a CPU board, the CPU itself mounted on that board takes this local bus master role.

2.2 Component Outline

- CREMSON
  MB86290A (Graphics Display Controller)

- PCI bridge
  PCI9054 (made by PLX) and EEPROM [an equivalent to 93CS56L]

- SDRAM
  32Mbyte
  1Mword x 16bit x 4bank, 100MHz (MB81F641642C-103) x 4pcs

- FIFO
  16Kword x 18bit, 10ns (IDT72V265LA10) x 2pcs

- RGB Encoder MB3516A

- NTSC Decoder CXA1621A

- Video Sync Separator LM1881

- 4Fsc Generator EL4584C

- 8bit DIP Switch
  Read only

- 8bit LED
  Write only

- LED
  Power on (Power supply indicator)

- CPU Board Interface Connector
  100pin half pitch x 3

- VGA Output Connector
  Dsub15pin female connector

- S-VIDEO Output Connector

- Composite Video Input/Output Connectors
  Input x 1, Output x 1

2.3 Power Supply

All the power sources are supplied through interface connectors in either PCI bus mode or Local CPU board combination mode.

Power connections on this board are as follows:

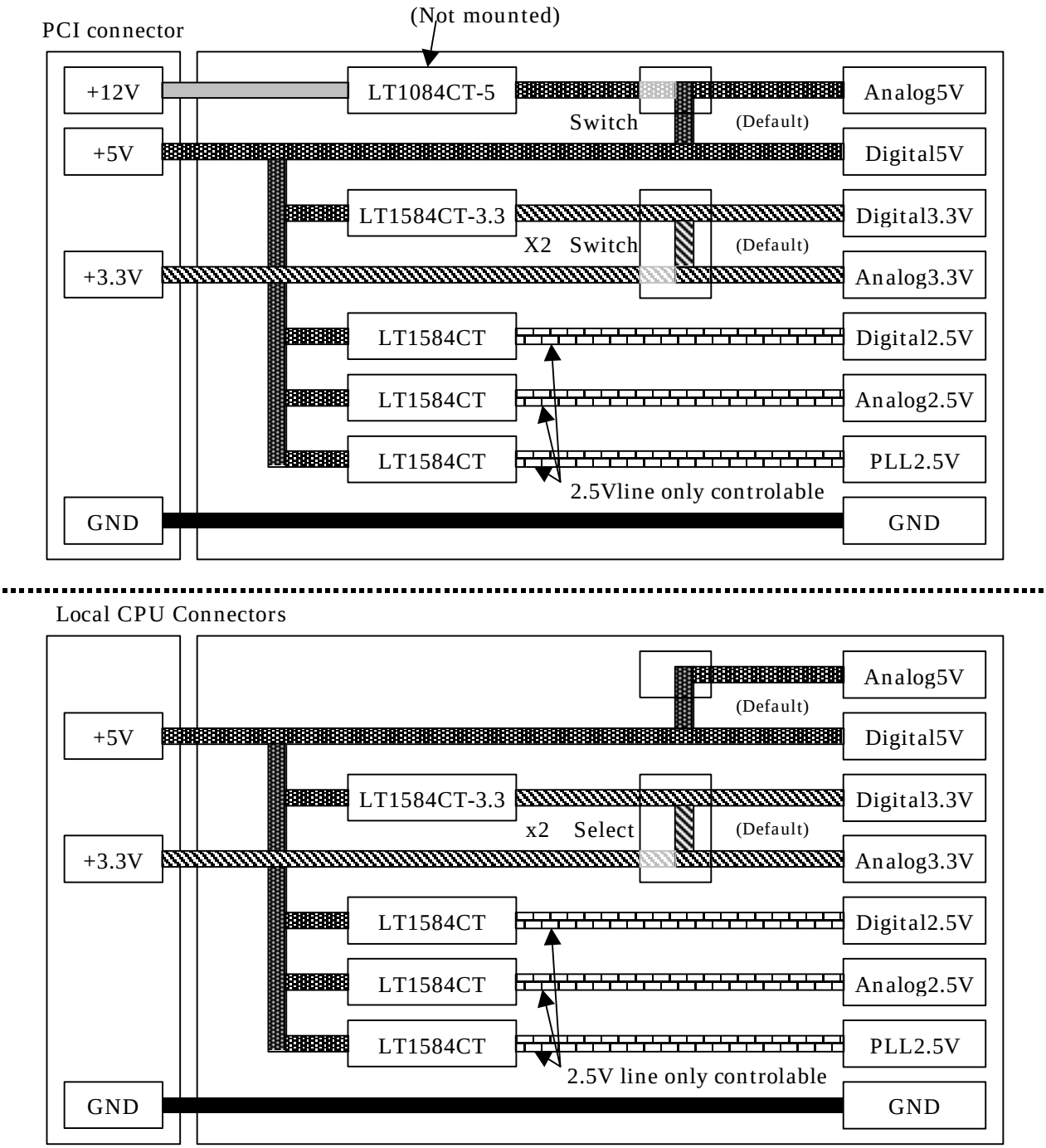

Fig 2-1. MB86290EB01 Power Supply Lines

3 Hardware Block Diagram

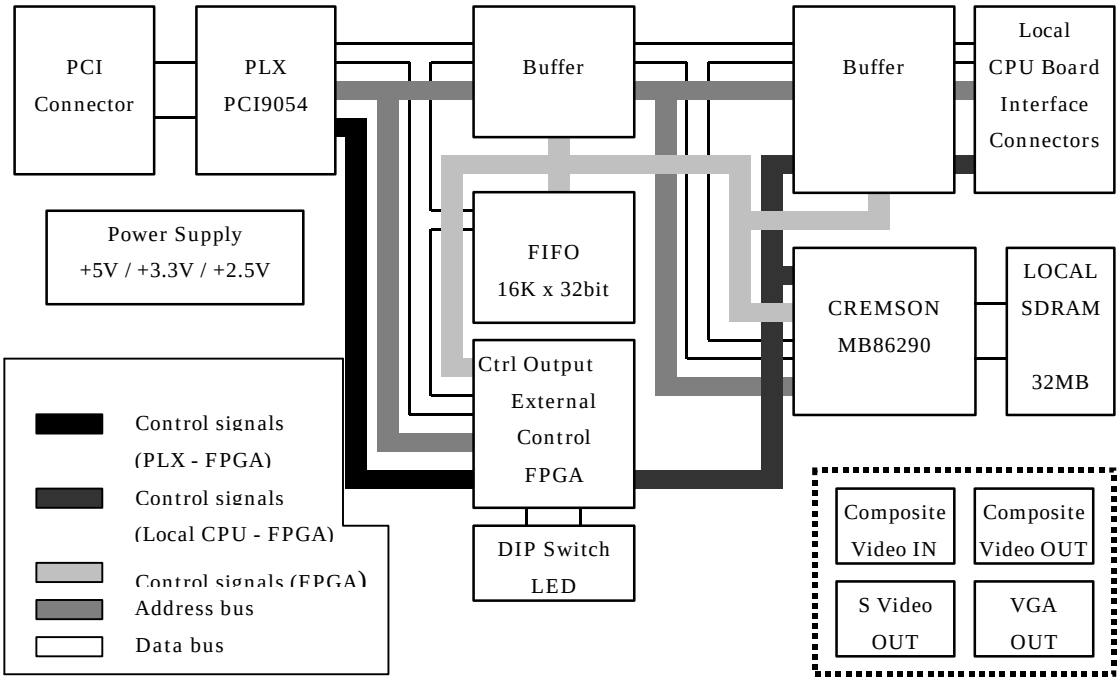

Fig 3-1. MB86290EB01 Hardware Block Diagram

4 Memory Map

4.1 Memory Map in PCI bus access mode

1000 0000h 11FB FFFFh	Cremson Frame Memory Area	32bit	PCI Local Address Space 0
11FC 0000h 11FF FFFFh	Cremson Register Area	32bit	
1200 0000h 13FF FFFFh	Cremson Reserved Area	32bit	
1400 0000h 1400 00FFh	PLX PCI9054 Internal Register Area	32bit	
1400 0100h 1400 01FFh	FPGA Internal Register Area	32bit	
2000 0000h 2000 FFFFh	FIFO Write Access Area	32bit	PCI Local Address Space 1
2000 0000h 2000 FFFFh	FIFO Write Reserved Area	32bit	

Table 4-1. MB86290EB01 Memory Map (PCI bus access mode)

4.2 Memory Map in Local CPU access mode

1000 0000h 11FB FFFFh	Cremson Frame Memory Area	32bit	SH_CS4
11FC 0000h 11FF FFFFh	Cremson Register Area	32bit	
1200 0000h 13FF FFFFh	Cremson Reserved Area	32bit	
1400 0000h 1400 00FFh	PLX PCI9054 Internal Register Area	32bit	SH_CS5 &A12=0
1400 0100h 1400 01FFh	FPGA Internal Register Area	32bit	SH_CS5 &A12=1

Table 4-2. MB86290EB01 Memory Map (Local CPU access mode)

4.3 Register Map

Device	Register	Address	Access	Data Size	True State	R/W
LEDR	LED Register	0x1400 0100	32bit	7:0	1=Light	RW
CTLR	Control Register	0x1400 0104	32bit	7:0	1	RW
DIPSWR	DIP Switch Register	0x1400 0108	32bit	7:0	Off=1	RO
FSTR	FIFO Status Register	0x1400 010C	32bit	7:0	1	PCI RO
FIFO WAA	FIFO Write Access Area	0x2000 0000-0x2000 FFFF	32bit	31:0	1	PCI WO

Table 4-3. MB86290EB01 Register Map

4.4 Board Configuration Register

- Name : CTLR
- Address : 1400 0104H
- Mode : Read / Write

Bit	Name	Function	0	1
D7	ESE	External Synch Enable	Disable (Default)	Enable the external Even/Odd signal input to Cremson in External synch mode

This bit must be set after the ESY bit of the Display Control Register(DCM) of Cremson is set to “1”.

Bit	Name	Function	0	1
D6	1LW	FIFO DMA Transfer Mode	Single address 32byte burst transfer (Default)	Single address 4byte burst transfer

This bit is valid in PCI bus access mode only.

Bit	Name	Function	0	1
D0	FTH	External FIFO access control	Disable (Default)	Enable to access to the local memory field and internal FIFO port of Cremson

This bit is valid in PCI bus access mode only.

Table 4-4. Board Configuration Register Bit Assignment

4.5 FIFO Status Register

- Name : FSTR
- Address : 1400 010CH
- Mode : Read Only

Bit	Name	Function	1
D7	FF	FIFO Full	External FIFO is full (16384word of data is set)
D6	FE	FIFO Empty	External FIFO is empty (No valid data is set)
D5	FAF	FIFO Almost Full	External FIFO is almost full SW2-4=Off : 15361 - 16384 words of data is set SW2-4=On : 16257 - 16384words of data is set
D4	FAE	FIFO Almost Empty	External FIFO is almost empty SW2-4=Off : 0 - 1023 words of data is set SW2-4=On : 0 - 127 words of data is set

Table 4-5. FIFO Status Register Bit Assignment

5 External Appearance

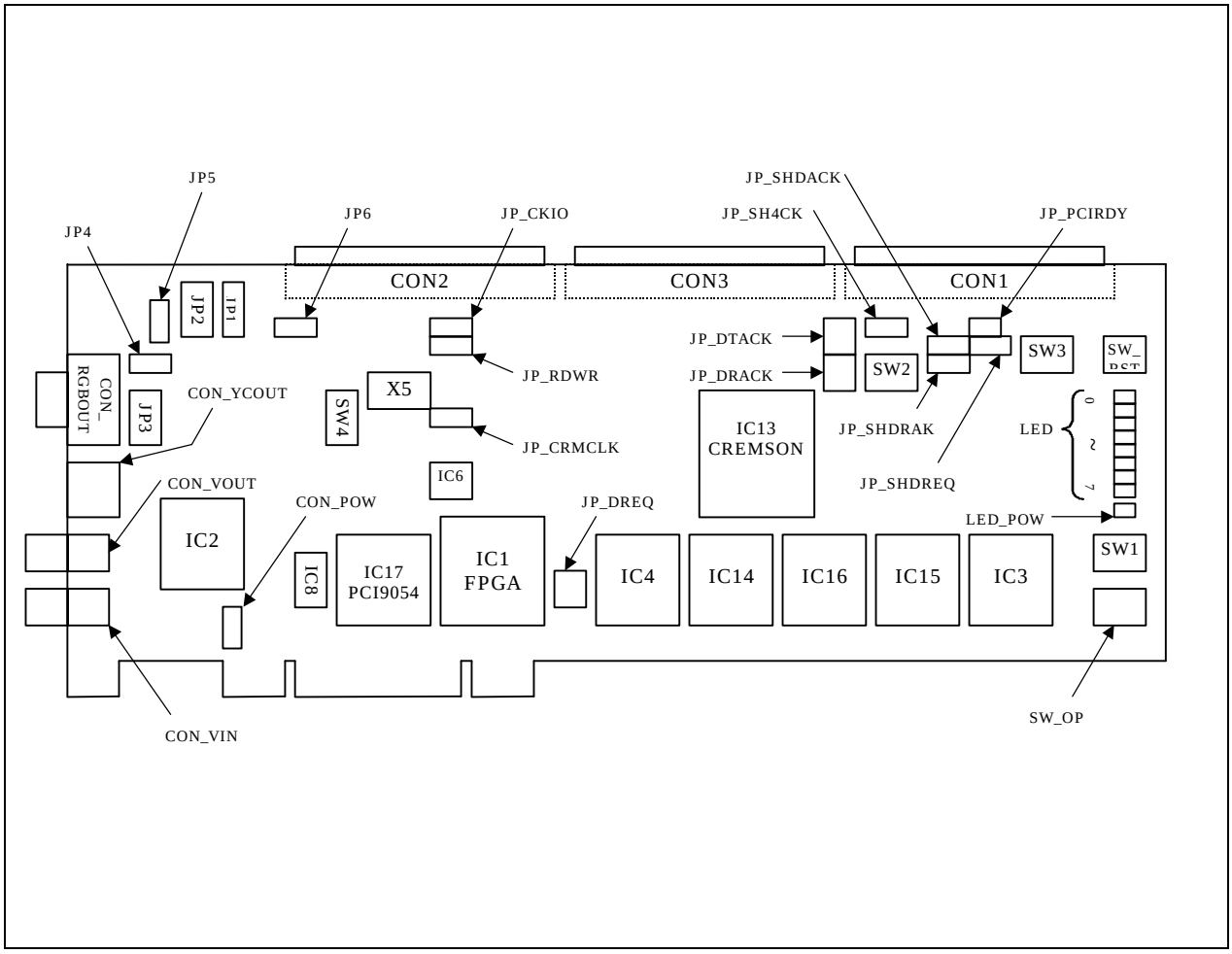

Fig 5-1. MB86290EB01 External Appearance

5.1 Switch Settings

Switch	Function	Set	Description
SW1	General purpose	OFF=1 ON=0	Bit1 : MLB Bit8 : MSB (Default is all OFF)
SW2-1	PCI9054 TEST signal input	ON	Normal mode (Default)
		OFF	PCI9054 test mode
SW2-2	PCI9054 BIGEND# pin input	ON	Local Bus is Big Endian
		OFF	Local Bus is Little Endian (Default)
SW2-3	CREMSON Local SDRAM MD63 - MD32 mode set	ON	MD63 - MD32 are applicable (Default)
		OFF	MD63 - MD32 are not applicable
SW2-4	FIFO LD# pin input	Refer section 4.5	
SW2-5,6	Cremson operation mode (Host CPU type option)	Bit5,6	(Note) 1=OFF,0=ON
		0,0	SH3, FR30
		0,1	V832
		1,0	SH4 (Default)
		1,1	Reserved
SW2-7	Cremson Internal clock option	ON	Internal PLL (Default)
		OFF	Host bus clock
SW2-8	Cremson Video I/F External synch input clock	ON	4fsc clock (Default)
		OFF	2fsc clock
SW3-1:6	Cremson test pin input		OFF=H level, ON=L level
SW3-7,8	Reserved		
SW4-1	GV signal(RGB switch) setting (1) (valid when JP6 is set to 1-2)	ON	GV=L(Cremson output is selected)
		OFF	GV=H(Video input is selected)
SW4-2,3	Reserved		
SW4-4	EL4584C PROGA pin input		OFF=H level, ON=L level
SW4-5	EL4584C PROGB pin input		OFF=H level, ON=L level
SW4-6	EL4584C PROGC pin input		OFF=H level, ON=L level
SW4-7	EL4584C DIVSEL pin input		OFF=H level, ON=L level
SW4-8	EL4584C COAST pin input		OFF=H level, ON=L level
SW_OP-1 ~ 7	Reserved Always 1 - 6:OFF, 7:ON		
SW_OP-8	GV signal setting (2)	Refer the section of JP6	
SW-RST	Reset input		

Table 5-1. MB86290EB01 Switch Settings

5.2 Jumper Settings

Jumper	Function	Set	Description
JP1	Cremson RGB output signal connection (1)	Short	Input to RGB switch and connect 75 ohm terminator (Default)
		Open	Not input to RGB switch and no 75 ohm terminator is connected
JP2	Cremson RGB output signal connection (2)	1-2	Connect RGB output of Cremson to MB3516(NTSC encoder)
		2-3	Connect RGB switch output to MB3516(NTSC encoder) (Default)
JP3	CREMSON RGB output signal connection (3)	1-2	Connect RGB output of Cremson to VGA connector directly
		2-3	Connect output signal of MB3516 to VGA connector (Default)
JP4	MB3516 CSYNC signal	1-2	CSYNC output of Cremson
		2-3	CSYNC output of LM1881(Sync separator) (Default)
JP5	MB3516 FSC clock input	1-2	X-Tal output (3.579545MHz) (Default)
		2-3	DCLKO output of Cremson
JP6 SW_OP-8	NJM2286(RGB switch) Control signal	1-2, SW=On	SW4-1 is valid (Refer SW4-1 section)
		Open, SW=Off	GV output of Cremson is valid (Default)
		Other settings	Prohibited
JP_CRMCLK	Cremson Bus clock input	1-2	Positive clock (Default)
		2-3	Negative (inverted) clock
JP-PCIRDY	Local CPU interface Wait signal Pull-Up setting	Short	Wait signal is pulled up
		Open	Wait signal is not pulled up (Default)
JP_CKIO	SH I/F Local Bus clock	1-2	SH3 CPU board is applied
		2-3	SH4 CPU board is applied
JP_RDWR	SH I/F RDWR signal	1-2	SH3 CPU board is applied
		2-3	SH4 CPU board is applied
JP_SH4CK	SH4 I/F Local Bus clock	1-2	CKIO1 signal is used
		2-3	CKIO2 signal is used
JP_SHDACK	SH I/F DACK signal	1-2	DACK0 signal is used
		2-3	DACK1 signal is used
JP_SHDRAK	SH I/F DRAK signal	1-2	DRAK0 signal is used
		2-3	DRAK1 signal is used
JP_SHDREQ	SH I/F DREQ signal	1-2	DREQ0 signal is used
		2-3	DREQ1 signal is used
JP_DTACK	SH I/F DTACK signal	2-4	Fixed (Default)
JP_DRACK	SH I/F DRACK signal	2-4	Fixed (Default)
JP_DREQ	SH I/F DREQ signal	2-4	Fixed (Default)

Table 5-2. MB86290EB01 Jumper Settings

5.3 Switch and Jumper Settings of Video Output Control Block

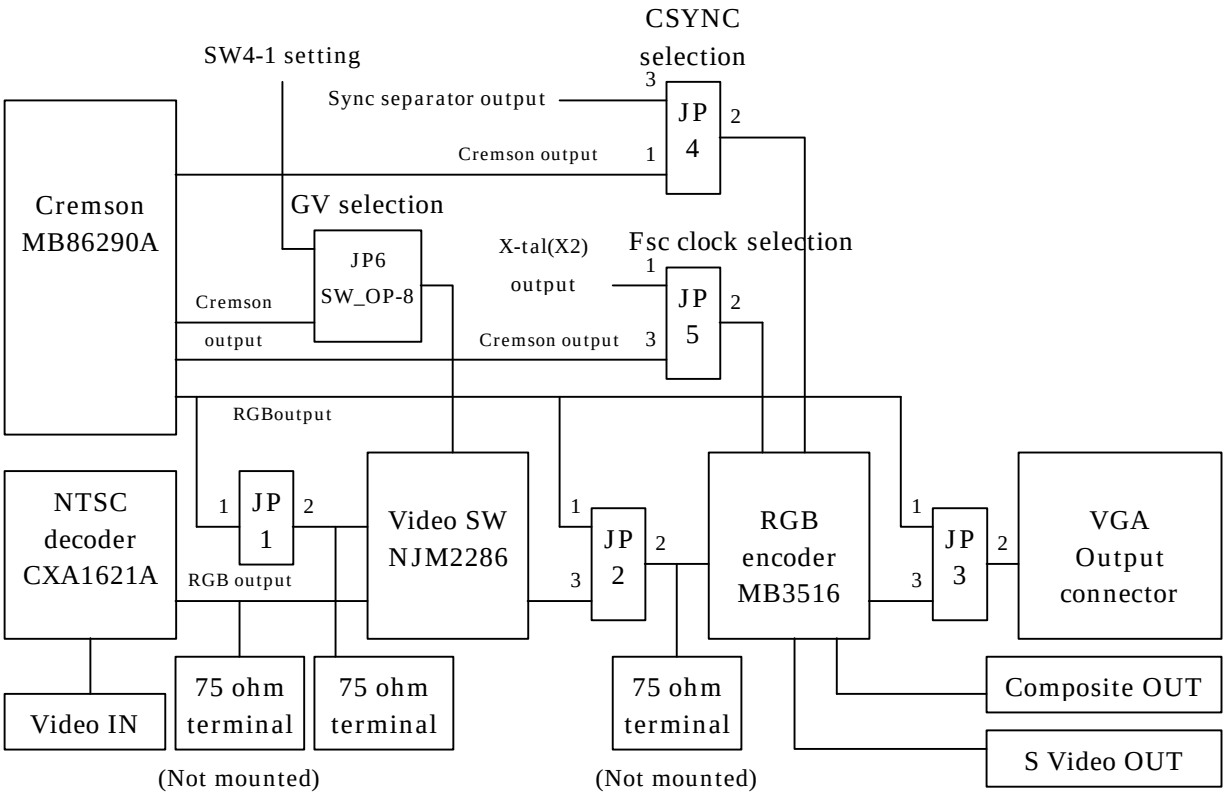

Fig 5-2. MB86290EB01 Video Control Block Diagram

Setting	JP1	JP2	JP3	JP4	JP5	JP6	SW_OP-8
RGB output from Cremson is directly connected to VGA connector	Short:*1 Open:*2	2-3 (Don't care)	1-2	2-3 (Don't care)	1-2 (Don't care)	Open (Don't care)	Off (Don't care)
VIDEO SW output is connected to each OUT connector (VBA/Composite/S Video)	Short	2-3	2-3	2-3	1-2	Open	Off

*1 : With 75 ohm terminal

*2 : Without 75 ohm terminal

Table 5-3. MB86290EB01 Switch Jumper setting table for video output control block

5.4 SH CPU Board Interface Connectors

This board has three special connectors to interface to local CPU board (SH3:HD7709A and SH4:HD7750 are the expected host CPU for this board). By hooking a specific CPU board to these interface connectors, an embedded stand alone system can be configured.

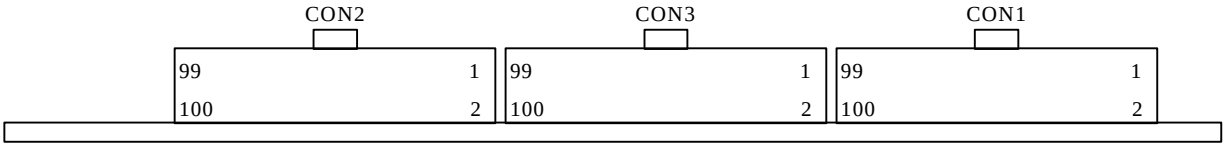

Fig 5-3. MB86290EB01 Front View of CPU Interface Connectors

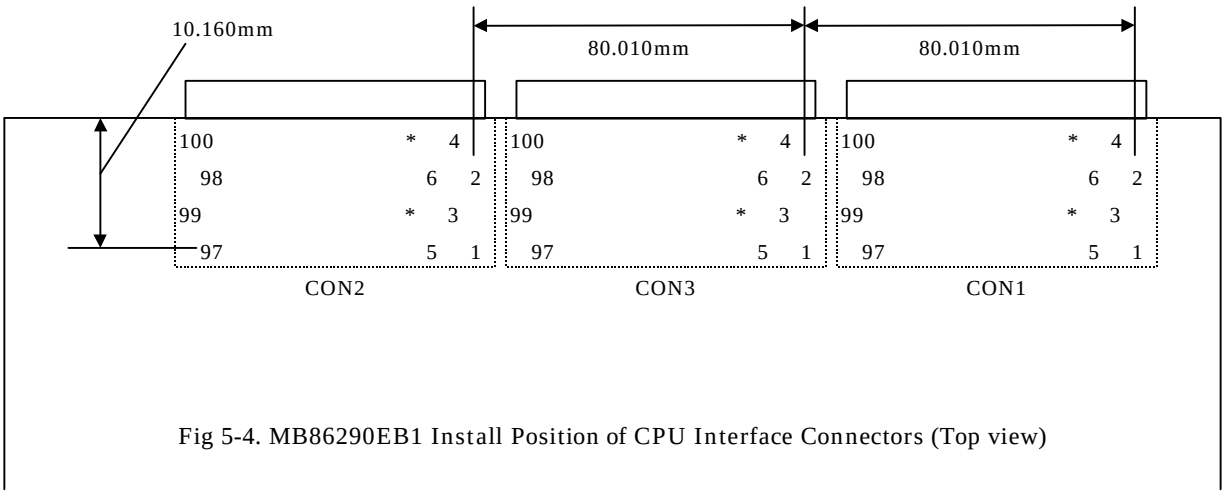

Fig 5-4. MB86290EB1 Install Position of CPU Interface Connectors (Top view)

Note) Part number of these connectors (female type:CON1 - CON3)
TX14-100R-LT-MH1 (JAE)

CPU board side connectors (male type)
TX15-100P-LT-MH1 (JAE)
http://www.jae.com/frame.htm

5.5 Signal Pin Assignment

CON1(SH4 Connect only)				CON2(SH3 Connect only)			
1	GND	2	GND	1	GND	2	GND
3	GND	4	GND	3	GND	4	GND
5	VCC3*	6	VCC3*	5	VCC3*	6	VCC3*
7	VCC3*	8	VCC3*	7	VCC3*	8	VCC3*
9	N.C.	10	N.C.	9	SH3_CKIO	10	N.C.
11	N.C.	12	N.C.	11	N.C.	12	N.C.
13	N.C.	14	N.C.	13	SH_WAIT	14	N.C.
15	N.C.	16	N.C.	15	~SH_BACK	16	~SH_BREQ
17	N.C.	18	N.C.	17	N.C.	18	N.C.
19	N.C.	20	N.C.	19	N.C.	20	N.C.
21	N.C.	22	N.C.	21	N.C.	22	N.C.
23	N.C.	24	N.C.	23	N.C.	24	N.C.
25	N.C.	26	N.C.	25	N.C.	26	N.C.
27	N.C.	28	N.C.	27	N.C.	28	N.C.
29	N.C.	30	N.C.	29	DRAK1	30	DRAK0
31	N.C.	32	N.C.	31	~RESETOUT	32	N.C.
33	N.C.	34	N.C.	33	~DREQ0	34	DACK0
35	N.C.	36	N.C.	35	~DREQ1	36	DACK1
37	N.C.	38	N.C.	37	N.C.	38	N.C.
39	N.C.	40	N.C.	39	N.C.	40	N.C.
41	GND	42	GND	41	GND	42	GND
43	N.C.	44	N.C.	43	N.C.	44	N.C.
45	N.C.	46	N.C.	45	N.C.	46	N.C.
47	N.C.	48	N.C.	47	N.C.	48	N.C.
49	N.C.	50	N.C.	49	N.C.	50	N.C.
51	~SH_IRL0	52	~SH_IRL1	51	N.C.	52	N.C.
53	~SH_IRL2	54	~SH_IRL3	53	N.C.	54	N.C.
55	~DREQ0	56	~DREQ1	55	N.C.	56	N.C.
57	DRAK0	58	DRAK1	57	N.C.	58	N.C.
59	DACK0	60	DACK1	59	N.C.	60	N.C.
61	~CKIO2ENB	62	N.C.	61	N.C.	62	N.C.
63	SH4_RDWR	64	N.C.	63	~SH_IRL0	64	~SH_IRL1
65	N.C.	66	N.C.	65	~SH_IRL2	66	~SH_IRL3
67	N.C.	68	~SH_BS	67	N.C.	68	N.C.
69	SH_BACK	70	~SH_BREQ	69	N.C.	70	N.C.
71	N.C.	72	N.C.	71	N.C.	72	N.C.
73	N.C.	74	SH_WAIT	73	N.C.	74	N.C.
75	N.C.	76	N.C.	75	N.C.	76	N.C.
77	N.C.	78	N.C.	77	N.C.	78	N.C.
79	CKIO2	80	N.C.	79	~SH_BS	80	N.C.
81	N.C.	82	N.C.	81	N.C.	82	N.C.
83	CKIO1	84	N.C.	83	N.C.	84	N.C.
85	N.C.	86	N.C.	85	N.C.	86	N.C.
87	~RESETOUT	88	N.C.	87	N.C.	88	N.C.
89	N.C.	90	N.C.	89	N.C.	90	N.C.
91	N.C.	92	N.C.	91	N.C.	92	N.C.
93	VCC3*	94	VCC3*	93	VCC3*	94	VCC3*
95	VCC3*	96	VCC3*	95	VCC3*	96	VCC3*
97	GND	98	GND	97	GND	98	GND
99	GND	100	GND	99	GND	100	GND

*Vcc3 : +3.3V power supply pin

+3.3V power is generated by the on board regulator, this pin is not used in this board.

Table 5-4. MB86290EB01 CPU Interface Connector Pin Assignment (1)

CON3(SH3 & SH4 Common)			
1	GND	2	GND
3	GND	4	GND
5	VCC5	6	VCC5
7	VCC5	8	VCC5
9	A0*	10	A1*
11	SH_A2	12	SH_A3
13	SH_A4	14	SH_A5
15	SH_A6	16	SH_A7
17	SH_A8	18	SH_A9
19	SH_A10	20	SH_A11
21	SH_A12	22	SH_A13
23	SH_A14	24	SH_A15
25	SH_A16	26	SH_A17
27	SH_A18	28	SH_A19
29	SH_A20	30	SH_A21
31	SH_A22	32	SH_A23
33	SH_A24	34	SH_A25
35	N.C.	36	N.C.
37	N.C.	38	N.C.
39	N.C.	40	N.C.
41	GND	42	GND
43	SH_D0	44	SH_D1
45	SH_D2	46	SH_D3
47	SH_D4	48	SH_D5
49	SH_D6	50	SH_D7
51	SH_D8	52	SH_D9
53	SH_D10	54	SH_D11
55	SH_D12	56	SH_D13
57	SH_D14	58	SH_D15
59	SH_D16	60	SH_D17
61	SH_D18	62	SH_D19
63	SH_D20	64	SH_D21
65	SH_D22	66	SH_D23
67	SH_D24	68	SH_D25
69	SH_D26	70	SH_D27
71	SH_D28	72	SH_D29
73	SH_D30	74	SH_D31
75	~SH_CS0	76	~SH_WE0
77	~SH_CS1	78	~SH_WE1
79	~SH_CS2	80	~SH_WE2
81	~SH_CS3	82	~SH_WE3
83	~SH_CS4	84	N.C.
85	~SH_CS5	86	N.C.
87	~SH_CS6	88	N.C.
89	N.C.	90	N.C.
91	~SH_RD	92	SH3_RDWR
93	VCC5	94	VCC5
95	VCC5	96	VCC5
97	GND	98	GND
99	GND	100	GND

*A0,A1 : Not used

Table 5-5. MB86290EB01 CPU Interface Connector Pin Assignment (2)