

MB86291 <Scarlet> LSI Errata Sheet

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APPENDIX 1 [BLPO register]

1. details of the bug

Because of a bug in write function of BLPO (Broken Line Pattern Offset) register which is described in Specification [10.1.6 draw mode register], an arbitrary value cannot be set to BLPO register.

2. cause of the bug

It is the cause that BLPO register is overwritten with the value of BLPO mirror register which has internally the value which was written to BLPO register.

3. measure

It is in the following cases that the bug causes a problem.

A: A broken line is used.

B: Another primitive is drawn. Or a not continuous broken line is used.

C: A continuation of the broken line of A is drawn so that it may be continued to the line of A.

In this case, an arbitrary value has to be applied to BLPO register at process of C. But this cannot be performed because of this bug.

There is the following method as an avoidable measure to the bug.

Please change the broken line pattern.

For example, when you want to draw the following the broken line pattern(direction: from left to right) again,

□□■■■■□□□■□□□■□□■■■...



When you want to continue drawing from here.

Please change the broken line pattern to ■□□□■□□■■■

Then clear the broken line pointer and start drawing.

4. correction of hardware

This bug will be corrected at the time of the following revision.

APPENDIX 2 [differences of texture]

1. details of the bug

In case the triangle with texture is drawn using Z coordinates or alpha / logical operation, ST coordinates may shift and the texture pattern may blur.

2. cause of the bug

When wait is generated at Z-buffer READ or frame buffer READ, the divider for texture perspectives continues moving while some of main pipeline was stopped. This causes this bug.

3. measure

There is no perfect avoidable measure. The blur of texture pattern becomes inconspicuous by using bi-linear filtering.

4. correction of hardware

no hardware correction is planned for this bug.

APPENDIX 3 [geometry firmware]

1. details of the bug

About the geometry process the product specification says that the coordinates after conversion of view port are necessary to fit in less than [-4096, 4095]. But this specification is not fulfilled about an arbitrary polygon.

In an arbitrary polygon, when view port conversion of the coordinates before generation of geometry clip is performed, the coordinates after conversion may not fit within the limit of [-4096,4095]. In this case, the arbitrary polygon may not be drawn correctly.

Similarly, when view port conversion of the coordinates before generation of W clip is carried out, the coordinates after conversion may not fit within the limit of [-4096,4095]. So, an arbitrary polygon may not be correctly drawn at the time of W clip generating.

2. cause of the bug

In drawing of an arbitrary polygon, with reference to the flag the process that paints over the pixel whose flag stands is performed. The cause of this bug is that renewal of the circumscription quadrangle used as the domain information on reference of the flag has not worked correctly.

The circumscription quadrangle is updated with the coordinates after clip processing usually. However, it turned out that there is a case where the circumscription quadrangle is updated with the coordinates before clip processing. Therefore, the coordinates exceeding [-4096,4095] may be used as a circumscription quadrangle. In this case, the drawing space of the drawing engine is exceeded and the flag reference drawing may not be performed correctly. It causes this bug.

3. measure

by application

This measure is effective only to primitive = PolygonInt (including nclip_PolygonInt). It is inapplicable to polygon.

[step1]

As for this fault, renewal of the circumscription quadrangle of an arbitrary polygon does not work correctly. However, if a circumscription quadrangle is updated by application as follows, it will be correctly drawn in function. ("High-speed 2D line drawing register", a secret register, by the side of the drawing engine is used for a circumscription quadrangle.)

Please set up the size of a circumscription quadrangle so that the arbitrary polygon may be in inside. Hardware makes reference to the flag in this circumscription quadrangle and paints over the pixel whose flag stands. In order to correspond to all cases, set up the size of a circumscription quadrangle to become the same as that of the drawing clip frame. Then, it is drawn correctly.

However, if this process is performed to each arbitrary polygon, the flag reference time of the circumscription quadrangle will cause a problem. Therefore, please examine this method together with the method of the following STEP2.

before correction	after correction
G_Begin (Polygon.Int)	G_Begin (Polygon.Int)
vertex "	vertex "
vertex "	vertex "
vertex "	vertex "
...	...
G_End	renewal of a circumscription quadrangle * //the arbitrary circumscription quadrangles which can contain an arbitrary polygon
	G_End

[step2]

The method of drawing some arbitrary polygons by one process is shown below.

There is the method of once sending G_End at last besides the former method of sending G_End to G_Begin each time. (In addition, this method is not exhibited by Specification.) This method is effective when an arbitrary polygon does not overlap, and it can suppress the flag reference drawing to only 1 time. If it overlaps, only the overlapping pixel may not be drawn. This is because the renewal of the flag is performed using XOR.

For example, this way seems effective in a case that draws many buildings with an arbitrary polygon on the whole screen. However, in a bird view, an arbitrary polygon may overlaps at back of a screen.

before correction	after correction
G_Begin (Polygon.Int)	G_Begin (Polygon.Int)
vertex "	vertex "
vertex "	vertex "
vertex "	vertex "
...	...
G_End	G_BeginCont (Polygon.Int)
G_BeginCont (Polygon.Int)	vertex "
Vertex "	vertex "
Vertex "	vertex "
Vertex "	...
...	Renewal of a circumscription quadrangle // the arbitrary circumscription quadrangles which can contain an arbitrary polygon
renewal of a circumscription quadrangle	G_End //Finally G_End is performed once,
G_End	

[operation at the time of applying this process to polygon]

When step1 is given, the result before processing and the result after processing are the same. Although this bug is not avoidable, it serves as maintenance of present condition.

When step2 is given, only the arbitrary polygon that drew at the last is drawn.

In that case, in order to draw the following arbitrary polygon correctly, it is necessary to have the flag cleared by application, since the flag of the arbitrary polygon drawn previously remains.

4. correction of hardware

This bug will be corrected at the time of the following revision.

APPENDIX 4 [timing of DREQ negate]

1. details of the bug

Even if it makes DREQ into negate-on mode, long WAIT will be occur in XRDY at the time of dual address DMA.

2. cause of the bug

Inside Scarlet just before a buffer becomes full, DREQ has been negated. However, negate of DREQ will be canceled if one data of DMA is transferred. (DREQ is asserted in the state of internal buffer full.) It causes this bug.

3. measure

- use local transfer.
- transfer using CPU write transfer, checking the opening of FIFO.
- do not perform drawing that requires long WAIT at the time of dual DMA.
- Please perform polling of CTR register all the time at the time of dual DMA use, and if FIFO is buried more than half, perform the mask of DREQ. (The byte write of 1 is performed to HostBase+0005h.) And release the mask if it becomes below a half.

4. correction of hardware

This bug will be corrected at the time of the following revision.

APPENDIX 5 [read of CTR register]

1. details of the bug

If CTR register is read at the time of local transfer, long WAIT times may occur.

2. cause of the bug

When CTR register is going to be read while carrying out drawing which has the generation of long-term WAIT inside, CTR is not read until drawing finishes. It causes this bug.

3. measure

- Please do not read CTR register during local transfer.
- When CTR needs to be read during local transfer, please read CTR after canceling CTR mirror. (The mirror can be canceled by writing 1 to HostBase+001ch. <undocumented register>)
- Please do not perform drawing which requires long-term WAIT at the time of dual DMA.
- Please perform polling of CTR register all the time at the time of dual DMA use, and if FIFO is buried more than half, perform the mask of DREQ. (The byte write of 1 is performed to HostBase+0005h) And release the mask if it becomes below a half.

4. correction of hardware

This bug will be corrected in the next revision.

APPENDIX 6 [drawing omission of DrawRectP and DrawBitmapP command]

1. details of the bug

The case where a triangle, a straight line, and a point are drawn by Scarlet rendering command is considered

- DrawPixel
- DrawPixelZ
- DrawLine
- DrawLine2i
- DrawLine2iP
- DrawTrap
- DrawVertex2i
- DrawVertex2iP

The above Rendering command is performed. And the following Rendering command is performed immediately after it.

- DrawRectP
- DrawBitmapP

In this case, drawing for number words of the drawing start place of ▪ DrawRectP DrawBitmapP ▪ may not be performed.

2. cause of the bug

In two PacketGroups of the above, the hardware which is actually taking charge of drawing is different. Therefore, the drawing change may not be performed pertinently. It causes this bug.

3. measure

When you perform Rendering command in the order of the above, please execute the command of DrawFlushFB before Rendering command of {DrawRectP DrawBitmapP}.

This phenomenon does not happen, when drawing a triangle, a straight line, and a point by using Scarlet geometry command.

Note : Scarlet Geometry command means the command which starts by G_Begin and is finished as G_End.

4. correction of hardware

This bug will be corrected at the time of the following revision.

APPENDIX 7 [initialization of W layer]

1. details of the bug

WYC bit of WM register(W layer) is not initialized by reset.

2. cause of the bug

This bug is based on lack of initialization logic.

3. measure

Please set up the register by HOST CPU. Usually, it is simultaneously performed at the time of setup of the W layer procedure.

4. correction of hardware

This bug will be corrected in next revision.