FUJITSU SEMICONDUCTOR
HARDWARE MANUAL

MB87P2020

Jasmine

Color LCD/CRT/TV Controller

Short specification

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Revision History

Version	Date	Remark
1.0	29. May 00	Initial Release
1.1	30. May 00	Electrical Specification added
1.2	06. June 00	Clock settings added
1.3	15. June 00	Some Buffer types added
1.4	20. June 00	Customer proposals included
1.5	28. June 00	DC section added
1.6	12. July 00	DC characteristics corrected
1.7	01. Nov. 00	Pinning for ULB data and address bus changed
1.8	28. Nov. 00	Clock chapter extended
1.9	18. Dec. 00	Some minor changes
2.0	08. Mar. 01	Completed feature comparison, command list, electrical specification. Added DRAM/APLL,/DAC supply, power on sequence, current consumption. Started AC specification.
2.1	30. Mar. 01	Detailed register and flag description added

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1 Overview

1.1 Application overview

The MB87P2020 *"Jasmine"* is a colour LCD/CRT graphic display controller (GDC) interfacing to MB91xxxx micro controller family and supports a wide range of display devices. The architecture is designed to meet the low cost, low power requirements in embedded and automotive applications. It is compatible to the "Lavender" GDC device and comes with 1MByte integrated video memory and additional features.

Jasmine supports almost all LCD panel types (digital or analog interface) and CRTs or other progressive scanned monitors/displays which can be connected via the analog RGB output. Products requiring digital camera input can take advantage of the supported direct digital video interface. The graphic instruction set is optimized for minimized traffic at the MCU interface because it's the most important performance issue of co-processing graphic acceleration systems.

The Jasmine is a graphic display controller especially for automotive applications. It supports a set of 2D drawing functions with built in Pixel Processor, a video scaler interface, units for physical and direct video memory access and a powerful video output stream formatter for a great variety of connectable displays.

Figure 1-1 displays an application block diagram in order to show the connection possibilities of Jasmine.

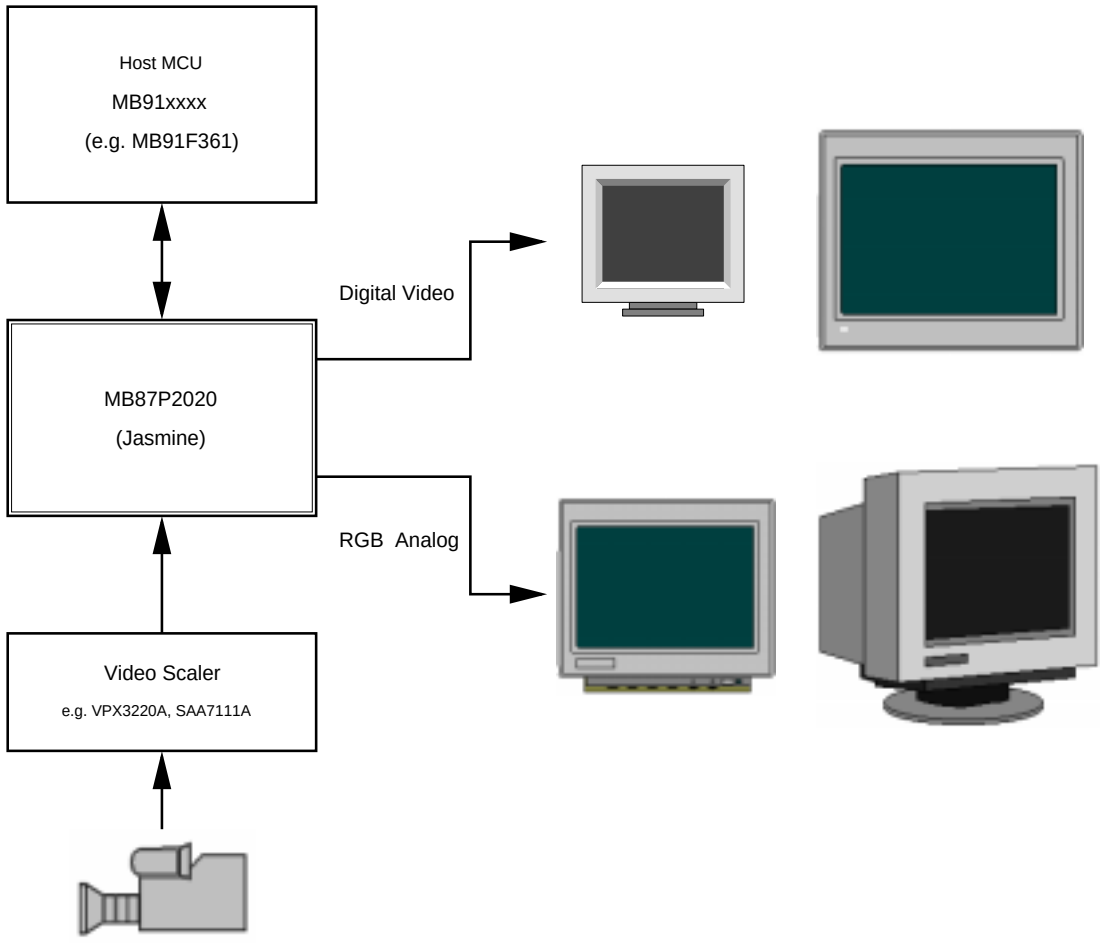


Figure 1-1: Jasmine application overview

1.2 Graphics Display Controller with embedded SDRAM

Figure 1-2 shows all main components of Jasmine graphics controller. The User Logic Bus controller (ULB), Clock Unit (CU) and Serial Peripheral Bus (SPB) are connected to the User Logic Bus interface of 32 bit Fujitsu RISC microprocessors. 32 and 16 bit access modes are supported.

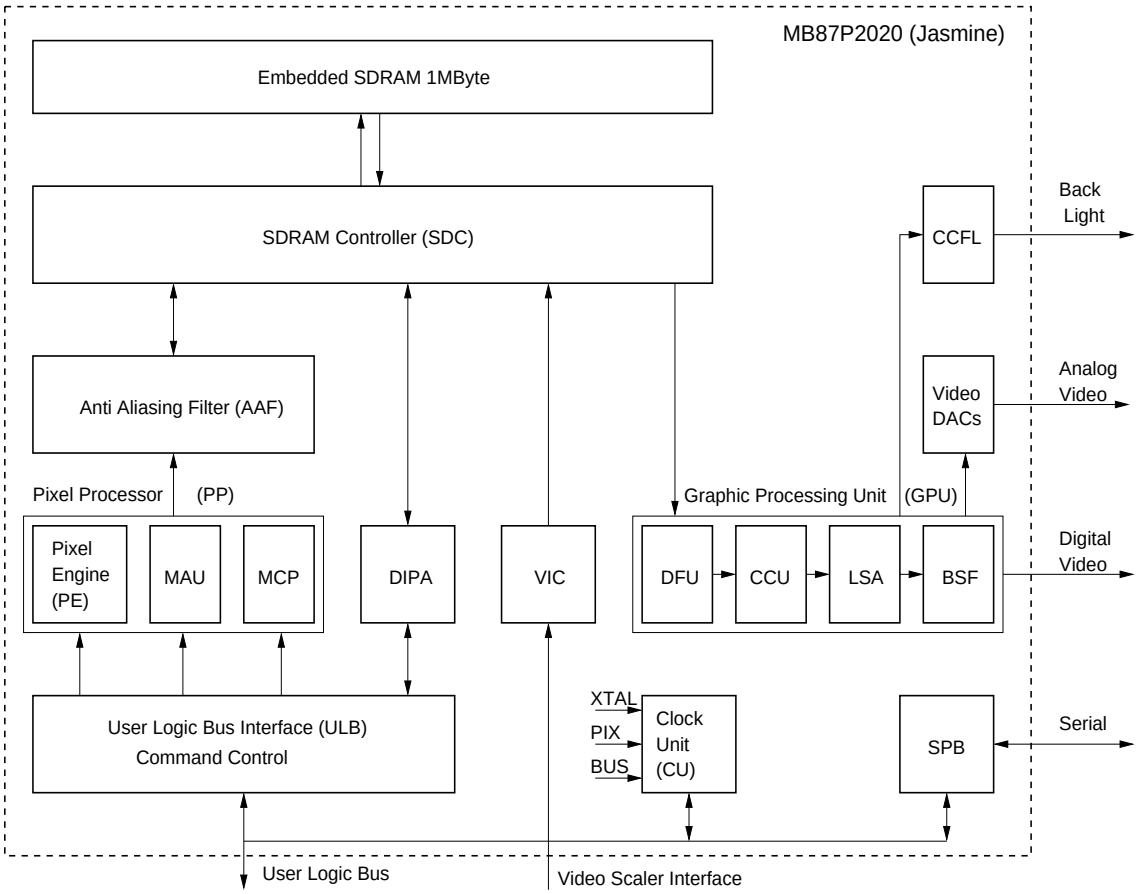


Figure 1-2: Component overview for Jasmine graphics controller

Table 1-1: Jasmine components

Shortcut	Meaning	Main Function
CCFL	Cold Cathode Fluorescence Lamp	Cold cathode driver for display backlight
CU	Clock Unit	Clock gearing supply, Power save
DAC	Digital Analog Converter	Digital analog conversation for analog display
DPA (part of DIPA)	Direct Physical memory Access	Memory mapped SDRAM access with address decoding
GPU	Graphics Processing Unit	Frame buffer reader which converts to video data required by display
DFU (part of GPU)	Data Fetch Unit	Video data acquisition

Table 1-1: Jasmine components

Shortcut	Meaning	Main Function
CCU (part of GPU)	Color Conversion Unit	Colour format conversion to common intermediate overlay format
LSA (part of GPU)	Line Segment Accumulator	Layer overlay
BSF (part of GPU)	BitStream Formatter	Intermediate format to physical display Format converter, Sync generation
IPA (part of DIPA)	Indirect Physical memory Access	Memory mapped SDRAM access with command register and FIFO
MAU (part of PP)	Memory Access Unit	Pixel access to SDRAM
MCP (part of PP)	Memory CoPy	Copying of pixel blocks
PE (part of PP)	Pixel Engine	Drawing of geometrical figures
PP	Pixel Processor	Handling of pixel based functions
SDC	SDRAM Controller	SDRAM controlling and arbitration
SPB	Serial Peripheral Bus	Serial interface (master)
ULB	User Logic Bus (see MB91360 series specification)	Address- and command decoding
VIC	Video Interface Controller	YUV-/RGB-Interface to video grabber

The ULB provides an interface to host MCU (MB91360 series). The main functions are MCU (User Logic Bus) control inclusive wait state handling, address decoding and device controls, data buffering / synchronisation between clock domains and command decoding. Beside normal data and command read and write operation it supports DMA flow control for full automatic data transfer from MCU to Jasmine and vice versa. Also an interrupt controlled data flow is possible and various interrupt sources inside the graphics controller can be programmed.

The Clock Unit (CU) provides all necessary clocks to module blocks of Jasmine and a FR compliant (ULB) interface to host MCU. Main functions are clock source select (XTAL, ULB clock, display clock), programmable clock multiplier/divider with APLL, power management for all Jasmine devices and the generation of synchronous RESET signal.

For Fujitsu internal purposes one independent macro is build in the Jasmine ASIC, the Serial Peripheral Bus (SPB). It’s a single line serial interface. There is no interaction with other Jasmine components.

All drawing functions will be executed in the Pixel Processor (PP). It consists of three main components Pixel Engine (PE), Memory Access Unit (MAU) and Memory Copy (MCP). All functions provided by these blocks are related to operations with pixel addresses {X, Y} possibly enhanced with layer information. Jasmine has 16 layers supported by hardware, four of them can be visible at the same time. Each layer is capable of storing any data type (graphic or video data with various colour depths) only restricted to the bandwidth limitation of video memory at a given operating frequency.

Drawing functions are executed in the PE by writing commands and their dedicated parameter sets. All commands can be taken from the command list in section 1.6. Writing of uncompressed and compressed bitmaps/textures, drawing of lines, poly-lines and rectangles are supported by the PE. There are many special modes such as duplicating data with a mirroring function.

Writing and reading of pixels in various modes is handled by MAU. Single transfers and block or burst transfers are possible. Also an exchange pixel function is supported.

With the MCP unit it is possible to transfer graphic blocks between layers of the same colour representation very fast. Only size, source and destination points have to be given to duplicate some picture data. So it offers an easy and fast way to program moving objects.

All PP image manipulation functions can be fed through an Antialiasing Filter (AAF). This slows down the drawing speed but is as much faster as a software realisation. Due to the algorithm shrinks the graphic size by two this has to be compensated by doubling the drawing parameters i.e. the co-ordinates of line endpoints.

DIPA stands for Direct/Indirect Physical Access. This unit handles rough video data memory access without pixel interpretation (frame buffer access). Depending on the colour depth (bpp, bit per pixel) one or more pixel are stored in one data word. DPA (Direct PA) is a memory-mapped method of physical access. It is possible in word (32 bit), half word (16 bit) or byte mode. The whole video memory or partial window (page) can be accessed in a user definable address area of Jasmine. IPA (Indirect PA) is controlled per ULB command interface and IPA access is buffered through the FIFOs to gain high access performance. It uses the command GetPA and PutPA, which are supporting burst accesses, possibly handled with interrupt and DMA control.

For displaying real-time video within the graphic environment Jasmine has a video interface for connection of video-scaler chips, e.g Intermetall's IC VPX32xx series or Phillips SAA711x. Additional the video input can handle CCIR standard conform digital video streams. Several synchronisation modes are implemented and work with frame buffering of one up to three pictures. With line doubling and frame repetition there exist a large amount of possibilities for frame rate synchronisation and interlaced to progressive conversion as well. Due to the strict timing of most graphic displays the input video rate has to be independent from the output format. So video data is stored as same principles as for graphic data using up to three of the sixteen layers.

The SDC is a memory controller, which arbitrates the internal modules and generates the required access timings for SDRAM devices. With a special address mapping and an optimized algorithm for generating control commands the controller can derive full benefit from internal SDRAM. This increases performance respective at random (non-linear) memory access.

The most complex part of Jasmine is its graphic data processing unit (GPU). It reads the graphic/video data from up to four layers from video memory and converts it to the required video output streams for a great variety of connectable display types. It consists of Data Fetch Unit (DFU), Color Conversion Unit (CCU) which comes with 512 words by 24-bit colour look up table, Line Segment Accumulator (LSA) which does the layer overlay and finally the Bitstream Formatter (BSF). The GPU has such flexibility for generating the data streams, video timings and sync signals to be capable of driving a great variety of known display types.

Additional to the digital outputs video DACs provides the ability to connect analog video destinations. A driver for the displays Cold Cathode Fluorescence Lamp (CCFL) makes the back light dimmable. It is synchronised with the vertical frequency of the video output to avoid visible artefacts during modulating the lamp.

1.3 Jasmine features and functions

Table 1-2: Lavender and Jasmine features in comparison

MB87J2120 (Lavender)	MB87P2020 (Jasmine)
General features	
• no **internal** SDRAM • 2M words x 32 Bit **external** SDRAM (64 Mbit)	• 256k words x 32 Bit **internal** SDRAM (8 Mbit)
• Package: BGA-256P-M01	• Package: FPT-208P-Mxx
• Chip select sharing for up to four GDC devices	no change
• synchronized reset (needs applied clock)	• immediate asynchronous reset, synchronized reset release
Pixel manipulation functions	
• 2D drawing and bitmap functions - Lines - Rectangular Area - Polygon - Uncompressed Bitmap - Compressed Bitmap (TGA format)	no change
• Pixel Memory Access Functions - Put Pixel - Put Pixel FC (fixed color) - Put Pixel Word (packed) - Exchange Pixel - Get Pixel	no change
• Layer Register for text and bitmap functions	• Layer Register for all drawing functions (simplifies pixel addressing)
• Copy rectangular areas between layers	no change
• Anti Aliasing Filter (AAF) - resolution increase by factor 2 for each dimension (2x2 filter operator)	• additional 4x4 AAF operator size
Display	
• Bitstream Formatter for a great variety of connectable display types (single/dual/alternate scan) • Free programmable display support for: - Passive Matrix LCD (single/dual scan) - Active Matrix (TFT) Displays - Electroluminescent Displays - Field Emission Displays - TV compatible output - CRTs...	• new Twin Display Mode feature (simultaneous digital and analog output without limitation of DIS_D[23:16] that carry special sync signals).

Table 1-2: Lavender and Jasmine features in comparison

MB87J2120 (Lavender)	MB87P2020 (Jasmine)
• 24 bit digital video output (RGB)	no change
• On-Chip Video DAC, 50M Samples/s (dot clock)	no change
• Flexible three-stage sync signal programming (trigger position/sequence, combining and delay) for up to 8 signal outputs	no change
• Colour keying between two limits	no change
• Brightness modulation for displays with a Cold Cathode Fluorescence Lamp back-light	no change
• Display resolution/drawing planes up to 16384 pixels for each dimension	no change
• 4 layer + background colour simultaneous display and graphic overlay, programmable Z-order • Blinking, transparency and background attributes	no change
• Free programmable display section of a layer	no change
• Separable Colour LUT with 256 entries x 24 Bit	• Colour LUT expansion to 512 entries
• Duty Ratio Modulation (DRM) for pseudo hue/ grey levels	no change
• Hardware support for 16 layers, usable for graphic/video without restrictions	no change
• Performance sharing with adjustable priorities and configurable block sizes for memory transfers enable maximal throughput for a wide range of applications	no change
• Variable and display independent colour space concept: Layers with 1, 2, 4, 8, 16, 24 bit per pixel can be mixed and converted to one display specific format (logical-intermediate-physical format mapping)	• YUV to RGB converter is included into GPU in order to allow YUV coded layers • Gamma correction RAMs are included (3x256x8Bit)
Physical SDRAM access	
• Memory mapped direct physical access for storage of non-graphics data or direct image access	no change
• Indirect physical memory access for high bandwidth multipurpose data/video memory access	no change

Table 1-2: Lavender and Jasmine features in comparison

MB87J2120 (Lavender)	MB87P2020 (Jasmine)
MCU interface	
• 32/16 Bit MCU interface, designed for direct connection of MB91xxxx family (8/16/32Bit access) • DMA support (all MB91xxxx modes) • Interrupt support	no change
Video interface	
• Video interface VPX32xx series by Micronas Intermetall, Phillips SAA711x and others	• additional CCIR conform input mode
• Video synchronization with up to 3 frame buffers	no change
Clock generation	
• Flexible clocking concept with on-chip PLL and up to 4 external clock sources • Clock sources: - XTAL - ULB bus clock - Pixel clock - Additional external clock pin (MODE[3])	• additional clock input dedicated RCLK pin instead of MODE[3]
• Separate power saving for each sub-module	no change

1.4 Clock supply and generation

1.4.1 Clock overview

Jasmine has a flexible clocking concept where four input clocks (OSC_IN/OUT, DIS_PIXCLK, ULB_CLK, RCLK) can be used as clock source for Core clock (CLKK) and Display clock (CLKD). A block diagram of clock distribution within Jasmine is shown in figure 1-3.

The user can choose by software whether to take the direct clock input or the output of an APLL independent for Core- and Display clock. Both output clocks have different dividers programmable by software (DIV x for CLKD and DIV z for CLKK). The clock gearing facilities offer the possibility to scale system performance and power consumption as needed.

Beside these two configurable clocks (CLKK and CLKD) Jasmine needs two additional internal clocks: CLKM and CLKV (see also figure 1-3).

CLKV is exclusively for video interface and is connected to input clock pin VSC_CLKV. CLKM is used for User Logic Bus (ULB) interface and is connected to input clock ULB_CLK. As already mentioned ULB_CLK can also be used to build CLKK and/or CLKD.

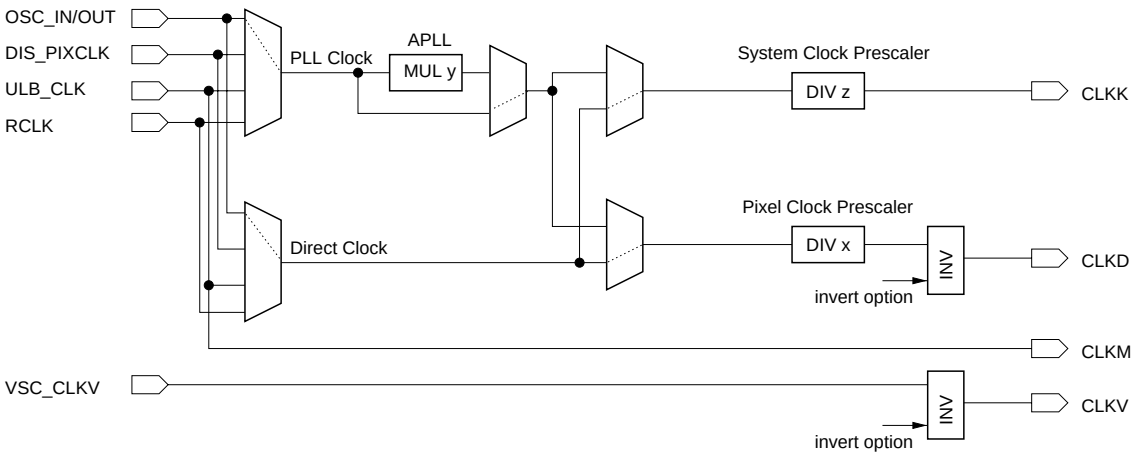


Figure 1-3: Clock gearing and distribution

Table 1-3 shows all clocks used by Jasmine with their requirements.

Table 1-3: Clock supply

Clock	Type	Symbol	Requirements			Unit
			Min	Typ	Max	
XTAL clock	input	OSC_IN, OSC_OUT	12	-	64	MHz
Direct clock	input	RCLK	ULB_CLK	-	64	MHz
ULB clock	input	ULB_CLK	-	-	64	MHz
Pixel clock	input	DIS_PIXCLK	-	-	54	MHz
Video clock	input	VSC_CLKV	-	-	54[a]	MHz
Core clock	internal	CLKK	ULB_CLK	-	64	MHz
Display clock	internal	CLKD	-	-	54	MHz
Video clock	internal	CLKV	-	-	54[a]	MHz
ULB clock	internal	CLKM	-	-	64	MHz

a. The video interface is designed to achieve 54 MHz but there is a side condition that video clock should be smaller than half of core clock.

1.5 Register overview

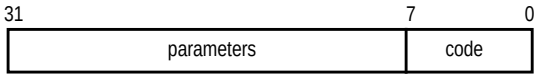
Table 1-4 contains an overview on Jasmine address ranges including decoding priority. The priority takes care about the controllability of Jasmine even for wrong memory settings.

Table 1-4: Register address space for Jasmine

Priority	Address range	Target component/Register
1	0x0000	Command register
	0x0004	Input FIFO
	0x0008	Output FIFO
	0x000C - 0x0020	Flag/Interrupt mask register
	0x0024 - 0x009B	ULB
	0x0100 - 0x0217	SDC
	0x1000 - 0x1243	GPU - LDR
	0x1300 - 0x1383	GPU - MDR
	0x1400 - 0x143B	GPU - MTX
	0x2000 - 0x23FF	GPU - CLUT
	0x2400 - 0x2FFF	GPU - GAMMA
	0x3000 - 0x3263	GPU - DIR
	0x3270	GPU - SDC
	0x4000 - 0x4023	VIC
	0x4100 - 0x4133	PP
	0x4200 - 0x420B	DIPA
	0x4400 - 0x4407	CCFL
	0x4500 - 0x450F	AAF
	0xFC00 - 0xFC07	CU
	0xFC08 - 0xFCFF	empty
	0xFD00 - 0xFD0F	SPB
	0xFD10 - 0xFFFF	empty
2	other Lavender/Jasmine chips	empty
3	SDRAM window1 range	SDRAM
4	SDRAM window0 range	SDRAM
5	Empty area within SDRAM space	empty

1.6 Command description

Jasmine command register width is 32 Bit. It is divided into command code and parameters:



Partial writing of command register is supported.

Not all commands need parameters. In these cases parameter section is ignored.

In table 1-5 all commands are listed with mnemonic, command code and command parameters (if necessary), command function, registers read by command, source and target for command data (separated by input and output data if necessary).

Table 1-5: Command List

Mnemonic	Code	Function	Registers	Data source	Data target
SwReset	00_H	stop command mode of Pixel-Engine and reset FIFO addressing	-	-	-
PutBM	01_H	store “Bit-Map” data in V-RAM; start at $\{X_{min},Y_{min}\}$, stop at $\{X_{max},Y_{max}\}$ Parameter: Bitmap color data $n = (X_{max} - X_{min}+1) * (Y_{max}-Y_{min}+1) * bpp / 32$ I/O-control: RDY-signal, busy-flag, prog. interrupt Optional: DMA input FIFO flow control	target layer icolor icolor_en $\{X_{min},Y_{min}\}$ $\{X_{max},Y_{max}\}$ direction mirror	I-FIFO ([color data]n)	Video RAM
PutCP	02_H	store compressed data (run-length coded) in V-RAM; start at $\{X_{min},Y_{min}\}$, stop at $\{X_{max},Y_{max}\}$ Parameter: run length coded data $n = (X_{max} - X_{min}+1) * (Y_{max} - Y_{min}+1)$ * compression factor I/O-control: RDY-signal, busy-flag, prog. interrupt Optional: DMA input FIFO flow control	target layer icolor icolor_en $\{X_{min},Y_{min}\}$ $\{X_{max},Y_{max}\}$ direction mirror	FIFO ([coded data]n)	Video RAM

Table 1-5: Command List

Mne-monic	Code	Function	Registers	Data source	Data target
DwLine	03_H	"Draw a Line" calculate pixel data and store into V-RAM Parameter: line start point $\{X_{start}, Y_{start}\}$ line end point $\{X_{end}, Y_{end}\}$ I/O-control: RDY-signal, busy-flag, interrupt Optional: DMA input FIFO flow control	target layer if enabled, lcolor	I-FIFO ([{X_{start}, Y_{start}}, {X_{end}, Y_{end}}]+)	Video RAM
DwRect	04_H	"Draw an Area (rectangle)" calculate pixel data and store into V-RAM Parameter: rectangle start point $\{X_{start}, Y_{start}\}$ rectangle end point $\{X_{end}, Y_{end}\}$ I/O-control: RDY-signal, busy-flag, interrupt Optional: DMA input FIFO flow control	target layer if enabled, rcolor	I-FIFO ([{X_{start}, Y_{start}}, {X_{end}, Y_{end}}]+)	Video RAM
PutTxtBM	05_H	Draw uncompressed pixel with fixed foreground and background color Parameter: Color enable data n = (X_{max} - X_{min}+1) * (Y_{max} - Y_{min}+1)/ 32 I/O-control: RDY-signal, busy-flag, interrupt Optional: DMA input FIFO flow control	target layer $\{X_{min}, Y_{min}\}$ $\{X_{max}, Y_{max}\}$ fcolor bcolor bcolor_en[a] direction mirror	I-FIFO ([color enable data]n)	Video RAM
PutTxtCP	06_H	Draw compressed pixel with fixed foreground and back-ground color Parameter: run length coded data n = (X_{max} - X_{min}+1) * (Y_{max} - Y_{min}+1) * compression factor / 32 I/O-control: RDY-signal, busy-flag, interrupt Optional: DMA input FIFO flow control	target layer $\{X_{min}, Y_{min}\}$ $\{X_{max}, Y_{max}\}$ fcolor bcolor bcolor_en[a] direction mirror	I-FIFO ([coded data]n)	Video RAM

Table 1-5: Command List

Mne-monic	Code	Function	Registers	Data source	Data target
PutPixel	07H	store pixel data in V-RAM Parameter: pixel coordinates {X,Y} color data for one pixel (right-aligned) I/O-control: RDY-signal, busy-flag, prog. inter-rupt Optional: DMA input FIFO flow control		I-FIFO ([{X,Y}, single color data]+)	Video RAM
PutPxWd	08H	store pixel word data in V-RAM word count = pixel count / bpp Parameter: pixel coordinates of first pixel {X,Y} color data word for layer bpp I/O-control: RDY-signal, busy-flag, prog. inter-rupt Optional: DMA input FIFO flow control		I-FIFO ([{X,Y}, color data]+)	Video RAM
PutPxFC	09H	store pixel data in V-RAM with fixed color Parameter: pixel coordinates {X,Y} I/O-control: RDY-signal, busy-flag, prog. inter-rupt Optional: DMA input FIFO flow control	pcolor	I-FIFO ([{X,Y}]+)	Video RAM
GetPixel	0AH	load pixel data from V-RAM Parameter: pixel coordinates {X,Y} Return: color data for one pixel (right-aligned) I/O-control: RDY-signal, busy-flag, prog. inter-rupt Optional: DMA input and output FIFO flow control		I-FIFO ({X,Y}+) Video RAM	Control O-FIFO ([single color data]+)

Table 1-5: Command List

Mne-monic	Code	Function	Registers	Data source	Data target
XChPixel	$0B_H$	store pixel data in V-RAM and load old pixel data in output FIFO Parameter: pixel coordinates {X,Y} Return: old color data for one pixel (right aligned) I/O-control: RDY-signal, busy-flag, prog. inter-rupt Optional: DMA input and output FIFO flow control		I-FIFO ([{X,Y}, single color data]+)	Control
				Video RAM	O-FIFO ([single color data]+)
MemCP	$0C_H$	Copy rectangular region from one layer to another Parameter: source start point $\{X_{Smin}, Y_{Smin}\}$, with source layer information (L_S) source end point $\{X_{Smax}, Y_{Smax}\}$ target start point $\{X_{Tmin}, Y_{Tmin}\}$ with target layer information L_T I/O-control: RDY-signal, busy-flag, interrupt Optional: DMA input FIFO flow control		I-FIFO ([{X_{Smin},Y_{Smin}, L_S}, {X_{Smax}, Y_{Smax}}, {X_{Tmin},Y_{Tmin}, L_T}]+)	Video RAM
PutPA	$0D_H$	store data in V-RAM directly with address auto-increment Parameter: physical address, data words I/O-control: RDY-signal, busy-flag, prog. inter-rupt Optional: DMA input FIFO flow control	-	I-FIFO (physical address, [data word]+)	Video RAM

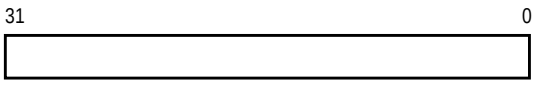
Table 1-5: Command List

Mne-monic	Code	Function	Registers	Data source	Data target
GetPA	{n, $0E_H$}	load data from V-RAM with address auto-increment, stop after n. words Parameter: physical start address, number of words to be read (n) Return: n data words I/O-control: RDY-signal, busy-flag, prog. interrupt Optional: DMA output FIFO flow control	-	I-FIFO (physical start address)	Control
				Video RAM	O-FIFO ([data word]n)
DwPoly	$0F_H$	'Draw a Polygon' calculate pixel data and store into V-RAM Parameter: line start point {X_{start},Y_{start}} (first point only) line end point {X_{end},Y_{end}} (start point is endpoint of previous pixel) I/O-control: RDY-signal, busy-flag, interrupt Optional: DMA input FIFO flow control	target layer if enabled, plcolor	I-FIFO ({X_{start},Y_{start}}, [{X_{end},Y_{end}}]+)	Video RAM
NoOp	FF_H	no operation	-	-	-

a.If bcolor_en=0 at a PutTxtBM or PutTxtCP command only foreground pixels are transferred to video memory. This mode requires closing processing queue by a NoOp-SwReset sequence before using the next command.

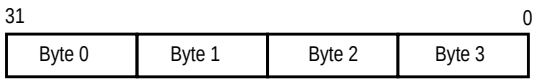
Legend, symbols from command list table:

- physical byte address

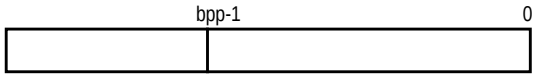


Note: Depending on video memory size not all addresses are used.

- data word

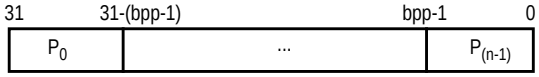


- single color data



bpp...24, 16, 8, 4, 2, 1 Bit

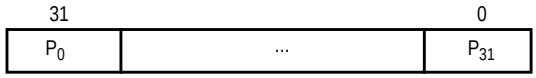
- color data



bpp...24, 16, 8, 4, 2, 1 Bit
n...count of pixel per word

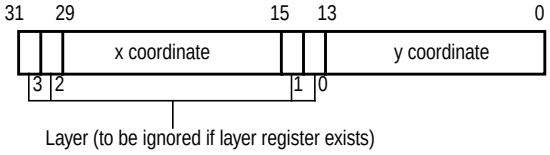
bpp	n
24	1
16	2
8	4
4	8
2	16
1	32

- color enable data



(...)	Source or Target FIFO data
[...]n	Deliver data in '[...]' n times
[...]+	Deliver data in '[...]' at least one time

- {X,Y} Pixel coordinates



2 Pinning and Buffer Types

2.1 Pinning

Table 2-1: Jasmine pinning

Pin	Name	Buffer type	Description
1	MODE[0]	BFNNQLX	Mode Pin
2	MODE[1]	BFNNQLX	Mode Pin
3	GND	GND	
4			Place holder for analog area
5	A_GREEN	OTAMX	Analog Green
6	DAC2_VSSA1	ITAVSX	DAC Ground
7	DAC2_VDDA1	ITAVDX	DAC Supply 2.5V
8	A_BLUE	OTAMX	Analog Blue
9	DAC1_VDDA1	ITAVDX	DAC Supply 2.5V
10	DAC1_VSSA1	ITAVSX	DAC Ground
11	A_VRO	OTAMX	DAC Full Scale Adjust
12	DAC1_VSSA	ITAVSX	DAC Ground
13	DAC1_VDDA	ITAVDX	DAC Supply 2.5V
14	A_RED	OTAVX	Analog Red
15	DAC3_VDDA1	ITAVDX	DAC Supply 2.5V
16	DAC3_VSSA1	ITAVSX	DAC Ground
17	VREF	ITAMX	DAC test pin VREF
18			Place holder for analog area
19	VDDI	VDDI#	Core supply 2.5 V
20	TEST	ITCHX	Fujitsu test pin
21	VSC_CLKV	ITFHX	Video Scaler Clock
22	RESETX	ITFUHX	Reset (pull up)
23	OSC_OUT	YB002AAX	XTAL output
24	VDDE[0]		IO supply 3.3V
25	OSC_IN	YI002AEX	XTAL input
26	GND	GND	
27	VDDI	VDDI#	Core supply 2.5 V
28	RDY_TRIEN	B3NNLMX	Control RDY pin behaviour
29	APLL_AVDD		APLL supply 2.5V

Table 2-1: Jasmine pinning

Pin	Name	Buffer type	Description
30	APLL_AVSS		APLL GND
31	RCLK	ITFHX	Reserved clock
32	ULB_A[20]	BFNNQLX	ULB Interface Address
33	ULB_A[19]	BFNNQLX	ULB Interface Address
34	VDDI	VDDI#	Core supply 2.5 V
35	ULB_A[18]	BFNNQLX	ULB Interface Address
36	ULB_A[17]	BFNNQLX	ULB Interface Address
37	ULB_A[16]	BFNNQLX	ULB Interface Address
38	GND	GND	GND
39	ULB_A[15]	BFNNQLX	ULB Interface Address
40	ULB_A[14]	BFNNQLX	ULB Interface Address
41	ULB_A[13]	BFNNQLX	ULB Interface Address
42	ULB_A[12]	BFNNQLX	ULB Interface Address
43	VDDE	VDDE#	IO supply 3.3V
44	ULB_CLK	ITFHX	ULB Interface Clock
45	ULB_A[11]	BFNNQLX	ULB Interface Address
46	ULB_A[10]	BFNNQLX	ULB Interface Address
47	ULB_A[9]	BFNNQLX	ULB Interface Address
48	ULB_A[8]	BFNNQLX	ULB Interface Address
49	ULB_A[7]	BFNNQLX	ULB Interface Address
50	GND	GND	GND
51	ULB_A[6]	BFNNQLX	ULB Interface Address
52	ULB_A[5]	BFNNQLX	ULB Interface Address
53	ULB_A[4]	BFNNQLX	ULB Interface Address
54	ULB_A[3]	BFNNQLX	ULB Interface Address
55	ULB_A[2]	BFNNQLX	ULB Interface Address
56	ULB_A[1]	BFNNQLX	ULB Interface Address
57	ULB_A[0]	BFNNQLX	ULB Interface Address
58	ULB_CS	BFNNQLX	ULB Interface Chip Select
59	ULB_RDX	BFNNQLX	ULB Interface Read
60	GND	GND	GND
61	VDDE	VDDE#	IO supply 3.3V
62	ULB_DACK	BFNNQLX	ULB Interface DMA Acknowledge

Table 2-1: Jasmine pinning

Pin	Name	Buffer type	Description
63	ULB_D[31]	BFNNQMX	ULB Interface Data
64	ULB_D[30]	BFNNQMX	ULB Interface Data
65	ULB_D[29]	BFNNQMX	ULB Interface Data
66	GND[1]		GND
67	VDDE[1]		IO supply 3.3V
68	ULB_D[28]	BFNNQMX	ULB Interface Data
69	ULB_D[27]	BFNNQMX	ULB Interface Data
70	ULB_D[26]	BFNNQMX	ULB Interface Data
71	ULB_D[25]	BFNNQMX	ULB Interface Data
72	GND	GND	GND
73	VDDI	VDDI#	Core supply 2.5 V
74	VDDE[2]		IO supply 3.3V
75	ULB_D[24]	BFNNQMX	ULB Interface Data
76	ULB_D[23]	BFNNQMX	ULB Interface Data
77	ULB_D[22]	BFNNQMX	ULB Interface Data
78	ULB_D[21]	BFNNQMX	ULB Interface Data
79	VDDI	VDDI#	Core supply 2.5 V
80	GND[2]		GND
81	ULB_D[20]	BFNNQMX	ULB Interface Data
82	ULB_D[19]	BFNNQMX	ULB Interface Data
83	ULB_D[18]	BFNNQMX	ULB Interface Data
84	ULB_D[17]	BFNNQMX	ULB Interface Data
85	GND	GND	GND
86	VDDI	VDDI#	Core supply 2.5 V
87	ULB_D[16]	BFNNQMX	ULB Interface Data
88	ULB_D[15]	BFNNQMX	ULB Interface Data
89	ULB_D[14]	BFNNQMX	ULB Interface Data
90	ULB_D[13]	BFNNQMX	ULB Interface Data
91	GND[3]		GND
92	VDDE[3]		IO supply 3.3V
93	ULB_D[12]	BFNNQMX	ULB Interface Data
94	ULB_D[11]	BFNNQMX	ULB Interface Data
95	ULB_D[10]	BFNNQMX	ULB Interface Data

Table 2-1: Jasmine pinning

Pin	Name	Buffer type	Description
96	GND	GND	GND
97	VDDE	VDDE#	IO supply 3.3V
98	ULB_D[9]	BFNNQMX	ULB Interface Data
99	ULB_D[8]	BFNNQMX	ULB Interface Data
100	ULB_D[7]	BFNNQMX	ULB Interface Data
101	ULB_D[6]	BFNNQMX	ULB Interface Data
102	VDDE[4]		IO supply 3.3V
103	GND[4]		GND
104	ULB_D[5]	BFNNQMX	ULB Interface Data
105	ULB_D[4]	BFNNQMX	ULB Interface Data
106	ULB_D[3]	BFNNQMX	ULB Interface Data
107	GND	GND	GND
108	ULB_D[2]	BFNNQMX	ULB Interface Data
109	VDDE[5]		IO supply 3.3V
110	SDRAM_VCC[0]		SDRAM supply 2.5V
111	ULB_D[1]	BFNNQMX	ULB Interface Data
112	ULB_D[0]	BFNNQMX	ULB Interface Data
113	GND[5]		GND
114	VDDE	VDDE#	IO supply 3.3V
115	SDRAM_VCC[1]		SDRAM supply 2.5V
116	ULB_RDY	OTFTQMX	ULB Interface Ready
117	ULB_DSTP	BFNNQMX	ULB Interface DMA Stop
118	SDRAM_VCC[2]		SDRAM supply 2.5V
119	GND	GND	GND
120	ULB_DREQ	OTFTQMX	ULB Interface DMA Request
121	ULB_INTRQ	OTFTQMX	ULB Interface Interrupt Request
122	ULB_WRX[0]	ITFHX	ULB Interface Write Enable (D[31:24])
123	VDDI	VDDI#	Core supply 2.5 V
124	ULB_WRX[1]	ITFHX	ULB Interface Write Enable (D[23:16])
125	SDRAM_VCC[3]		SDRAM supply 2.5V
126	ULB_WRX[2]	ITFHX	ULB Interface Write Enable (D[15:8])
127	ULB_WRX[3]	ITFHX	ULB Interface Write Enable (D[7:0])
128	SDRAM_PBI	IPBIX	SDRAM Test mode

Table 2-1: Jasmine pinning

Pin	Name	Buffer type	Description
129	VDDE[7]		IO supply 3.3V
130	GND	GND	GND
131	VDDI	VDDI#	Core supply 2.5 V
132	SDRAM_TBST	ITBSTX	SDRAM test mode
133	SDRAM_TTST	ITTSTX	SDRAM test mode
134	VPD	VPDX	Fujitsu Tester Pin
135	DIS_D[0]	B3NNLMX	Display Data
136	DIS_D[1]	B3NNLMX	Display Data
137	DIS_D[2]	B3NNLMX	Display Data
138	VDDI	VDDI#	Core supply 2.5 V
139	DIS_D[3]	B3NNLMX	Display Data
140	DIS_D[4]	B3NNLMX	Display Data
141	DIS_D[5]	B3NNLMX	Display Data
142	GND	GND	GND
143	DIS_D[6]	B3NNLMX	Display Data
144	DIS_D[7]	B3NNLMX	Display Data
145	DIS_D[8]	B3NNLMX	Display Data
146	DIS_D[9]	B3NNLMX	Display Data
147	VDDE	VDDE#	IO supply 3.3V
148	DIS_D[10]	B3NNLMX	Display Data
149	DIS_D[11]	B3NNLMX	Display Data
150	DIS_D[12]	B3NNLMX	Display Data
151	DIS_D[13]	B3NNLMX	Display Data
152	DIS_D[14]	B3NNLMX	Display Data
153	DIS_D[15]	B3NNLMX	Display Data
154	GND	GND	GND
155	VDDE[8]		IO supply 3.3V
156	DIS_D[16]	B3NNLMX	Display Data
157	DIS_D[17]	B3NNLMX	Display Data
158	DIS_D[18]	B3NNLMX	Display Data
159	DIS_D[19]	B3NNLMX	Display Data
160	DIS_D[20]	B3NNLMX	Display Data
161	DIS_D[21]	B3NNLMX	Display Data

Table 2-1: Jasmine pinning

Pin	Name	Buffer type	Description
162	DIS_D[22]	B3NNLMX	Display Data
163	DIS_D[23]	B3NNLMX	Display Data
164	GND	GND	GND
165	VDDE	VDDE#	IO supply 3.3V
166	DIS_CKEY	B3NNLMX	Display Colour Key
167	DIS_PIXCLK	B3NNNMX	Display Pixel Clock (programmable in/out)
168	DIS_VSYNC	B3NNLMX	Display programmable sync
169	DIS_HSYNC	B3NNLMX	Display programmable sync
170	DIS_VREF	B3NNLMX	Display programmable sync
171	VSC_D[0]	BFNNQLX	Video Scaler Data Input
172	VSC_D[1]	BFNNQLX	Video Scaler Data Input
173	VSC_D[2]	BFNNQLX	Video Scaler Data Input
174	VSC_D[3]	BFNNQLX	Video Scaler Data Input
175	VSC_D[4]	BFNNQLX	Video Scaler Data Input
176	GND	GND	GND
177	VDDI	VDDI#	Core supply 2.5 V
178	VDDE[9]		IO supply 3.3V
179	MODE[2]	BFNNQLX	Mode Pin
180	MODE[3]	BFNNQLX	Mode Pin
181	VSC_D[5]	BFNNQLX	Video Scaler Data Input
182	VSC_D[6]	BFNNQLX	Video Scaler Data Input
183	VDDI	VDDI#	Core supply 2.5 V
184	VSC_D[7]	BFNNQLX	Video Scaler Data Input
185	VSC_D[8]	BFNNQLX	Video Scaler Data Input
186	VSC_D[9]	BFNNQLX	Video Scaler Data Input
187	VSC_D[10]	BFNNQLX	Video Scaler Data Input
188	VSC_D[11]	BFNNQLX	Video Scaler Data Input
189	GND	GND	GND
190	VDDI	VDDI#	Core supply 2.5 V
191	VSC_D[12]	BFNNQLX	Video Scaler Data Input
192	VSC_D[13]	BFNNQLX	Video Scaler Data Input
193	VSC_D[14]	BFNNQLX	Video Scaler Data Input
194	VSC_D[15]	BFNNQLX	Video Scaler Data Input

Table 2-1: Jasmine pinning

Pin	Name	Buffer type	Description
195	VSC_VREF	BFNNQLX	Video Scaler Vertical Reference
196	VSC_VACT	BFNNQLX	Video Scaler VACT
197	VSC_ALPHA	BFNNQLX	Video Scaler ALPHA
198	VSC_IDENT	BFNNQLX	Video Scaler Field identification
199	SPB_BUS	BFNNQHX	SPB Interface
200	GND	GND	GND
201	VDDE	VDDE#	IO supply 3.3V
202	SPB_TST	BFNNQHX	SPB Test
203	CCFL_FET2	OTFTQMX	CCFL FET driver
204	CCFL_FET1	OTFTQMX	CCFL FET driver
205	CCFL_IGNIT	OTFTQMX	CCFL supply control IGNITION
206	GND[6]		GND
207	VDDE[10]		IO supply 3.3V
208	CCFL_OFF	OTFTQMX	CCFL supply control OFF

2.2 Buffer Types

Table 2-2: Buffer types for Jasmine

Buffer type	Description
B3NNLMX	Bidirectional True buffer (3.3V CMOS, IOL=4mA,Low Noise type)
BFNNQHX	Bidirectional True buffer (5V Tolerant, IOL=8mA, High speed type)
BFNNQLX	Bidirectional True buffer (5V Tolerant, IOL=2mA, High speed type)
BFNNQMX	5V tolerant, bidirectional true buffer 3.3V CMOS, IOL/IOH=4mA
IPBIX	Input True Buffer for DRAM TEST (2.5V CMOS with 25K Pull-up) (SDRAM test only)
ITAMX	Analog Input buffer
ITAVDX	Analog Power Supply
ITAVSX	Analog GND
ITBST	Input True Buffer for DRAM TEST (2.5V CMOS with 25K Pull-down) (SDRAM test only)
ITCHX	Input True buffer (2.5V CMOS)
ITFHX	5V tolerant 3.3V CMOS Input
ITFUHX	5V tolerant 3.3V CMOS Input, 25 k Pull-up
ITTSTX	Input True buffer for DRAM TEST Control (2.5V CMOS with 25K Pull-down)

Table 2-2: Buffer types for Jasmine

Buffer type	Description
OTAMX	Analog Output
OTFTQMX	5 V tolerant 3.3V tri-state output, IOL/IOH=4mA
VPDX	3.3V CMOS input, disable input for Pull up/down resistors, connect to GND
YB002AAX	Oscillator Output
YI002AEX	Oscillator Pin Input

3 Electrical Specification

3.1 Maximum Ratings

The maximum ratings are the limit values that must never be exceeded even for an instant. As long as the device is used within the maximum ratings specified range, it will never be damaged.

The Cx71 series of CMOS ASICs has five types of output buffers for driving current values, each of which has a different maximum output current rating.

Table 3-1: Maximum Ratings

Parameter	Symbol	Requirements	Unit
Supply voltage	VDDI VDDE SDRAM_VCC APLL_AVDD DAC_VDDA	-0.5 to +3.0 -0.5 to +4.0 VDDI VDDI -0.5 to +3.0	V
Input voltage	VI	-0.5 to VDD + 0.5 (<= 4.0V)[a] -0.5 to VDDE + 4.0 (<= 6.0V)[b]	V
Output voltage	VO	-0.5 to VDD +0.5 (<= 4.0V)[a] -0.5 to VDDE + 4.0[b] <L/H- State> -0.5 to VDDE + 4.0 (<= 6.0V)[b] <Z- State>	V
Storage temperature	TST	-55 to +125	˚C
Junction temperature	Tj	-40 to +125	
Ambient temperature	Ta	-40 to +85	
Output current[c]	IO	+/-13	mA
Supply pin current for one VDD/GND pin	ID	60	mA

a.for 3.3V interface
b.for 5.0V tolerant
c.The maximum output current which always flows in the circuit.

3.1.1 Power-on sequence

Jasmine is a dual power supply device. For power ON/OFF sequence, there is no specific restriction, but the following sequences are recommended:

Power-ON: VDDI (internal, 2.5V) -> VDDE (external, 3.3V) -> Signal

Power-OFF: Signal -> VDDE (external, 3.3V) -> VDDI (internal, 2.5V)

It is restricted that VDDE only is supplied continuously for more than 1 minute while VDDI/DRAM supply is off. If the time exceeds 1 minute, it may affect the reliability of the internal transistors.

When VDDE is changed from off to on, the internal state of the circuit may not be maintained due to the noise by power supply. Therefore, the circuit should be initialized after power is on.

3.1.2 External Signal Levels

External signal levels must not be higher than power supply voltage by 0.5V or more (3.3V inputs). If a signal with 0.5V or more than VDDE is given to an input buffer the current will flow internally to supply, which can give a permanent damage to the LSI.

In addition, when power supply becomes on or off, signal levels must not be higher than the power supply voltage by 0.5V or more. This means that signals must not be applied before power on / after power off.

If an external signal (5V) is input at a 5V tolerant input before the device in question is powered-on, it will give the LSI a permanent damage.

3.1.3 APLL Power Supply Level

APLL (Analog PLL) power supply level must not be higher than power supply voltage VDDI. Please take care of APLL power supply not to be over VDDI level at Power ON/OFF sequence.

3.1.4 DAC supply

DAC supply is isolated from other 2.5V supply.

3.1.5 SDRAM Supply

SDRAM supply must be as same level as VDDI.

3.2 Recommended Operating Conditions

The recommended operating conditions are the recommended values for assuring normal logic operation.

As long as the device is used within the recommended operating conditions, the electrical characteristics described below are assured.

Table 3-2: Operating conditions

Parameter		Symbol	Requirements			Unit
			Min	Typ	Max	
Supply voltage		VDDE	3.0	3.3	3.6	V
		VDDI	2.3	2.5	2.7	
		DAC_VDDA	2.3	2.5	2.7	
High-level input voltage	3.3V	VIH	2.0	-	VDDE+ 0.3	V
	5V Tolerant		2.0	-	5.5	
Low-level input voltage	3.3V	VIL	-0.3	-	0.8	V
	5V Tolerant		-0.3	-	0.8	
Junction temperature		Tj	-40	-	125	˚C
Ambient temperature		Ta	-40	-	85	˚C

3.3 DC Characteristics

The DC characteristics assure the worst values of the static characteristics of input/output buffers within the range specified at the recommended operating conditions.

Table 3-3: DC characteristics

Parameter	Symbol	Test conditions	Requirements			Unit
			Min	Typ	Max	
Supply current[a b]	IDDS	ASIC master type T7	-	-	0.2	mA
High-level output voltage	VOH	IOH= -100uA	VDDE-0.2	-	VDDE	V
Low-level output voltage	VOL	IOL= 100uA	0	-	0.2	V
High-level output current	IOH	L type VOH=VDDE- 0.4V	-2	-	-	mA
		M type VOH=VDDE- 0.4V	-4	-	-	mA
		H type VOH=VDDE- 0.4V	-8	-	-	mA

Table 3-3: DC characteristics

Parameter	Symbol	Test conditions	Requirements			Unit
			Min	Typ	Max	
Low-level output current	IOL	L type VOL=0.4V	2.0	-	-	mA
		M type VOL=0.4V	4.0	-	-	mA
		H type VOL=0.4V	8.0	-	-	mA
Input leakage current per pin[b]	IL		-	-	+/-5	uA
Input pull-up/ pull-down resistor[c]	RP		10	25	70	kOhm
Output short-circuit current[d]	IOS	L type	-	-	+/-40	mA
		M type	-	-	+/-60	mA
		H type	-	-	+/-120	mA

a.VIH = VDD and VIL = VSS, memory is in stand-by mode, Analog cells (APLL, DACs, DAC-VREF) are at power down mode, Tj = 25˚C
b.Input pins have to be static. If an input buffer with pull-up/pull-down resistor is used, the input leakage current may exceed the above value
c.Either a buffer without a resistor or with a pull-up/pull-down resistor can be selected from the input and bidirectional buffers.
d.Maximum supply current at the short circuit of output and VDD or VSS. For 1 second per pin.

Following table shows current/power consumption for Jasmine under special operating conditions. Core clock, which has most influence is varied over specified range. Please note, if other parameters varied that given values can be exceeded.

Table 3-4: Maximum core current consumption

Frequency [MHz]	APLL Divider/Multiplier Setup[a]	Core/Analog supply [mA]	DRAM supply [mA]	Power consumption [mW]
16	5 / 7	84.1	9.2 (3.8)[b]	360 (346)
20	5 / 9	104.4	11.5 (4.8)	421 (403)
36	6 / 20	180.7	20.7 (9.1)	652 (621)
48	5 / 23	232.4	27.6 (10.6)	811 (765)
64	2 / 15	294.0	36.8 (12.6)	1001 (936)

a.Values interpreted with n+1
b.Values for DRAM supply in parenthesis are measured while running an usual application.

Measurement conditions:

- Oscillator 12.0 MHz
- Video clock 13.5 MHz, Pixel Clock (display) 6.0 MHz, ULB_CLK 16 MHz
- VDDI = 2.7V, VDDE = 3.6V

- I/O current assumed 30 mA, this varies in given environments/applications. Part of I/O power consumtion was 30mA * 3.6V = 108mW (fixed within this mesurement environment).

3.4 AC Characteristics

3.4.1 Clock inputs

OSC_IN, OSC_OUT are dedicated ports for crystal oscillator connection. Hence OSC_IN may be used as direct clock input, then specification applies as stated for the other possible clock inputs.

ULB_CLK, RCLK, VSC_CLKV, DIS_PIXCLK give the ability to feed in external clock directly. For usage of different clock inputs see Clock Unit specification.

- DIS_PIXCLK can be configured as input or output

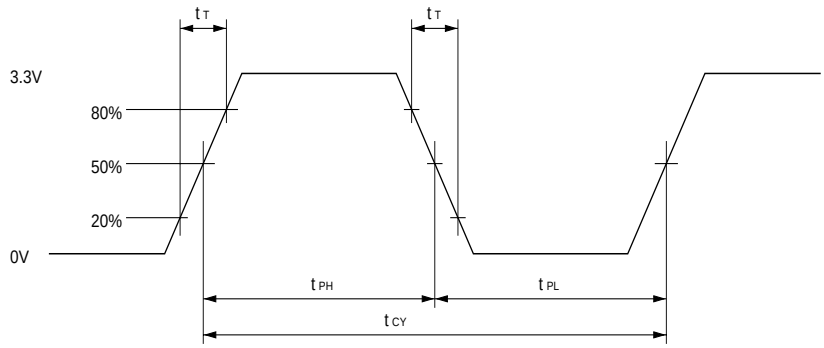


Figure 3-1: AC characteristics measurement conditions

- Transition Time t_T max. 2ns
- V_{IH} = 2.0V, V_{IL} = 0.8V (3.3V CMOS Interface Input)

Table 3-5: Timing Specification

Clock	Parameter	Symbol	Min	Max
ULB_CLK (routed to CLKM, MCU interface)	ULB Clock Cycle Time	t_{CYU}	15.625 ns	-
	ULB Clock High Pulse Width	t_{PHU}	7 ns	-
	ULB Clock Low Pulse Width	t_{PLU}	7 ns	-
RCLK (routed to CLKK, core clock without APLL)	RSV Clock Cycle Time	t_{CYR}	15.625 ns	-
	RSV Clock High Pulse Width	t_{PHR}	7 ns	-
	RSV Clock Low Pulse Width	t_{PLR}	7 ns	-
VSC_CLKV (video interface clock)	Video Clock Cycle Time	t_{CYV}	18.50 ns	-
	Video Clock High Pulse Width	t_{PHV}	9.25 ns	-
	Video Clock Low Pulse Width	t_{PLV}	9.25 ns	-

Table 3-5: Timing Specification

Clock	Parameter	Symbol	Min	Max
DIS_PIXCLK (routed to CLKD as external display clock)	Display Clock Cycle Time	t_{CYD}	18.50 ns	-
	Display Clock High Pulse Width	t_{PHD}	9.25 ns	-
	Display Clock Low Pulse Width	t_{PLD}	9.25 ns	-

3.4.2 MCU User Logic Bus Interface

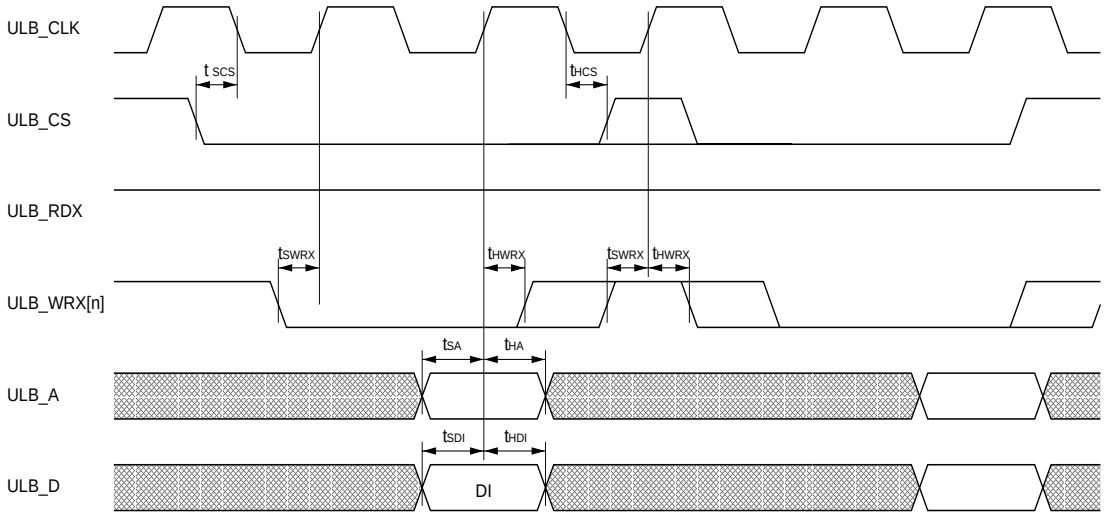


Figure 3-2: ULB write access (followed by another write)

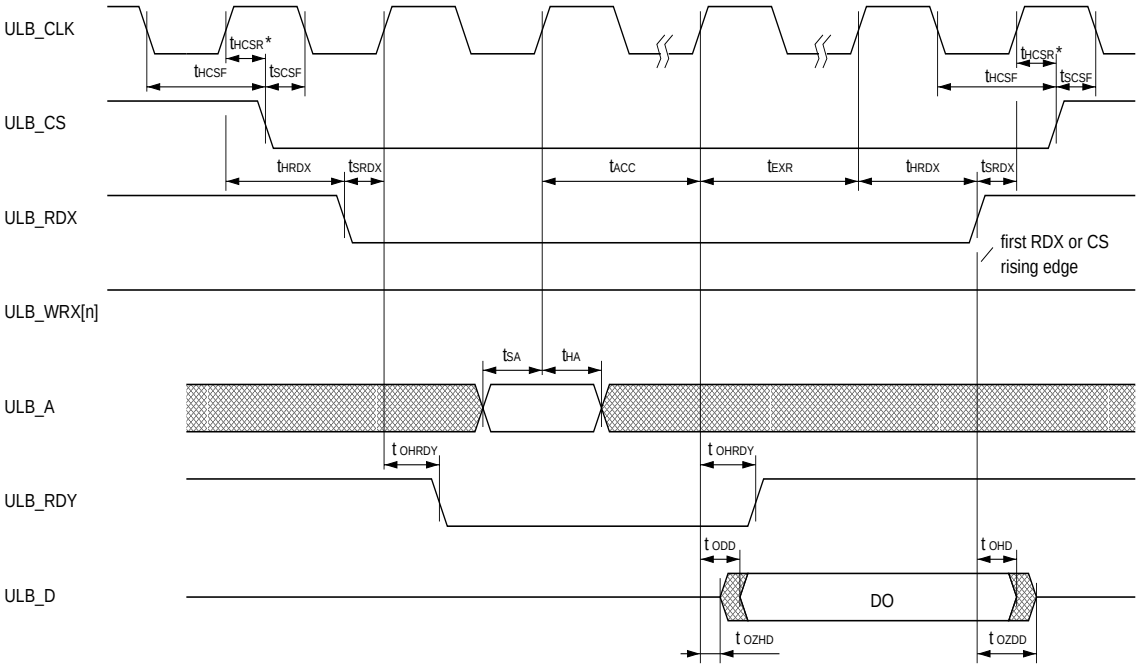


Figure 3-3: ULB read access

Table 3-6: Timing Specification

Parameter	Symbol	Min	Max
Chip Select Setup Time (falling)	t_{SCSF}	tbd	-
Chip Select Hold Time (falling)	t_{HCSF}	tbd	-
Chip Select Hold Time (rising)[a]	t_{HCSR}*	tbd	-
Read Setup Time	t_{SRDX}	tbd	-
Read Hold Time	t_{HRDX}	tbd	-
Write Setup Time	t_{SWRX}	tbd	-
Write Hold Time	t_{HWRX}	tbd	-
Address Setup Time	t_{SA}	tbd	-
Address Hold Time	t_{HA}	tbd	-
Input Data Setup Time	t_{SDI}	tbd	-
Input Data Hold Time	t_{HDI}	tbd	-
Ready Output Hold Time	t_{OHRDY}	tbd	tbd
Output Data Delay Time	t_{ODD}	tbd	tbd
Output Data Hold Time	t_{OHD}	tbd	tbd
Output Data Tri-state Hold Time	t_{OZHD}	tbd	tbd
Output Data Tri-state Delay Time	t_{OZDD}	tbd	tbd

Table 3-6: Timing Specification

Parameter	Symbol	Min	Max
Access Time	t_{ACC}	1 T_{ULB_CLK}	variable[b]
External Reaction Time	t_{EXR}	0 T_{ULB_CLK}	-

a.More restrictive specification to rising edge of CLK_ULB is only needed if SPB will be used.
b.Access time varies with whole number of ULB_CLK periods for different Jasmine register addresses.

3.4.3 Interrupt

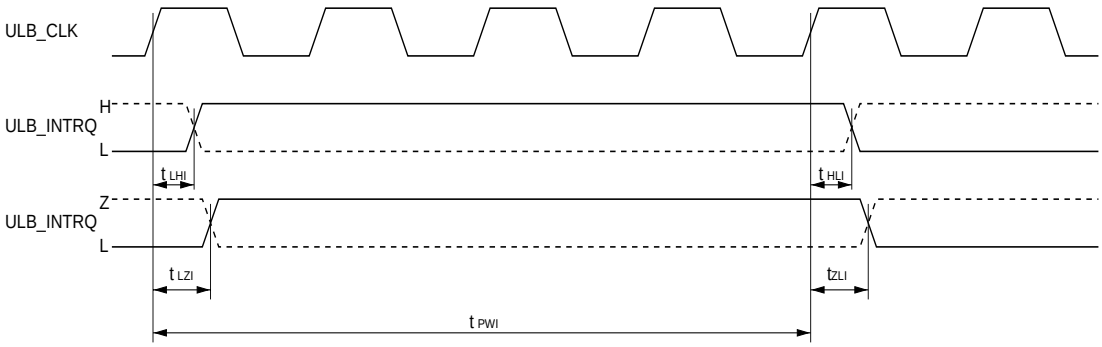


Figure 3-4: Interrupt output timing

Table 3-7:

Parameter	Symbol	Min	Max
Output delay time for LH edge	tLHI		
Output delay time for HL edge	tHLI		
Output delay time for LZ edge	tLZI		
Output delay time for ZL edge	tZLI		
Interrupt Pulse Width	tPWI		

3.4.4 DMA Control Ports

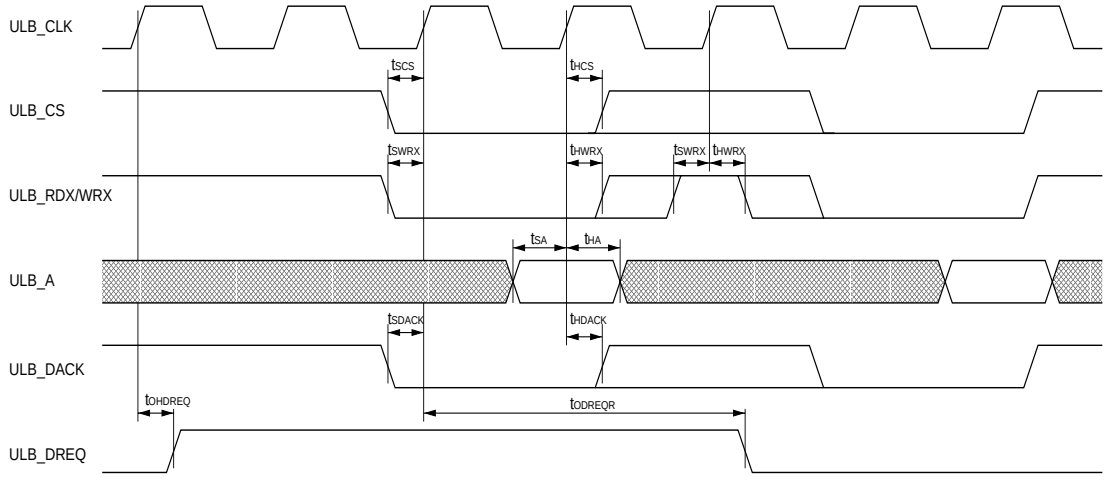


Figure 3-5: DMA block/burst access

3.4.5 Display Interface (Digital)

3.4.6 Display Interface (Analog)

3.4.7 Video Input

3.4.8 CCFL FET Driver

3.4.9 Serial Peripheral Bus

3.4.10 Special and Mode Pins

Mode[3:0], RDY_TRIEN, VPD, TEST are static pins.

RESETX is asynchronous, thus no timing relation to any CLK can be specified. Minimum low pulse width is <Min: tbd, Max: tbd>.

3.5 Mounting / Soldering

Mounting and soldering is explained in Fujitsu package data book, chapter 2.

4 Appendix

4.1 Control Registers

Table 4-1 shows all registers and bit groups of MB87P2020 (Jasmine) with a short explanation.

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
CMD	0x0000			Command register	
		31:8	PAR	Command parameter	0
		7:0	CODE	Command code	0xFF (NoOp)
IFIFO	0x0004	31:0	-	Input FIFO	-
OFIFO	0x0008	31:0	-	Output FIFO	-
FLNOM	0x000C	31:0	-	Flag register (normal write access)[a]	0x20400000
FLRST	0x0010	31:0	-	Flag register (reset write access)[a] 1: Reset flag at this position	0x20400000
FLSET	0x0014	31:0	-	Flag register (set write access)[a] 1: Set flag at this position	0x20400000
INTNOM	0x0018	31:0	-	Interrupt mask register (normal write access)[a] 1: use flag for interrupt	0
INTRST	0x001C	31:0	-	Interrupt mask register (reset write access)[a] 1: Reset mask at this position	0
INTSET	0x0020	31:0	-	Interrupt mask register (set write access)[a] 1: Set mask at this position	0
INTLVL	0x0024	31:0		Interrupt level/edge settings[a] 1: positive edge of flag triggers interrupt 0: high level of flag triggers interrupt	0
INTREQ	0x0028			Interrupt request length	
		5:0	INTCLK	Interrupt request length in ULB clocks (CLKM)	0x10

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
RDYTO	0x002C			RDY timeout control register	
		7:0	RDYTO	RDY timeout length in ULB clocks (CLKM)	0xFF
		8	RDTOEN	RDY timeout enable 1: enable RDY timeout	1
RDYADDR	0x0030			RDY timeout address register (read only)	
		20:0	ADDR	Address where RDY timeout occurred	0
IFCTRL	0x0034			MCU interface control register	
		9:8	SMODE	Sample mode for bus control signals 00: 3 point mode 01: 2 of 3 point mode 10: 2 point mode 11: 1 point mode	0
		5	DRINV	1: invert ULB_DREQ	0
		4	DSINV	1: invert ULB_DSTP	0
		3	INTINV	1: invert ULB_INTRQ	0
		2	DRTRI	1: open drain for ULB_DREQ	0
		1	DSTRI	1: open drain for DSTP	0
		0	INTTRI	1: open drain for ULB_INTRQ	0
WNDOF0	0x0040	20:0	OFF	MCU offset for SDRAM window 0	0x10’0000
WNDSZ0	0x0044	20:0	SIZE	Size of SDRAM window 0	0x10’0000
WNDOF1	0x0048	20:0	OFF	MCU offset for SDRAM window 1	0x10’0000
WNDSZ1	0x004C	20:0	SIZE	Size of SDRAM window 1	0x10’0000
WNDSD0	0x0050	19:0	OFF	SDRAM offset for SDRAM window 0	0
WNDSD1	0x0054	19:0	OFF	SDRAM offset for SDRAM window 1	0
SDFLAG	0x0058	0	EN	’1’: enable SDRAM space ’0’: any access to SDRAM space is ignored	0

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
IFUL	0x0080			Input FIFO limits	
		22:16	UL	Input FIFO upper limit for flag- or interrupt controlled flow control IFH=1 if IFLOAD >= IFUL:UL	0x0C
		6:0	LL	Input FIFO lower limit for flag- or interrupt controlled flow control IFL=1 if IFLOAD <= IFUL:LL	0x03
OFUL	0x0084			Output FIFO limits	
		22:16	UL	Output FIFO upper limit for flag- or interrupt controlled flow control OFH=1 if OFLOAD >= OFUL:UL	0x3C
		6:0	LL	Output FIFO lower limit for flag- or interrupt controlled flow control OFL=1 if OFLOAD <= IFUL:LL	0x0F
IFDMA	0x0088			Input FIFO limits for DMA transfer	
		22:16	UL	Upper limit for DMA access to input FIFO (not used)	0x0A
		6:0	LL	Lower limit for DMA access to input FIFO	0x3C
OFDMA	0x008C			Output FIFO limits for DMA transfer	
		22:16	UL	Upper limit for DMA access from output FIFO	0x0A
		6:0	LL	Lower limit for DMA access from output FIFO (not used)	0x3C
DMAFLAG	0x0090			DMA flag register	
		12:8	DSTP	Duration of DSTP signal. This value can be set in order to ensure a save MCU-DMAC reset. Normally the default value should work.	7
		2	MODE	’1’: DMA demand mode ’0’: DMA block/step- or burst mode	0
		1	EN	’1’: enable DMA	0
		0	IO	’1’: use DMA for input FIFO ’0’: use DMA for output FIFO	1

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
FLAGRES	0x0094			Flag behaviour register[a]	
		31:0	-	1: set flag to dynamic behaviour[b] 0: set flag to static behaviour	0x20400000
ULBDEB	0x0098			FIFO debug register (read only)	
		23:16	IFLC	Input FIFO load for current command **Attention**: This value changes with Jasmine core clock; correct sampling by MCU can't be ensured.	0x00
		15:8	OF	Output FIFO load **Attention**: This value changes with Jasmine core clock; correct sampling by MCU can't be ensured.	0x00
		7:0	IF	Input FIFO load independent from current command **Attention**: This value changes with Jasmine core clock; correct sampling by MCU can't be ensured.	0x00
CMDDEB	0x009C			Command debug register (read only)	
		31:8	PAR	Parameter for currently executed command	
		7:0	CMD	Code for currently executed command	
SDSE-QRAM [32]	0x0100-0x017C			SDRAM sequencer RAM (32 words)	
		12:7	ADDR	Microcode sequencer address argument	undef
		6:4	INST	Microcode instruction: run, ret, call, loop, srw, rrw, pde, pdx - coded 0 to 7)	undef
		3	RAS	Container command for SDRAM (RAS)	undef
		2	CAS	Container command for SDRAM (CAS)	undef
		1	WE	Container command for SDRAM (WE)	undef

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
SDMODE	0x0200			SDRAM Mode Register, bit [12:10, 8:7] reserved, set to ’0’	
		9	BRST	1: Burst write enable	0
		6:4	CL	CAS latency (2/3)	0
		3	ILB	1: Interleave burst 0: Sequential burst	0
		2:0	BLEN	Burst length (0=1, 1=2, 2=4, 3=8, 7=full)	0
SDINIT	0x0204	15:0	IP	Sysclocks of SDRAM power up initialization period (200 us)	0x4E20
SDRFSH	0x0208	15:0	RP	Sysclocks of SDRAM row refresh period (16 us)	0x0640
SDWAIT	0x020C			SDRAM timings (refer to SDRAM manual)	
		20	OPT	Bank interleave optimization	1
		19:16	TRP	RAS Precharge Time - 1	0x2
		15:12	TRRD	RAS to RAS Bank Active Delay Time - 1	1
		11:8	TRAS	RAS Active Time - 1	0x5
		7:4	TRCD	RAS to CAS Delay Time - 1	0x2
		3:0	TRW	Read to Write recovery time	0x3
SDIF	0x0210			SDRAM port interface timing (scalable clock delay) - is ignored by Jasmine	
		7:6	TAO	Address output delay (default 1)	0
		5:4	TDO	Data output delay	0
		3:2	TDI	Data sampling delay	0
		1:0	TOE	Tristate control delay	0
SDCFLAG	0x0214			Used as busy/sres flag during initialization	
		1	DQMEN	1: Enable DQM partial write optimization	0
		0	BUSY	Set busy flag during microprogram upload	0
PHA[16]	0x1000 - 0x103C			Physical layer address in SDRAM	
		19:0	OFS	Address offset (RA, BA, CA, BYTE),bits[9:0] fixed to zero	undef

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
DSZ[16]	0x1040 - 0x107C			Layer domain size	
		29:16	X	X dimension of layer Size	undef
DP1[16]	0x1080 - 0x10BC			First pixel in domain (memory offset)	
		29:16	X	Offset for X dimension	undef
		13:0	Y	Offset for Y dimension	undef
WSZ[16]	0x10C0 - 0x10FC			Display window size for layer	
		29:16	X	Size in X dimension	undef
		13:0	y	Size in Y dimension	undef
WOF[16]	0x1100 - 0x113C			Layer offset for display	
		29:16	X	Offset for X dimension	undef
		13:0	y	Offset for Y dimension	undef
LTC[16]	0x1140 - 0x117C			Transparent colour for layer	
		23:0	COL	Colour code depending on layer colour depth (LSB aligned)	undef
LBC[16]	0x1180 - 0x11BC			Blink colour for layer	
		23:0	COL	Colour code depending on layer colour depth (LSB aligned)	undef
LAC[16]	0x11C0 - 0x11FC			Blink alternative colour for layer	
		23:0	COL	Colour code depending on layer colour depth (LSB aligned)	undef
LBR[16]	0x1200 - 0x123C			Blink rate for layer	
		15:8	OFF	Number of frames for alternate colour	undef
		7:0	ON	Number of frames for blink colour	undef
CSPC[16]	0x1240 - 0x127C			Colour space code and flag register	
		9	LDE	Line doubling enable	undef
		8	TE	Transparency enable	undef
		3:0	CSC	Colour space code	undef

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
CFORMAT	0x1300	31:16	LITC	Layer to intermediate transfer codes	0x0000
		7	GAMEN	1: Gamma table enable	0
		6	IPOLEN	1: Interpolation for YUV422 colour code enable	0
		5	GFORCE	1: Force Gamma conversation for RGB>= 16bpp	0
		3:0	CSC	Intermediate colour space code	0xf
BACKCOL	0x1304			Background colour register	
		24	EN	1: Background colour enable	1
		23:0	COL	Background colour depending on colour depth for intermediate colour space	0x000000
MBC	0x1308			Blink control register	
		15:0	EN	Blink enable (one bit for each layer)	0x0000
		31:16	CBS	Current blink state (read only)	0x0000
ZORDER	0x130C			Z-Order register	
		19:16	EN	Enable (one bit for each plane)	0x0
		15:12	TM0	Topmost layer number	0x0
		11:8	TM1		0x0
		7:4	TM2		0x0
		3:0	TM3	Bottom layer number	0x0
CLUTOF [16]	0x1340 - 0x137C			16 CLUT offsets (1 per layer)	
		7:0	OFS	CLUT offset for layer	undef
DRM[14]	0x1380- 0x13B4			Duty ratio modulator pseudo levels, 14 words	
		5:0	PGL	Pseudo level (PGL/64 Frames)	0x00
CLUT [512]	0x2000 - 0x27FC			Colour Lock Up Table	
		23:16	RED	Red amplitude of logical colour	undef
		15:8	GRN	Green amplitude of logical colour	undef
		7:0	Blue	Blue amplitude of logical colour	undef

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
GAMMA [256]	0x2800 - 0x2BFC			Gamma Table	
		23:16	R	Red mapping	undef
		15:8	G	Green mapping	undef
		7:0	B	Blue mapping	undef
PHSIZE	0x3000			Display physical size	
		29:16	X	Width	0x0000
		13:0	Y	Height	0x0000
PHFRM	0x3004			Physical format register	
		27	POL	Xfref polarity 0=odd field ref is low	0
		26	VSYAE	Xvsync edge (0=Low/High edge, 1=High/Low edge)	0
		25	HSYAE	Xhsync edge (0=Low/High edge, 1=High/Low edge)	0
		24	IES	0: Internal Sync 1: External Sync	0
		17:16	SM	Scan mode	0
		12	FTE	1: Field toggle enable	0
		11:8	BSC	Bitstream format code	0x0
		4	RBSW	Swap R/B channel for RGB111	0
		3:0	CSC	Physical colour space code	0x0
PHSCAN	0x3008	29:16	SCLK	Physical size in scan clocks (Pixel*BPP/BitsPerScanclock)	0
DUALSCOF	0x300C	13:0	OFS	Dual scan Y offset	0
MTIMODD [2]	0x3010 - 0x3014			Master timing, odd field, First word start, next word stop.	
		30:16	X	X dimension (2’s complement)	
		14:0	y	Y dimension (2’s complement)	0x0000
MTMEVEN [2]	0x3018			Master timing, even field, First word start, next word stop. (X values from MTIMODD[0,1])	
		14:0	Y	Y dimension (2’s complement)	0x0000
MTIMON	0x3020	0	ON	Master timing switch (0=off,1=on)	0

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
TIMDIAG	0x3024			Diagnostic timing position output (read only)	
		30:16	X	Current X position (2's complement)	0x0000
		15	FIELD	Current field	0
		14:0	Y	Current Y position (2's complement)	0x0000
SPG [6,4]	0x3030 - 0x308C			These registers contain 6 Sync Pulse Generators (SPG0-SPG5) with each 4 registers.	0
SPGPSON [6]	0: 0x3030, 1: 0x3040, 2: 0x3050, 3: 0x3060, 4: 0x3070, 5: 0x3080			Sync pulse generator 0, position to switch on:	
		30:16	X	X position (2's complement)	0x0000
		15	FIELD	Field flag 0: odd; 1: even	0
		14:0	Y	Y position (2's complement)	0x0000
SPGMKON	0: 0x3034, 1: 0x3044, 2: 0x3054, 3: 0x3064, 4: 0x3074, 5: 0x3084			SPG 0: don't care vector for 'Position on' match. (1=do not include this bit into position matching)	
		30:16	X	X mask	0x0000
		15	FIELD	Field mask	0
		14:0	Y	Y mask	0x0000
SPGPSOF	0: 0x3038, 1: 0x3048, 2: 0x3058, 3: 0x3068, 4: 0x3078, 5: 0x3088			SPG: 0 position to switch off:	
		30:16	X	X position (2's complement)	0x0000
		15	FIELD	Field flag (0=odd, 1=even field)	0
		14:0	Y	Y position (2's complement)	0x0000
SPGMKOF	0: 0x303C, 1: 0x304C, 2: 0x305C, 3: 0x306C, 4: 0x307C, 5: 0x308C			SPG: 0 don't care vector for 'Position off' match (1=do not include this bit into position matching)	
		30:16	X	X mask	0x0000
		15	FIELD	Field mask	0
		14:0	Y	Y mask	0x0000
SSQCY-CLE	0x30FC	5:0	SC	Actual length of sequencer cycle (SC = Num -1)	0x0

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
SSQCNTS [64]	0x3100 - 0x31FC			Sync sequencer RAM contents (64 Words)	
		31	OUT	Output value for scan position	undef
		30:16	SEQX	X scan position (2's complement)	undef
		15	FIELD	Field flag (0: odd;1: even)	undef
		14:0	SEQY	Y scan position (2's complement)	undef
SMX [8,2]	0x3200 - 0x323C			Array definition for sync mixer (SMX0-SMX7)	0
SMXSIGS	0: 0x3200, 1: 0x3208, 2: 0x3210, 3: 0x3218, 4: 0x3220, 5: 0x3228, 6: 0x3230, 7: 0x3238			Sync mixer	
		14:12	S4	Signal select Signal to select: 0:const.zero 1:Sequencer out 2...7: SPG0...SPG5	0
		11:9	S3		0
		8:6	S2		0
		5:3	S1		0
		2:0	S0		0
SMXFCT	0: 0x3204, 1: 0x320C, 2: 0x3214, 3: 0x321C, 4: 0x3224, 5: 0x322C, 6: 0x3234, 7: 0x323C			Function table	
		31:0	FT	Output value = function_table[a] a=S4*2^4+S3*2^3+S2*2^2+S1*2^1+S0*2^0 Sn: SMXSIGS_Sn(SMXm)	0x00000000
SSWITCH	0x3240			Output signal delay (sync switch) register	
		7:0	CD	Sync switch, (0=no; 1=0.5 display clock (CLKD) cycles delay)	0x00
PIX-CLKGT	0x3248			Pixel clock gate register; gate is output of SM7	
		3	HC	Clock divider (0=1:1;1=1:2)	0
		2	CP	Clock polarity (0=true; 1=inverted)	0
		1	GON	Clock gate enable (1=on/0=off)	0
		0	GT	Gate type (0=And; 1=Or)	0

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
CKLOW	0x3250			Colour key lower limits (according to physical colour space) Pin DIS_CKEY is activated when all pixel channels lie within their limits (including limits).	
		24	OP	Key out polarity (0=active high, 1=active low)	0
		23:16	LLR	Red channel	0x00
		15:8	LLG	Green channel	0x00
		7:0	LLB	Blue/monochrome channel	0x00
CKUP	0x3254			Colour key upper limits (according to physical colour space) Pin DIS_CKEY is activated when all pixel channels lie within their limits (including limits).	
		23:16	ULR	Red channel	0x00
		15:8	ULG	Green channel	0x00
		7:0	ULB	Blue/monochrome channel	0x00
ACLAMP	0x3258			Clamping values for analog outputs (DACs)	
		23:16	ACLR	Red channel	0x00
		15:8	ACLG	Green channel	0x00
		7:0	ACLB	Blue channel	0x00
DCLAMP	0x325C	23:0	DCL	Blanking clamping value for digital outputs	0x000000
MAINEN	0x3260			Main display output enable flags	
		29	REFOE	1: (internal) reference voltage disable (0=on;1=off)	0
		28	DACOE	1: DAC output (A_BLUE, A_GREEN, A_RED) enable	0
		27	CKOE	1: DIS_CKEY output enable	0
		26	VROE	1: DIS_VREF output enable	0
		25	VSOE	1: DIS_VSYNC output enable	0
		24	HSOE	1: DIS_HSYNC output enable	0
		23:0	DOE	1: DIS_D[23:0] output enable	0x000000

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
SDCP	0x3270			SDRAM Controller request priorities	
		15:8	IFL	Input FIFO load (read-only)	0x00
		6:4	HP	High priority	0x7
		2:0	LP	Low priority	0x3
VIC-START	0x4000			Input layer start coordinates (memory offset for video)	
		29:16	X	X offset	0x0000
		13:0	Y	Y offset	0x0000
VICALPHA	0x4004			Replace colour when alpha pin (VSC_ALPHA) is active Colour depth depends on layer	
		23:0	COL	Alpha colour	0x000000
VICCTRL	0x4008			Input control word	
		7	BSWAP	Swap external channels A and B to internal channels iA and iB. 0: A->iA, B->iB 1: A->iB, B->iA	0
		6	ALEN	1:Enable alpha; 0:Disable alpha	0
		5	PORT	Port mode 1: Double port (port iA and iB) 0: Single port (port iA only)	1
		4	CLOCK	Video Clock (VSC_CLKV) mode for data sampling 1: Double clock mode (both edges) 0: Single clock mode (rising edge only)	0
		3:0	MODE	Colour mode for video input: 0x4: RGB555 0x5: RGB565 0x6: RGB888 0x7: YUV422 0x8: YUV444 0xE: YUV555 0xF: YUV655	0x6

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
VICFC-TRL	0x400C			Field control word	
		22	ODDFST	Field order within a Frame: 1:Odd field is top field 0:Even field is top field	0
		21	FRAME	Video mode 1:Frame mode (interleave fields in one layer) 0:Field mode (store one field in one layer)	0
		20	SKIP	Field skip enable for selected fields 1: Skip every 2nd filed of each type 0:Use every field	0
		18	VICEN	1: General VIC enable	0
		17	EVENEN	1: Enable even fields	0
		16	ODDEN	1: Enable odd fields	0
		11:8	THIRD	3rd layer number	0x7
		7:4	SEC	2nd layer number	0x0
		3:0	FIRST	1st layer number	0x6
VICPC-TRL	0x4010			Polarity settings for video control pins	
		3	ALPHA	VSC_ALPHA: 1: Low active 0: High active	0
		2	FIELD	VSC_IDENT: 1: Odd field low active 0: Odd field high active	0
		1	VACT	VSC_VACT: 1: Low active, 0: High active	0
		0	VREF	VSC_VREF: 1: Low active, 0: High active	0
VICF-SYNC	0x4014			Control register for video I/O synchronization	
		16	REL	1: VIC is faster than GPU; 0: GPU is faster than VIC	0
		15	SYNC	1: Three layer mode: 0: Two layer mode	0
		14:0	SLEVEL	Switch level for layer switch in two layer sync mode	0

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
SDRAM	0x401C			SDRAM request priority control register	
		2:0	LP	Low priority	0x2
		6:4	HP	High priority	0x6
VICBSTA	0x4020			VIC status register (read only)	
		18	FE	FIFO empty flag	1
		17	FF	FIFO full flag	0
		16	AERR	Address error	0
		15:13	FSM	FSM state	0x7
		12:10	ADD	Add_status	0x0
		9	CLR	Clear	0
		8:7	REQ	Req_state	0x0
		6:0	LOAD	FIFO load	0x00
VICRLAY	0x4024			Video layer debug register (read only)	
		19:16	AOVL	Current output layer (to GPU)	undef
		11:8	LIVL	Last input layer (VIC)	undef
		3:0	AIVL	Current input layer (VIC)	undef
VICVI-SYN	0x4028			Video path control register	
		25:24	DEL	Negative data delay with respect to VSC_VACT signal	0
		20:16	SHUFF	Bus shuffler for data ports iA, iB, iA_delayed and iA_negedge	0
		8	START	Selector for VIC_SYNC flag[a] source: 0: Video write start; 1: Video read start	0
		1:0	SEL	Selector for video input protocol: 00: VPX; 01: CCIR-TRC; 10: CCIR external sync 11: reserved	00
VICLI-MEN	0x402C	0	LIMENA	1: Enable video limitation unit	

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
VICLIMH	0x4030			Horizontal limitation settings	
		26:16	HEN	Horizontal window length including offset	0x000
		10:0	HOFF	Horizontal window offset	0x000
VICLIMV	0x4034			Vertical limitation settings	
		26:16	VEN	Vertical window length including offset	0x000
		10:0	VOFF	Vertical window offset	0x000
EXTPC-TRL	0x4038			Polarity control register for CCIR mode with external video synchronization.	
		3	ALPHA	Alpha (pin VSC_ALPHA) 0: high active 1: low active	0
		2	PARITY	Parity (pin VSC_IDENT) 0: polarity unchanged 1: invert polarity	0
		1	HREF	Horizontal reference signal (pin VSC_VACT) 0: high active 1: low active	0
		0	VREF	Vertical reference signal (pin VSC_VREF) 0: high active 1: low active	0
BGCOL	0x4100			Background pixel colour	
		24	EN	1: Enable background colour	0
		23:0	COL	Background colour data	0x000000
FGCOL	0x4104	23:0		Foreground pixel colour	0x000000
IGNOR-COL	0x4108			Ignored pixel colour (PutBM, PutCP)	
		24	EN	1: enable ignore colour	0
		23:0	COL	Ignore colour data	0x000000
LINECOL	0x410C	23:0	COL	Line colour (DwLine)	0x000000
PIXCOl	0x4110	23:0	COL	Colour for pixel with fixed colour (PutPxFC)	0x000000
PLCOL	0x4114	23:0	COL	Polygon colour (DwPoly)	0x000000
RECTC-COL	0x4118	23:0	COL	Rectangle colour (DwRect)	0x000000

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
XYMAX	0x411C			Pixel stop address for pixel processor bitmap commands (PutBM, PutCP, PutTxtBM, PutTxtCP)	
		29:16	XMAX	X dimension for stop point	0x0000
		15:0	YMAX	Y dimension for stop point	0x0000
XYMIN	0x4120			Start address for pixel processor bitmap commands (PutBM, PutCP, PutTxtBM, PutTxtCP)	
		29:16	XMIN	X dimension for start point	0x0000
		15:0	YMIN	Y dimension for start point	0x0000
PPCMD	0x4124			Configuration for pixel processor commands	
		28	ULAY	1: Use target layer for drawing and pixel commands too	0
		27:24	LAY	Target layer for commands PutBM, PutCP, PutTxtBM,PutTxtCP	0x0
		8	DIR	Direction for sequential commands PutBM, PutCP, PutTxtBM, PutTxtCP 0: Horizontal, 1:Vertical	0
		1:0	MIR	Mirror for sequential commands PutBM, PutCP, PutTxtBM, PutTxtCP 00: No mirror, 01: X-mirror, 10: Y-mirror,11:XY-mirror	0x0
SDCPRIO	0x4128	2:0	PRIO	Priority for SDC interface	0x0
REQCNT	0x412C	7:0	MFB	MFB+1: Maximum FIFO-block size before activating a SDRAM request (0<=MFB<64)	0x00
READINIT	0x4130	0	RCR	Read control registers for pixel processor (address range: 0x4100-0x4130) 0: read back PP internal register 1: read back PP user writeable register	0
DIPAC-TRL	0x4200			DIPA control register	
		18:16	PDPA	DPA priority for SDC access	0x0000
		2:0	PIPA	IPA priority for SDC access	0x0000

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
DIPAIF	0x4204			IPA input FIFO control register	
		31:16	IFMAX	Input FIFO max. block size	0x0001
		15:0	IFMIN	Input FIFO min. block size	0x0001
DIPAOF	0x4208			IPA output FIFO control register	
		31:16	OFMAX	Output FIFO max. block size	0x0001
		15:0	OFMIN	Output FIFO min. block size	0x0001
CCFL1	0x4400			CCFL control register	
		27	EN	1: CCFL enable	0
		26	PROT	1: Protect old settings during configuration	0
		25	SNCS	Synchronization Select 0: internal (vsync from GPU), 1: software	0
		24	SYNC	1: Synchronization trigger by software	0
		7:0	SCL	Timebase scale factor (Derived from System clock (CLKK))	0x00
CCFL2	0x4404			CCFL Duration Register (Unit: 4 Timebase Clocks)	
		31:16	FLASH	Flash Duration	0x0000
		15:8	PAUSE	Pause Duration	0x00
		7:0	IGNT	Ignition Duration	0x00

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
CLKCR	0xFC00			Clock configuration register	
		31:30	DCS	Direct clock source 00: Crystal (pins OSC_IN and OSC_OUT), 01: Pixel clock (pin DIS_PXCLK) 10: MCU clock (pin ULB_CLK) 11: Reserved clock (pin RCLK)	00
		29:24	SCP	System clock (CLKK) prescaler	0
		23:22	PCS	PLL clock source 00: Crystal (pins OSC_IN and OSC_OUT), 01: Pixel clock (pin DIS_PXCLK) 10: MCU clock (pin ULB_CLK) 11: Reserved clock (pin RCLK)	00
		21:16	PFD	PLL feedback divider	0x00
		15	SCSL	System clock (CLKK) select 0: direct clock source 1: PLL clock source	0
		14	PCSL	Pixel clock (CLKD) select 0: direct clock source 1: PLL clock source	0
		13	IPC	Pixel clock (CLKD) invert 0: not inverted 1: inverted	0
		12	PCOD	Pixel clock output (DIS_PXCLK) disable 0: internal pixel clock (CLKD output) 1: external pixel clock (DIS_PXCLK input)	1
		11	DBG	1: Core clock (CLKK) debug mode (output at pin SPB_TST)	0
		10:0	PCP	Pixel clock prescaler value	0x000

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
CLKPDR	0xFC04			Clock power down register	
		31:24	ID	Chip ID (read only) 0: MB87J2120 (Lavender) 1: MB87P2020 (Jasmine)	1
		15	MRST	1: Master hardware reset	0
		14	LCK	PLL lock (read only) 1: PLL has locked to input frequency	undef
		13	-	reserved; set to 0	0
		11	RUN	PLL enable 1: PLL on 0: PLL off	0
		10	GPU	1: Enable GPU clocks	0
		9	ULB	1: Enable ULB clocks	0
		8	SPB	1: Enable SPB clock	0
		7	CCFL	1: Enable CCFL clock	0
		6	SDC	1: Enable SDC clock	0
		5	VIS	1: Enable VIC clocks	0
		4	DIPA	1: Enable DIPA clock	0
		2	MCP	1: Enable MCP clock	0
		1	MAU	1: Enable MAU clock	0
		0	PE	1: Enable PE clock	0
SPBTRP	0xFD00			Transmit and Receive data register	
		31:24	TDRM	Transmitter data register (MSB)	0x00
		23:16	TDRL	Transmitter data register (LSB)	0x00
		15:8	RDRM	Receiver data register (MSB)	0x00
		7:0	RDRL	Receiver data register (LSB)	0x00
SPBPSIR	0xFD04			Prescaler selection and interrupt/ reset detection register	
		31:24	FSRM	Frequency selection register (MSB)	0x00
		23:16	FSRL	Frequency selection register (LSB)	0x00
		15:8	DPRM	Interrupt/reset detection point register (MSB)	0xFF
		7:0	DPRL	Interrupt/reset detection point register (LSB)	0xFF

Table 4-1: Register address space for Jasmine

Register		Bits	Group Name	Description	Default value
Name	**Address**				
SPBCS	0xFD08			Control and status register	
		31:24	CSR	Control/Status register	0x00
		23:16	ACR	Address/command register	0x00
		15:8	FLSR	Field length selection register	0x00
		7:0	PMR	Phase measurement register	0x00
SPBBITR	0xFD0C	31:24	BRR	Bits received Register	0x00

a. See chapter 4.2 for a description of bit groups for flags.

b. Dynamic behaviour means that a hardware flag reset is possible.

4.2 Flags

Table 4-2 contains all flags for MB87P2020 (Jasmine).

In order to avoid data inconsistencies during bit masking within flag register a mask (and/or gating) process is implemented in hardware for flag register. To distinguish between flag set-, reset- and direct write access different addresses are used[1]:

- FLNOM (0x000C): normal write operation
- FLRST (0x0010): reset operation (1: reset flag on specified position; 0: don't touch)
- FLSET (0x0014): set operation (1: set flag on specified position; 0: don't touch)

All of these three addresses write physically to one register with three different methods.

For reading all three addresses return the value of flag register.

Every flag can have a different reset behaviour. With help of register FLAGRES the application can choose whether the hardware is allowed to reset the desired flag (*dynamic* behaviour) or not (*static* behaviour). With dynamic behaviour the flag follows the driving hardware signal while with static behaviour the application is responsible for resetting the flag in order to catch next event. In table 4-2 the default reset behaviour at system start up is given in last column.

Table 4-2: Flags for MB87P2020 (Jasmine)

Name	Bit	Short name	Description	Default behaviour
VIC_SYNC	31	VICSYN	A frame or field has been written or read from/to SDRAM Which event is signalled by this flag depends on VIC settings: VICFCTRL_FRAME determines the storage type within SDRAM (field or frame). For details see VIC description and table 4-1. VICVISYN_START determines whether a write or read start should trigger the flag	static

1. Additionally all access types (word, halfword and byte) are possible for each of these addresses.

Table 4-2: Flags for MB87P2020 (Jasmine)

Name	Bit	Short name	Description	Default behaviour
RDY_TO	30	ERDY	RDY timeout error has occurred See ULB description and table 4-1 (register RDYTO and RDYADDR)	static
DPA_WR_EN	29	RDPA	1: DPA write access is enabled. This flag has to be polled before each DPA (write-) access to ensure a save SDRAM access[a]. **Otherwise data loss may occur**.	dynamic
RDY_DPA	28	FDPA	1: DPA has finished SDRAM access and is ready for next one.	static
RDY_IPA	27	RIPA	1: IPA is ready for command execution	static
RDY_MCP	26	RMCP	1: MCP is ready for command execution	static
RDY_MAU	25	RMAU	1: MAU is ready for command execution	static
RDY_PE	24	RPE	1: PE is ready for command execution	static
ERR_MCP_BPP	23	EBPP	1: Colour depth for source- and target layer is different during MemCP command In this error case MCP reads data from input FIFO but performs no further actions.	static
CMD_WR_EN	22	CWEN	1: Command register can be written. This flag has to be polled before a command can be written[a]. **Otherwise data loss and synchronization loss between Jasmine and MCU may occur**.	dynamic
EXT_INT0	21	EINT0	1: Lavender/Jasmine external interrupt occurred This interrupt is currently assigned to SPB device which is implemented on chip but outside the Lavender/Jasmine core.	static
SDC_TIMEOUT	20	STOUT	After reset: Flag is set (’1’) when SDRAM initialisation time is over Else: Flag is set (’1’) when SDC forces SDRAM refresh. This is a sign for high SDRAM bus load.	static
GPU_SYNC	19	GSYNC	This flag is directly connected to GPU Sync Mixer 6[b]. The Sync Mixer default settings generate no sync signal.	static
GPU_BWVIO	18	BWVIO	1: GPU bandwidth violation occurred which means that the GPU didn’t receive requested data from SDRAM. This flag indicates a high SDRAM bus load.	static
ERR_CMD_OV	17	EOV	1: A command pipeline overflow has occurred. A command was sent to Jasmine while CWEN flag was ’0’.	static

Table 4-2: Flags for MB87P2020 (Jasmine)

Name	Bit	Short name	Description	Default behaviour
ERR_CMD_CODE	16	ECODE	1: Wrong error code was written to command register This command code is internally treated as NoOp command.	static
ERR_D_UF	15	EDATA	1: Execution device (PP or IPA) tried to read from empty input FIFO This may indicate a wrong behaviour of execution device.	static
BUSY_DPA	12	BDPA	1: DPA is performing an SDRAM access.	static
BUSY_IPA	11	BIPA	1: IPA is executing a command	static
BUSY_MCP	10	BMCP	1: MCP is executing a command	static
BUSY_MAU	9	BMAU	1: MAU is executing a command	static
BUSY_PE	8	BPE	1: PE is executing a command	static
OF_LOW	7	OFL	1: Output FIFO load is equal or lower than programmable output FIFO lower limit (OFUL_LL).	static
OF_HIGH	6	OFH	1: Output FIFO load is equal or higher than programmable output FIFO upper limit (OFUL_UL).	static
OF_EMPTY	5	OFE	1: Output FIFO is empty.	static
OF_FULL	4	OFF	1: Output FIFO is full.	static
IF_LOW	3	IFL	1: Input FIFO load is equal or lower than programmable input FIFO lower limit (IFUL_LL).	static
IF_HIGH	2	IFH	1: Input FIFO load is equal or higher than programmable input FIFO upper limit (IFUL_UL).	static
IF_EMPTY	1	IFE	1: Input FIFO is empty.	static
IF_FULL	0	IFF	1: Input FIFO is full.	static

a. Alternative this flag can cause an interrupt and writing can be done inside Interrupt Service Routine (ISR).

b. See GPU description for details about Sync Mixer settings.