FUJITSU SEMICONDUCTOR
MICROCONTROLLER MANUAL

CM25–10113–1E

F²MC-8L FAMILY MICROCONTROLLERS

MB89140 SERIES

HARDWARE MANUAL

FUJITSU

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■ PREFACE

The terms in this manual are defined as follows:

(1) A clock cycle is one clock cycle of the oscillation frequency.

(2) A system clock cycle is the clock frequency divided by the gear function (see 2.2). One cycle time of the system clock varies with the settings of the CS1 and CS0 bits of the SYCC register. With some internal resources, the gear change will cause changes in operating speed. See 3.4 for details.

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1. GENERAL

The MB89140 series of single-chip microcontrollers use the F^{2}MC-8L CPU core to enable high-speed processing at low voltages, and features a 25 segment VFD (Vacuum Fluorescent Display) driver. They contain resources such as timers, a serial interface, an A/D converter and an external interrupt input to provide a wide variety of applications for commercial and industrial equipment, including portable equipment.

The MB89140 series of single-chip microcontrollers has twenty-five V_{CC}-40VP-channel high voltage ports which makes it suitable for VFD display application such as microwave oven, fan heater, room air conditioner, dashboard controller, and so on.

1.1 FEATURES

- Minimum instruction execution time: 0.5 µs (at oscillation frequency of 8 MHz)
- CPU core as commonly used for MB89860 series
  - Instruction system best for controller
    - Multiplication and division instructions
    - 16-bit operation
    - Instruction test and branch instruction
    - Bit handling instruction, etc.
- Operation at low voltage (A/D converter unused)
- 25 segment VFD (Vacuum Fluorescent Display) driver.
- Low current dissipation (applicable to dual-circuit clock)
- Internal high-withstand-voltage ports
- 5 timers
  - 8-bit PWM timer (available as reload timer)
  - 12-bit MPG timer (available as PPG output, PWM output and reload timer)
  - 8/16-bit timer/counter (available as two 8-bit timers)
  - 21-bit time-base counter
- Single serial interface
  - Transfer direction selected for communication with various equipment
- A/D converter
  - Successive approximation type with 10-bit resolution
- 2-channel external interrupt input
  - Two channels can be selected independently to cancel the low-power consumption modes (selectable from rising edge, falling edge, or both edges).
  - The INT1 can be applied from –0.7 V to 7.0 V (N-channel open drain).
- Low-power consumption modes
  - Stop mode (The oscillation stops to minimize current consumption.)
  - Sleep mode (The CPU stops to cut current consumption to about 30% of normal.)
- Reset output or power-on reset available option can be selected.
- Packages
  - SDIP-64 and QFP-64 packages

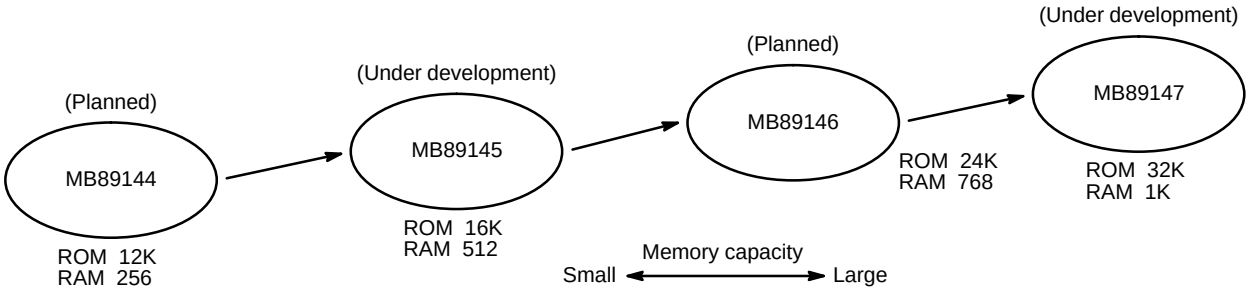


Fig. 1.1 MB89140 series

1.2 PRODUCT SERIES

Table 1-1 lists the types and functions of the MB89140 series of microcontrollers.

Table 1-1 Types and Functions of MB89140 Series of Microcontrollers

Model Name	MB89144	MB89145	MB89146	MB89147	MB89P147 MB89W147	MB89PV140
Classification	Mass-produced product (Mask ROM product)				OTPROM/ EPROM product	Piggyback/evaluation product for evaluation and development
ROM capacity	12K × 8 bit	16K × 8 bit	24K × 8 bit	32K × 8 bit	Internal 32K × 8 bits	External 32K × 8 bits (Piggyback)
RAM capacity	256 × 8 bit	512 × 8 bit	768 × 8 bit	1K × 8 bit	Internal 1K × 8 bits	Internal 1024 × 8 bits
CPU functions	Number of basic instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum instruction execution time: 0.5 µs/8 MHz to 8.0 µs/8 MHz and 61 µs/32.768 kHz Interrupt processing time: 4.5 µs/8 MHz to 72.0 µs/8 MHz and 562.5 µs/32.768 kHz Note: The above times vary with gear function.					
Port	High-withstand-voltage output port (P-channel open drain): 8 (P60 to P67 for large current) 16 (P40 to P47, P50 to P57 for small current) Buzzer output (P-channel open drain, high-withstand-voltage): 1 (Large current) Output port (CMOS): 4 (P20 to P23) Input port (CMOS): 2 (P70 to P71; serve as X0A and X1A pins when two clocks used) I/O port (CMOS): 23 (P00 to P07, P10 to P17, P30, P32 to P37) I/O port (N-channel open drain): 1 (P31) Total: 55					
VFD	25 segment					
Time-base timer	Capable of generating four internal pulses of 0.26 ms, 0.51 ms, 1.02 ms and 0.524 s (at oscillation frequency of 8.0 MHz)					
8-bit PWM timer (Timer 1)	8-bit timer operation (toggle output possible, 1, 2, 8 or 16 system clock cycles of operating clock) 8-bit resolution PWM operation (conversion cycle: 128 µs to 2.0 ms at oscillation frequency of 8.0 MHz and maximum gear speed)					
12-bit MPB timer (Timer 4)	12-bit resolution PWM operation (maximum conversion cycle: 2048.4 µs to 16.4 ms 12-bit resolution reload timer operation (toggle output possible) 12-bit resolution PPG operation (minimum resolution: 0.5 µs at oscillation frequency of 8.0 MHz and maximum gear speed)					
8/16-bit timer/counter (Timers 2 and 3)	8/16-bit timer operation (operating clock, internal clock and external trigger). See 2.2 for details. 8/16-bit event counter operation (selectable from rising edge, falling edge, or both edges)					

Table 1-1 Types and Functions of MB89140 Series of Microcontrollers (Continued)

Model Name	MB89144	MB89145	MB89146	MB89147	MB89P147 MB89W147	MB89PV140
Serial I/O	8-bit length 1 channel Transfer clock (external, 4, 8 or 16 system clock cycles)					
A/D converter	10-bit resolution, 12 channels A/D conversion mode (conversion time: 16.5 µs at 8 MHz and maximum gear speed) Sense mode (conversion time: 9.0 µs at 8 MHz and maximum gear speed) Continuous start by external activation or internal timer					
External interrupt	2 independent channels (edge selection, interrupt vector, interrupt source flag) Interrupt mode selectable from rising edge, falling edge, or both edge. Analog noise filter built in For releasing Stop/Sleep modes (edge detection possible in Stop mode)					
Standby mode	Sleep, Stop and Watch mode					
Process	CMOS					
Package	DIP-64P-M01 (SDIP-64)/FPT-64P-M06 (QFP64)					MDP-64C-P02/ MQP-64C-P01
Operating voltage	2.7 V to 6.0 V*					2.7 V to 6.0 V

* Operating voltage varies depending to the condition such as frequency or others.

1.3 BLOCK DIAGRAM

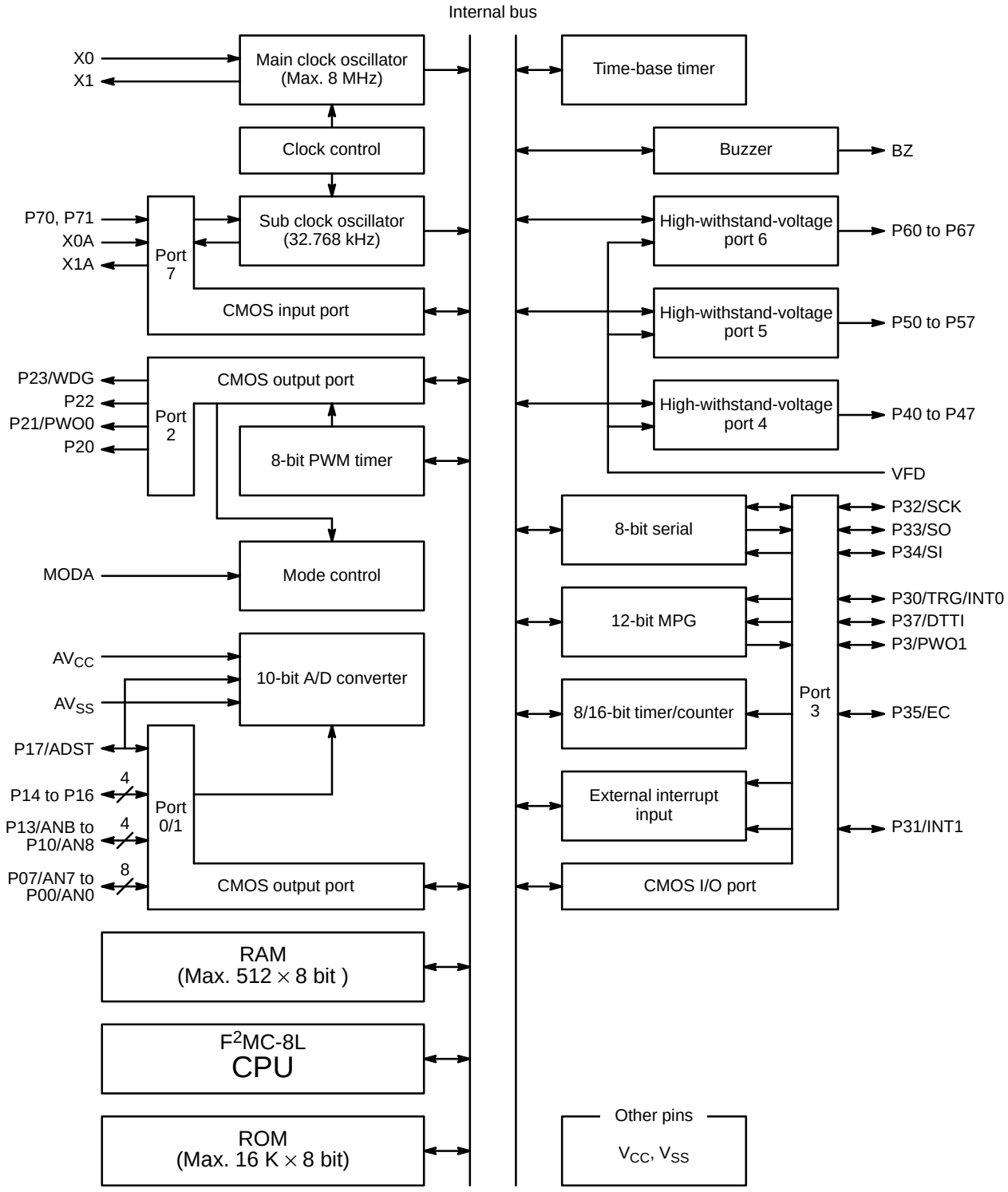
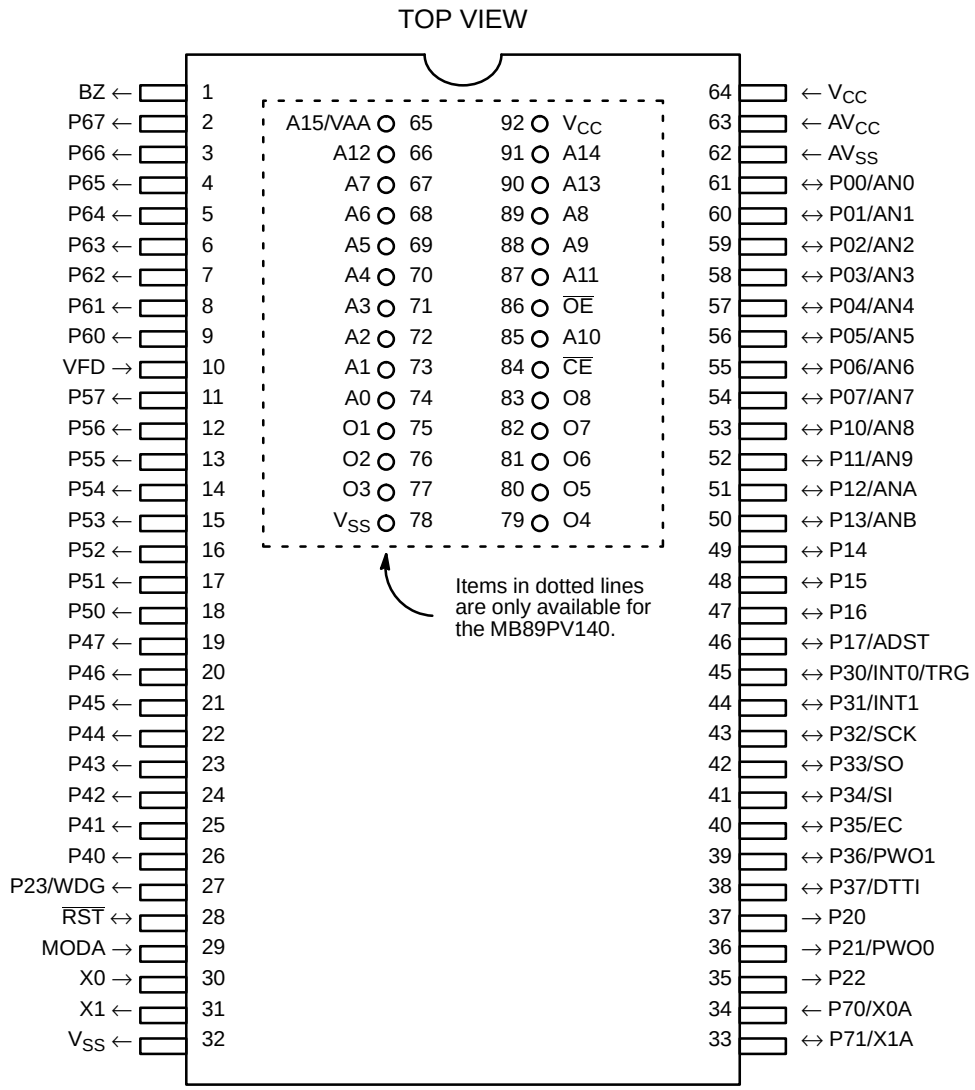


Fig. 1.2 Block Diagram

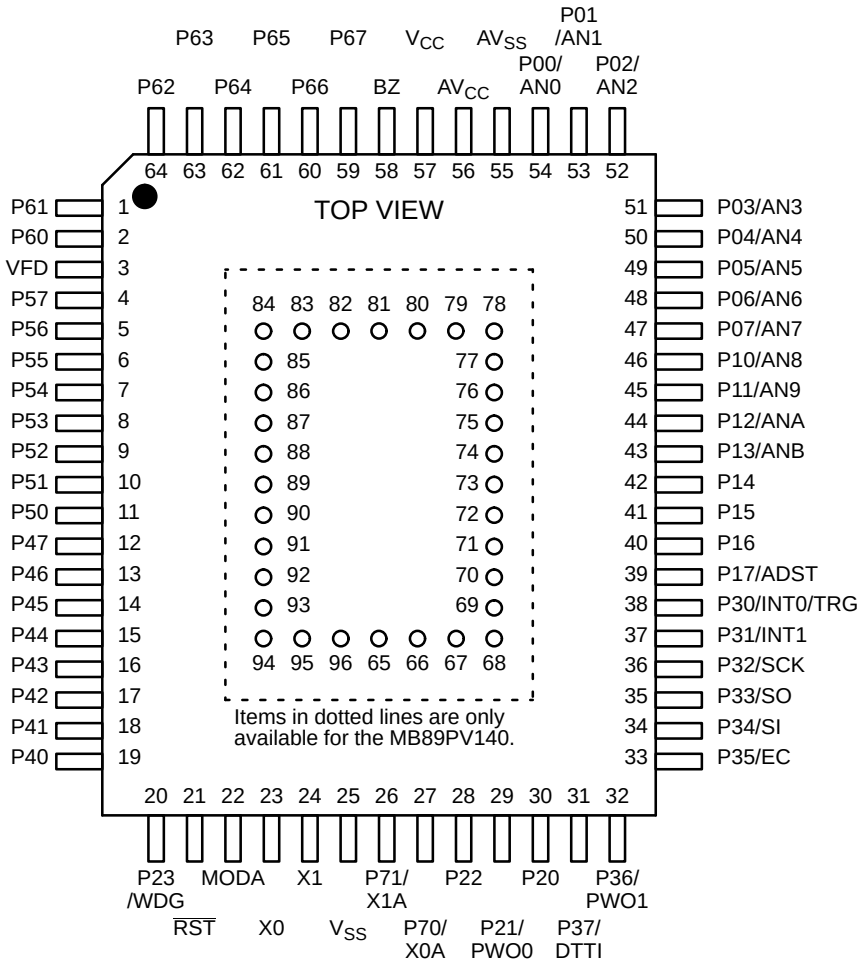
1.4 PIN ASSIGNMENT



The SH-DIP64 cautions are as follows:

- Pins 33 and 34 serve as input-only ports when used as general-purpose ports.
- Pin 28 serves as an output pin when the reset output option is selected.
- P07 to P00 and P13 to P10 serve as analog input ports after reset. When using them as port inputs, registers PCR0 and PCR1 must be set.

Fig. 1.3 Pin Assignment (DIP-64P-M01, MDP-64C-P02)



Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	A15/V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

Fig. 1.4 Pin Assignment (FPT-64P-M06, MDP-64C-P01)

1.5 PIN FUNCTION DESCRIPTION

Table 1-2 and NO TAG lists the pin function and Figure 1.3 shows the input/output circuit configurations.

Table 1-2 Pin Function Description

Pin No.		Pin Name	Circuit type	Function
SDIP	QFP			
30	23	X0	A	**Used for main clock oscillation** A crystal resonator should be used.
31	24	X1		
29	22	MODA	B	**Used for input of operation mode select signals** Usually connected to V_{SS}. This pin serves as the V_{PP} pin for EPROM-mounted models.
28	21	$\overline{RST}$	C	**Used for input/output of reset signals** Consists of an N-channel open-drain output with a pull-up resistor and hysteresis input. When the reset on option is selected, a Low level is output from this pin according to the internal source. The internal circuit is initialized at input of a Low level. A noise canceler is built in.
54 to 61	47 to 54	P07/AN7 to P00/AN0	F	**General-purpose I/O ports** Input is hysteresis type containing a noise filter. Although these ports also serves as analog input pins, analog input does not pass through the noise filter for hysteresis input.
46	39	P17/ADST	I	**General-purpose I/O port** Input is hysteresis type containing a noise filter. This port also serves as an external start pin for the A/D converter.
47 to 49	40 to 42	P16 to P14	I	**General-purpose I/O ports** Input is hysteresis type containing a noise filter.
50 to 53	43 to 46	P13/ANB to P10/AN8	F	**General-purpose I/O ports** Input is hysteresis type containing a noise filter. Although these ports serve as analog input pins, analog input does not pass through the noise filter for hysteresis input.
34	27	X0A/P70	A/J	Can be selected as a general-purpose input port or sub-clock generating pin by the mask option. When using as a general-purpose input pin, input is hysteresis type containing a noise filter.
33	26	X1A/P71	A/J	Can be selected as a general-purpose input port or sub-clock generating pin by the mask option. When using as a general-purpose input pin, input is hysteresis type containing a noise filter.
35	28	P22	D	**General-purpose output port**
27	20	P23/WDG	D	**General-purpose output port** This port also serves as a watchdog output pin (see 2.2 for watch dog timer).
36	29	P21/PWO0	D	**General-purpose output port** This port also serves as a PWM output pin for the 8-bit PWM timer.
37	30	P20	D	**General-purpose output port**

Table 1-2 Pin Function Description (Continued)

Pin No.		Pin Name	Circuit type	Function
SDIP	QFP			
38	31	P37/DTTI	I	**General-purpose I/O port** Input is hysteresis type containing a noise filter. When overcurrent is detected, the external rising or falling edge can be input to inactivate the 12-bit MPG output.
39	32	P36/PWO1	I	**General-purpose I/O port** Input is hysteresis type containing a noise filter. This port also serves as a 12-bit MPG output pin.
40	33	P35/EC	I	**General-purpose I/O port** Input is hysteresis type containing a noise filter. This port also serves as an external clock input pin for the 8/16-bit timer/counter.
41	34	P34/SI	I	**General-purpose I/O port** Input is hysteresis type containing a noise filter. This port also serves as an external clock input pin for the 8-bit timer/counter.
42	35	P33/SO	I	**General-purpose I/O port** Input is hysteresis type containing a noise filter. This port also serves as a serial data output pin for the 8-bit serial interface.
43	36	P32/SCK	I	**General-purpose I/O port** Input is hysteresis type containing a noise filter. This port also serves as a serial transfer clock pin for the 8-bit serial interface.
44	37	P31/INT1	E	**General-purpose I/O port** Consists of an N-channel open-drain output and hysteresis input containing a noise filter. This port also serves as an external interrupt pin. Interrupt input is also hysteresis type containing a noise filter.
45	38	P30/INT0/TRG	I	**General-purpose I/O port** Input is hysteresis type containing a noise filter. This port can also be used as an external interrupt pin or MPG trigger input pin. Interrupt input is also hysteresis type containing a noise filter.
1	58	BZ	H	**Used for buzzer output only** This pin also serves as a P-channel high-withstand-voltage open-drain output port.
19 to 26	12 to 19	P47 to P40	G	**P-channel high-withstand-voltage open drain output ports for small current** Two types of microcontrollers are provided: one has a pull-down resistor between these ports and the VFD pin, and the other does not.
11 to 18	4 to 11	P57 to P50	G	**P-channel high-withstanding-voltage open drain output ports for small current** Two types of microcontrollers are provided: one has a pull-down resistor between these ports and the VFD pin, and the other does not.
2 to 9	59 to 2	P67 to P60	G	**P-channel high-withstand-voltage open-drain output ports for large current** Two types of microcontrollers are provided: one has a pull-down resistor between these ports and the VFD pin, and the other does not.
10	3	VFD	—	**Used for voltage supply connected to pull-down resistors for ports 4, 5 and 6** This pin serves as an NC pin for microcontrollers without a pull-down resistor and the MB89PV140 microcontroller.

Table 1-2 Pin Function Description (Continued)

Pin No.		Pin Name	Circuit type	Function
SDIP	SDIP			
64	57	V_{CC}	—	**Used for power supply**
32	25	V_{SS}	—	**Used for power supply (GND)**
63	56	AV_{CC}	—	**Used for power supply for A/D converter**
62	55	AV_{SS}	—	**Used for power supply for A/D converter** Must be used at same potential as V_{SS} pin

Table 1-3 Pin for External-ROM

Pin No.		Pin Name	Circuit type	Function
SDIP	QFP			
65	66	V_{PP}	Output	**High-level output pin**
66 67 68 69 70 71 72 73 74	67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	Output	**Address-output pins**
75 76 77	77 78 79	01 02 03	Input	**Data-input pins**
78	80	V_{SS}	Output	**Power (GND) pin**
79 80 81 82 83	82 83 84 85 86	04 05 06 07 08	Input	**Data-input pins**
84	87	$\overline{CE}$	Output	**Chip-enable pin for ROM** A High level is output in the standby mode.
85	88	A10	Output	**Address-output pin**
86	89	$\overline{OE}$	Output	**Output-enable pin for ROM** A Low level is always output.
87 88 89	91 92 93	A11 A9 A8	Output	**Address-output pins**
90	94	A13	Output	**Address-output pin**
91	95	A14	Output	**Address-output pin**
92	96	V_{CC}	Output	**Power pin for EPROM**

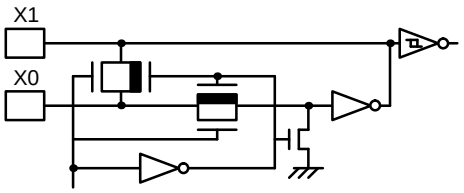
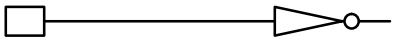
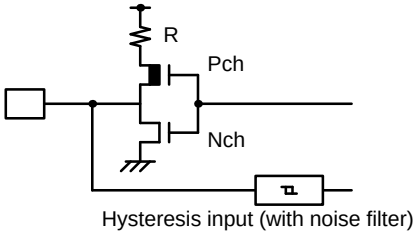
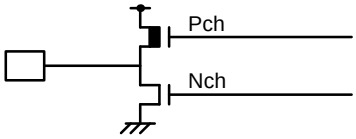
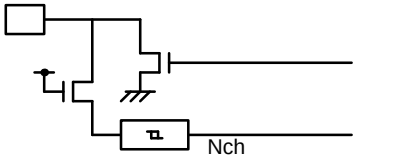
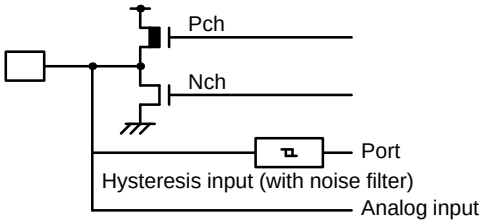
Classification	Circuit	Remarks
A		• Feedback resistor: About 2 MΩ
B		• CMOS input
C		• Output pull-up resistor (Pch): About 50 kΩ (5 V) • CMOS hysteresis input (with noise filter)
D		• CMOS output
E		• N-ch open drain output • CMOS hysteresis input (with noise filter)
F		• CMOS output • CMOS hysteresis input (with noise filter; analog input excluded)

Fig. 1.5 Input/Output Circuit Configurations

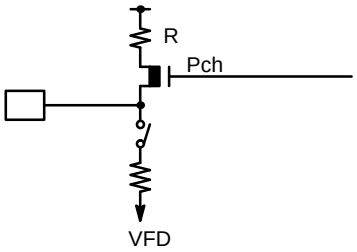
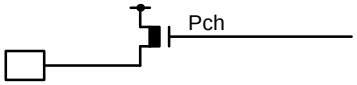
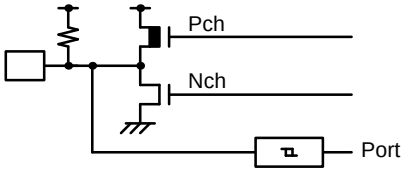
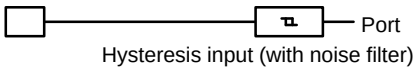
Classification	Circuit	Remarks
G		• P-channel high-withstand-voltage open-drain output • Microcontrollers with and without pull-down resis tor provided (excluding MB89V140 microcontroller)
H		• P-channel high-withstand-voltage open-drain output
I		• CMOS output • CMOS hysteresis input (with noise filter) • The pull-up resistor is optional.
J		• CMOS hysteresis input (with noise filter)

Fig. 1.5 Input/Output Circuit Configurations (Continued)

1.6 HANDLING DEVICES

(1) Preventing latch-up

Latch-up may occur if a voltage higher than V_{CC} or lower than V_{SS} is applied to the input or output pins other than port 40 to 47, or if voltage exceeding the rated value is applied between V_{CC} and V_{SS}. However, voltages of up to 7 V can be applied to the P31/INT1 pin irrespective of V_{CC}.
When latch-up occurs, the supply current increases rapidly, sometimes resulting in overheating and destruction. Therefore, no voltage exceeding the maximum ratings should be used.

(2) Handling unused input pins

Leaving unused input pins open may cause a malfunction. Therefore, these pins should be set to pull-up or pull-down.

(3) Setting internal connection (IC) pin

Always set IC (internal connections) open.

(4) Variations in supply voltage

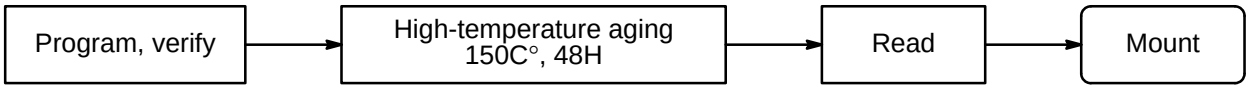
Although the specified V_{CC} supply voltage operating range is assured, a sudden change in the supply voltage within the specified range may cause a malfunction. Therefore, the voltage supply to the IC should be kept as constant as possible. The V_{CC} ripple (P-P value) at the supply frequency (50 to 60 Hz) should be less than 10% of the typical V_{CC} value, or the coefficient of excessive variation should be less than 0.1 V/ms. instantaneous change when the power supply is switched.

(5) Precautions for external clocks

It takes some time for oscillation to stabilize after changing the mode to power-on reset (option selection) and stop. Consequently, an external clock must be input.

(6) Recommended screening conditions

High-temperature aging is recommended for screening before OPTROM-mounted microcontrollers are mounted.



- Writing yield
  The test for writing all bits cannot be executed for microcontrollers where the OPTROM microcomputer program is not written. Therefore, the 100% writing yield may not be always assured.

(7) Sequence for application of power and analog inputs to A/D converter

Power supplies (AV_{CC} and AV_{SS}) and analog inputs (AN0 to ANB) to the A/D converter should be turned on after or at the same time the digital power supply (V_{CC}) is turned on.

When the power supplies is turned off, the digital power supply (V_{CC}) should be turned off and the power supplies (AV_{CC} and AV_{SS}) and analog inputs (AN0 to ANB) to the A/D converter are turned off.

2. HARDWARE CONFIGURATION

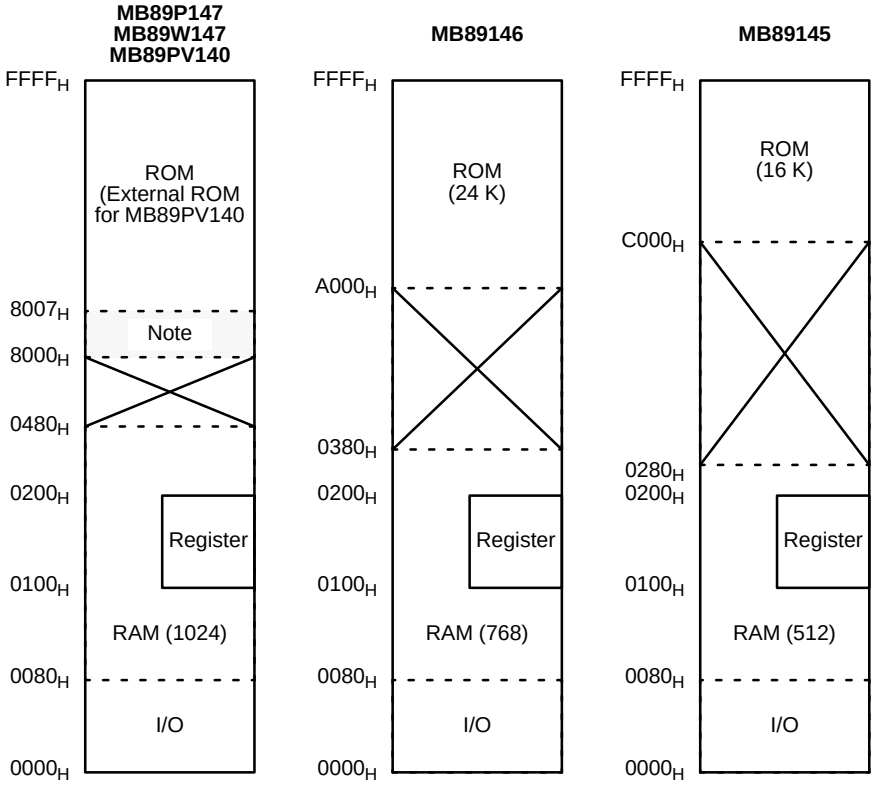
CPU

2.1 CPU

● This section describes the memory space and register composing CPU hardware.

■ Memory Space

The MB89140 series of microcontrollers have a memory area of 64K bytes. All I/O, data, and program areas are located in this space. The I/O area is near the lowest address and the data area is immediately above it. The data area may be divided into register, stack, and direct-address areas according to the applications. The program area is located near the highest address and the tables of interrupt and reset vectors and vector-call instructions are at the highest address. Figure 2.1 shows the structure of the memory space for the MB89140 series of microcontrollers.



Note: To make the user program available between the EPROM-mounted and mask-ROM-mounted microcontrollers, no user program should be written at the option EPROM area between **8000_H** to **8006_H** (see APPENDIX 2 for details).

Fig. 2.1 Memory Space of MB89140 Series of Microcontrollers

CPU

- I/O area

This area is where various resources such as control and data registers are located. The memory map for the I/O area is given in APPENDIX A.

- RAM area

This area is where the static RAM is located. Addresses from **0100_H** to **$01FF_H$** are also used as the general-purpose register area.

- ROM area

This area is where the internal ROM is located. Addresses from **$FFC0_H$** to **$FFFF_H$** are also used for the table of reset and vector-call instructions. Table 2-1 shows the correspondence between each interrupt number or reset and the table addresses to be referenced for the MB89145 series of microcontrollers.

Table 2-1 Table of Reset and Interrupt Vectors

	Table address	
	Upper data	Lower data
CALLV #0	$FFC0_H$	$FFC1_H$
CALLV #1	$FFC2_H$	$FFC3_H$
CALLV #2	$FFC4_H$	$FFC5_H$
CALLV #3	$FFC6_H$	$FFC7_H$
CALLV #4	$FFC8_H$	$FFC9_H$
CALLV #5	$FFCA_H$	$FFCB_H$
CALLV #6	$FFCC_H$	$FFCD_H$
CALLV #7	$FFCE_H$	$FFCF_H$

	Table address	
	Upper data	Lower data
Interrupt #11	$FFE4_H$	$FFE5_H$
Interrupt #10	$FFE6_H$	$FFE7_H$
Interrupt #9	$FFE8_H$	$FFE9_H$
Interrupt #8	$FFEA_H$	$FFEB_H$
Interrupt #7	$FFEC_H$	$FFED_H$
Interrupt #6	$FFEE_H$	$FFEF_H$
Interrupt #5	$FFF0_H$	$FFF1_H$
Interrupt #4	$FFF2_H$	$FFF3_H$
Interrupt #3	$FFF4_H$	$FFF5_H$
Interrupt #2	$FFF6_H$	$FFF7_H$
Interrupt #1	$FFF8_H$	$FFF9_H$
Interrupt #0	$FFFA_H$	$FFFB_H$
Reset mode	———	$FFFD_H$
Reset vector	$FFFE_H$	$FFFF_H$

Note: $FFFC_H$ is already reserved.

CPU

■ Arrangement of 16-bit Data in Memory

When the MB89140 series of microcontrollers handle 16-bit data, the data written at the lower address is treated as the upper data and that written at the next address is treated as the lower data as shown in Figure 2.2.

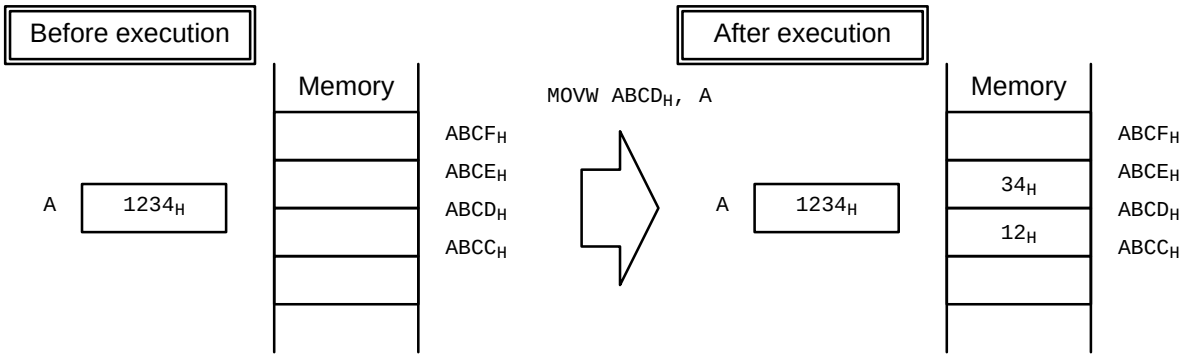


Fig. 2.2 Arrangement of 16-bit Data in Memory

This is the same as when 16-bits are specified by the operand during execution of an instruction. Bits closer to the OP code are treated as the upper byte and those next to it are treated as the lower byte. This is also the same when the memory address or 16-bit immediate data is specified by the operand.

[Example]

```
MOV A, 5678H          ; Extended address
MOV A, #1234H         ; 16-bit immediate data
```

Assemble

```
      ⋮
XXXXH XX XX
XXXXH 60 56 78        ; Extended address
XXXXH E4 12 34        ; 16-bit immediate data
XXXXH XX
      ⋮
```

Fig. 2.3 Arrangement of 16-bit Data during Execution of Instruction

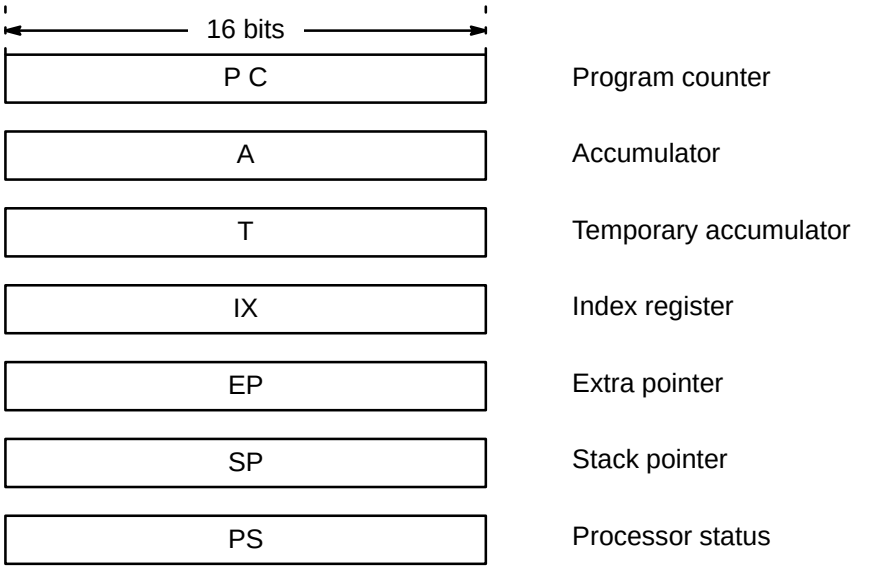
Data saved in the stack by an interrupt is also treated in the same manner.

CPU

■ Internal Registers in CPU

The MB89140 series of microcontrollers have dedicated registers in the CPU and general-purpose registers in memory.

- Program counter (PC) — 16-bit long register indicating location where instructions stored
- Accumulator (A) — 16-bit long register where results of operations stored temporarily; the lower byte is used to execute 8-bit data processing instructions.
- Temporary accumulator (T) — 16-bit long register; the operations are performed between this register and the accumulator. The lower one byte is used to execute 8-bit data processing instructions
- Stack pointer (SP) — 16-bit long register indicating stack area
- Processor status (PS) — 16-bit long register where register pointers and condition codes stored
- Index register (IX) — 16-bit long register for index modification
- Extra pointer (EP) — 16-bit long register for memory addressing



The 16 bits of the processor status (PS) can be divided into 8 upper bits for a register bank pointer (RP) and 8 lower bits for a condition code register (CCR). (See Figure 2.4.)

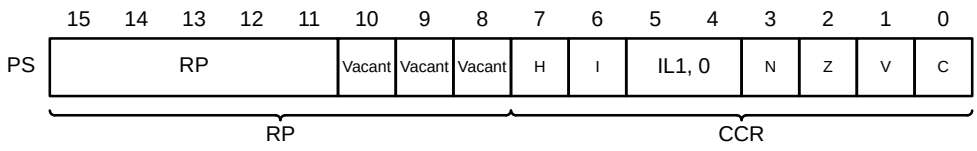


Fig. 2.4 Structure of Processor Status

CPU

The RP indicates the address of the current register bank and the contents of the RP; the real addresses are translated as shown in Figure 2.5.

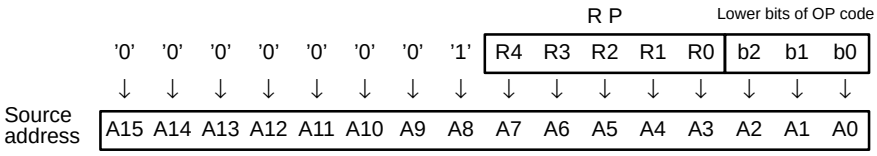


Fig. 2.5 Rule for Translating Real Addresses at General-purpose Register Area

The CCR has bits indicating the results of operations and transfer data contents, and bits controlling the CPU operation when an interrupt occurs.

- H-flag — H-flag is set when a carry or a borrow out of bit 3 into bit 4 is generated as a result of operations; it is cleared in other cases. This flag is used for decimal-correction instructions.
- I-flag — An interrupt is enabled when this flag is 1 and is disabled when it is 0. The I-flag is 0 at reset.
- IL1 and IL0 — These bits indicate the level of the currently-enabled interrupt. The CPU executes interrupt processing only when an interrupt with a value smaller than the value indicated by this bit is requested.

IL1	IL0	Interrupt level	High and low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = No interrupt

- N-flag — The N-flag is set when the most significant bit is 1 as a result of operations; it is cleared when the MSB is 0.
- Z-flag — Z-flag is set when the bit is 0 as a result of operations; it is cleared in other cases.
- V-flag — V-flag is set when a two's complement overflow occurs as a result of operations; it is reset when an overflow does not occur.
- C-flag — C-flag is set when a carry or a borrow out of bit 7 is generated as a result of operations; it is cleared in other cases. When the shift instruction is executed, the value of the C-flag is shifted out.

CPU

- General-purpose registers
  General-purpose registers are 8-bit long registers for storing data.

The 8-bit long general-purpose registers are in the register banks in memory. One bank has eight registers and up to 32 banks are available for the MB89140 series of microcontrollers, respectively. The register bank pointer (RP) indicates the currently-used bank.

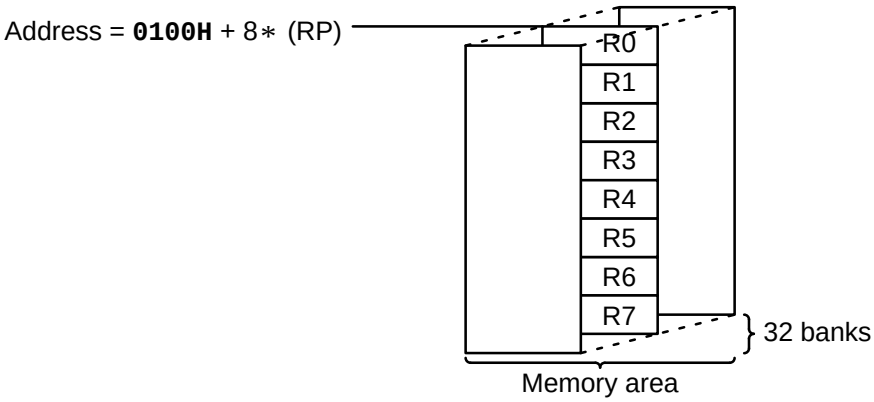


Fig. 2.6 Register Bank Configuration

CPU

■ Operation Modes

The MB89140 series of microcontrollers is used in the single-chip mode.

The memory map for each mode is as follows:

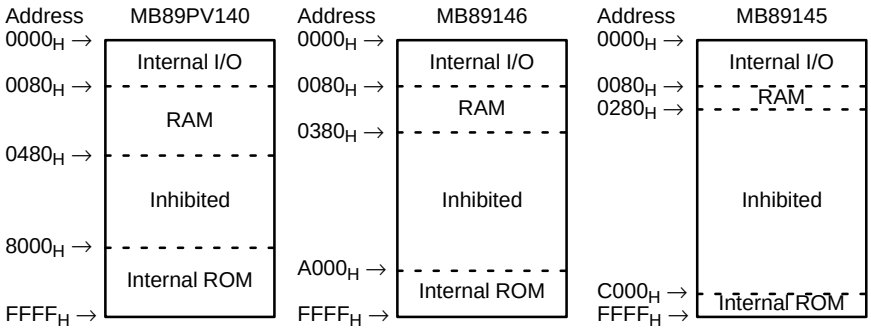


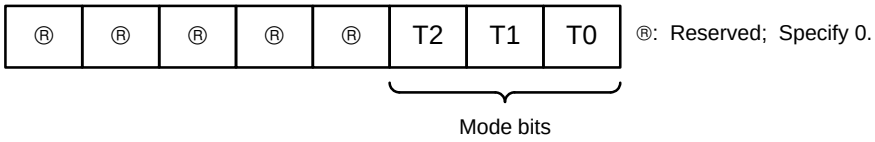
Fig. 2.7 Memory Map in Various Modes

The mode that the device enters depends on the states of the device-mode pins and the contents of the mode data fetched during the reset sequence.

The relationship between the states and operations of the device-mode pins is shown below.

MODA	Description
0	Reset vectors are read from the internal ROM.
1	Write mode for products containing EPROM.

The mode data should be set as follows:

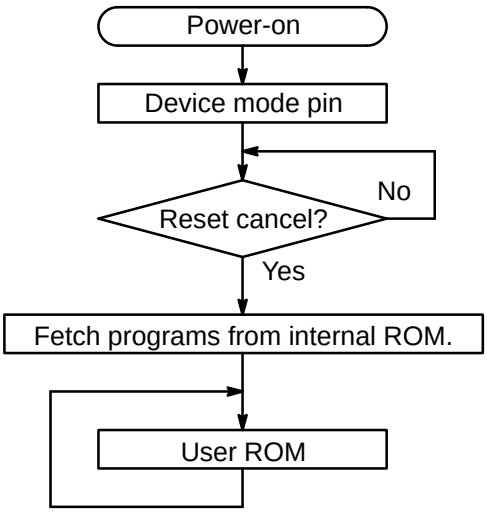


T2	T1	T0	Operation
0	0	0	Select single-chip mode.
Other than above			Reserved. Do not set.

CPU

As shown in the flowchart below, the single-chip mode is set according to the status of the device mode pins and the mode data fetched during the reset sequence.

Setting procedure	Mode selected	Mode pin	Mode data
(1)→(2)	Single-chip mode	0	XXXXX000



(1) Set 0 at the MODA pin.

(2) All pin ports fetch internal mode data and reset vectors.

MAIN/SUBCLOCK CONTROL BLOCK

2.2 MAIN/SUB CLOCK CONTROL BLOCK

● This block controls the standby operation, oscillation stabilization time, software reset, and clock switching.

■ Block Diagram

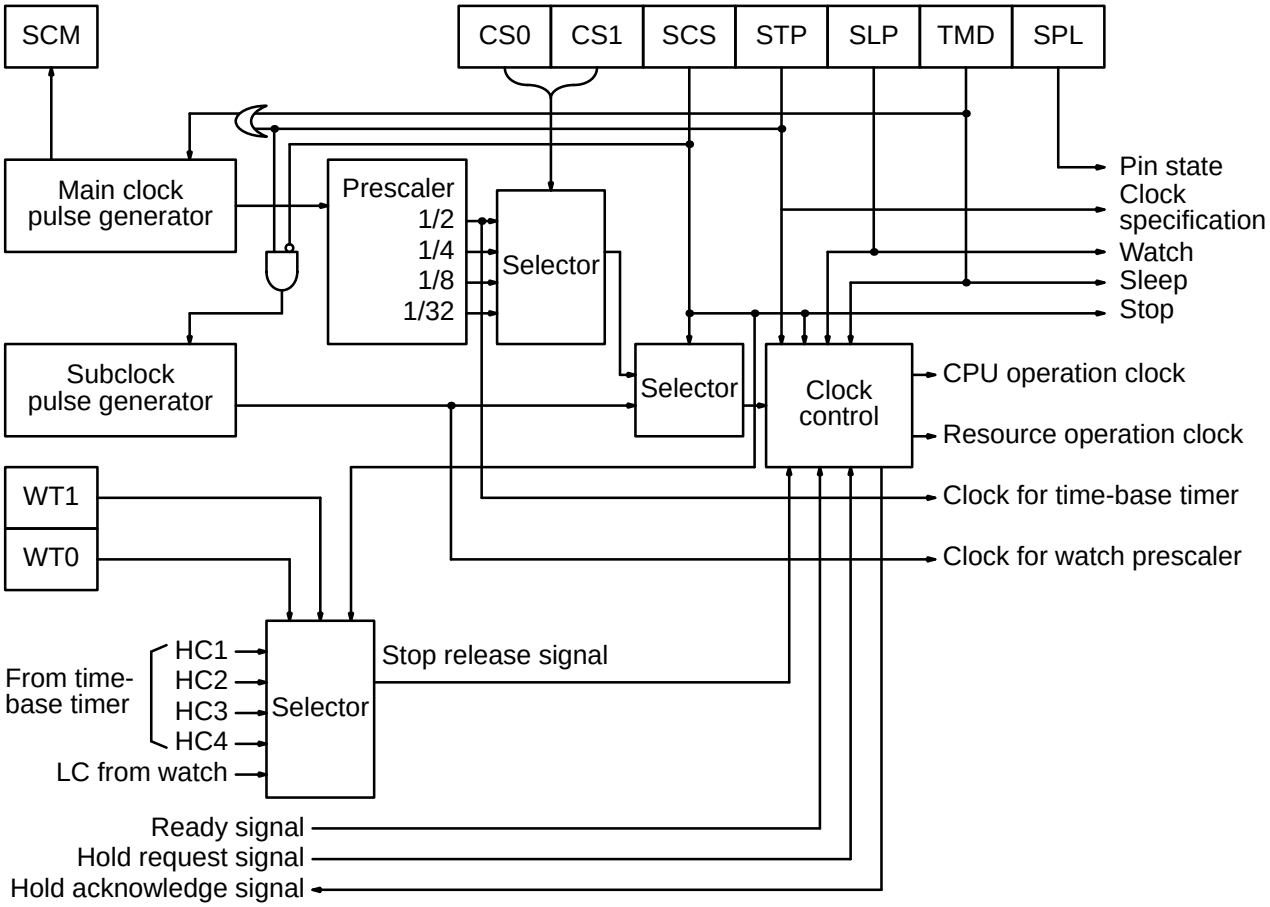
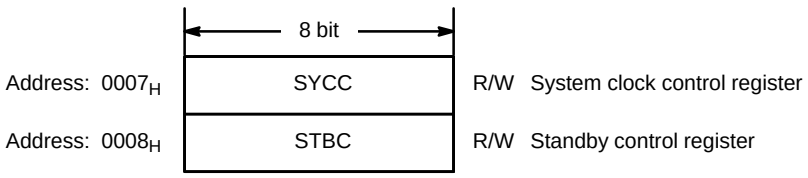


Fig. 2.8 Machine Clock Control Block Diagram

■ Register List

Main/sub clock control block consists of standby control register (STBC) and system clock control register (SYCC).



MAIN/SUBCLOCK CONTROL BLOCK

Address: 0007_H SYCC

Address: 0008_H STBC

■ Description of Registers

The detail of each register is described below.

(1) Standby-control register (STBC)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0008_H	STP	SLP	SPL	RST	TMD	—	—	—
	(W)	(W)	(R/W)	(W)	(W)			

Initial value
$00010XXX_B$

[Bit 7] STP: Stop bit
This bit is used to specify switching CPU to the stop mode.

0	No operation
1	Stop mode

This bit is cleared at reset or stop cancellation.
0 is always read when this bit is read.

[Bit 6] SLP: Sleep bit
This bit is used to specify switching the CPU and resources to the sleep mode.

0	No operation
1	Sleep mode

This bit is cleared at reset, sleep or stop cancellation.
0 is always read when this bit is read.

[Bit 5] SPL: Pin state specifying bit
This bit is used to specify the external pin state in the stop mode.

0	Holds state and level immediately before stop mode
1	High impedance

This bit is cleared at resetting.

[Bit 4] RST: Software reset bit
This bit is used to specify the software reset.

0	Generates 16-cycle reset signal
1	No operation

1 is always read when this bit is read.

Note: If a software reset is performed during operation in a submode, an oscillation stabilization period is required to switch to the main mode. Therefore, a reset signal is output during the oscillation stabilization period.

MAIN/SUBCLOCK CONTROL BLOCK

[Bit 3] TMD: Watch bit
This bit is used to specify switching to the watch mode.

0	No operation
1	Watch mode

Writing at this bit is possible only in the submode (SCS = 0). 0 is always read when this bit is read. This bit is cleared at an interrupt request or reset.

Address: 0007_H SYCC

Address: 0008_H STBC

(2) System clock control register (SYCC)

This register controls the clock for operating the CPU and resources.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0007_H	SCM	—	—	WT1	WT0	SCS	CS1	CS0
	(R)			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
	Initial value X--MM100$_B$							

[Bit 7] SCM: System clock monitor bit
This bit is used to check whether the current system clock is the main clock or subclock.

0	Subclock (Main clock is stopping or oscillation of main clock stablizing)
1	Main clock

[Bits 4 and Bit 3] WT1 and WT0: Oscillation stabilization time select bits
These bit are used to select the oscillation stabilization wait time of the main clock.

WT1	WT0	Oscillation stabilization time	Oscillation stabilization time with 8 MHz source clock
1	1	Approximate $2^{18}/f_{CH}$	32.8 ms
1	0	Approximate $2^{17}/f_{CH}$	16.4 ms
0	1	Approximate $2^{14}/f_{CH}$	2.0 ms
0	0	Approximate $2^4/f_{CH}$	0 ms

f_{CH}: Oscillation frequency of main clock

If the main mode is specified by the system clock select bit (SCS), the mode switches to main mode after the selected wait time has elapsed.

The oscillation stabilization time after resetting is determined by the initial value.

This bit should not be rewritten during oscillation stabilization or concurrently with switching of the sub-clock to the main clock.

The oscillation stabilization time for the main clock is generated by dividing the frequency of the main clock. Since the oscillation cycle is unstable immediately after oscillation starts, the above times should be used as the standard.

MAIN/SUBCLOCK CONTROL BLOCK

[Bit 2] SCS: System clock select bit
This bit is used to select the system clock mode.

0	Selects subclock (32.768 kHz) mode
1	Selects main clock (8 MHz) mode

[Bits 1 and 0] CS1 and CS0: System clock select bits (Gear function)
If the main mode is specified by the system clock select bit (SCS), the system clock is as given in the table below.

CS1	CS0	Instruction cycle	Instruction execution time at 8 MHz source clock
0	0	$64/f_{CH}$	8.0 µs
0	1	$16/f_{CH}$	2.0 µs
1	0	$8/f_{CH}$	1.0 µs
1	1	$4/f_{CH}$	0.5 µs

f_{CH}: frequency of main clock

MAIN/SUBCLOCK CONTROL BLOCK

■ Description of Operation

Main/sub clock block has normal and low-power consumption mode. The low-power consumption mode are described below.

(1) Low-power consumption mode

This chip has three operation modes. The sleep mode, and stop mode in the table below reduce the power consumption. In the main mode, four system clocks can be selected according to the system condition to minimize power consumption.

Table 2-2 Operating State of Low-power Consumption Modes

Clock mode of CPU	(CS1, CS0)	State mode	Clock pulse		Each operating clock pulse (3 MHz main clock)				Wake-up source in each mode
			Main	Sub	CPU	Time-base timer	Each resource	Clock	
Main mode	(1, 1)	RUN	Oscillates	Oscillates	4 MHz	4 MHz	4 MHz	32.768 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP	Stops			Stops	Stops		External interrupt
	(1, 0)	RUN	Oscillates	Oscillates	2.0 MHz	4 MHz	2.0 MHz	32.768 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP	Stops			Stops	Stops		External interrupt
	(0, 1)	RUN	Oscillates	Oscillates	1.0 MHz	4 MHz	1.0 MHz	32.768 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP	Stops			Stops	Stops		External interrupt
	(0, 0)	RUN	Oscillates	Oscillates	250 kHz	4 MHz	250 kHz	32.768 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP	Stops			Stops	Stops		External interrupt
Submode	—	RUN	Stops	Oscillates	32.768 kHz	Stops	32.768 kHz	32.768 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP		Stops			Stops	Stops	External interrupt
Watch mode			Stops	Oscillates	Stops	Stops	Stops	32.768 kHz	Watch external interrupt

- The submode stops oscillation of the main clock.
- The SLEEP mode stops only the operating clock pulse of the CPU; other operations are continued.
- The WATCH mode stops the functions of all chips other than the special resources.
- The STOP state stops the oscillation. Data can be held with the lowest power consumption in this mode.

MAIN/SUBCLOCK CONTROL BLOCK

(a) WATCH mode

- Switching to WATCH mode
  - Writing 1 at the TMD bit of the STBC register switches the mode to WATCH mode. Writing is invalid if 1 is set at the SCS bit (bit 2) of the SYCC register.
  - The WATCH mode stops all chip functions except the watch prescaler, external interrupt, and wake-up functions. Therefore, data can be held with the lowest power consumption.
  - The input/output pins and output pins during the WATCH mode can be controlled by the SPL bit of the STBC register so that they are held in the state immediately before entering the WATCH mode or so that they enter the high-impedance state.
  - If an interrupt is requested when 1 is written at the TMD bit , instruction execution continues without switching to the WATCH mode.
  - In the WATCH mode, the values of registers and RAM immediately before entering the WATCH mode are held.
- Canceling WATCH mode
  - The WATCH mode is canceled by inputting the reset signal and requesting an interrupt.
  - When the reset signal is input during the WATCH mode, the CPU is switched to the reset state and the WATCH mode is canceled.
  - When an interrupt higher than level 11 is requested from a resource during the WATCH mode, the WATCH mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the WATCH mode.
  - If the WATCH mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Therefore, the reset sequence is not executed unless the oscillation stabilization time is elapsed. The oscillation stabilization time will be that of the main clock selected by the WT1 and WT0 bits. However, when Power-on Reset is not specified by the mask option, the CPU is not switched to the oscillation stabilization wait state, even if the WATCH mode is canceled by inputting the reset signal.

(b) SLEEP mode

- Switching to Sleep mode
  - Writing 1 at the SLP bit (bit 6) of the STBC register switches the mode to SLEEP mode.
  - The SLEEP mode is the mode to stop clock pulse operating the CPU; only the CPU stops and the resources continue to operate.
  - If an interrupt is requested when 1 is written at the SLP bit (bit 6), instruction execution continues without switching to the SLEEP mode.
  - In the SLEEP mode, the values of registers and RAM immediately before entering the SLEEP mode are held.

MAIN/SUBCLOCK CONTROL BLOCK

- Canceling SLEEP mode
  - The SLEEP mode is canceled by inputting the reset signal and requesting an interrupt.
  - When the reset signal is input during the SLEEP mode, the CPU is switched to the reset state and the SLEEP mode is canceled.
  - When an interrupt level higher than 11 is requested from a resource during the SLEEP mode, the SLEEP mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the SLEEP mode.

(c) STOP mode

- Switching to STOP mode
  - Writing 1 at the STP bit (bit 7) of the STBC register switches the mode to STOP mode.
  - The STOP mode varies when the main clock is operating and when the subclock is operating.

    When the main clock is operating: The main clock stops but the subclock does not stop. All chip functions except the watch function stop. However, no watch interrupt can be accepted.

    When subclock is operating: Both the main clock and subclock stop. All chip functions stop.
  - The input/output pins and output pins during the STOP mode can be controlled by the SPL bit (bit 5) of the STBC register so that they are held in the mode immediately before entering the STOP mode, or so that they enter in the high-impedance state.
  - If an interrupt is requested when 1 is written at the STP bit (bit 7), instruction execution continues without switching to the STOP mode.
  - In the STOP mode, the values of registers and RAM immediately before entering the STOP mode are held.
- Canceling STOP mode
  - The STOP mode is canceled either by inputting the reset signal or by requesting an interrupt.
  - When the reset signal is input during the STOP mode, the CPU is switched to the reset state and the STOP mode is canceled.
  - When an interrupt higher than level 11 is requested from the external interrupt circuit during the STOP mode, the STOP mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the STOP mode.
  - Four oscillation stabilization times of the main clock can be selected by the WT1 and WT0 bits. The oscillation stabilization time of the subclock is fixed (at $2^{15}/f_{CH}$ — f_{CH}: frequency of subclock).

MAIN/SUBCLOCK CONTROL BLOCK

– If the STOP mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Therefore, the reset sequence is not executed unless the oscillation stabilization time is elapsed. The oscillation stabilization time corresponds to the oscillation stabilization time of the main clock selected by the WT1 and WT0 bits. However, when Power-on Reset is not specified by the mask option, the CPU is not switched to the oscillation stabilization wait state even if the STOP mode is canceled by inputting the reset signal.

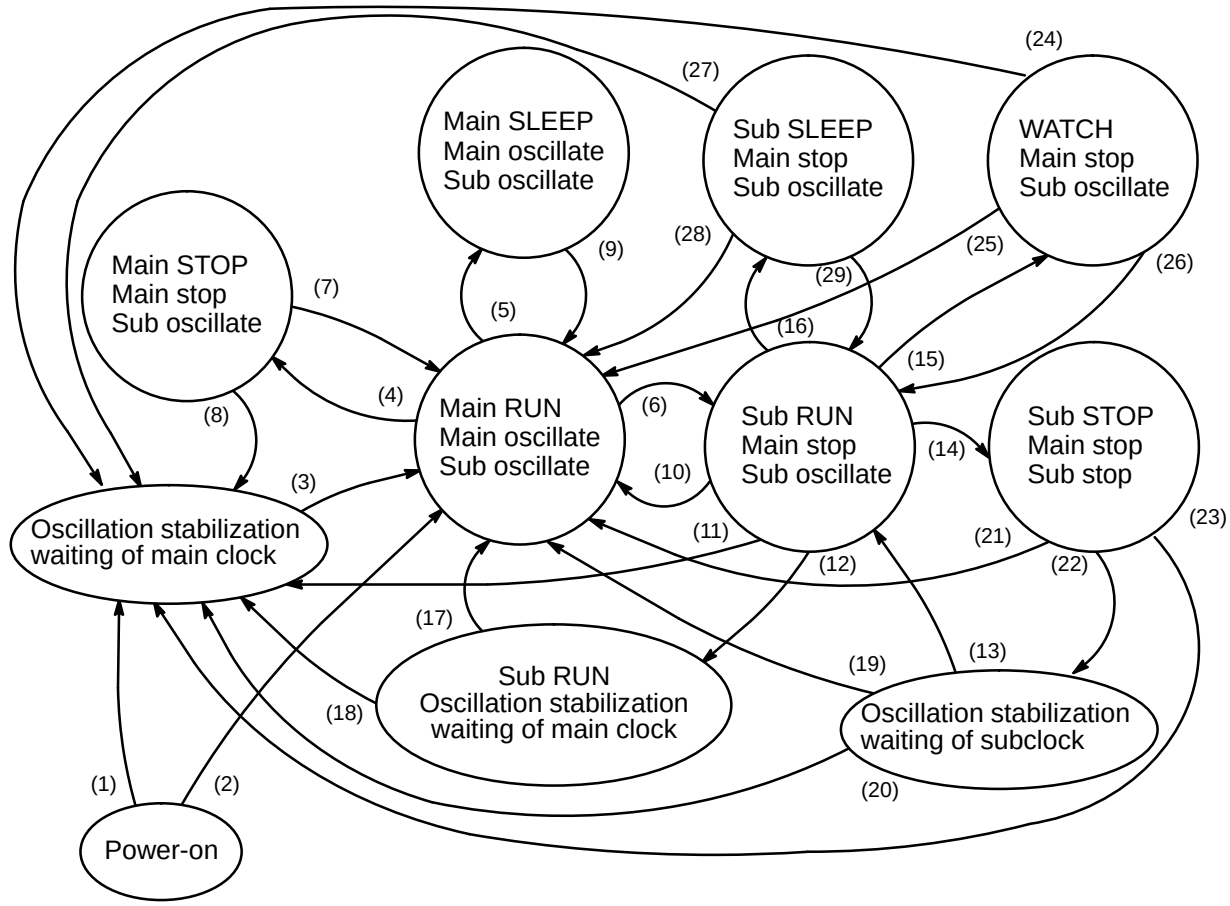
(2) Setting low power consumption mode

STBC Register			Mode
STP (Bit 7)	SLP (Bit 6)	TMD (Bit 3)	
0	0	0	Normal
0	0	1	WATCH
0	1	0	SLEEP
1	0	0	STOP
1	×	×	Disable

Note: When the mode is switched from the subclock mode to the main clock mode, do not set the Stop, Sleep, and Watch modes. If the SCS bit of the SYCC register is rewritten from 0 to 1, set the above modes after the SCM bit of the SYCC register has been set to 1.

MAIN/SUBCLOCK CONTROL BLOCK

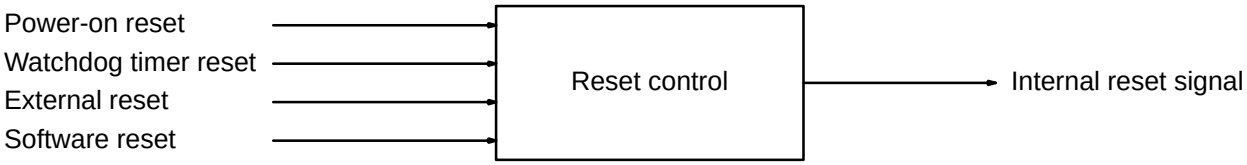
(3) State transition diagram at low power consumption mode



(1) When power-on reset option is selected
(2) When power-on reset option is not selected
(3) After oscillation stabilized
(4) Set STP bit to 1.
(5) Set SLP bit to 1.
(6) Set SCS bit to 0.
(7) External reset when power-on reset option not selected
(8) External reset or interrupt when power-on reset option selected
(9) External reset or interrupt
(10) External reset when power-on reset option not selected
(11) External reset or other reset when power-on reset option selected
(12) Set SCS bit to 1.
(13) After oscillation stabilized
(14) Set STP bit to 1.
(15) Set TMD bit to 1.
(16) Set SLP bit to 1.
(17) External reset after oscillation stabilized or when power-on reset option not selected
(18) External reset or other reset when power-on reset option selected
(19) External reset after oscillation is stabilized or when power-on reset option not selected
(20) External reset when power-on reset option selected
(21) External reset when power-on reset option not selected
(22) Interrupt
(23) External reset when power-on reset option selected
(24) External reset when power-on reset option selected
(25) External reset when power-on reset option not selected
(26) Interrupt
(27) External reset when power-on reset option selected
(28) External reset when power-on reset option not selected
(29) Interrupt

MAIN/SUBCLOCK CONTROL BLOCK

■ Reset Control Section



- Reset

There are four types of resets as shown in Table 2-3.

Table 2-3 Sources of Reset

Reset name	Description
Power-on reset	Turns power on
Watchdog reset	Overflows watchdog timer
External-pin reset	Sets external-reset pin to Low
Software reset	Writes 0 at RST (bit 4) of STBC

When the power-on reset and reset during the stop state are used, the oscillation stabilization time is needed after the oscillator operates. The time-base timer or watch prescaler controls this stabilization time. Consequently, the operation does not start immediately even after canceling the reset.

However if Power-on Reset Disabled is selected by the mask option, no oscillation stabilization time is required in any state after external pins have been released from the reset.

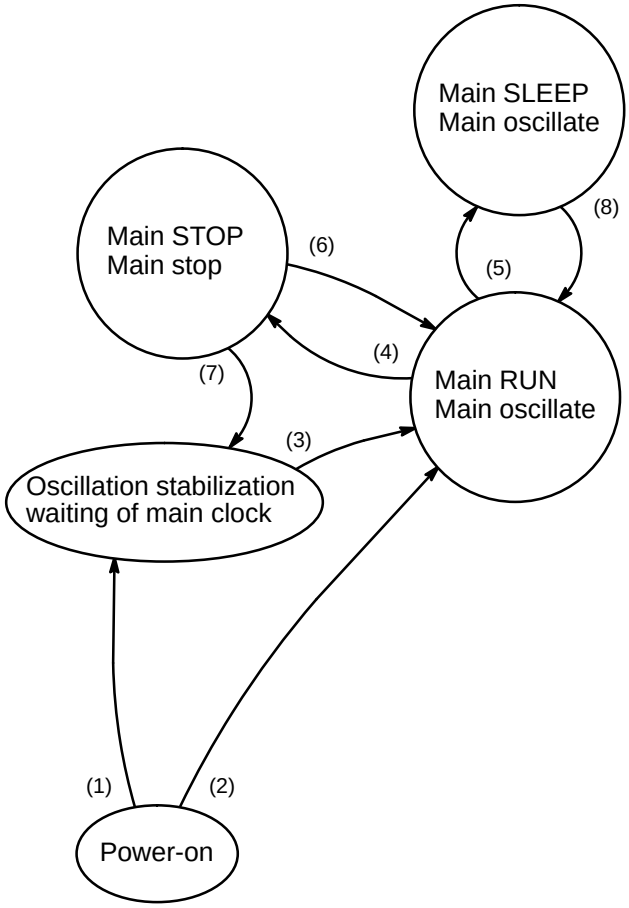
Note: If the Power-on Reset unavailable option is selected, keep the $\overline{\text{RST}}$ pin Low until the oscillation stabilization time selected in the option has elapsed after power-on.

MAIN/SUBCLOCK CONTROL BLOCK

■ Single Clock

The single clock can be selected by the mask option. In the single clock operation, the functions are the same as those of the double clock module except that the subclock mode cannot be set. In the single-circuit clock operation, the P71/X1A and P70/X0A function as input ports.

- State transition diagram



(1) When power-on reset option selected
(2) When power-on reset option not selected
(3) After oscillation stabilized
(4) Set STP bit to 1.
(5) Set SLP bit to 1.
(6) External reset when power-on reset option not selected
(7) External reset or interrupt when power-on reset option selected
(8) External reset or interrupt

INTERRUPT CONTROLLER

2.3 INTERRUPT CONTROLLER

● The interrupt controller for the F^{2}MC-8L family is located between the F^{2}MC-8L CPU and each resource. This controller receives interrupt requests from the resources, assigns priority to them, and transfers the priority to the CPU; it also decides the priority of same-level interrupts.

■ Block Diagram

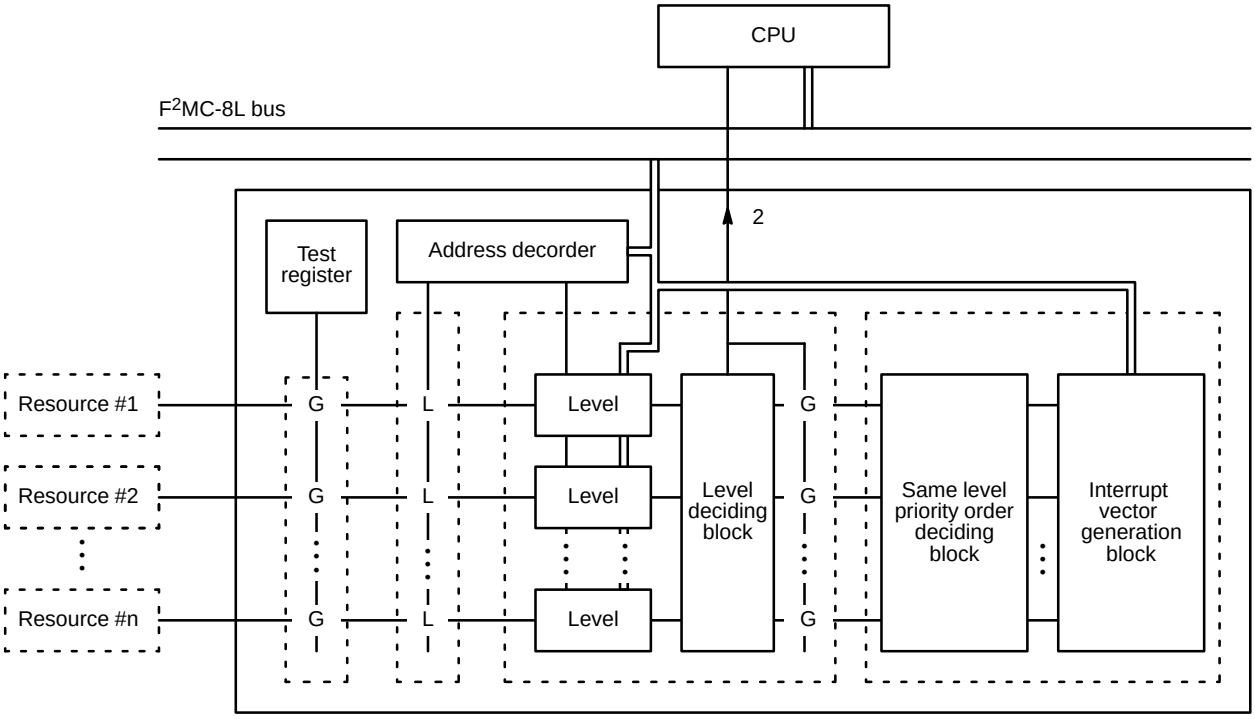
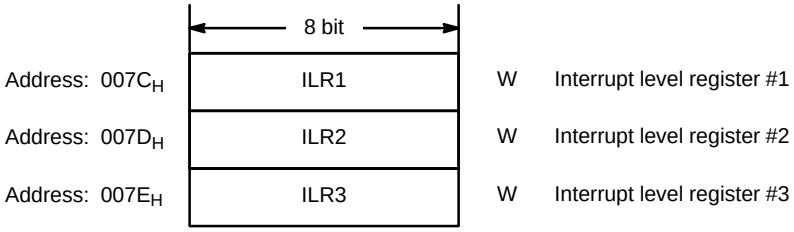


Fig. 2.9 Interrupt Controller Block Diagram

■ Register List

Interrupt controller consists of interrupt-level registers (ILR1, 2, and 3).



INTERRUPT CONTROLLER

Address: $007C_H$ ILR1

Address: $007D_H$ ILR2

Address: $007E_H$ ILR3

■ Description of Registers

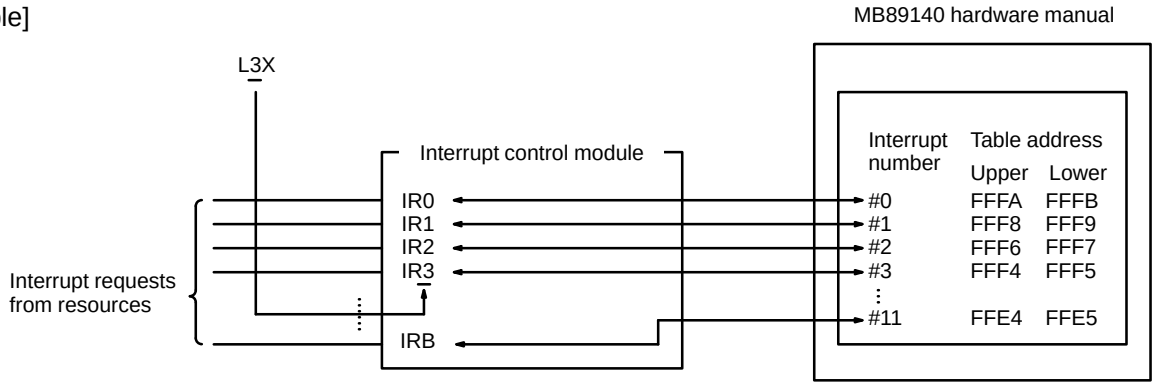
The detail of each register is described below.

- Interrupt level register (ILRX: Interrupt Level Register X)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $007C_H$	L31	L30	L21	L20	L11	L10	L01	L00
Address: $007D_H$	L71	L70	L61	L60	L51	L50	L41	L40
Address: $007E_H$	LB1	LB0	LA1	LA0	L91	L90	L81	L80
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)
								Initial value 11111111_B

The ILRX sets the interrupt level of each resource. The digits in the center of each bit correspond to the interrupt numbers.

[Example]



When an interrupt is requested from a resource, the interrupt controller transfers the interrupt level based on the value set at the 2-bits of the ILRX corresponding to the interrupt to the CPU. The relationship between the 2 bits of the ILRX and the required interrupt levels is as follows:

Lx1	Lx0	Required interrupt level
0	×	1
1	0	2
1	1	3 (None)

INTERRUPT CONTROLLER

■ Description of Operation

The functions of interrupt controllers are described below.

- Interrupt functions

The MB89140 series of microcontrollers have 12 inputs for interrupt requests from each resource. The interrupt level is set by 2-bit registers corresponding to each input. When an interrupt is requested from a resource, the interrupt controller receives it and transfers the contents of the corresponding level register to the CPU. The interrupt to the device is processed as follows:

(a) An interrupt source is generated inside each resource.
(b) If an interrupt is enabled, an interrupt request is output from each resource to the interrupt controller by referring to the interrupt-enable bit inside each resource.
(c) After receiving this interrupt request, the interrupt controller determines the priority of simultaneously-requested interrupts and then transfers the interrupt level for the applicable interrupt to the CPU.
(d) The CPU compares the interrupt level requested from the interrupt controller with the IL bit in the processor status register.
(e) As a result of the comparison, if the priority of the interrupt level is higher than that of the current interrupt processing level, the contents of the I-flag in the same processor status register are checked.
(f) As a result of the check in step (e), if the I-flag is enabled for an interrupt, the contents of the IL bit are set to the required level. As soon as the currently-executing instruction is terminated, the CPU performs the interrupt processing and transfers control to the interrupt-processing routine.
(g) When an interrupt source is cleared by software in the user's interrupt processing routine, the CPU terminates the interrupt processing.

Figure 2.10 outlines the interrupt operation for the MB89140 series of microcontrollers.

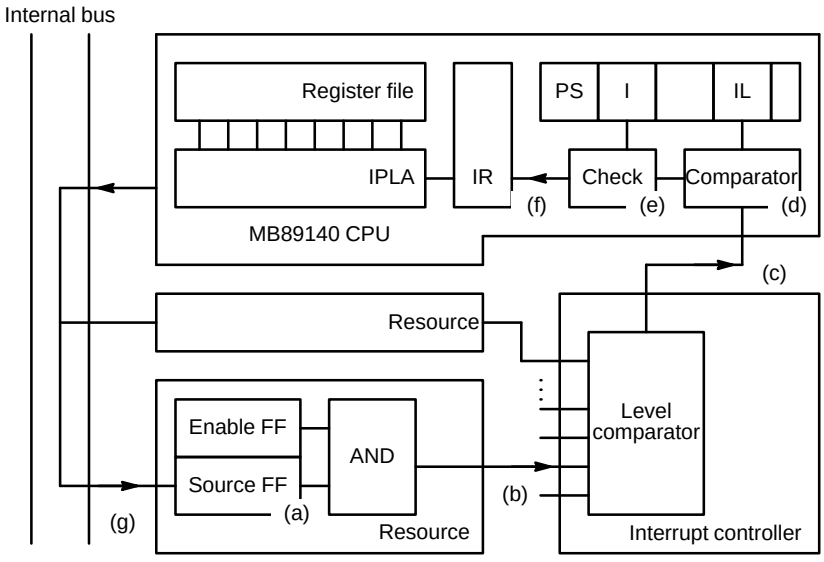


Fig. 2.10 Interrupt-processing Flowchart

I/O PORTS

2.4 I/O PORTS

- The MB89140 series of microcontrollers have eight parallel ports (55 pins, including a buzzer pin). Ports 0, 1 and 3 serve as CMOS I/O ports; port 2 serves as a CMOS output-only port; ports 4, 5 and 6 serve as P-channel open-drain high-withstand-voltage ports; port 7 serves as an input-only port. Ports 0 and 1 are also used as analog input ports.
- Ports 0, 1, 2 and 3 are also used as resources.
- The BZ pin serves as a P-channel open-drain high-withstand-voltage pin only for buzzer output.

■ List of port functions

Table 2-4 List of Port Functions

Pin name	Input type	Output type	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P00 to P07*1	CMOS (Hysteresis)	CMOS push-pull	Parallel ports 00 to 07	P07	P06	P05	P04	P03	P02	P01	P00
			Resource	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
P10 to P17*1	CMOS (Hysteresis)	CMOS push-pull	Parallel ports 10 to 17	P17	P16	P15	P14	P13	P12	P11	P10
			Resource	ADST	—	—	—	ANB	ANA	AN9	AN8
P20 to P23	—	CMOS push-pull	Parallel ports 20 to 23	—	—	—	—	P23	P22	P21	P20
			Resource	—	—	—	—	WDG	—	PWO0	—
P30 to P37	CMOS (Hysteresis)	CMOS push-pull*2	Parallel ports 30 to 37	P37	P36	P35	P34	P33	P32	P31	P30
			Resource	DTTI	PWO1	EC	SI	SO	SCK	INT1	INT0/ TRG
P40 to P47	—	P-channel open-drain high-withstand voltage	Parallel ports 40 to 47	P47	P46	P45	P44	P43	P42	P41	P40
P50 to P57	—	P-channel open-drain high-withstand voltage	Parallel ports 50 to 57	P57	P56	P55	P54	P53	P52	P51	P50
P60 to P67	—	P-channel open-drain high-withstand voltage	Parallel ports 60 to 67	P67	P66	P65	P64	P63	P62	P61	P60
P70 to P71	CMOS (Hysteresis)	—	Parallel ports 70 and 71	—	—	—	—	—	—	P71*3	P70*3

Notes:

*1 To use P07 to P00 and P13 to P10 as input ports, they must be declared for use as general-purpose input ports at the PCR0 and PCR1 registers after resetting.

*2 P31 serves as an N-channel open-drain pin.

*3 P70 and P71 serve as X0A and X1A pins when the dual-circuit is selected by the mask option.

I/O PORTS

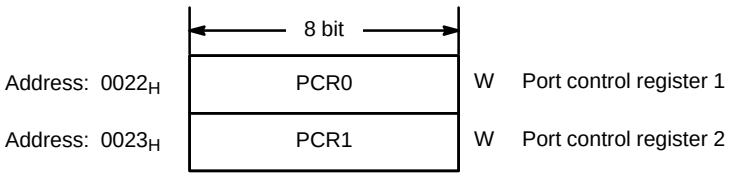
■ Register list

I/O port consists of the following registers.

Table 2-5 Port register

Register name	read/ write	Address	Initial value
Ports 00 to 07 data register (PDR0)	R/W	0000_H	$XXXXXXXX_B$
Ports 00 to 07 data direction register (DDR0)	W	0001_H	00000000_B
Ports 10 to 17 data register (PDR1)	R/W	0002_H	$XXXXXXXX_B$
Ports 10 to 17 data direction register (DDR1)	W	0003_H	00000000_B
Ports 20 to 27 data register (PDR2)	R/W	0004_H	$----0000_B$
Reserve		0005_H	
Ports 30 to 37 data register (PDR3)	R/W	$000C_H$	$XXXXXXXX_B$
Ports 30 to 37 data direction register (DDR3)	W	$000D_H$	00000000_B
Ports 40 to 47 data register (PDR4)	R/W	0010_H	00000000_B
Ports 50 to 57 data register (PDR5)	R/W	0011_H	00000000_B
Ports 60 to 67 data register (PDR6)	R/W	0012_H	00000000_B
Ports 70 to 77 data register (PDR7)	R	0013_H	$------XX_B$

■ Port control register (PCR0, PCR1)



Address: 0022_H PCR0

Address: 0023_H PCR1

- Port control register (PCR0, PCR1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0022_H	P07	P06	P05	P04	P03	P02	P01	P00
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)
								Initial value 00000000_B
Address: 0023_H	—	—	—	—	P13	P12	P11	P10
					(W)	(W)	(W)	(W)
								Initial value $----0000_B$

I/O PORTS

These registers enable P07 to P00 and P13 to P10 to be used as general-purpose port inputs after resetting. Write 1 at bits corresponding to each pin.

Register value	Status
0	Used as analog input port. Inhibited for use as general-purpose port input. 0 is read when PDR is read.
1	Used as general-purpose input port (DDR register must be to 0). Inhibited for use as analog input port.

■ Description of functions

The function of each port is described below.

(1) P00 to P07: CMOS-type I/O ports (used as analog input)
P10 to P13: CMOS-type I/O ports (used as analog input)

- Switching input and output
  These ports have a data-direction register (DDR) and port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input.
- Operation for output port (DDR = 1)
  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.
- Operation for input port (DDR = 0)
  When settings the input, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read. When 1 is written at the PCR0 and PCR1 registers, the values of corresponding pins are read as 0 (see Figure 2.11).
- State when reset
  The DDR is initialized to 0 by resetting and the output impedance goes High at all bits. The PDR is not initialized by resetting. Therefore, set the PDR value before setting the DDR to output. After resetting, each port is inhibited for use as an input port, which is fixed to Low (see Figure 2.11). When using as an input port, each port must be declared for use as an input port by writing 0 at the corresponding bits of the PCR0 and PCR1 registers.
- State in stop modes
  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR.

I/O PORTS

- Analog input
  When using as an analog input, set 0 at the DDR to turn off the output transistor. If the bits of the PCR0 and PCR1 registers corresponding to the ports to be used as analog inputs are 1, write 0 at these registers to inhibit use as general-purpose input ports. At this time, 0 is always read even if the value of each port is read (input ports cannot be read).

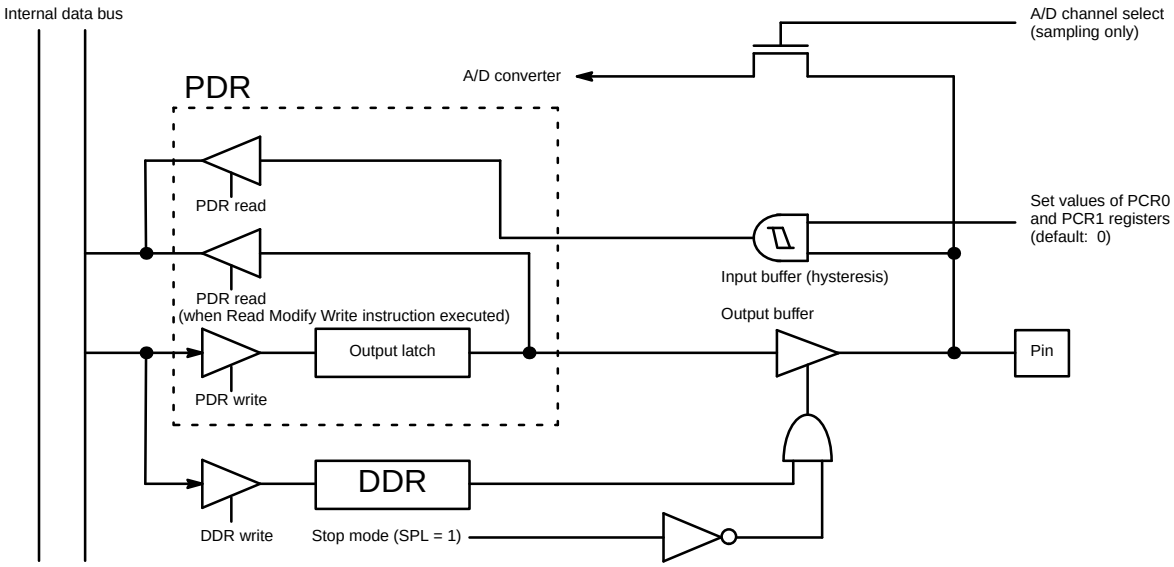


Fig. 2.11 Ports 00 to 07 and 10 to 13

(2) P14 to P16: CMOS-type I/O ports

- Switching input and output
  These ports have a data-direction register (DDR) and port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input.
- Operation for output port (DDR = 1)
  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.
- Operation for input port (DDR = 0)
  When settings the input, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.
- State when reset
  The DDR is initialized to 0 by resetting and the output impedance goes High at all bits. The PDR is not initialized by resetting. Therefore, set the value of the PDR before setting the DDR to output.

I/O PORTS

- State in stop modes
  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR.

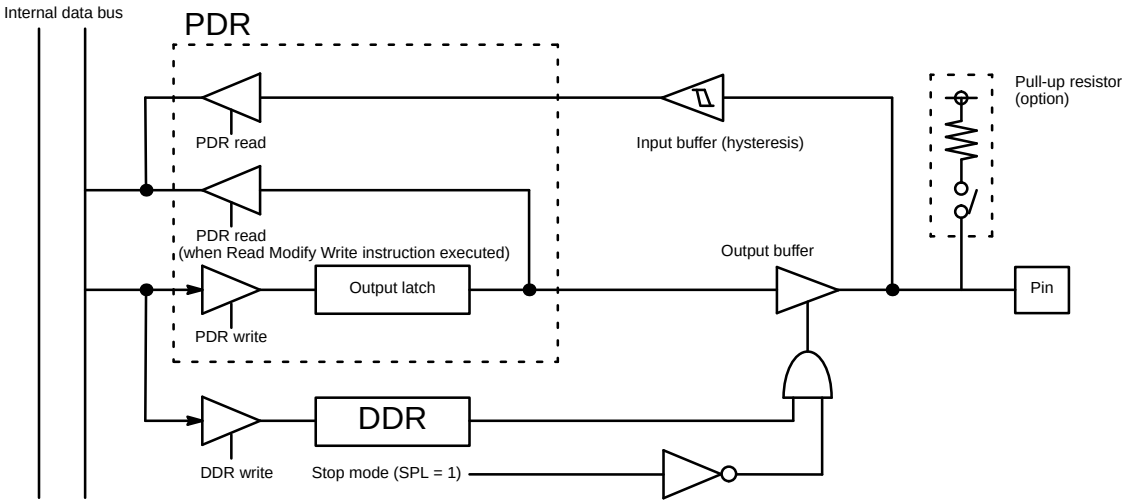


Fig. 2.12 Ports 14 to 16

(3) P20 to P23: CMOS-type output ports
(used as resource output, excluding P20 and P22)

- Operation for output port
  The value written at the PDR is output to the pin. Since the content of the output latch is always read when the PDR is read, the bit-processing instruction can be used even if the output level varies with load.
- Resource output operation (P23 and P21)
  When using as the resource output, setting is performed by the resource output enable bit. (See the description of each resource.)
- State when reset
  At reset, all pins are set to High impedance. When a vector is fetched, the output from each port is enabled and all pins start serving as output ports. At reset, the PRD is initialized to 0 and Low level is output at all pins.
- State in stop modes
  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR.

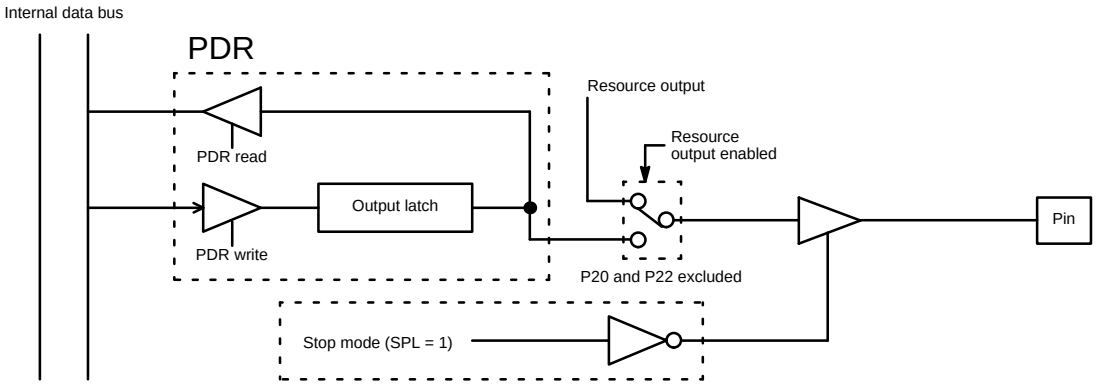


Fig. 2.13 Ports 20 to 23

I/O PORTS

(4) P70 and P71: CMOS-type input ports

- Input port operation
  The PDR can only be read and the value of the pin is always read.

Note: When the dual-circuit clock option is selected, P71 and P70 serve as X1A and X0A pins.

- State when reset
  The PDR cannot be initialized by reset.

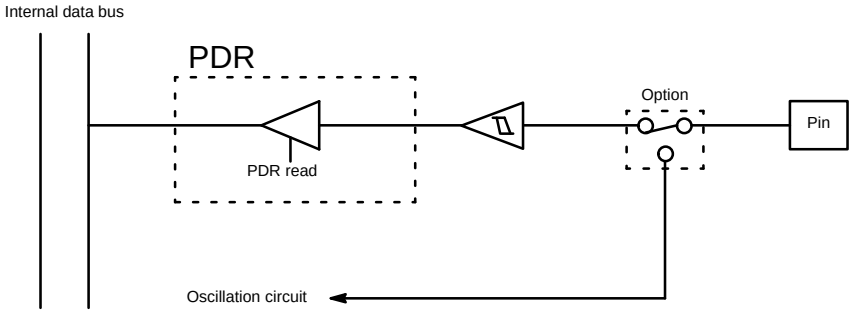


Fig. 2.14 Ports 70 and 71

(5) P30 and P32 to P35 and P17: CMOS type I/O ports
(also used as resource I/O)

- Switching input and output
  This port has a data-direction register (DDR) and a port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input.

- Operation for output port (DDR = 1)
  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

- Operation for input port (DDR = 0)
  When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

- Resource output operation
  When using as the resource output, setting is performed by the resource output enable bit. (See the description of each resource.) Since the resource output enable bit has priority in switching input and output, even if the DDR is set to 0, any bit is set as the resource output when output is enabled at each resource. Even if the output from each resource is enabled, the read value of the port is effective, so the resource output value can be checked.

I/O PORTS

- Resource input operation
  The pin value at a port with the resource input function is always input for the resource input irrespective of the setting of the DDR and resource. Set the DDR to input when using an external signal for the resource input.
- State when reset
  When reset, the DDR is initialized to 0 and the output impedance goes High at all bits. When reset, the PDR is not initialized. Therefore, set the value of the PDR before setting the DDR to output.
- State in stop modes
  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR.

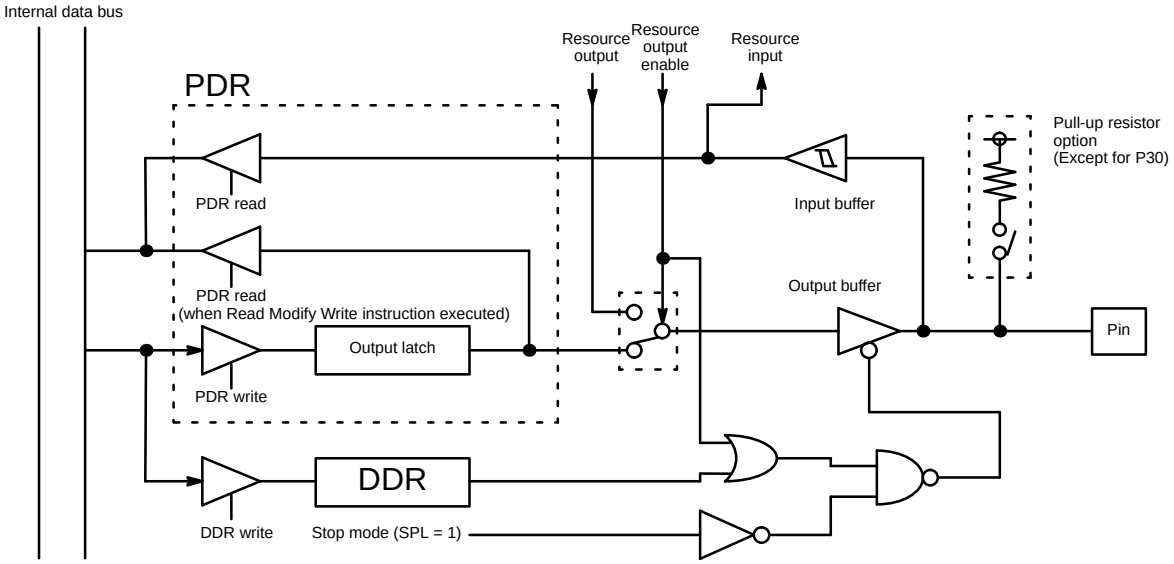


Fig. 2.15 Ports 35 to 32, 30 and 17

(6) P31: N-ch open-drain-type ports (also used as resource input)

- Switching input and output
  This port has a data-direction register (DDR) and a port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input.
- Operation for output port (DDR = 1)
  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

I/O PORTS

- Operation for input port (DDR = 0)
  When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.
- Resource input operation
  This pin is used both as a resource input and as a port. The value of the pin is always input to the port serving as the resource input (irrespective of the setting conditions of the PDR and resource). When using an external signal at the resource, set the DDR to 0.
- State when reset
  When reset, the DDR is initialized to 0 and the output impedance goes High at all bits. When reset, the PDR is not initialized. Therefore, set the value of the PDR before setting the DDR to output.
- State in stop modes
  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR.

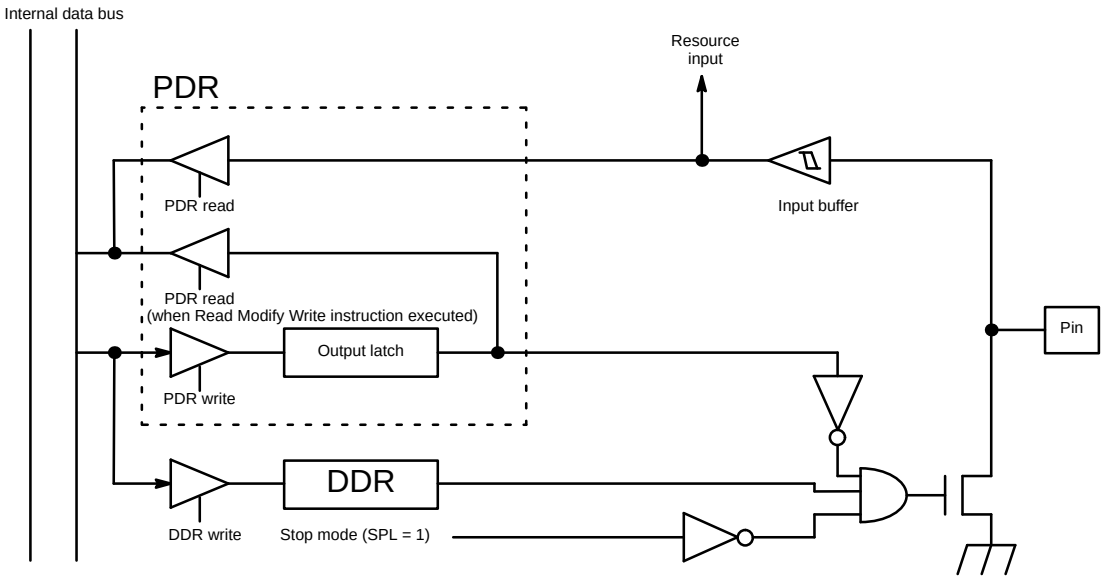


Fig. 2.16 Port 31

(8) P40 to P47: P-ch open-drain high-withstand-voltage output ports
P50 to P57: P-ch open-drain high-withstand-voltage output ports
P60 to P67: P-ch open-drain high-withstand-voltage output ports

- Operation for output port
  The value written at the PDR is output to the pin. When the PDR is read in this port, usually, the contents of the output latch is read instead of the value of the pin.
- State when reset
  The PDR is initialized to 0 at reset, so the output register is turned off at all bits.

I/O PORTS

- State in watch mode
  When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

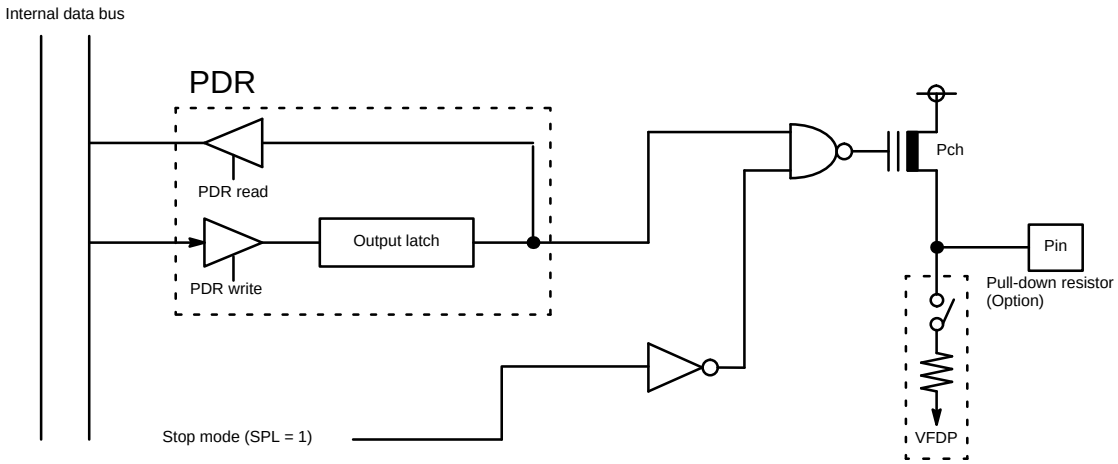


Fig. 2.17 Ports 40 to 47, 50 to 57 and 60 to 67

(9) BZ: P-ch open-drain high-withstand-voltage output

- Buzzer output
  A waveform at the frequency set by the buzzer register (BUZR) is output to the pin.
- State when reset
  When reset, the buzzer register (BUZR) is initialized to 0 and the output impedance goes High.
- State in Stop mode
  With the SPL bit of the standby control register is set to 1, the output impedance goes High irrespective of the BUZR value.

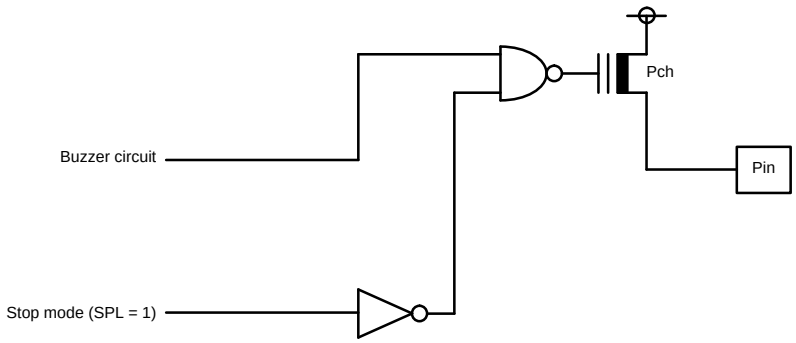


Fig. 2.18 BZ

WATCH PRESCALER

2.5 WATCH PRESCALER

- This prescaler has a 15-bit binary counter
- Four interval times and three clock pulses can be selected.
- This function cannot be used when the single clock module is selected by the mask option.

■ Block Diagram

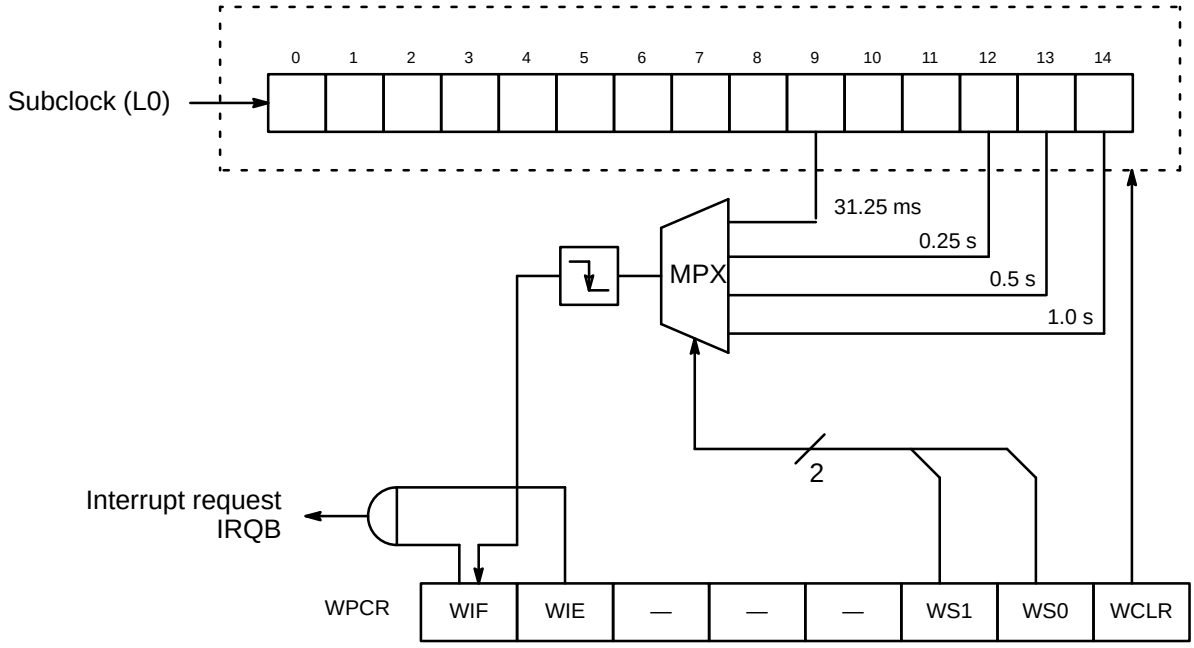
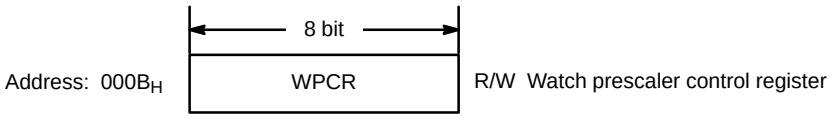


Fig. 2.19 Watch Prescaler Block Diagram

■ Register list

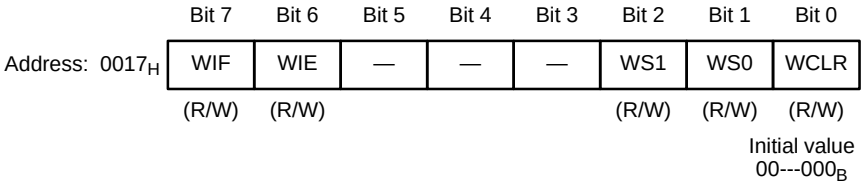


■ Description of Registers

The detail of watch prescaler is described below.

Address: 000B$_H$ WPCR

• Watch prescaler control register (WPCR)



WATCH PRESCALER

[Bit 7] WIF: Watch interrupt flag
When writing, this bit is used to clear the watch interrupt flag.

0	Clears watch interrupt flag
1	No operation

When reading, this bit indicates that the watch interrupt has occurred.

0	Watch interrupt not occurred
1	Watch interrupt occurred

1 is read when the Read Modify Write instruction is read. If the WIF bit is set to 1 when the WIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 6] WIE: Watch interrupt enable bit
This bit is used to enable an interrupt by the watch.

0	Interrupt by watch disabled
1	Interrupt by watch enabled

[Bit 1 and 0] WS1, WS0: Interrupt interval time specification bit by watch
These bits are used to specify the interrupt cycles.

WS1	WS0	Interrupt cycle	Value at f_{CL} = 32.768 kHz
0	0	$2^{10}/f_{CL}$	31.25 ms
0	1	$2^{13}/f_{CL}$	0.25 s
1	0	$2^{14}/f_{CL}$	0.50 s
1	1	$2^{15}/f_{CL}$	1.00 s

f_{CL}: Subclock oscillation frequency

[Bit 0] WCLR: Bit clearing watch prescaler
This bit is used to clear the watch prescaler.

0	Watch prescaler cleared
1	No operation

1 is always read when this bit is read.

WATCHDOG TIMER RESET

2.6 WATCHDOG TIMER RESET

● Either of a signal output from the time-base timer for counting with the main clock or a signal output from the watch prescaler for counting with the subclock can be selected as a clock. It is possible to select whether or not a watchdog time-out detect signal is output (only when power-on reset available option selected).

■ Block Diagram

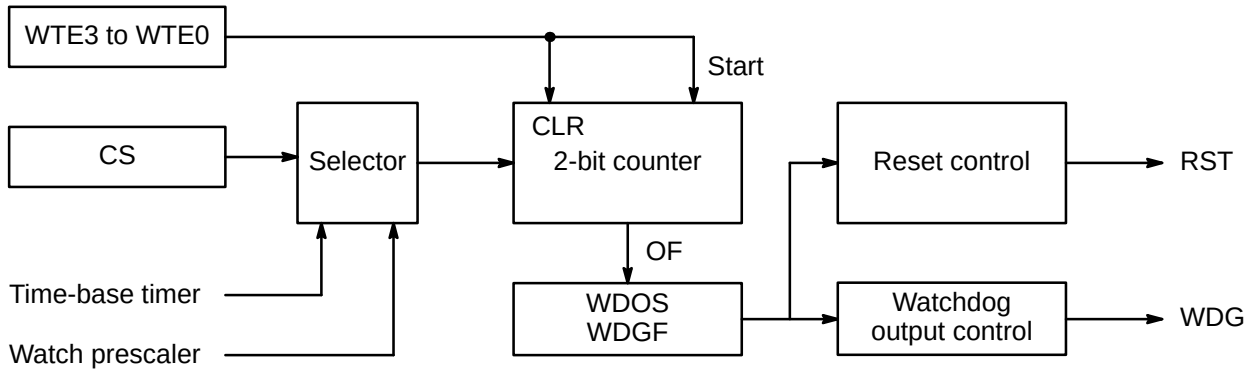
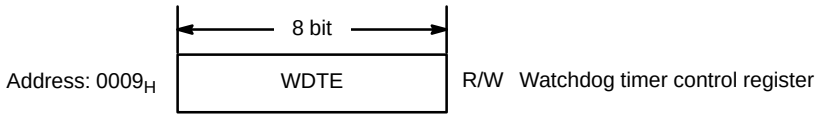


Fig. 2.20 Watchdog Timer Reset Block Diagram

■ Registers

The watchdog timer reset has watchdog timer control register (WDTE).

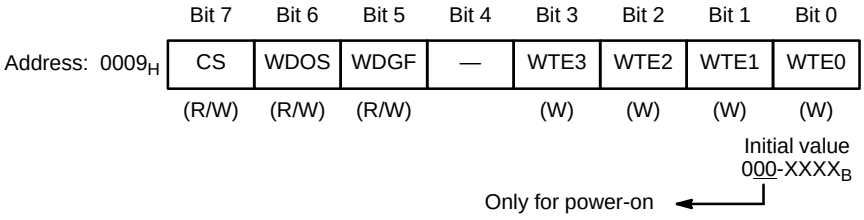


■ Description of Register

The detail of the watchdog timer control register (WDTE) is described below.

Address: 0009_H WDTE

• Watchdog timer control register (WDTE)



WATCHDOG TIMER RESET

[Bit 7] CS: Clock source switching bit
This bit is used to select a count clock from either the watch prescaler or time-base timer.

0	Time-base timer cycle = $1/2^{22}$ /f_{CH}
1	Watch prescaler cycle = $1/2^{14}$ /f_{CL}

f_{CH}: Main clock frequency
f_{CL}: Subclock frequency

Note: Set this bit as soon as the watchdog timer is started. Do not change the bit after the timer is started. When using the submode, always select the watch prescaler. Do not select the watchdog prescaler for the single-circuit clock.

[Bit 6] WDOS: Watchdog output select bit
Bit 6 is used to select output from the pin when the watchdog timer causes a time-out. (This function cannot be used when the power-on reset unavailable option is selected, write 0 in this case.)

0	Output from $\overline{RST}$ pin (P23 as general-purpose output pin; reset occurs)
1	Output from P23/WDG pin (reset does not occur)

Note: This bit is not cleared by the reset conditions. This register is cleared only by a power-on reset.

[Bit 5] WDGF: Watchdog output set bit
Bit 5 is set to 1 when a time-out of the watchdog timer is detected. In this case, the WDG signal is output when the WDOE is 1. Clearing this bit stops output of the WDG signal. (This function cannot be used when the power-on reset unavailable option is selected, write 0 in this case).

The meaning of each bit to be read is as follows:

0	No operation
1	Time-out detected by watchdog timer (WDG output)

1 is always read when the Read Modify instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change or affect other bits.

Note: This bit is not cleared by the reset conditions. This register is cleared only by a power-on reset.

WATCHDOG TIMER RESET

[Bits 3 to 0] WTE3 to WTE0: Watchdog timer control bit
These bits are used to control the watchdog timer.

First write only after reset

0101	Watchdog timer started
Other than the above	No operation

Second and later write

0101	Watchdog timer counter cleared
Other than the above	No operation

The watchdog timer can be stopped only by reset. 1111 is read when these bit are read.

■ Description of operation

The watchdog timer enables detection of a program malfunction.

(1) Starting watchdog timer

The watchdog timer starts when 0101 is written at the watchdog timer control bits.

(2) Clearing watchdog timer

When 0101 is written at the watchdog timer control bits after start, the watchdog timer is cleared. The counter of the watchdog timer is cleared when changing to the standby mode (STOP, SLEEP, WATCH).

(3) Watchdog timer reset

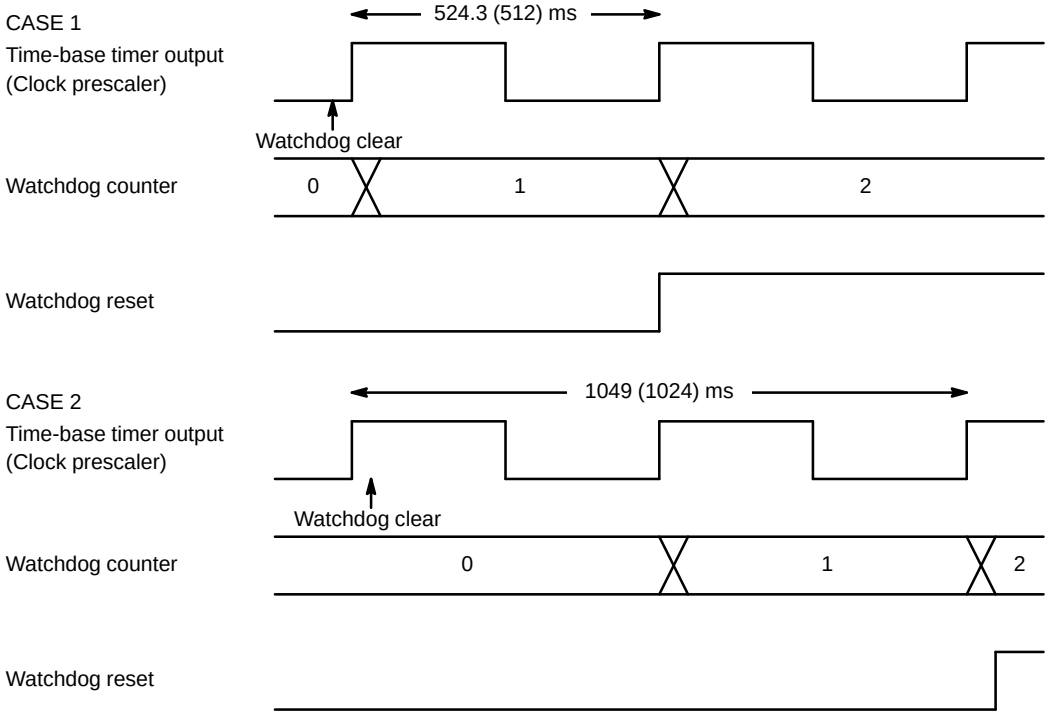
If the watchdog timer is not cleared within the time given in the table below, a watchdog timer reset occurs to reset the chip internally.

	Clock source	
	Time-base timer	**Watch prescaler**
Minimum time	Approx. 524.3 ms	Approx. 512 ms
Maximum time	Approx. 1049 ms	Approx. 1024 ms

Main clock: 8 MHz clock
Subclock: 32.768 kHz clock

WATCHDOG TIMER RESET

The relationship between the 2-bit counter of the watchdog timer and the time-base timer (clock prescaler) is as follows:

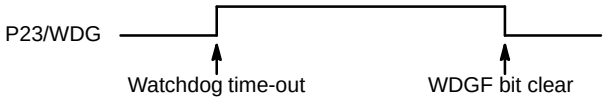


As shown above, the interval time of the watchdog timer changes as shown in the above table according to the watchdog reset timing.

(4) Stopping watchdog timer

Once started, the watchdog timer cannot be stopped until a reset occurs.

(5) WDG signal operation
(WDOS bit 1 with power-on reset available option selected)

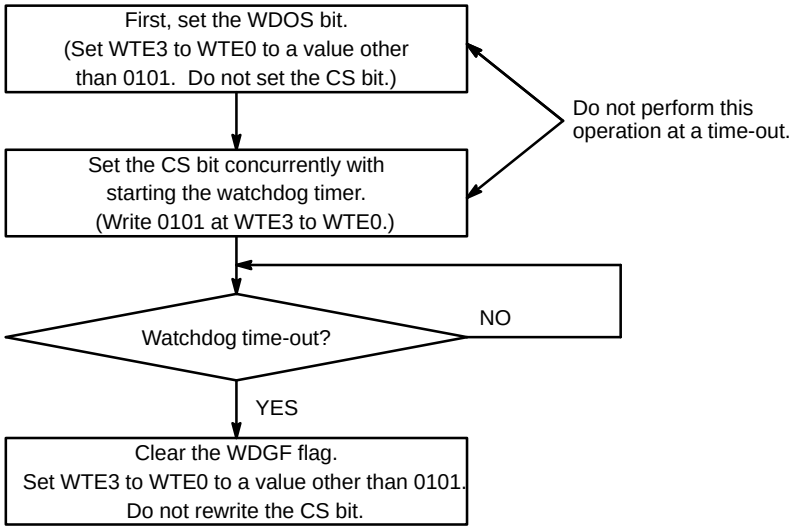


Notes:

1. The WDOS and WDGF bits are cleared only by a power-on reset. Therefore, if the power-on reset unavailable option is selected, this WDG output cannot be used.
2. With the power-on reset available option selected and the WDGF bit set to 1, reset does not occur even if the watchdog timer causes a time-out.
3. If the power-on reset unavailable option is selected, the initial values of the WDGS and WDGF bits become disabled.
4. Reset occurs with the power-on reset unavailable option selected and the watchdog timer at time-out. At this time, the reset signal will be output if the reset output available option is selected.
5. The WDG signal continues to output a High level even when an external or software reset occurs.

WATCHDOG TIMER RESET

Set the WDTE register as follows:

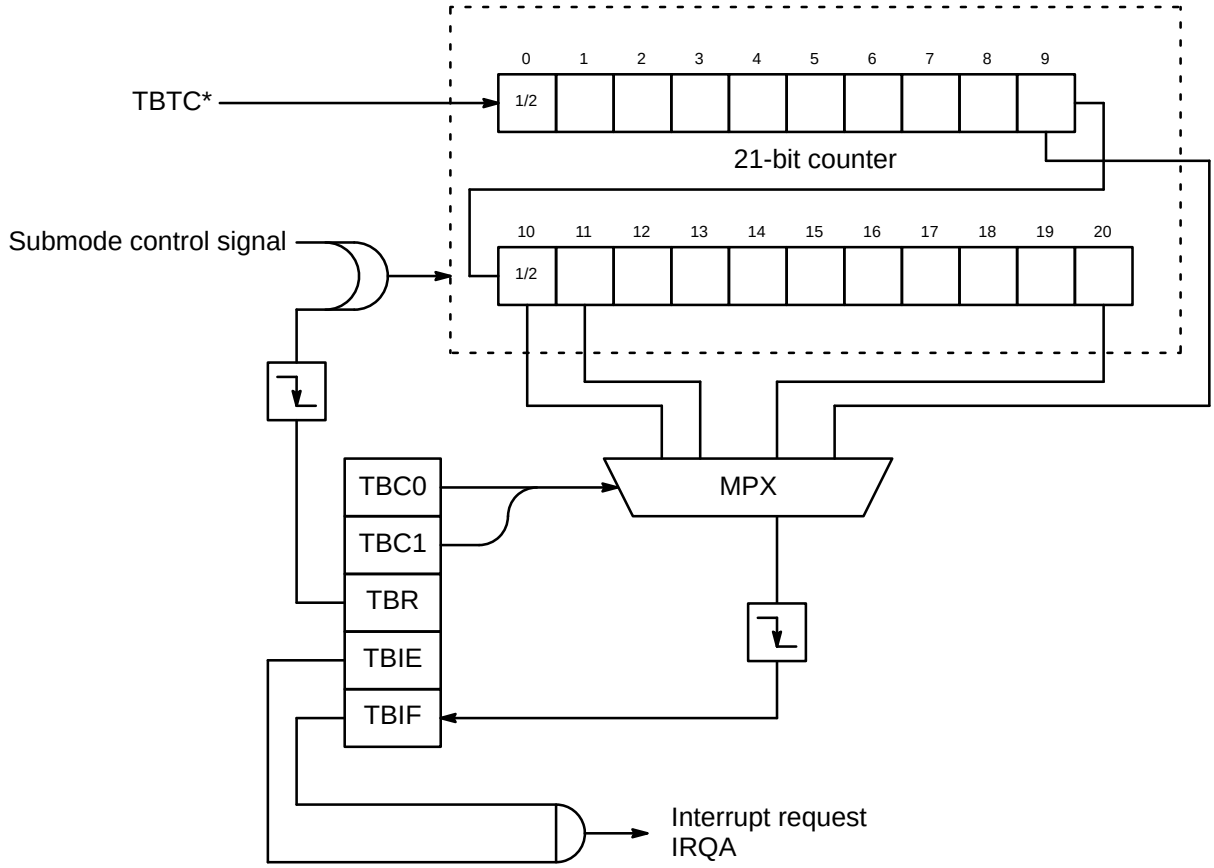


TIME-BASE TIMER

2.7 TIME-BASE TIMER

- This timer has a 21-bit binary counter and uses a clock pulse with 1/2 oscillation of the main clock.
- Four interval times can be selected.
- This function cannot be used when the main clock is stopped.
- The clock source of this timer does not change even with a gear change (1/2 oscillation frequency).

■ Block Diagram

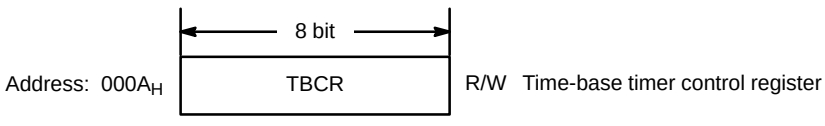


* TBTC is a clock pulse with 1/2 oscillation of the original oscillation.

Fig. 2.21 Time-base Timer Block Diagram

■ Register list

The time-base timer has time-base timer control register (TBCR).



TIME-BASE TIMER

Address: $000A_H$ TBCR

■ Description of Registers

The detail of time-base timer control register (TBCR) is described below.

(1) Time-base timer control register (TBCR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $000A_H$	TBOF	TBIE	—	—	—	TBC1	TBC0	TBR
	(R/W)	(R/W)				(R/W)	(R/W)	(W)
								Initial value $00---000_B$

[Bit 7] TBOF: Interval timer overflow bit
When writing, this bit is used to clear the interval timer overflow flag.

0	Interval timer overflow flag cleared
1	No operation

When reading, this bit indicates that an interval timer overflow has occurred.

0	Interval timer overflow not occurred
1	Interval timer overflow occurred

1 is read when the Read Modify Write instruction is read. If the TBIF bit is set to 1 when the TBIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 6] TBIE: Interval-timer interrupt enable bit
This bit is used to enable an interrupt by the interval timer.

0	Interval interrupt disabled
1	Interval interrupt enabled

[Bit 2 and 1] TBC1, TBC2: Interval time specification bit
These bits are used to specify interval timer cycle.

TBC1	TBC0	Interval time	8 MHz source clock
0	0	0.26 ms	$2^{11}/f_{CH}$
0	1	0.51 ms	$2^{12}/f_{CH}$
1	0	1.02 ms	$2^{13}/f_{CH}$
1	1	0.524 s	$2^{22}/f_{CH}$

f_{CH}: main clock frequency

[Bit 0] TBR: Time-base timer clear bit
This bit is used to clear time-base timer.

0	Time-base timer cleared
1	No operation

1 is always read when this bit is read.

8-Bit PWM TIMER (TIMER 1)

2.8 8-BIT PWM TIMER (TIMER 1)

- This timer can be used as an 8-bit timer or PWM controller with 8-bit resolution.
- Four clock pulses can be selected.

■ Block Diagram

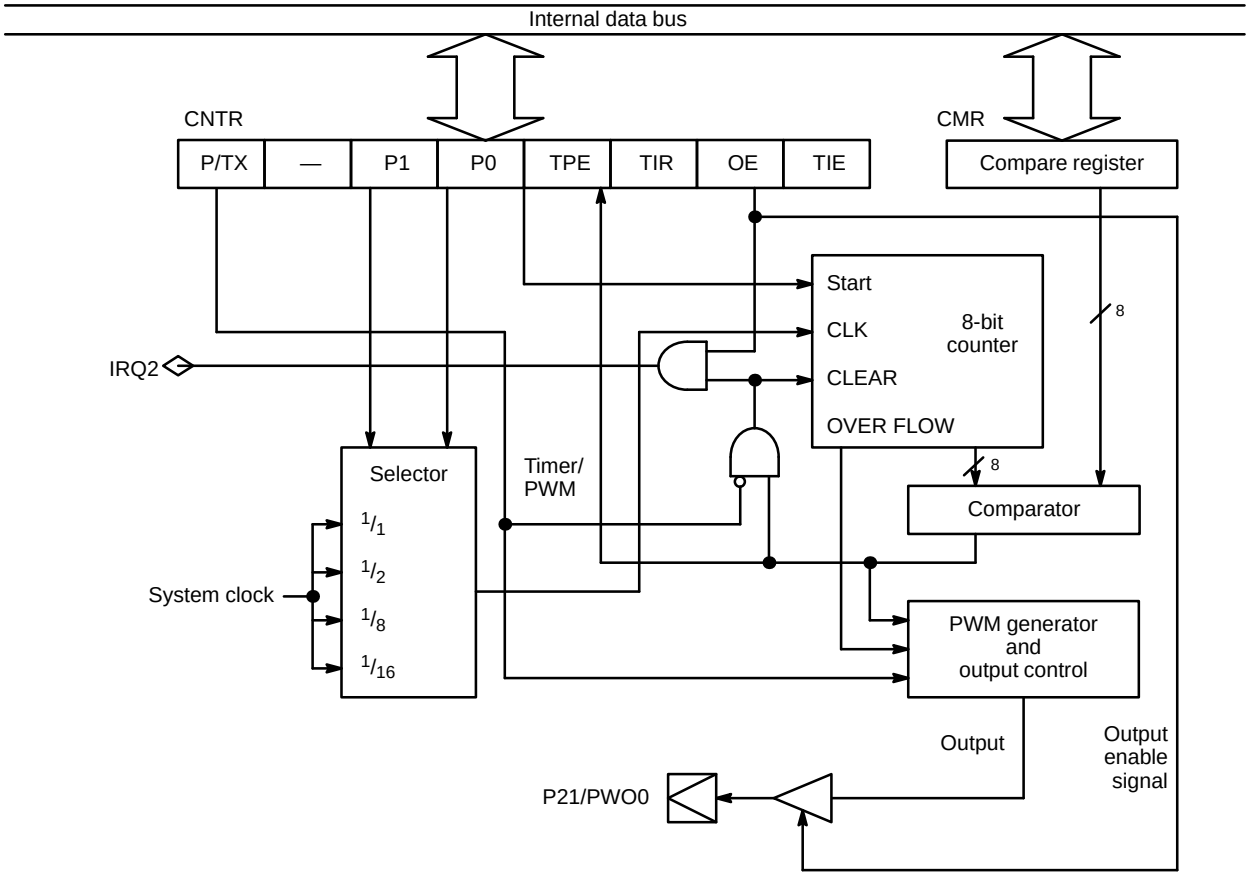
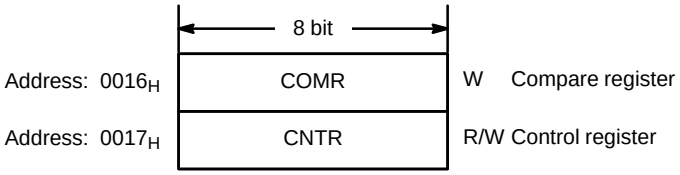


Fig. 2.22 8-bit PWM Timer (Timer 1) Block Diagram

■ Register list

8-bit PWM timer consists of control registers (CNTR) and compare registers (COMR).



8-Bit PWM TIMER (TIMER 1)

Address: 0016_H COMR

Address: 0017_H CNTR

■ Description of Register

The detail of watch prescaler is described below.

(1) Control register (CNTR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0017_H	P/TX	—	P1	P0	TPE	TIR	OE	TIE
	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
								Initial value $0\text{-}000000_B$

[Bit 7] P/TX: Timer/PWM operation switching bit
The operation is performed as the timer when this bit is set to 0, and as the PWM controller when bit 7 is set to 1.

0	Timer
1	PWM controller

The timer/PWM operation mode should be switched when the counter operation is stopped (TPE = 0), the interrupt is enabled (TIE =0), and the interrupt request flag is cleared (TIR = 0).

[Bits 5 and 4] P1, P0: Clock select bit
The following four system clock cycles can be selected by P1 and P0.

P1	P0	System clock cycle of PWM timer	At 8 MHz and Maximum gear speed
0	0	1 system clock cycle	0.5 µs
0	1	2 system clock cycles	1.0 µs
1	0	8 system clock cycles	4.0 µs
1	1	16 system clock cycles	8.0 µs

(One system clock is 500 ns at 8.0 MHz and maximum gear speed.)

These bits must not be rewritten during counting (TPE = 1).

[Bit 3] TPE: Counter operation enable bit
When Bit 3 is set to 1, the timer or PWM control circuit starts operation.

0	Counting stop
1	Counting start

[Bit 2] TIR: Interrupt request flag bit
When an interrupt source occurs, Bit 2 goes to 1. To clear the generated interrupt source, write 0 at this bit.

The meaning of each bit to be read is as follows:

0	Counter and CMR values do not agree
1	Counter and CMR values agree

8-Bit PWM TIMER (TIMER 1)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change or affect other bits.

Note: In the PWM operation mode, neither the read nor write values of this bit have any meaning.

[Bit 1] OE: Output signal control bit
When Bit 1 is 1, the port serves as the timer/PWM output. In the timer operation mode, a signal that is reversed each time the values of the counter and compare register agree, is output. In the PWM operation mode, a PWM signal is output.

0	General-purpose port pin (P21)
1	Counter/PWM output pin (PWO0)

When this bit is 1, the port functions as the timer/PWM output pin even after the DDR of P21 is set to input (bit 2 of DDR2).

[Bit 0] TIE: Interrupt enable bit (timer mode)
When this bit is set to 1, an interrupt occurs when the values of the counter and compare register agree.

0	Counter interrupt generation disabled
1	Counter interrupt generation enabled

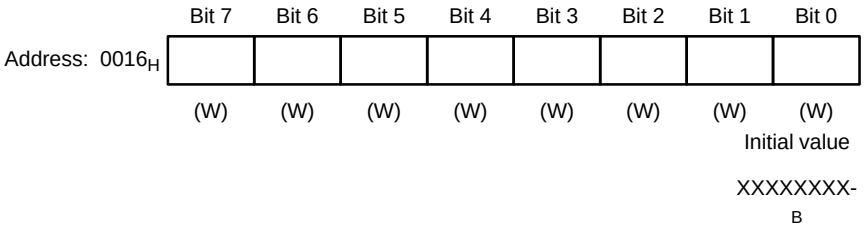
In the PWM operation mode, an interrupt does not occur irrespective of the value of this bit.

Address: 0016_H COMR

Address: 0017_H CNTR

(2) Compare register (COMR)

In the timer operation mode, this register is used to set the value to be compared with the value of the counter, and to clear the counter when the values of the counter and this register agree. In the PWM operation mode, the High pulse width can be specified by the value of this register.



8-Bit PWM TIMER (TIMER 1)

■ Operation description

(1) Timer operation

Setting the P/TX bit of the CNTR to 1, gives the timer operation mode is performed. When the TPE bit of the CNTR is set to 1, the counter starts incrementing from 00H. When the value of the counter agrees with that of the COMR, the counter is cleared on the next count clock pulse and starts incrementing. Therefore, the TIR bit is set and the output pin is reversed (when the TPE bit is 0, the output pin is fixed to Low level) in cycles of the count clock pulses when $\mathbf{00_H}$ is written at the COMR, or in cycles 256 times longer than those of the count clock pulses when $\mathbf{FF_H}$ is written.

If the value of the COMR is rewritten in the timer operation mode, it becomes effective from the next cycle. When the value of the counter is $\mathbf{00_H}$, the value of the COMR is transferred to the comparator latch.

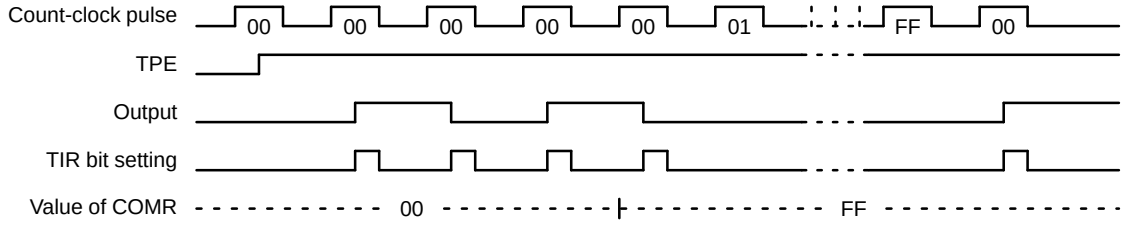


Fig. 2.23 Timer Operation

If the TIE bit of the CNTR is set to 1, an interrupt occurs when the values of the counter and COMR agree. During interrupt processing, the TIR bit is used as the interrupt flag. The TIR bit is set irrespective of the value of the TIE bit. However, if the values of the counter and the COMR agree, the TIR bit is set to 1 even after an interrupt is disabled.

Writing 0 at the TIR bit permits clearing of the interrupt source or the TIR bit. When the Read Modify Write instruction is read, the TIR bit is set so that 1 is always read to prevent erroneous clearing.

The count clock pulse can be selected from four clock pulses from the prescaler by the clock pulse select bits P0 and P1 of the CNTR.

(2) PWM operation

Setting the P/TX bit of the CNTR to 1, gives the PWM operation mode. The COMR specifies the duty of the output pulse. Pulses can be output with 1/256 resolution and a duty of 0% to 99.6%. When 0 ($\mathbf{00_H}$) is written at the COMR, the duty of the PWM output pulse is 0%; when 128 ($\mathbf{80_H}$) is written, the duty is 50%, and when 255 ($\mathbf{FF_H}$) is written, the duty is 99.6%.

The value of the COMR is transferred to the comparator latch when the value of the counter is $\mathbf{00_H}$. If the value of the COMR is rewritten in the PWM operation mode, it becomes effective from the next cycle.

8-Bit PWM TIMER (TIMER 1)

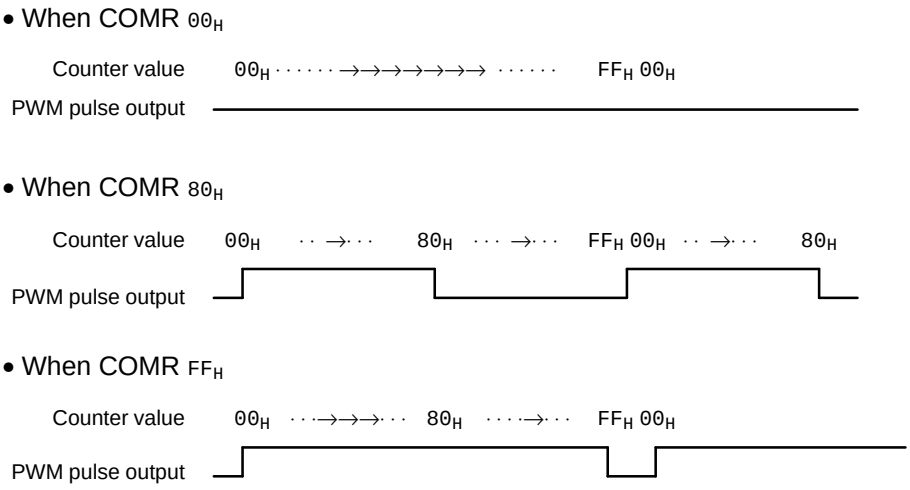


Fig. 2.24 PWM Pulse Output

The TIR bit of the CNTR in the PWM operation mode has no meaning. No interrupt occurs irrespective of TIE bit.

The cycle and frequency of the PWM pulse can be changed by switching the count clock pulse. The count clock pulse can be selected from four clock pulses from the prescaler (PWM timer channel 1 output) by the clock pulse select pits P0 and P1 of the CNTR.

8/16-BIT TIMER (TIMER 2 AND TIMER 3)

2.9 8/16-BIT TIMER (TIMER 2 AND TIMER 3)

- Three internal clock pulses and one external clock pulse can be selected.
- External input can be selected from the rising edge, falling edge, or both edges.
- Operable in 8-bit 2-ch mode or 16-bit 1-ch mode

■ Block Diagram

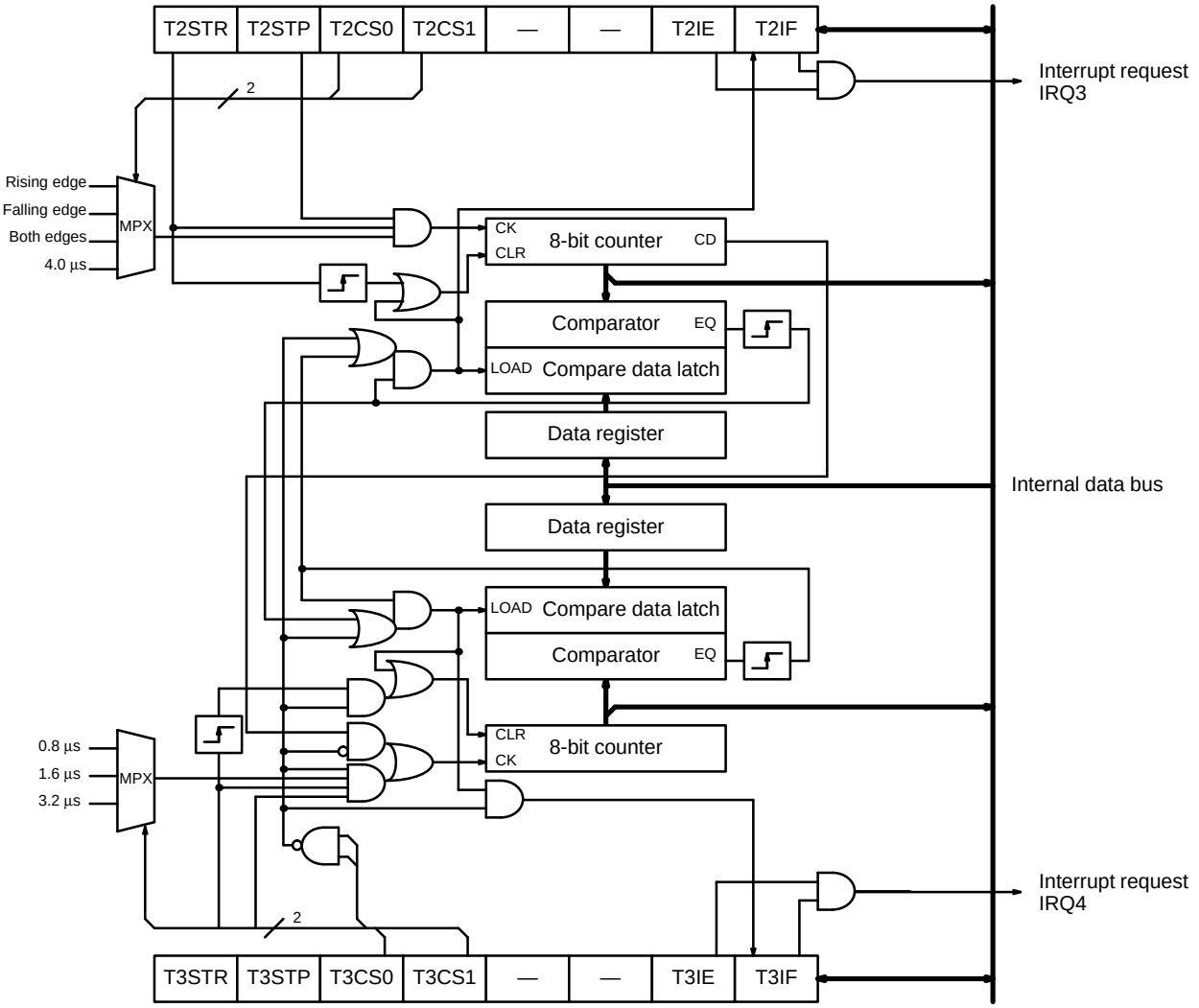


Fig. 2.25 8/16-bit Timer Block Diagram

8/16-BIT TIMER
(TIMER 2 AND TIMER 3)

■ Register List

	8 bit	
Address: 0018_H	T3CR	R/W Timer-3 control register
Address: 0019_H	T2CR	R/W Timer-2 control register
Address: $001A_H$	T3DR	R/W Timer-3 data register
Address: $001B_H$	T2DR	R/W Timer-2 data register

■ Description of Register Details

The detail of each register is described below.

Address: 0018_H T3CR
Address: 0019_H T2CR
Address: $001A_H$ T3DR
Address: $001B_H$ T2DR

(1) Timer 2 control register (T2CR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0019_H	T2IF	T2IE	—	—	T2CS1	T2CS0	T2STP	T2STR
	(R/W)	(R/W)	—	—	(R/W)	(R/W)	(R/W)	(R/W)
								Initial value $X000XXX0_B$

[Bit 7] T2IF: Interrupt request flag bit
(When write)

0	Interrupt request flag clearing
1	No operation

(When read)

0	No interrupt request
1	Interval interrupt request

[Bit 6] T2IE: Interrupt-enable bit

0	Interrupt disabled
1	Interrupt enabled

[Bit 5]: Reserved; write 0 when writing.
[Bit 4]: Reserved; write 0 when writing.

[Bit 3 and 2] T2CS1, T2CS0: Clock source select bit

T2CS1	T2CS0	Time cycle at 8 MHz and Maximum gear speed	System clock cycle
0	0	Rising edge of external clock pulse	
0	1	Falling edge of external clock pulse	
1	0	Both edges of external clock pulse	
1	1	4.00 μs	8 system clock cycle

Note: One system clock cycle is 500 ns at 8 MHz and maximum gear speed.

8/16-BIT TIMER
(TIMER 2 AND TIMER 3)

[Bit 1] T2STP: Timer-stop bit

0	Counting continued without clearing counter
1	Counting suspended

[Bit 0] T2STR: Timer-start bit

0	Terminates operation
1	Clears counter and starts operation

Address: 0018_H T3CR
Address: 0019_H T2CR
Address: $001A_H$ T3DR
Address: $001B_H$ T2DR

(2) Timer 3 control register (T3CR)

Address: 0018_H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3IF	T3IE	—	—	T3CS1	T3CS0	T3STP	T3STR
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value
$X000XXX0_B$

[Bit 7] T3IF: Interrupt request flag bit
(When write)

0	Interrupt request flag clearing
1	No operation

(When read)

0	No interrupt request
1	Interval interrupt request

[Bit 6] T31E: Interrupt-enable bit

0	Interrupt disabled
1	Interrupt enabled

[Bit 5]: Reserved; write 0 when writing.
[Bit 4]: Reserved; write 0 when writing.

[Bit 3 and 2]: T3CS1, T3CS0: Clock source select bit

T2CS1	T2CS0	Time cycle at 8 MHz and Maximum gear speed	System clock cycle
0	0	1.0 µs	2 system clock cycle
0	1	2.0 µs	4 system clock cycle
1	0	4.0 µs	8 system clock cycle
1	1	16-bit mode	—

Note: When bit 2 and 3 use only timer 2, set this bit to except 11.

8/16-BIT TIMER
(TIMER 2 AND TIMER 3)

[bit 1] T3STP: Timer stop bit

0	Operation continued without clearing counter
1	Count operation suspended

[Bit 0] T3STR: Timer start bit

0	Operation stopped
1	Operation started after clearing counter

Address: 0018_H T3CR

Address: 0019_H T2CR

Address: $001A_H$ T3DR

Address: $001B_H$ T2DR

(3) Timer 1 and 2 data registers (T2DR and T2DR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $001B_H$								
Address: $001A_H$	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
								Initial value $XXXXXXXX_B$

Write data is the set interval times and read data is the counted value.

8/16-BIT TIMER (TIMER 2 AND TIMER 3)

■ Description of Operation

(1) 8-bit internal clock mode

In the 8-bit internal clock mode, three internal clock inputs can be selected by setting the clock source select bits (T2CS1 and T2CS0, T3CS1 and T3CS0) of the timer control registers (T2CR and T3CR). The timer data registers (T2DR and T3DR) serve as interval time setting registers.

To start the timer, set the interval time to the timer data registers, write 1 at the timer start bits (T2STR and T3STR) of the timer control registers to clear the counter to $\mathbf{00}_H$, and load the values of the timer data registers into the compare latch. Then, counting starts.

When the values of the counter agree with the set value of the timer data registers, the interval interrupt request flags (T2IF and T3IF) are set to 1. At this time, the counter is cleared to $\mathbf{00}_H$, the values of the timer data registers are reloaded into the compare latch, and counting is continued. If the interrupt enable bits (T2IE and T3IE) are set to 1, an interrupt request is output to the CPU. Assuming the set value of the timer data register is n and the selected clock is ϕ, the interval time (T) can be calculated as follows.

$T = \phi \times (n + 1)$ [μs]

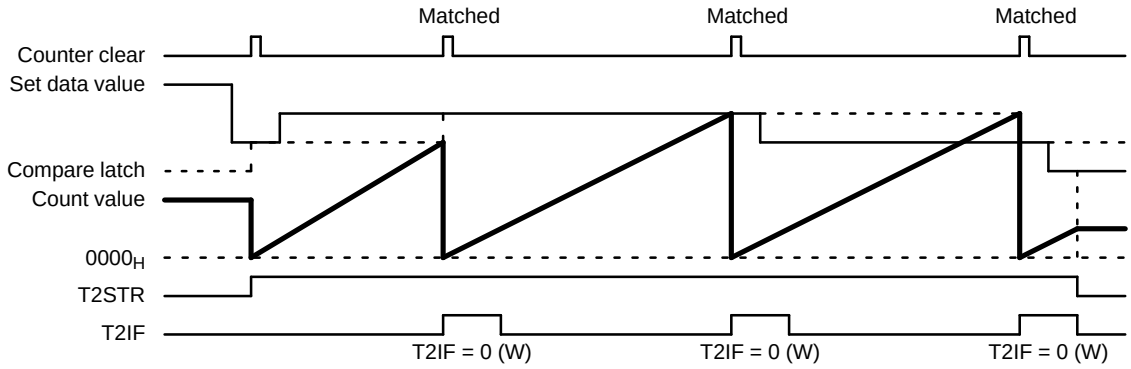


Fig. 2.26 Description Diagram for Internal Clock Mode Operation

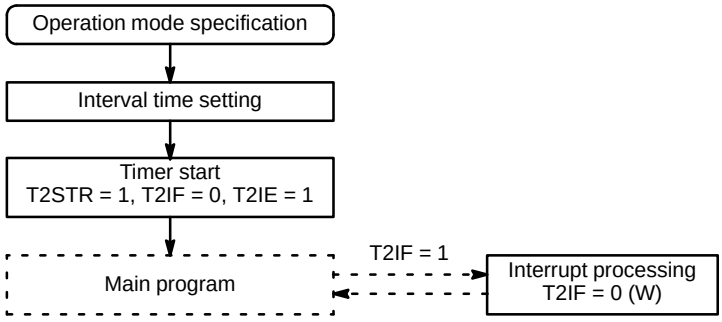


Fig. 2.27 Flow Diagram for Timer Setting

8/16-BIT TIMER
(TIMER 2 AND TIMER 3)

(2) 8-bit external clock mode

In the 8-bit external clock mode, the eternal clock input can be selected three various external clock inputs by setting the clock source select bits (T2CS1 and T2CS0) of the timer 2 control register (T2CR). The external-clock input pin of the timer corresponds to P33/EC.

To start the timer, write 1 at the timer start bit (T2STR) of the T2CR to clear the counter.

When the value of the counter agrees with that of the timer data register, the interval interrupt request flag bit (T2IF) is set to 1. At this time, if an interrupt is enabled (T2IE = 1), an interrupt request is output to the CPU.

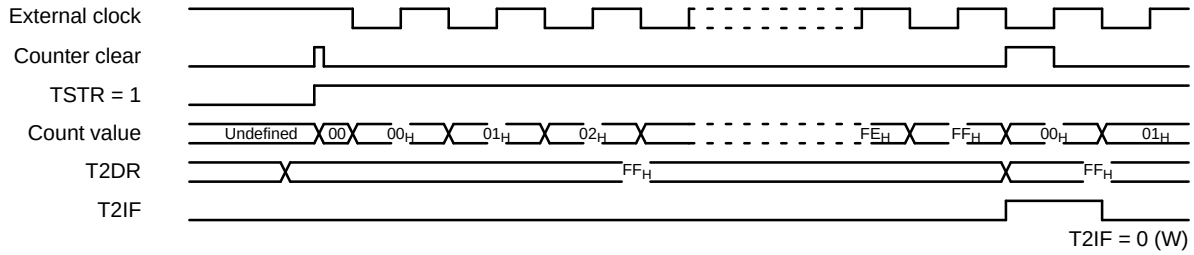


Fig. 2.28 External Cock Mode Operation Description Diagram

(4) Precautions for use of timer stop bit

If the timer stop bit is used to stop the timer, the input clock pulse is fixed to HIGH, Therefore, the count value varies depending on the level of the input clock pulse.

After using the timer stop bit to stop the timer, if 00 is written simultaneously at the timer stop and start bits, the count value may be incremented by one. Therefore, when using the timer stop bit to stop the timer, read the count data and then write 0 at the timer start bit (Figure 2.29)

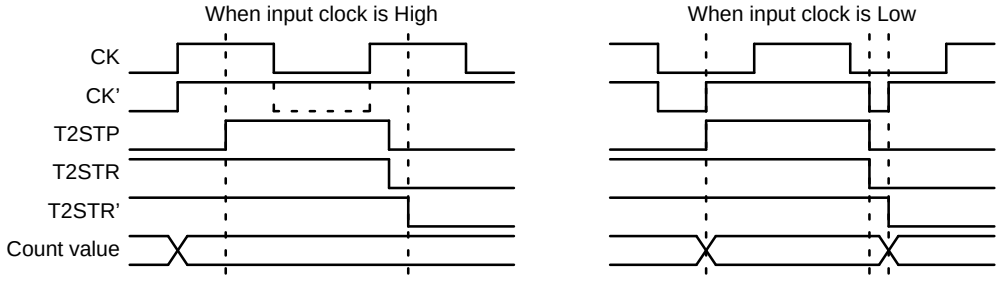


Fig. 2.29 Operation Diagram when Timer Stop Bit is Used

8/16-BIT TIMER (TIMER 2 AND TIMER 3)

(3) 16-bit mode

In the 16-bit mode, each bit of the timer control registers is as shown below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0019_H	T2IF	T2IE	—	—	T2CS1	T2CS0	T2STP	T2STR
Address: 0018_H	T3IF	T3IE	—	—	T3CS1	T3CS0	T3STP	T3STR
	No operation		Set to 00		Set to 11		No operation	

In the 16-bit mode, write 11 at the T3CS1 and T3CS0 bits of the T3CR and set 0 at the bit 5 and bit4.

When in the 16-bit mode, the timer is controlled by the T2CR. The timer data registers T3DR and T2DR use the upper and lower bytes, respectively.

The clock source is selected by the T2CS1 and T2CS0 bits of the T2CR. To start the timer, write 1 at the T2STR bit of the T2CR to clear the counter.

If the value of the counter agrees with that of the timer data register, the T2IF bit is set to 1. At this time, an interrupt request is output to the CPU if the T2IE bit is 1.

Note: To read the value of the counter in the 16-bit mode, always read the value twice to check that it is valid and then use the data.

See the 8-bit operation diagram for 16-bit mode operation.

(4) Starting and temporarily stopping timer

The operation of the timer is described below, using timer 2.

(a) When counting after clearing the counter

When the T2STR bit is 0, write 0 at the T2STP bit and 1 at the T2STR bit. When the T2STR bit is set from 0 to 1, the counter is cleared and the timer starts counting.

(b) When temporarily stopping timer to count without clearing counter

To stop counting temporarily, set the T2STP and T2STR bits to 11. To continue counting without clearing the counter from the temporarily-stopped state, set the T2STP and T2STR bits from 11 to 01.

The state of the timer corresponding to the settings of the T2STP and T2STR bits and the operation of the timer when started from the state (T2STP and T2STR bits = 01) are as follows:

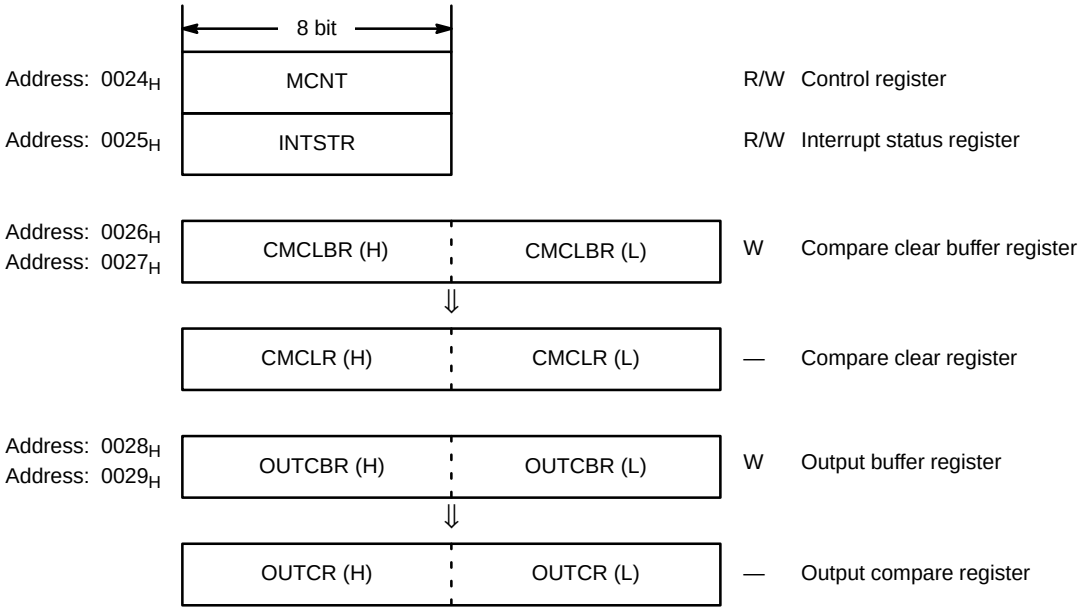
T2CS1	T2CS0	Timer state	Operation of timer when started from left state (bits 1 and 0 = 01)
0	0	Counting stop	Counts after clearing counter
0	1	Counting	Continues counting
1	0	Counting stop	Counts after clearing counter
1	1	Temporary counting stop	Continues counting without clearing counter

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

2.10 12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

- A 12-bit-long up timer is provided with one compare clear register for cycle setting and one compare register for output pin control to control one real-time waveform output pin.
- Four count clock sources can be selected.
- The PWM operation or PPG operation at start by an external or internal trigger can be selected on a programmable basis. This generator can also be used as a toggle output timer.

■ Register list



12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

■ Block diagram

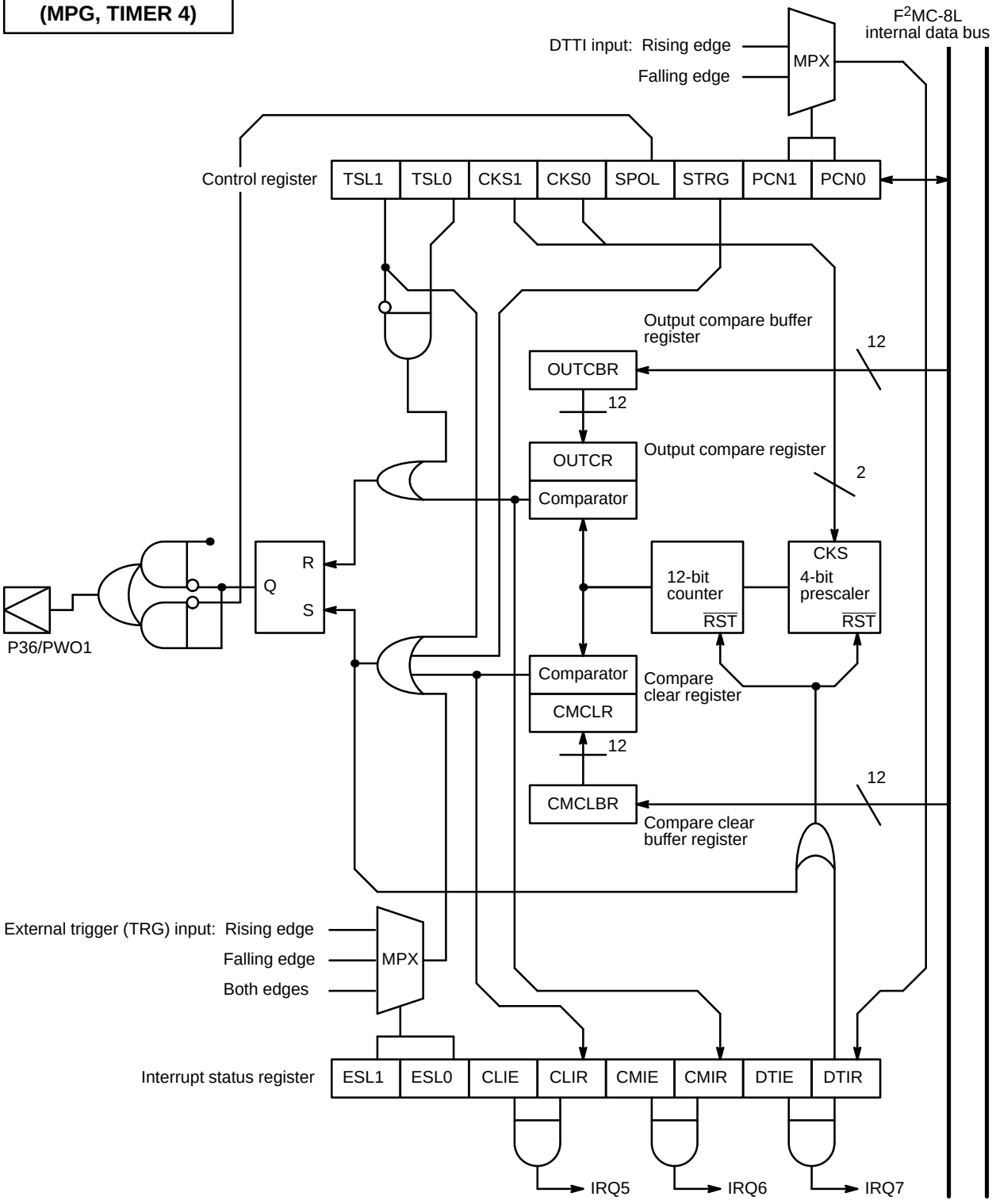


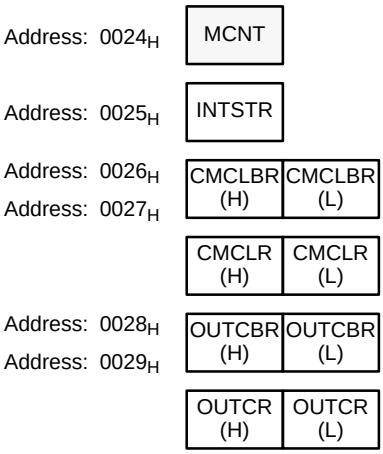
Fig. 2.30 MPG Block Diagram

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

■ Description of registers

(1) Control register (MCNT)

This register is used to select the count clock pulse of the timer and the PWM/PPG function, and to control setting of the software trigger.



(1) Interrupt level register (ILRX: Interrupt Level Register X)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0024H	TSL1	TSL0	CKS1	CKS0	SPOL	STRG	PCN1	PCN0
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value 00000000_B

[Bits 7 and 6] TSL1 and TSL0: Operation mode select bits

Bits 7 and 6 are used to select the operation mode. The PPG operation mode or PWM operation mode can be selected as the operation mode. External and software triggers can be selected in the PPG and PWM operation modes.

The retrigger enable mode or retrigger disable mode can be selected as the PPG operation mode, whereas the retrigger enable mode only is selected as the PWM operation mode.

TSL1	TSL0	Operation mode	
0	0	Stop	
0	1	PWM operation mode (retrigger enable)	
1	0	PPG operation mode	Retrigger disable
1	1		Retrigger enable

Retrigger enable mode: When the start trigger (software trigger or external trigger) is re-input during operation of the MPG, the counter and prescaler of the MPG are cleared and operation is restarted.

Retrigger disable mode: Even when the start trigger (software trigger or external trigger) is re-input during operation of the MPG, it is ignored and operation is continued.

When the PWM operation mode is selected, the initial output of the MPG enters the reset state (see the block diagram). When the PPG operation mode is selected, the initial state of the MPG output is changed to the set state.

When the stop mode is selected after the operation mode, the counter and prescaler are cleared to inactivate the MPG output.

The operation mode should be selected during operation stop.

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

[Bits 5 and 4] CKS1 and CKS0: Count clock pulse select bits

Bits 5 and 4 are used to select the count clock pulse (minimum resolution) in the PWM or PPG operation mode.

CKS1	CKS0	Clock pulse to be selected (at maximum gear speed)	Maximum cycle at maximum gear speed (4096 clock pulses)
0	0	1 system clock cycle (0.5 μs at 8 MHz)	2048.0 μs at 8 MHz (488 Hz)
0	1	2 system clock cycles (1.0 μs at 8 MHz)	4096.0 μs at 8 MHz (244 Hz)
1	0	4 system clock cycles (2.0 μs at 8 MHz)	8192.0 μs at 8 MHz (122 Hz)
1	1	8 system clock cycle (4.0 μs at 8 MHz)	1638.42 μs at 8 MHz (61 Hz)

One system clock cycle is 500 ns at 8 MHz and maximum gear speed.

These bits should be set during operation stop.

[Bit 3] SPOL: Output polarity select bit

Bit 3 is used to select the polarity of the waveform output from the MPG. This bit should be set during operation stop.

0	Outputs MPG output waveform with positive polarity
1	Reverses MPG output waveform for output

[Bit 2] STRG: Software trigger bit

When the internal trigger mode is selected, when 1 is set at this bit, the timer and prescaler are cleared and the timer is started. This bit also provides start by a software trigger. 0 is always read when this bit is read.

0	Ignored
1	Clears timer and prescaler to start timer

[Bits 1 and 0] PCN1 and PCN0: Port output select/overcurrent detect function control bits

Bits 1 and 0 are used to control whether or not the MPG pulse output pin is used as the general-purpose pin and set the effective/ineffective edge of the DTTI input for overcurrent detection. The operation mode should be set during operation stop.

When the DTTI input is enabled, if an error is detected outside the chip, the MPG output can be set to an inactive level (initial output) by inputting the edge. At this time, the timer and prescaler are cleared to the stopped state. To restart output, 0 must be written at the overcurrent detect interrupt request bit to clear the flag. At this time, the MPG restarts outputting the waveforms set when the DTTI input was detected from the timer value of 00_H after accepting the effective trigger input.

After the DTTI is input in the effective state (PCN1 = 1), if the operation mode is selected to clear the DTIR flag of the INSTR register, the MPG output goes inactive in the selected mode.

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

PCN1	PCN0	Operation mode	
0	0	(P36/PW01) general-purpose pin state	DTTI input ineffective
0	1	MPG pulse output	
1	0		Effective at rising edge of DTTI input
1	1		Effective at falling edge of DTTI input

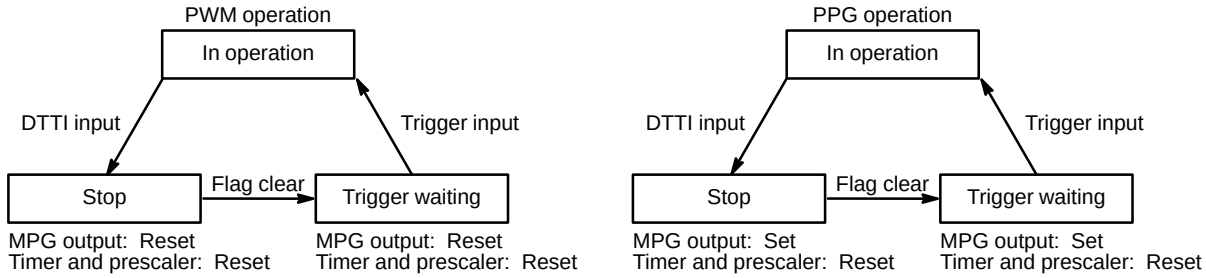


Fig. 2.31 Transition of DTTI Input

Address: 0024_H MCNT

Address: 0025_H INTSTR

Address: 0026_H CMCLBR (H) CMCLBR (L)

Address: 0027_H CMCLR (H) CMCLR (L)

Address: 0028_H OUTCBR (H) OUTCBR (L)

Address: 0029_H OUTCR (H) OUTCR (L)

(2) Interrupt status register (INTSTR)

This register is used to control the trigger input interrupt, compare match interrupt, and compare clear interrupt. It also selects the polarity of the external trigger edge.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0025_H	ESL1	ESL0	CLIE	CLIR	CMIE	CMIR	DTIE	DTIR
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value 00000000_B

[Bits 7 and 6] ESL1 and ESL0: External trigger select bits

Bits 7 and 6 are used to select the effective edge input of the external trigger. Input of the effective edge clears the timer and prescaler and starts the timer.

ESL1	ESL0	External trigger edge
0	0	No external trigger
0	1	When rising edge detected, timer cleared ⇒ timer started
1	0	When falling edge detected, timer cleared ⇒ timer started
1	1	When both edges detected, timer cleared ⇒ timer started

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

[Bit 5] CLIE: Compare clear match interrupt enable bit

Bit 5 is used to enable the compare clear match interrupt request.

0	Compare clear match interrupt request disabled
1	Compare clear match interrupt request enabled

[Bit 4] CLIR: Compare clear match interrupt request flag

Bit 4 is set to 1 when the compare clear match occurs.
Writing 0 clears this bit.
Writing 1 has no meaning.
1 is always read when the Read Modify Write instruction is read.

0	Compare clear match interrupt not requested
1	Compare clear match interrupt requested

[Bit 3] CMIE: Output compare match interrupt enable bit

Bit 3 is used to enable the compare match interrupt.

0	Output compare match interrupt request disabled
1	Output compare match interrupt request enabled

[Bit 2] CMIR: Output compare match interrupt request flag

Bit 2 is set to 1 when the compare match occurs.
Writing 0 clears this bit.
Writing 1 has no meaning.
1 is always read when the Read Modify Write instruction is read.

0	Output compare match interrupt not requested
1	Output compare match interrupt requested

[Bit 1] DTIE: Overcurrent detection interrupt enable bit

Bit 1 is used to enable the overcurrent detection interrupt request.

0	Overcurrent detection interrupt request disabled
1	Overcurrent detection interrupt request enabled

[Bit 0] DTIR: Overcurrent detection interrupt request flag

Bit 0 is set to 1 when the effective rising/falling edge is input to the DTTI input pin. This bit is not set when the PCN1 bit of the MCNT register is 0.
Writing 0 clears this bit.
Writing 1 has no meaning.
1 is always read when the Read Modify Write instruction is read.

0	No effective input to DTTI input pin
1	Effective input to DTTI input pin

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

Address: 0024_H	MCNT	
Address: 0025_H	INTSTR	
Address: 0026_H	CMCLBR (H)	CMCLBR (L)
Address: 0027_H	CMCLR (H)	CMCLR (L)
Address: 0028_H	OUTCBR (H)	OUTCBR (L)
Address: 0029_H	OUTCR (H)	OUTCR (L)

(3) Compare clear register (CMCLR)

This register is used to store the compare value of compare clear.

When the values of this register and timer agree, the timer is cleared. The value is transferred from the buffer register to the compare register.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
—	—	—	—	CLRB	CLRA	CLR9	CLR8

Initial value ----0000_B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0

Initial value 00000000_B

In the PPG operation mode, the match between the value of this register + 1 and the value of the timer is detected to clear the timer and set the MPG output.

In the PWM operation mode, the match between the value of this register + 1 and the value of the timer is detected to clear the timer and set the MPG output.

Address: 0024_H	MCNT	
Address: 0025_H	INTSTR	
Address: 0026_H	CMCLBR (H)	CMCLBR (L)
Address: 0027_H	CMCLR (H)	CMCLR (L)
Address: 0028_H	OUTCBR (H)	OUTCBR (L)
Address: 0029_H	OUTCR (H)	OUTCR (L)

(4) Compare clear buffer register (CMCLBR)

This register is used to store the compare value of compare clear.

The value written to the compare clear buffer register when the timer stops is written directly to the compare clear register.

Data transfer from the compare clear buffer register to the compare clear register after the timer starts is done when the compare clear match occurs.

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Address: 0026_H	—	—	—	—	CLRB	CLRA	CLR9	CLR8
					(W)	(W)	(W)	(W)

Initial value ----0000_B

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0027_H	CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

Initial value 00000000_B

Note: To write the value to the output compare register buffer register during PWM or PPG operation, use the load instruction. Some time should be taken to allow writing of the load instruction to terminate until the values of the compare clear register and timer agree.

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

Address: 0024_H	MCNT	
Address: 0025_H	INTSTR	
Address: 0026_H	CMCLBR (H)	CMCLBR (L)
Address: 0027_H	CMCLR (H)	CMCLR (L)
Address: 0028_H	OUTCBR (H)	OUTCBR (L)
Address: 0029_H	OUTCR (H)	OUTCR (L)

(5) Output compare register (OUTCR)

This register is used to store the compare value of output compare.

When the values of this register and timer agree, the output is set.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
—	—	—	—	CPRB	CPRA	CPR9	CPR8

Initial value ----0000_B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPR7	CPR6	CPR5	CPR4	CPR3	CPR2	CPR1	CPR0

Initial value 00000000_B

In the PPG operation mode, the output is cleared by the external trigger or software trigger input, and reset when the value of this register and the value of the timer agree.

In the PWM operation mode, the output is reset by the external trigger or software trigger input, and reset when the value of this register and the value of the timer agree.

The pulse width can be specified by the value of this register.

Address: 0024_H	MCNT	
Address: 0025_H	INTSTR	
Address: 0026_H	CMCLBR (H)	CMCLBR (L)
Address: 0027_H	CMCLR (H)	CMCLR (L)
Address: 0028_H	OUTCBR (H)	OUTCBR (L)
Address: 0029_H	OUTCR (H)	OUTCR (L)

(6) Output compare buffer register (OUTCBR)

This register is used to store the output compare value.

The value written to the output compare buffer register when the timer stops is written directly to the output compare register.

Data transfer from the output compare buffer register to the output compare register after the timer is started is done when the output compare clear match occurs.

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Address: 0028_H	—	—	—	—	CPRB	CPRA	CPR9	CPR8
					(W)	(W)	(W)	(W)

Initial value ----0000_B

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0029_H	CPR7	CPR6	CPR5	CPR4	CPR3	CPR2	CPR1	CPR0
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

Initial value 00000000_B

Note: Use the load instruction to write the value to the output compare register buffer register during PWM or PPG operation. Some time should be taken to allow writing of the load instruction to terminate until the values of the output compare register and timer agree.

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

■ Operation description

(1) PWM operation (counting)

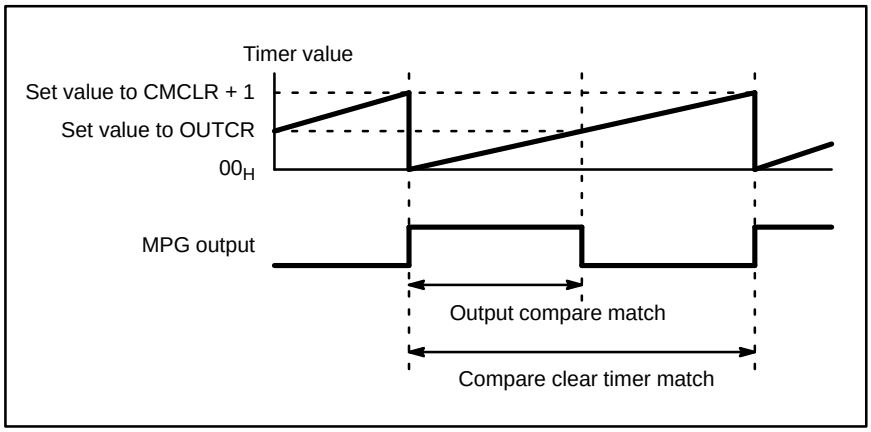


Fig. 2.32 Outline of PWM Output

As shown in Figure 2.32, the MPG can generate a PWM waveform. The repeat cycle is set by the value of the compare clear register, and the duty of the output pulse is set by the value of the output compare register.

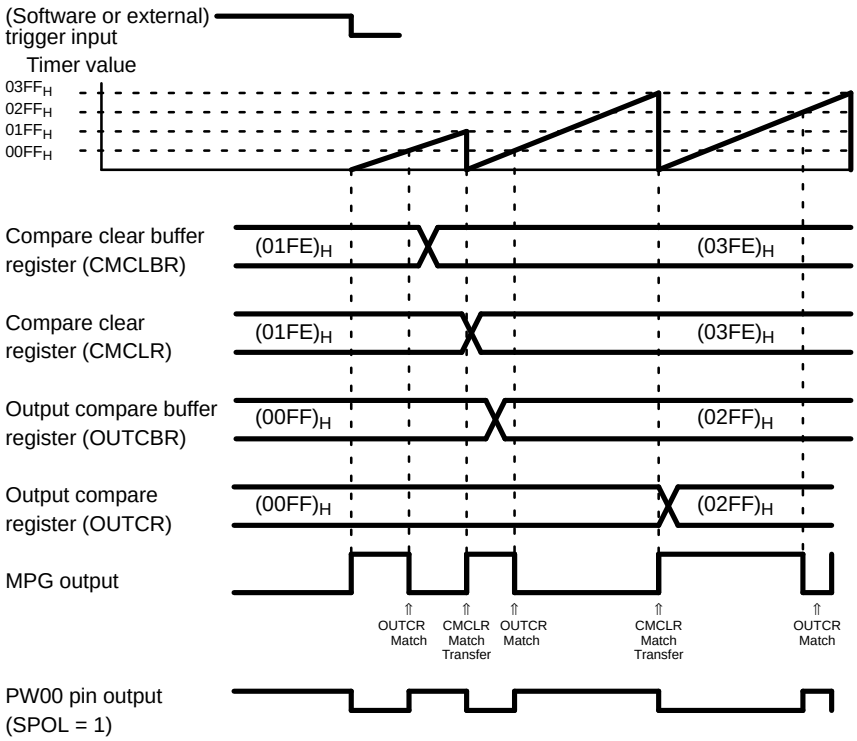
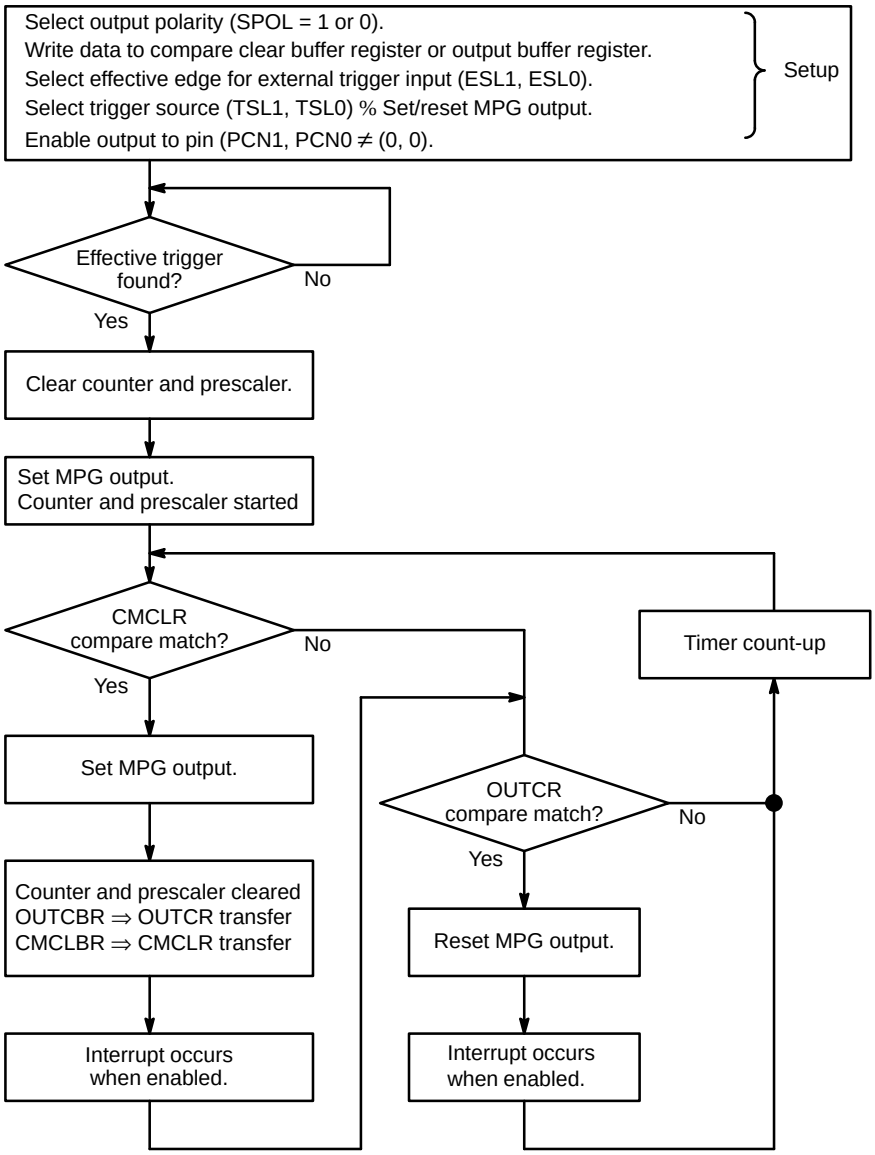


Fig. 2.33 Description of PWM Output Operation

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)



When the operation mode is set to “Stop” or when the DTTI input is performed with overcurrent detection enabled, the MPG output (pin state) goes inactive in this mode.

Fig. 2.34 Flowchart of PWM Operation

Setting the TSL1 and TSL0 bit of the CNTR to 0 and 1 gives the PWM operation mode. The cycle of the output pulse is determined by the value set at the CMCLR, and the count clock pulse selected by the CKS1 and CKS0 bits.

PWM cycle = (value set at CMCLR + 1) × cycle of count clock pulse

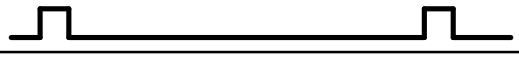
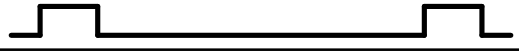
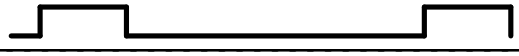
The pulse width is determined by the value set at the OUTCR, and the cycle of the count clock pulse.

PWM pulse width = value set at OUTCR × cycle of count clock pulse

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

For example, the relationship between the value set at the OUTCR and the duty with $\mathbf{7F_H}$ set at the CMCLR is given in Table 2-6 (the output polarity is assumed to be positive (SPOL = 0)).

Table 2-6 Relationship between value Set at OUTCR and Duty

Value set at OUTCR	Output wave form	Duty
$(00)_H$		0%
$(01)_H$		0.78%
$(02)_H$		1.56%
$(03)_H$		2.34%
≀	≀	≀
$(7D)_H$		97.6%
$(7E)_H$		98.4%
$(7F)_H$		99.2%
$(80)_H$ to $(3FF)_H$		100%

For (value set at OUTCR > value set at CMCLR) and (value set at OUTCR ≠ 0 and value set at CMCLR = 0), a waveform with a duty of 100% is output.

For (value set at OUTCR = 0 and value set at CMCLR = 0) and (value set at OUTCR = 0 and value set at CMCLR ≠ 0), a waveform with a duty of 0% is output.

Since the OUTCR and CMCLR have a buffer register, the value of the buffer can be rewritten before one cycle to change the cycle and duty.

The polarity of the output pulse can be changed by setting the SPOL bit. For the PWM operation flow, see Figure 2.34.

In the initial state, the timer and prescaler are stopped. The MPG output is in the reset state. Since the CMCLR and CMCLBR, and the OUTCBR and OUTCR are connected to each other, simultaneous writing is possible.

The PWM output is started by input of the selected trigger. First, the timer and prescaler are cleared and the MPG output enters the set state. Then, the counter starts incrementing.

The MPG output is reset if the values of the OUTCR and counter agree, and is set if the value of the CMCLR +1 and the value of the timer agree.

If the value of the OUTCR agrees with the value of the CMCLR +1, comparison with the value of the CMCLR + 1 proceeds and the MPG output is set.

The effective edge of the external trigger can be selected by setting the ESL1 and ESL0 bits.

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

The DTTI input pin makes the PWM output inactive at hardware in the event of an external error. With the DTTI input enabled, when an error is detected, the DTIR flag is set to inactivate the PWM output. The time required for this operation is 6 to 8 clock cycles.

Since the DTTI input is edge input, the rising or falling edge can be selected.

To restart the PWM output after recovery from an error, the DTIR flag must be cleared to provide the effective trigger input. In the event of an interrupt at DTTI input, other interrupt sources may be set. Therefore, to restart, all MPG interrupt sources should be cleared. The DTTI input block has a noise filter.

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

(2) PPG operation

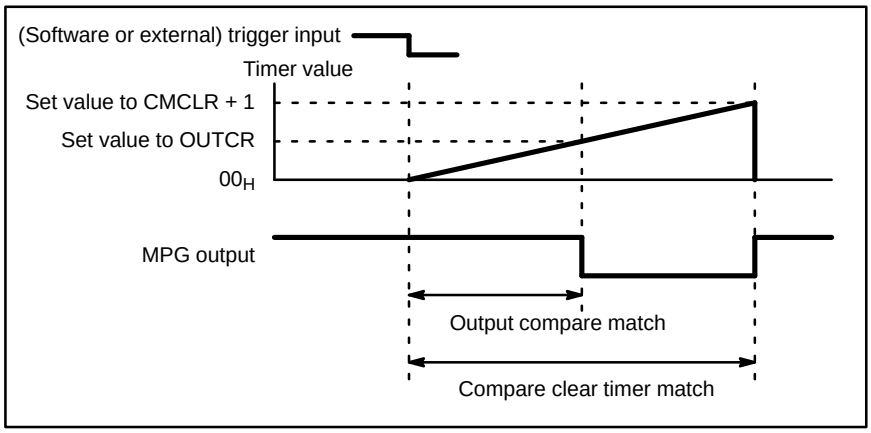


Fig. 2.35 Outline of MPG Output

As shown in Figure 2.35, the MPG can generate a PPG waveform. The MPG output is reset after input of the effective trigger and the time set by the output compare register has elapsed, and is set after the time set by the compare clear register has elapsed.

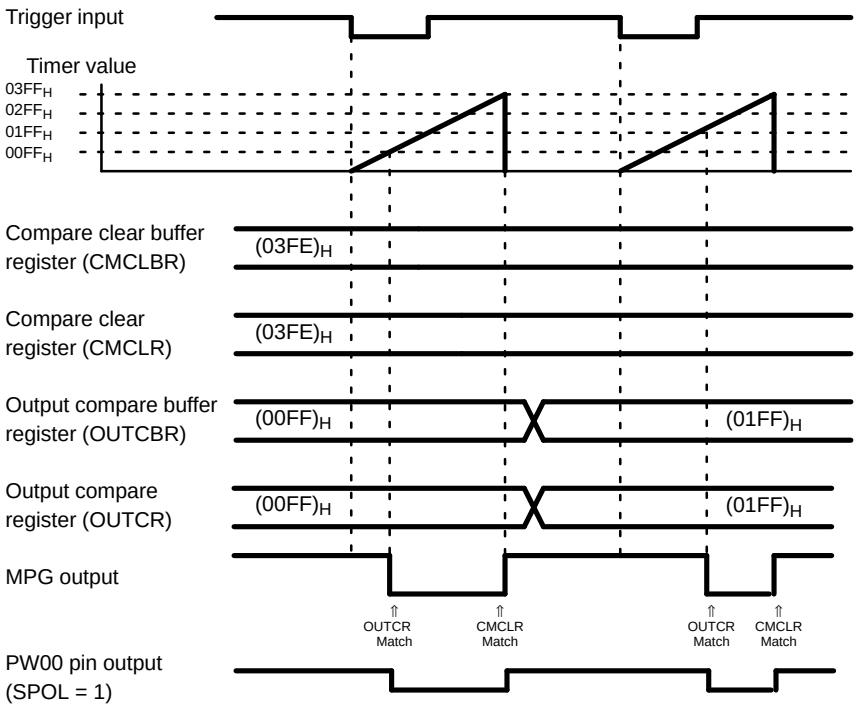
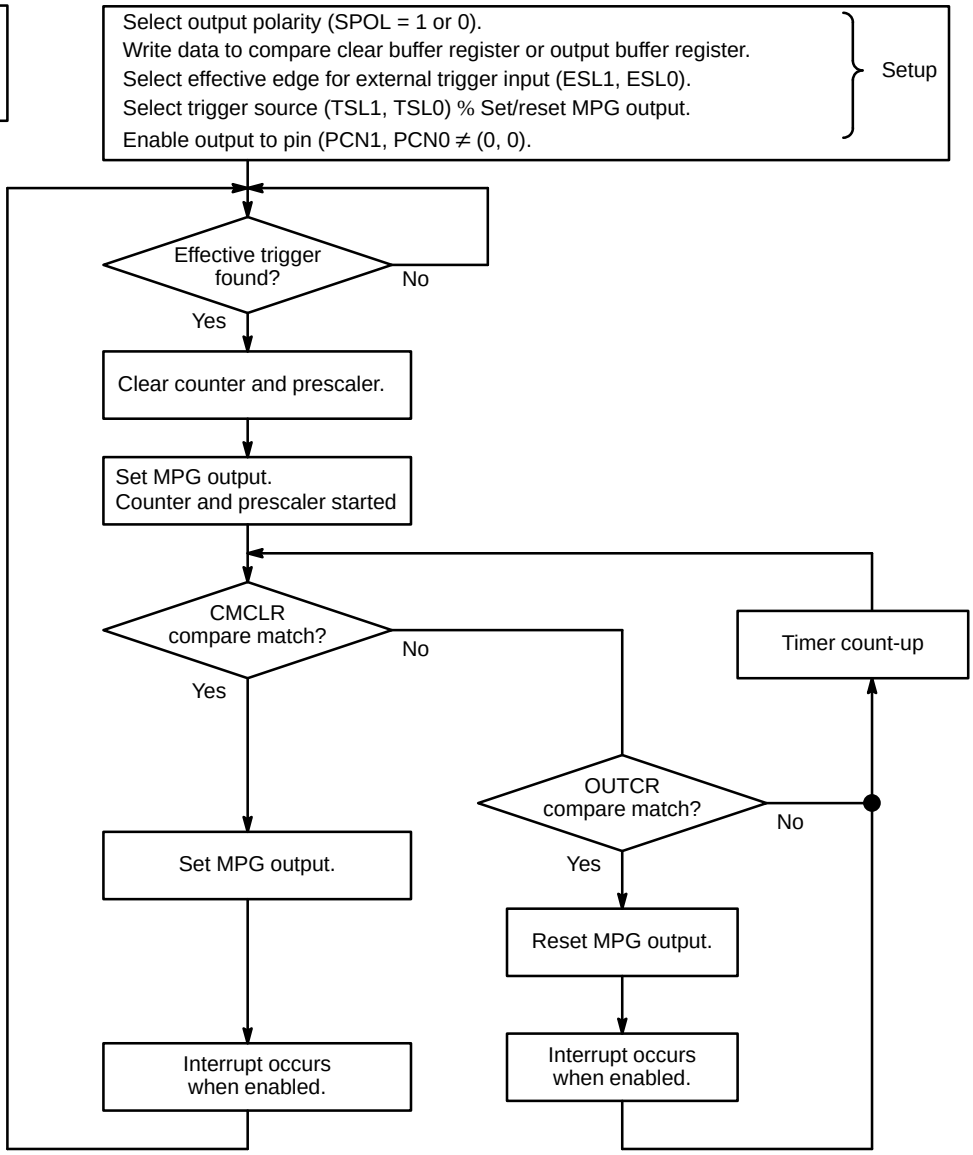


Fig. 2.36 Description of PPG Output Operation

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)



When the operation mode is set to “Stop” or when the DTTI input is performed with overcurrent detection enabled, the MPG output (pin state) goes inactive in this mode.

Fig. 2.37 Flowchart of PPG Operation

Setting the TSL1 and TSL0 bit of the CNTR to 0 and 1 or 1 and 1 gives the PPG operation mode. The PPG operation mode has two modes: retrigger disable and retrigger enable after effective trigger input.

The MPG output is reset after input of the effective trigger and the time set by the OUTCR has elapsed, and is set after the time set by the value of the CMCLR +1 has elapsed. In the initial state, the MPG output is in the set state.

The time from external trigger input to pulse output is as follows:

12-BIT MULTIPUL GENERATOR (MPG, TIMER 4)

Value set at OUTCBR × count clock cycle + 1.5 to 2 system clock cycles

The time from external trigger input to MPG reset is as follows:

(Value set at CMCLR +1) × count clock cycle + 1.5 to 2 system clock cycles

For CMCLR ≤ OUTCR, the MPG output is in the set state and the pulse is not output. For (OUTCR ≠ 0, CMCLR = 0), the MPG output is also in the set state.

When the value of the OUTCR agrees with the value of the CMCLR +1, the comparison with the value of the CMCLR + 1 proceeds and the MPG output is set.

The polarity of the output pulse can be changed by setting the SPOL bit. The set value must not be changed during pulse output. The operation flow for PPG output is shown in Figure 2.37.

The DTTI input pin is provided to inactivate the PPG output inactive at hardware in the event of an external error. When the DTTI input is set to effective, when an error is detected, the DTIR flag is set to inactivate the PPG output. The time required for this operation is 6 to 8 clock cycles (one system clock cycle is 500 ns at 8 MHz and maximum gear speed).

To restart the PPG output after recovery from an error, the DTIR flag must be cleared to input the effective trigger. In the event of an interrupt at DTTI input, other interrupt sources may be set. Therefore, to restart, all MPG interrupt sources should be cleared.

Since the DTTI input is edge input, the rising or falling edge can be selected. The DTTI input block has a noise filter.

8-BIT SERIAL I/O

2.11 8-BIT SERIAL I/O

- 8-bit serial data transfer is possible by the clock synchronous method.
- LSB first or MSB first can be selected for data transfer.
- Four shift-clock modes (three internal and one external) can be selected.

■ Block Diagram

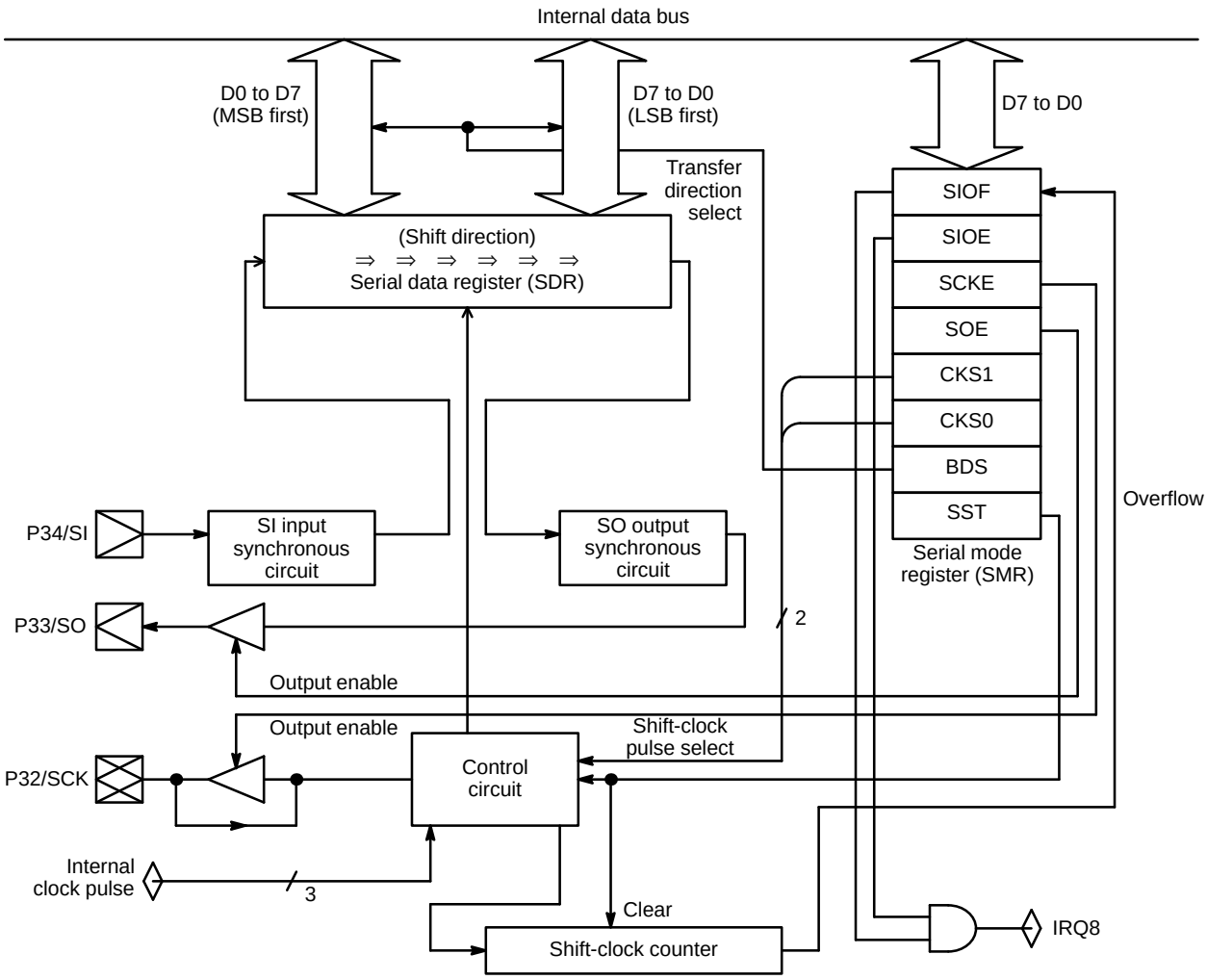
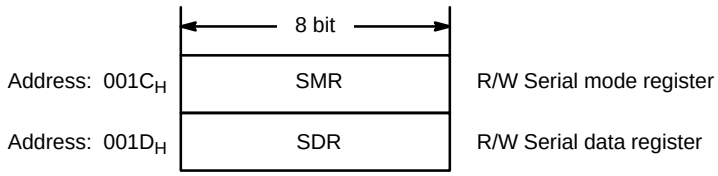


Fig. 2.38 8-bit Serial I/O Block Diagram

■ Register list

The 8-bit serial I/O consists of serial mode register (SMR) and serial data register (SDR).



8-BIT SERIAL I/O

Address: $001C_H$ SMR

Address: $001D_H$ SDR

■ Description of Registers

The detail of each register is described below.

(1) Serial-mode register (SMR)

The SMR is used to control serial I/O.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $001C_H$	SIOF	SIOE	SCKE	SOE	CKS1	CKS0	BDS	SST
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
	Initial value 00000000_B							

[Bit 7] SIOF: Serial I/O interrupt-request flag
This bit is used to indicate the serial I/O transfer state.
The meaning of each bit when reading is as follows:

0	Serial data transfer not terminated
1	Serial data transfer terminated

Note that 1 is always read when the Read Modify Write instruction is read. If this bit is set when an interrupt is enabled (SIOE = 1), an interrupt request is output to the CPU.

The meaning of each bit when writing is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

The end-of-transfer decision may be made by either the SST bit (bit 0 of the SMR) or by this bit.

[Bit 6] SIOE: Serial I/O interrupt-enable bit
This bit is used to enable a serial I/O interrupt request.

0	Serial I/O interrupt-output disable
1	Serial I/O interrupt-output enable

[Bit 5] SCKE: Shift-clock output-enable bit
This bit is used to control the shift-clock I/O pins.

0	General-purpose port pin (P32) or SCK input pin
1	SCK (shift clock) output pin

When using the P32/SCK pin as an external clock, always set the pin to input (bit 2 of DDR4 = 0).

8-BIT SERIAL I/O

[Bit 4] SOE: Serial-data output-enable bit
This bit is used to control the output pin for serial I/O.

0	General-purpose port pin (P33)
1	SO (serial data) output pin

When using P34/SI pin as SI pin, always set the DDR to input (bit 0 of DDR4 = 0).

[Bits 3 and 2] CKS1, CKS0: Shift-clock select bits
These bits are used to select the serial shift-clock modes.

CKS1	CKS0	Mode	Clock cycle at maximum gear speed	SCK
0	0	Internal shift-clock mode	4 system clock cycle	Output
0	1	Internal shift-clock mode	8 system clock cycle	Output
1	0	Internal shift-clock mode	16 system clock cycle	Output
1	1	External shift-clock mode	SCK	Input

Note: One system clock cycle is 500 ns at 8 MHz and maximum gear speed.

[Bit 1] BDS: Transfer direction select bit
At serial data transfer, this bit is used to select whether data transfer is performed from the least significant bit first (LSB first) or from the most significant bit first (MSB first).

0	LSB first
1	MSB first

Note that when this bit is rewritten after writing data to the SDR, the data become invalid.

[Bit 0] SST: Serial I/O transfer-start bit
This bit is used to start serial I/O transfer. The bit is automatically cleared to 0 when transfer is terminated.

0	Serial I/O transfer stop
1	Serial I/O transfer start

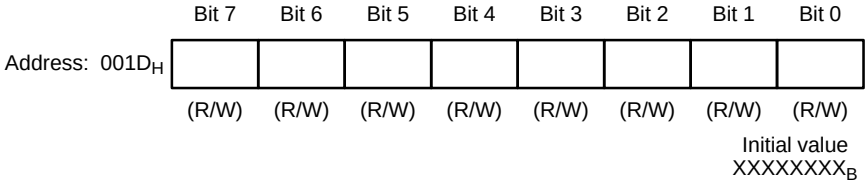
Before starting transfer, ensure that transfer is stopped (SST = 0).

Address: $001C_H$ SMR

Address: $001D_H$ SDR

(2) Serial-data register (SDR)

This 8-bit register is used to hold serial I/O transfer data. Do not write data to this register during the serial I/O operation.



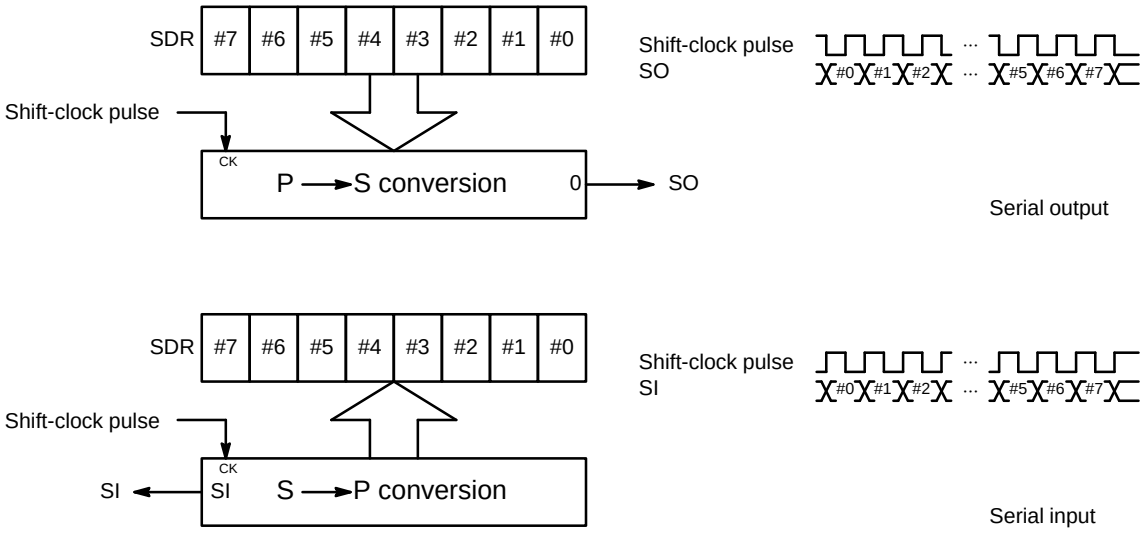
8-BIT SERIAL I/O

■ Description of Operation

The operation of 8-bit serial I/O is described below.

(1) Outline

This module consists of the serial-mode register (SMR) and serial-data register (SDR). At serial output, data in the SDR is output in bit serial to the serial output pin (SO) in synchronization with the falling edge of a serial shift-clock pulse generated from the internal or external clock. At serial input, data is input in bit serial from the serial input pin (SI) to the SDR at the rising edge of a serial shift-clock pulse.



(2) Operation modes

The serial I/O has three internal shift-clock modes and one external shift-clock mode according to the type of shift-clock, which are specified by the SMR. Mode switching or clock selection should be made with serial I/O stopped (SST bit (bit 0) of SMR = 0).

- Internal shift-clock mode
  Operation is performed by the internal clock. A shift-clock pulse with a duty of 50% is output from the SCK pin as a synchronous timing output. Data is transferred bit-by-bit at every clock pulse.

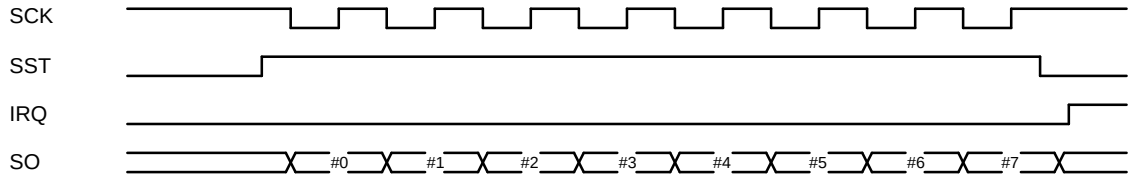
- External shift-clock mode
  Data is transferred bit-by-bit at every clock pulse in synchronization with the external shift-clock pulse input from the SCK pin. The transfer rate can be performed from DC to 8 clock cycles (1.00 MHz at 8 MHz).

Do not write data to the SMR and SDR during the serial I/O operation in either mode.

8-BIT SERIAL I/O

(3) Interrupt functions

This module can output an interrupt request to the CPU. To output an interrupt request, set the SIOE bit of the SMR to 1 to enable an interrupt and then set the interrupt flag SIOF bit of the SMR after 8-bit data transfer is terminated.

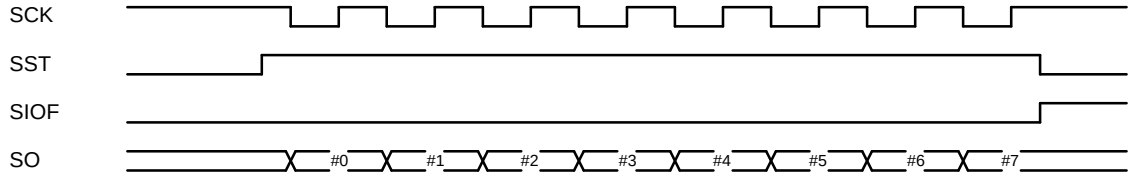


(4) Shift start/stop timing

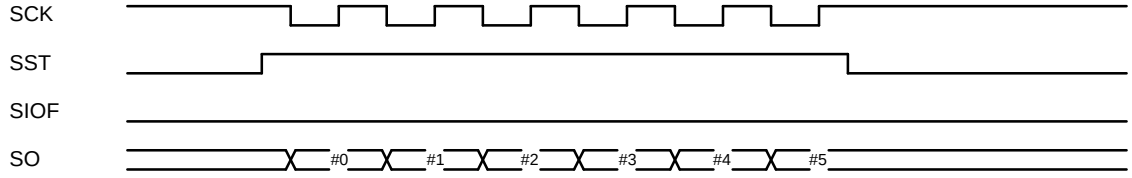
Data transfer starts when 1 is written at the SST bit of the SMR, and stops when 0 is written. When data transfer is terminated, the SST bit is automatically cleared to 0, which stops the operation.

• Internal shift-clock mode (LSB first)

[When transfer terminated]

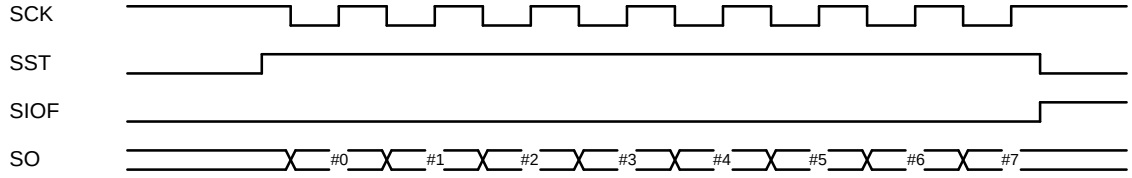


[When transfer suspended]

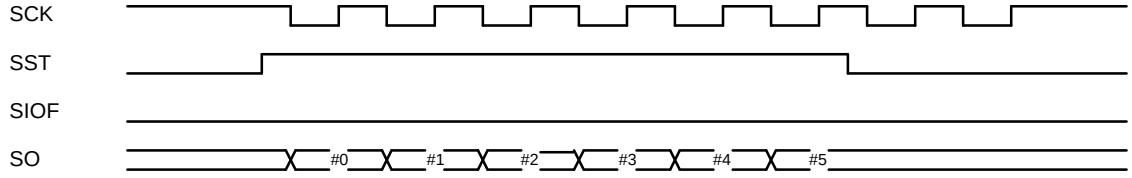


• External shift-clock mode (LSB first)

[When transfer terminated]



[When transfer suspended]



Note: When data is written at the SDR, the output data changes at the falling edge of the external-clock pulse.

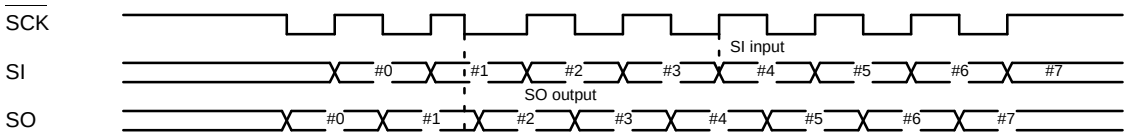
Fig. 2.39 Shift Start/Stop Timing

8-BIT SERIAL I/O

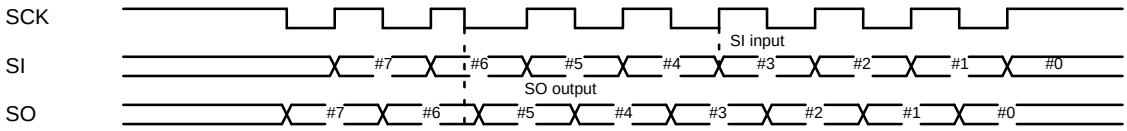
(5) Input/output shift timing

Data is output from the serial output pin (SO) at the falling edge of the shift-clock pulse, and is input from the serial input pin (SI) to the SDR at the rising edge of the shift-clock pulse.

• LSB first (BDS = 0)



• MSB first (BDS = 1)



DI7 to DI0 indicate input data, and DO7 to DO0 indicate output data.

Fig. 2.40 Input/Output Shift Timing

A/D CONVERTER

2.12 A/D CONVERTER

- 16.5 µs conversion time (at 8 MHz and maximum gear speed)
- 10-bit resolution
- RC sequential comparison A/D converter with sample and hold circuit
- Analog input can be selected from 12 channels by the program.
- End detection by interrupt or software polling
- Starting by software, by external pin trigger, or by timer unit can be selected by the program.

■ Block Diagram

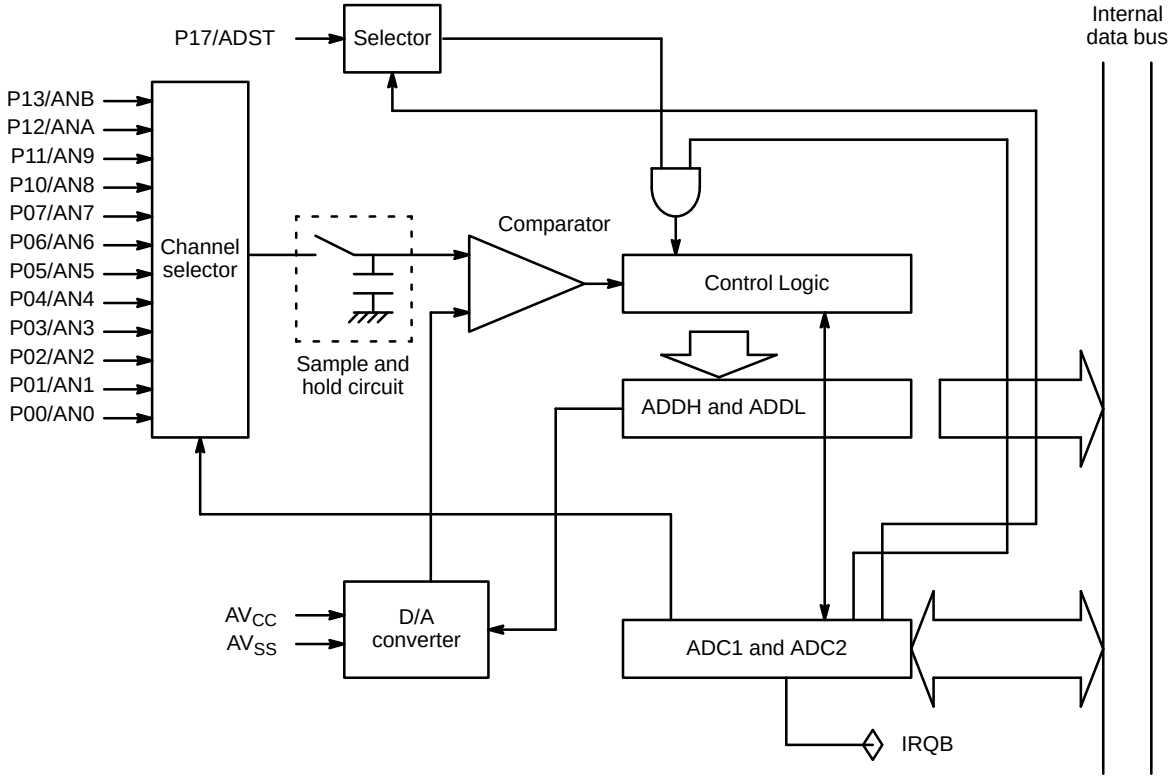
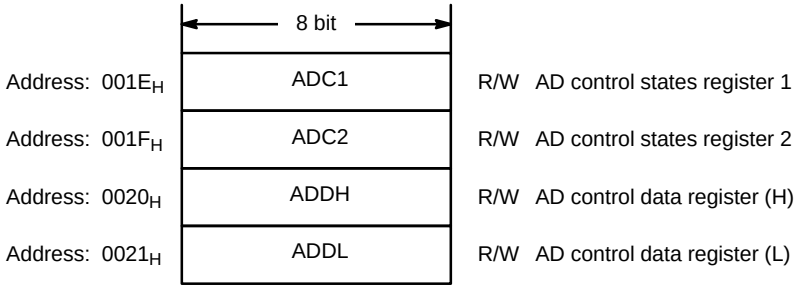


Fig. 2.41 A/D Converter Block Diagram

■ Register list

A/D converter consists of A/D control status registers 1 and 2 and ADC data register (ADCD).



A/D CONVERTER

Address: $001E_H$ ADC1

Address: $001F_H$ ADC2

Address: 0020_H ADDH

Address: 0021_H ADDL

■ Description of Register

The detail of each register is described below.

(1) ADC1 (A/D Converter control register)

This register is used to control the A/D converter and display its status.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $001E_H$	ANS3	ANS2	ANS1	ANS0	AD1	ADMV	SIFM	AD
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	(R/W)
								Initial value 00000000_B

[Bit 7 to Bit 4] ANS3 to ANS0: Analog input channel select bit
These three bits are used to select an analog input channel.

ANS3	ANS2	ANS1	ANS0	Channel selected	ANS3	ANS2	ANS1	ANS0	Channel selected
0	0	0	0	AN0	1	0	0	0	AN8
0	0	0	1	AN1	1	0	0	1	AN9
0	0	1	0	AN2	1	0	1	0	ANA
0	0	1	1	AN3	1	0	1	1	ANB
0	1	0	0	AN4	1	1	0	0	—
0	1	0	1	AN5	1	1	0	1	—
0	1	1	0	AN6	1	1	1	0	—
0	1	1	1	AN7	1	1	1	1	—

[Bit 3] ADI: Interrupt flag bit
The meaning of each bit to be read in the A/D mode is as follows:

0	Conversion not terminated
1	Conversion terminated

The meaning of each bit to be read in the sense mode is as follows:

0	Conditions specified by SIFM bit not met
1	Conditions specified by SIFM bit met

In both the A/D and sense modes, an interrupt request is output if this bit is set when the ADIE (bit 4) of the ADC2 is 1.

The meaning of each bit to be written in the A/D and sense modes is as follows:

0	This bit is cleared.
1	This bit is not changed.

When reading this bit with the Read Modify Write instructions, 1 is always read.

A/D CONVERTER

[Bit 2] ADMV: Processing progress flag
Bit 2 indicates the progress of conversion or comparison processing.

0	Converting and processing not progressing
1	Converting and processing progressing

[Bit 1] SIFM: Interrupt source setting bit
This bit is used to set the conditions for setting interrupt source conversion in the sense mode.

0	Set interrupt source when input voltage lower than voltage set by ADCD register.
1	Set interrupt source when input voltage higher than voltage set by ADCD register.

[Bit 0] AD: A/D conversion start bit
In both the A/D and sense modes, writing 1 at this bit starts A/D conversion when the EXT bit (bit 1) of the ADC2 is 0. Writing 0 at this bit has no meaning. 0 is always read. The meaning of each bit to be written is as follows:

0	No change
1	A/D conversion start (When EXT bit (bit 1) of ADC2 is 0)

Address: $001E_H$ ADC1
Address: $001F_H$ ADC2
Address: 0020_H ADDH
Address: 0021_H ADDL

(2) A/D converter control register 2 (ADC2)

The ADC2 is used to control the A/D converter and to indicate its operation status.

Address: $001F_H$

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	TIM1	TIM0	ADCK	ADIE	ADMD	EXT	TEST
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
							Initial value 00000001_B

[Bits 6 and 5] TIM1, TIM0: Conversion/comparison time select bits
Bits 6 and 5 are used to select the conversion time or comparison time.

TIM1	TIM0	Conversion time at 8 MHz and maximum gear speed	Comparison time at 8 MHz and maximum gear speed
0	0	33 system clock cycles (16.5 μs)	18 system clock cycles (9.0 μs)
0	1	48 system clock cycles (24.0 μs)	33 system clock cycles (16.5 μs)
1	0	66 system clock cycles (33.0 μs)	51 system clock cycles (25.5 μs)
1	1	90 system clock cycles (45.0 μs)	75 system clock cycles (37.5 μs)

A/D CONVERTER

[Bit 4] ADCK: External input clock pulse select bit
Bit 4 is used to select the clock pulse for starting by the external input clock pulse.

0	No change
1	Operation started (when EXT bit (bit 1) of ADC2 is 1)

[Bit 3] ADIE: Interrupt specification bit
This bit is used to specify interrupt enable/disable.

0	Interrupt disabled
1	Interrupt enabled

[Bit 2] ADMD: Function-switching bit
This bit is used to switch the A/D mode and sense mode.

0	A/D mode
1	Sense mode

[Bit 1] EXT: Start type select bit
Bit 1 is used to select the conversion start type.

0	Starts A/D conversion with AD bit (bit 0) of ADC1
1	Starts A/D conversion at rising edge of clock selected by ADCK bit (bit 4) of ADC2

[Bit 0] TEST: Test bit
This bit is used only for testing. Always write 1 at this bit. 1 is always read.

Address: $001E_H$ ADC1

Address: $001F_H$ ADC2

Address: 0020_H ADDH

Address: 0021_H ADDL

(3) A/D data registers H and L (ADDH and ADDL)

These registers are used to store the results of A/D conversion in A/D mode and write the comparison set value in the Sense mode. Two upper bits and eight lower bits are assigned to the ADDH and ADDL, respectively.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0020_H	—	—	—	—	—	—	9	8
							(R/W)	(R/W)
							Initial value $000000XX_B$	
Address: 0021_H	7	6	5	4	3	2	1	0
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
							Initial value $XXXXXXXX_B$	

A/D CONVERTER

• When A/D mode

In the A/D mode, the result of the A/D conversion is stored as soon as conversion is terminated. After the completion of conversion, the value of the register is held until conversion is restarted.

As soon as conversion is started, the value of the register becomes undefined. Therefore, the conversion value must always be read after the end of conversion before the next conversion is started.

• When Sense mode

In the Sense mode, the set value to be compared is written beforehand to this register.

The value of the register, once set, is held unchanged even after comparison.

Do not write data during conversion in either the A/D or sense modes.

■ Description of Operation

The operation of the AD converter is described below.

(1) A/D mode

• Start/restart by software
Writing 0 at the ADMD bit (bit 2) of the ADC2 gives the A/D mode. Writing 1 at the AD (bit 0) of the ADC1 starts the A/D conversion.

When 1 is written at the AD bit (bit 0) of the ADC1 during conversion, the conversion being executed is aborted to restart the next conversion.

• Start/restart by external clock pulse
Writing 1 at the EXT bit (bit 1) of the ADC2 in the A/D mode gives the standby state for starting by an external clock pulse. When the rising edge of the clock pulse selected by the ADCK bit (bit 4) of the ADC2 is detected, the conversion is started.

When the clock pulse is given at the rising edge during conversion, the conversion being executed is aborted to restart the conversion. If the conversion is started or restarted by the external clock pulse with the EXT bit (bit 1) of the ADC2 set to 1, it cannot be started or restarted by software.

• End
After completion of conversion, the results are stored in the data register and the ADI bit (bit 3) of the ADC1 is set. At this time, if the ADIE bit (bit 2) of the ADC2 is 1, an interrupt request occurs.

The results of conversion are held in the data register until the next conversion is started. Therefore, the conversion value should be read after conversion before the next conversion is started. As soon as the conversion is started, the previous conversion results are lost.

A/D CONVERTER

- Continuous start by external clock pulse
  Providing a clock pulse based on the conversion time and result reading time permits continuous starting of conversion.

(2) Sense mode

- Comparison/recomparison by software
  The set value to be compared is written beforehand to the data register.

  Writing 1 at the ADMD bit (bit 2) of the ADC2 and selects the Sense mode. Writing 1 at the AD bit (bit 0) of the ADC1 and starts comparison.

  When 1 is written at the AD bit (bit 0) of the ADC1 during comparison, the comparison being executed is aborted to restart comparison.

- Comparison/recomparison by external clock pulse
  The set value to be compared is written beforehand to the data register.

  Writing 1 at the EXT bit (bit 1) of the ADC2 in the Sense mode gives the standby state for starting by an external clock pulse. When the rising edge of the clock pulse selected by the ADCK bit (bit 4) of the ADC2 is detected, the comparison is started.

  When a clock pulse is provided at the rising edge during comparison, the comparison being executed is aborted to restart the comparison. If the comparison or recomparison is executed by the external clock pulse with the EXT bit (bit 1) of the ADC2 set to 1, it cannot be compared or recompared by software.

- End
  If the results of comparison meet the conditions set by the SIFM bit (bit 1) of the ADC1, the ADI bit (bit 3) of the ADC1 is set. At this time, if the ADIE bit (bit 2) of the ADC2 is 1, an interrupt request occurs.

  If the results of comparison do not meet the conditions, the ADI bit (bit 3) of the ADC1 is not set. In this case, the end of comparison should be fixed to when the ADMV bit (bit 2) of the ADC1 becomes 0.

  The set value written to the data register is held unchanged even after comparison.

- Continuous start by external clock pulse
  Providing a clock pulse based on the comparison time permits continuous starting of comparison.

A/D CONVERTER

■ Precautions for A/D converter

(1) In the Reset mode, conversion and comparison stop to initialize each register.

In the Stop mode, conversion and comparison stop to clear the flag bit (ADMV bit (bit 2) of the ADC1) in operation. The settings of other bits remain unchanged.

(2) If starting is performed by the external clock pulse, it cannot be done by software (AD bit (bit 1) of the ADC1).

(3) Do not rewrite the setting of each register during conversion and comparison.

To change the setting with starting by the external clock pulse, set the EXT bit (bit 1) of the ADC2 to 0 when the operation is stopped (ADMV bit (bit 2) of the ADC1 is 0), and then inhibit starting by the external clock pulse.

If the start is made by software (AD bit (bit 1) of the ADC1), the analog input channel for restart can be switched and the interrupt source in the Sense mode can be changed.

(4) To switch between the A/D and Sense modes, clear the interrupt flag bit (ADI bit (bit 3) of the ADC1).

(5) To perform continuous starting of conversion and comparison by the external clock pulse, set the time based on the conversion and comparison timing, and results reading.

The A/D conversion value is effective until the next conversion is started after conversion. The set value written at the data register in the Sense mode is held even after comparison.

BUZZER OUTPUT CIRCUIT

2.13 BUZZER OUTPUT CIRCUIT

- The buzzer output sound for checking key input can be output.
- Two frequencies can be output by setting the registers.

■ Block Diagram

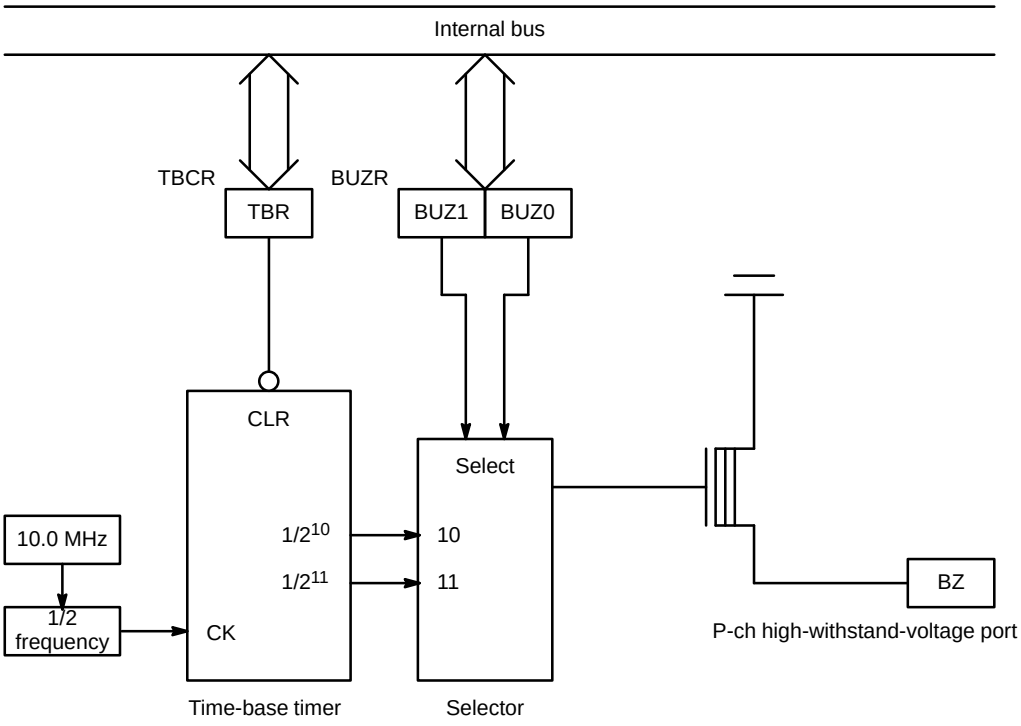
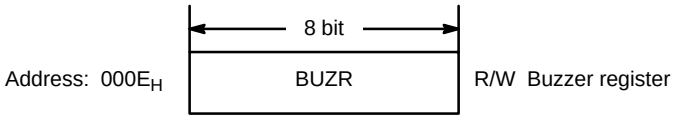


Fig. 2.42 Buzzer Output Circuit Block Diagram

■ Registers

The buzzer output block has buzzer register (BUZR).



BUZZER OUTPUT CIRCUIT

Address: $000E_H$ BUZR

■ Description of Registers

The detail of buzzer register is described below.

• Buzzer register (BUZR)

This 2-bit register enables buzzer output and selects the frequency.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $000E_H$	—	—	—	—	—	—	BUZ1	BUZ0
							(R/W)	(R/W)
							Initial value	
							------00_B	

[Bits 1 and 0] BUZ1, BUZ0: Buzzer-select bits
These bits are used to enable buzzer output and select the frequency. The buzzer output function is disabled by 00. In other cases, the frequencies listed in the table below are selected.

Table 2-7 Buzzer Output Frequencies (at 8.0 MHz of oscillation frequency)

BUZ1	BUZ0	Buzzer output frequency
0	0	High impedance
0	1	Set (H)
1	0	3.91 kHz
1	1	1.95 kHz

■ Description of Operation

This circuit outputs a signal for use as a check sound. The buzzer register is used to enable buzzer output and select the frequency. Setting 00 at the BUZR register produces a square wave of Hi-Z frequency, and setting 01 produces a square wave of High frequency.

Setting 10 or 11 at the BUZR register, and setting the square wave as above values.

■ Precautions for Buzzer Output Circuit

Part of the time-base timer is used as the buzzer output. Therefore, clear operation of the time-base timer affects the circuit.

EXTERNAL INTERRUPT CIRCUIT

2.14 EXTERNAL INTERRUPT CIRCUIT

- The edges of two external-interrupt sources (INT0 and INT1) can be detected to set the corresponding flag.
- An interrupt can be generated at the same time the flag is set.
- Both interrupt can release the STOP or SLEEP mode.

■ Block Diagram

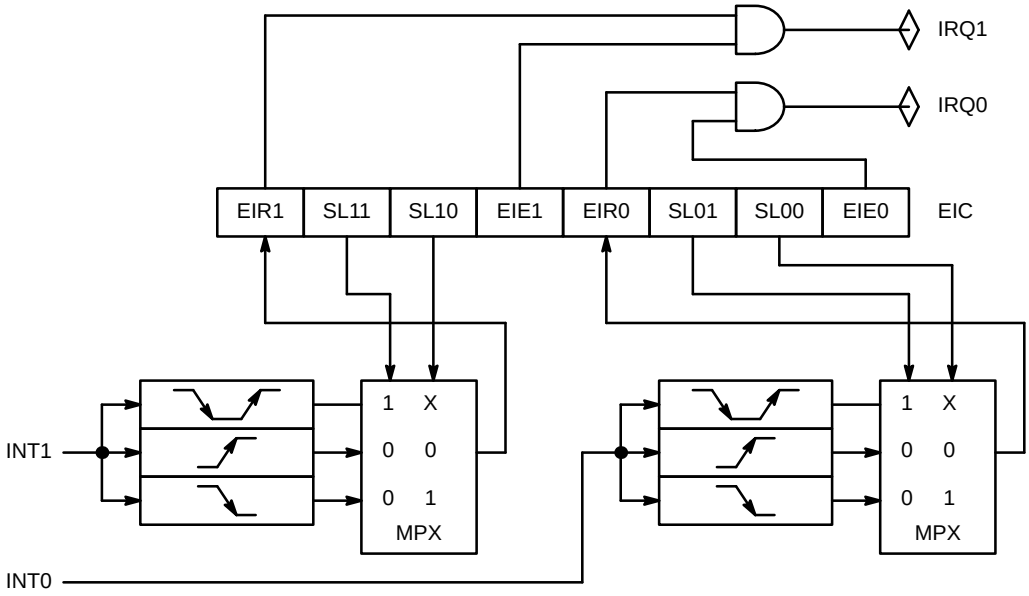
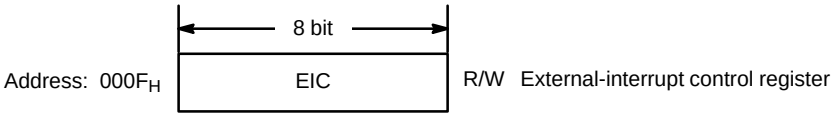


Fig. 2.43 External Interrupt Circuit Block Diagram

■ Register List



■ Description of Registers

Address: 000F$_H$ EIC

• External-interrupt control register (EIC)

The EIC controls an interrupt by the IRQ pin.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 000F$_H$	EIR1	SL11	SL10	EIE1	EIR0	SL01	SL00	EIE0
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
	Initial value 00000000$_B$							

EXTERNAL INTERRUPT CIRCUIT

[Bit 7] EIR1: External-interrupt request flag
When the edge specified by the SL10 and SL11 bits is input to the INT1 pin, bit 7 is set to 1. When the EIE1 bit is 1, an interrupt request (IRQ1) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT1 pin
1	Specified edge input to INT1 pin (IRQ1 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 6 and Bit 5] SL11, SL10: Edge-polarity mode select bit
These bits are used to control the input edge polarity of the INT1 pin.

SL11	SL10	Selection of external interrupt enable edge
1	×	Both-edge mode
0	1	Rising edge
0	0	Falling edge

[Bit 4] EIE1: Interrupt-enable bit
This bit is used to enable an external-interrupt request by the INT1 pin.

0	Interrupt request disabled
1	Interrupt request enabled by EIR1 setting

[Bit 3] EIR0: External-interrupt request flag
When the edge specified by the SL00 and SL01 bits is input to the INT0 pin, bit 3 is set to 1. When the EIE0 is 1, an interrupt request (IRQ0) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT0 pin
1	Specified edge input to INT0 pin (IRQ0 is output.)

1 is always read when the Read Modify Write instruction is read.

EXTERNAL INTERRUPT CIRCUIT

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 2 and Bit 1] SL01, SL00: Edge-polarity mode select bit
These bits are used to control the input edge polarity mode of the INT0 pin.

SL11	SL10	Selection of external interrupt enable edge
1	×	Both-edge mode
0	1	Rising edge
0	0	Falling edge

[Bit 0] EIE0: Interrupt-enable bit
Bit 0 is used to enable an external-interrupt request by the INT0 pin.

0	Interrupt request disabled
1	Interrupt request enabled by EIR0 setting

■ Precautions for Using External Interrupt Circuit

To enable the interrupt after reset is cleared, clear the interrupt flag at the same time. When the external interrupt request flags (EIR1 and EIR0) are set to 1, an interrupt request occurs immediately.

3. OPERATION

The operation of MB89140 is described below.

3.1 CLOCK PULSE GENERATOR

The MB89140 series of microcontrollers incorporate the system clock pulse generator. The crystal oscillator is connected to the X0 and X1 pins to generate clock pulses. Clock pulses can also be supplied internally by inputting externally-generated clock pulses to the X0 pin. The X1 pin should be kept open.

The X0A and X1A pins are used for the subclock and function in the same manner as the X0 and X1 pins.

When the single-channel clock option is selected, the X0A and X1A pins serve as the P70 and P71 pins respectively.

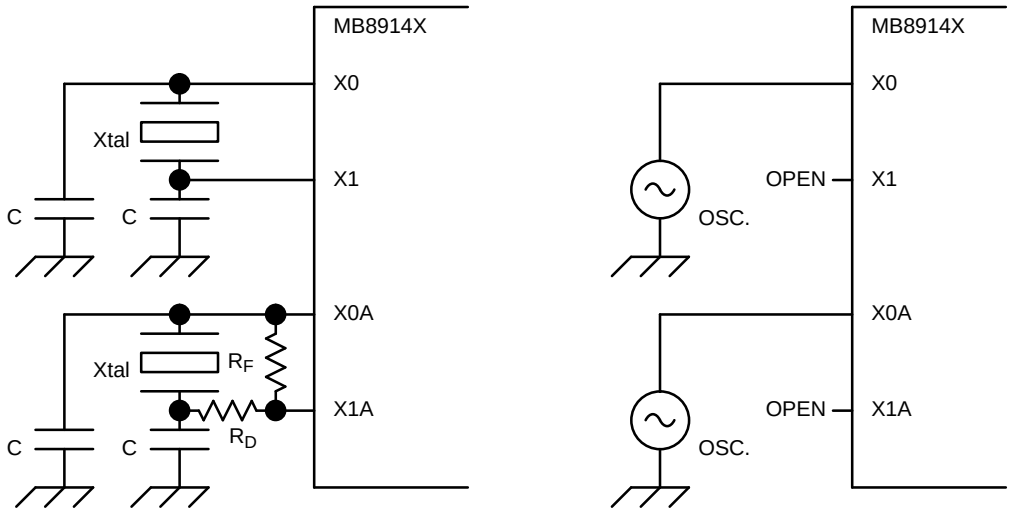


Fig. 3.1 Clock Pulse Generator

3.2 RESET

The detail of reset operation and reset sources are described below.

3.2.1 Reset Operation

When reset conditions occur, the MB89140 series of microcontrollers suspend the currently-executing instruction to enter the reset state. The contents written at the RAM do not change before and after reset. However, if a reset occurs during writing of 16-bit long data, data is written to the upper bytes and may not be written to lower bytes. If a reset occurs around write timing, the contents of the addresses being written are not assured.

When the reset conditions are cleared, the MB89140 series of microcontrollers are released from the reset state and start operation after fetching the mode data from address **$FFFD_H$**, the upper bytes of the reset vectors from address **$FFFE_H$**, and the lower bytes from address **$FFFF_H$**, in that order. Figure 3.2 shows the flowchart for the reset operation.

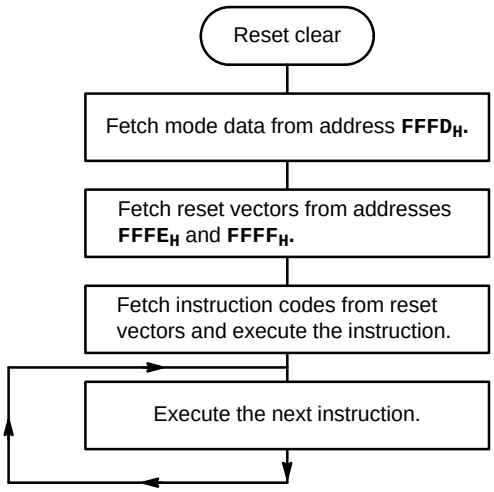
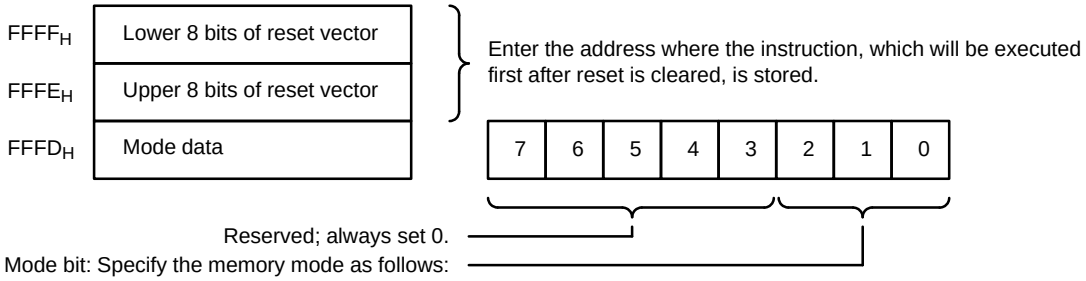


Fig. 3.2 Outline of Reset Operation

Figure 3.3 indicates the structure of data to be stored in addresses **$FFFD_H$**, **$FFFE_H$**, and **$FFFF_H$**.



T2	T1	T0	Operation
0	0	0	External-access disable (single chip)
Other than above			Reserved; do not set.

Fig. 3.3 Reset Vector Structure

3.2.2 Reset Sources

The MB89140 series of microcontrollers have the following reset sources.

(1) External pin	A Low level is input to the $\overline{RST}$ pin.
(2) Specification by software	0 is written at the RST bit of the standby-control register.
(3) Power-on	Power-on reset
(4) Watchdog function	The watchdog function is enabled by the watchdog-control register and reaccess to this register is not obtained within the specified time.

When the stop mode is cleared by reset or power-on reset, operation is started after elapse of the oscillation stabilization time.

For details, see pages 2-19 and 2-20.

Note: In modes other than Stop, the external reset input is sampled by the external clock pulse. Therefore, no reset input is accepted when external clock pulses are not supplied to the MB89140.

3.3 INTERRUPT

If the interrupt controller and CPU are ready to accept interrupts when an interrupt request is output from the internal resources or by an external-interrupt input, the CPU temporarily suspends the currently-executing instruction and executes the interrupt-processing program. Figure 3.4 shows the interrupt-processing flowchart.

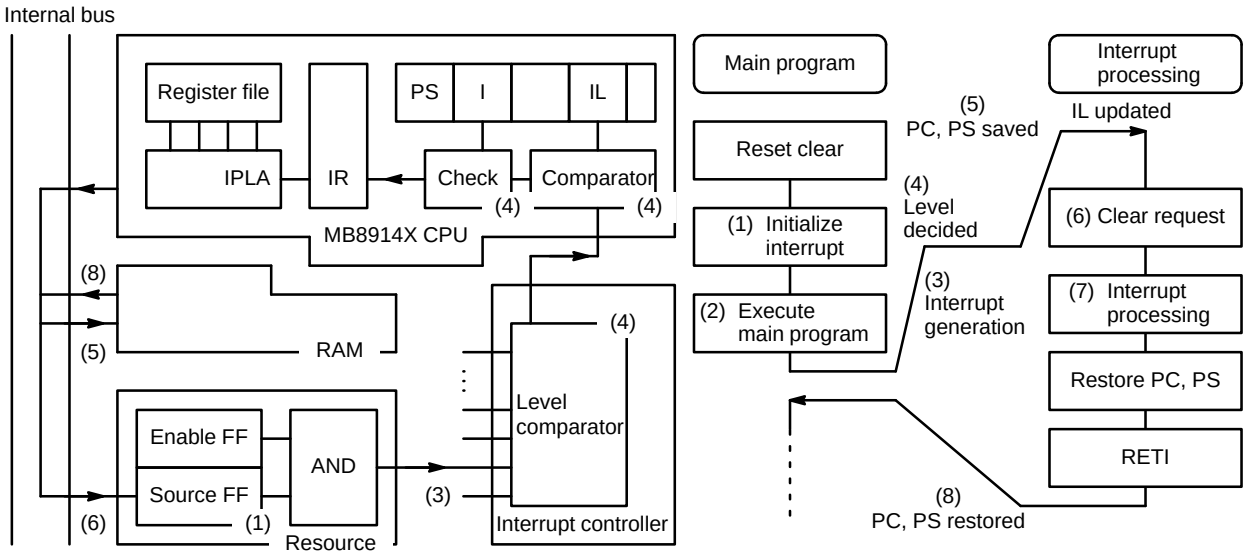


Fig. 3.4 Interrupt-processing Flowchart

All interrupts are disabled after a reset is cleared. Therefore, initialize interrupts in the main program (1). Each resource generating interrupts and the interrupt-level-setting registers (ILR1 to ILR3) in the interrupt controller corresponding to these interrupts are to be initialized. The levels of all interrupts can be set by the interrupt-level-setting registers (ILR1 to ILR3) in the interrupt controller. The interrupt level can be set from 1 to 3, where 1 indicates the highest level, and 2 the second highest level. Level 3 indicates that no interrupt occurs. The interrupt request of this level cannot be accepted. After initializing the registers, the main program executes various controls (2). Interrupts are generated from the resources (3). The highest-priority interrupt requests are identified from those occurring at the same time by the interrupt controller and are transferred to the CPU. The CPU then checks the current interrupt level and the status of the I-flag (4), and starts the interrupt processing.

The CPU performs the interrupt processing to save the contents of the current PC and PS in the stack (5) and fetches the entry addresses of the interrupt program from the interrupt vectors. After updating the IL value in the PS to the required one, the CPU starts executing the interrupt-processing routine.

Clear the interrupt sources (6) and process the interrupts in the user's interrupt-processing routine. Finally, restore the PC and PS values saved by the RETI instruction in the stack (8) to return to the interrupted instruction.

Note: Unlike the F^2MC-8 family, A and T are not saved in the stack at the interrupt time. If interrupts of the same level occur at the same time, IRQ0 takes precedence.

Table 3-1 lists the relationships between each interrupt source and interrupt vector.

Table 3-1 Interrupt Sources and Interrupt Vectors

Interrupt source	Upper vector address	Lower vector address
IRQ0 (External interrupt 0)	$FFFA_H$	$FFFB_H$
IRQ1 (External interrupt 1)	$FFF8_H$	$FFF9_H$
IRQ2 (8-bit PWM timer: Timer 1)	$FFF6_H$	$FFF7_H$
IRQ3 (8/16-bit timer/counter: Timer 2)	$FFF4_H$	$FFF5_H$
IRQ4 (8/16-bit timer/counter: Timer 3)	$FFF2_H$	$FFF3_H$
IRQ5 (12-bit MPG CMIR)	$FFF0_H$	$FFF1_H$
IRQ6 (12-bit MPG CLIR)	$FFEE_H$	$FFEF_H$
IRQ7 (12-bit MPG DTIR)	$FFEC_H$	$FFED_H$
IRQ8 (8-bit serial I/O)	$FFEA_H$	$FFEB_H$
IRQ9 (A/D converter)	$FFE8_H$	$FFE9_H$
IRQA (Interval timer)	$FFE6_H$	$FFE7_H$
IRQB (Watch)	$FFE4_H$	$FFE5_H$

3.4 LOW-POWER CONSUMPTION MODES

The MB89140 series of microcontrollers have three standby modes: sleep, stop, and watch to reduce the power consumption. Writing to the standby control register (STBC) switches to these three standby modes. See 2.2 for setting and releasing each mode.

The MB89140 series of microcontrollers have a double clock module, and the low-power consumption modes vary with the main clock and subclock modes. Whether or not an oscillation stabilization period is required at release from each low-power consumption mode depends on the mask option of the power-on reset (see the status transition chart in 2.2).

If the single clock module is specified with the mask option, the MB89140 series of microcontrollers can be used as single clocks. If the microcontrollers are used as single clocks without specifying the single clock module with the mask option, once the subclock mode is entered, it cannot be released. Therefore, when using these controllers as a single clock, specify the single clock module with the mask option.

Table 3-2 Low-power Consumption Mode at Each Clock Mode

Function		Note	Main mode			Sub-mode			
			RUN	SLEEP	STOP	RUN	SLEEP	STOP	Watch
Main clock		—	Operate	Operate	Stop	Stop	Stop	Stop	Stop
Subclock		—	Operate	Operate	Operate	Operate	Operate	Stop	Operate
CPU	Instruction	A	Operate	Stop	Stop	Operate	Stop	Stop	Stop
	ROM	A	Operate	Hold	Hold	Operate	Hold	Hold	Hold
	RAM	A							
Re-source	I/O	A	Operate	Hold	Hold	Operate	Hold	Hold	Hold
	Watch prescaler	B	Operate	Operate	Operate*1	Operate	Operate	Stop	Operate
	Time-based timer	B	Operate	Operate	Stop	Stop	Stop	Stop	Stop
	8-bit PWM	A	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	8/16-bit timer	A	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	12-bit MPG	A	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	8-bit SIO	A	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	10-bit A/D converter	A	Operate	Operate	Operate	Operate*2	Operate*2	Operate	Operate
	External interrupt	A	Operate	Operate	Operate	Operate	Operate	Operate	Operate
	Buzzer output	B	Operate	Operate	Stop	Stop	Stop	Stop	Stop
	Watchdog timer	B	Operate	Stop	Stop	Operate*3	Stop	Stop	Stop

Notes:
A The operating speed is affected by the clock mode (main clock or subclock) and the gear function.
B The operating speed is not affected by the clock mode (main clock or subclock) and the gear function.
*1 The watch prescaler performs counting but no timer interrupt occurs.
*2 Although operation is possible, do not use this.
*3 When clock source used as watch prescaler

3.5 PIN STATES FOR SLEEP, STOP AND RESET

The state of each pin of the MB89140 series of microcontrollers at sleep, stop and reset is as follows:

(1) Sleep The pin state immediately before the sleep state is held.

(2) Stop The pin state immediately before the stop state is held when the stop mode is started and bit 5 of the standby-control register (STBC) is set to 0; the impedance of the output and input/output pins goes High when the bit is set to 1.

(3) Reset When the MOD pin is 0, the impedance of all I/O and resource pins (excluding pins for pull-up option) goes High.

Table 3-3 Pin State of MB89140

Pin name	Normal	Sleep	Stop/Watch SPL = 0	Stop/Watch SPL = 1	Reset
X0	Input for oscillation	Input for oscillation	High impedance*2	High impedance*2	Input for oscillation
X1	Output for oscillation	Output for oscillation	High output	Mode input	Input for oscillation
MODA	Mode input	Mode input	Mode input	Mode input	Mode input
$\overline{RST}$	Reset input	Reset input	Reset input	Reset input	Reset input*5
P07/AN7 to P00/AN0	Port/resource input/output	Port/resource input/output	Port/resource input/output	High impedance*2	High impedance
P13/AN8 to P10/ANB	Port/resource input/output	Port/resource input/output	Port/resource input/output	High impedance*2	High impedance
P16 to P14	Port input/output	Port input/output	Port input/output	High impedance*2	High impedance
P23, P20	Port output	Port output	Port output	High impedance	High impedance*6
P22/WDG	Port output/ resource output	Port output/ resource output	Port output/ resource output	High impedance	High impedance*6
P21/PWO0	Port output/ resource output	Port output/ resource output	Port output/ resource output	High impedance	High impedance*6
P17/ADST P37/DTTI to P30/INT0/TRG	Port/resource input/output	Port/resource input/output	Port/resource input/output	High impedance*3	High impedance
P47 to P40	Port output	Port output	Port output	High impedance	High impedance
P57 to P50	Port output	Port output	Port output	High impedance	High impedance
P67 to P60	Port output	Port output	Port output	High impedance	High impedance
P70/X0A*1	Port input	Port input	Port input	High impedance*4	High impedance
P71/X1A*1	Port input	Port input	Port input	High impedance*4	High impedance
BZ	Buzzer output	Buzzer output	Buzzer output	High impedance	High impedance

*1 When the single-circuit clock or dual-circuit clock is selected, the same operation as X0 and X1 is performed.

*2 The input level is fixed to prevent leakage due to open input.

*3 The input of P30/INT0 and P31/INT1 should be fixed to High or Low.

*4 Low output is provided after reset is cleared.

*5 At power-on reset, a Low level is output during the oscillation stabilization time.

*6 Low output is provided after reset is cleared.

4. INSTRUCTIONS

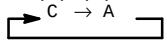
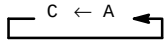
4.1 TRANSFER INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
2	MOV @IX+off,A	4	2	((IX)+off) ← (A)	–	–	–	– – – –	46
3	MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
4	MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
5	MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
6	MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
7	MOV A,dir	3	2	(A) ← dir	AL	–	–	+ + – –	05
8	MOV A,@IX+off	4	2	(A) ← ((IX)+off)	AL	–	–	+ + – –	06
9	MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
10	MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
11	MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
12	MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
13	MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
14	MOV @IX+off,#d8	5	3	((IX)+off)← d8	–	–	–	– – – –	86
15	MOV @EP,#d8	4	2	((EP))← d8	–	–	–	– – – –	87
16	MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
17	MOVW dir,A	4	2	(dir) ←(AH),(dir+1)← (AL)	–	–	–	– – – –	D5
18	MOVW @IX+off,A	5	2	((IX)+off)←(AH),((IX)+off+1)←(AL)	–	–	–	– – – –	D6
19	MOVW ext,A	5	3	(ext) ← (AH),(ext+1)←(AL)	–	–	–	– – – –	D4
20	MOVW @EP,A	4	1	((EP)) ← (AH),((EP)+1)← (AL)	–	–	–	– – – –	D7
21	MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
22	MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
23	MOVW A,dir	4	2	(AH)←(dir),(AL)←(dir+1)	AL	AH	dH	+ + – –	C5
24	MOVW A,@IX+off	5	2	(AH)←((IX)+off),(AL)←((IX)+off+1)	AL	AH	dH	+ + – –	C6
25	MOVW A,ext	5	3	(AH)←(ext),(AL)←(ext+1)	AL	AH	dH	+ + – –	C4
26	MOVW A,@A	4	1	(AH)←((A)),(AL)← ((A)+1)	AL	AH	dH	+ + – –	93
27	MOVW A,@EP	4	1	(AH)←((EP)),(AL) ←((EP)+1)	AL	AH	dH	+ + – –	C7
28	MOVW A,EP	2	1	(A) ←(EP)	–	–	dH	– – – –	F3
29	MOVW EP,#d16	3	3	(EP)←d16	–	–	–	– – – –	E7
30	MOVW IX,A	2	1	(IX)←(A)	–	–	–	– – – –	E2
31	MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
32	MOVW SP,A	2	1	(SP)← (A)	–	–	–	– – – –	E1
33	MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
34	MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
35	MOVW @A,T	4	1	((A)) ← (TH),((A)+1) ← (TL)	–	–	–	– – – –	83
36	MOVW IX,#d16	3	3	(IX)← d16	–	–	–	– – – –	E6
37	MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
38	MOVW PS,A	2	1	(PS)← (A)	–	–	–	+ + + +	71
39	MOVW SP,#d16	3	3	(SP)← d16	–	–	–	– – – –	E5
40	SWAP	2	1	(AH) ⇔ (AL)	–	–	AL	– – – –	10
41	SETB dir:n	4	2	(dir):n ← 1	–	–	–	– – – –	A8 to AF
42	CLRB dir:n	4	2	(dir):n ← 0	–	–	–	– – – –	A0 to A7
43	XCH A,T	2	1	(AL) ⇔ (TL)	AL	–	–	– – – –	42
44	XCHW A,T	3	1	(A) ⇔ (T)	AL	AH	dH	– – – –	43
45	XCHW A,EP	3	1	(A) ⇔ (EP)	–	–	dH	– – – –	F7
46	XCHW A,IX	3	1	(A) ⇔ (IX)	–	–	dH	– – – –	F6
47	XCHW A,SP	3	1	(A) ⇔ (SP)	–	–	dH	– – – –	F5
48	MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes

1. In byte transfer to A, T ← A is only for low bytes.
2. Operands for two or more operand instructions should be stored in the order designated in MNEMONIC (Opposite order to F^{2}MC-8 family).
3 ~ indicates the number of instruction cycles and # indicates the number of instruction bytes.

4.2 OPERATION INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	ADDC A,Ri	3	1	(A) ← (A)+(Ri)+C	–	–	–	+ + + +	28 to 2F
2	ADDC A,#d8	2	2	(A) ← (A)+d8+C	–	–	–	+ + + +	24
3	ADDC A,dir	3	2	(A) ← (A)+(dir)+C	–	–	–	+ + + +	25
4	ADDC A,@IX+off	4	2	(A) ← (A)+((IX)+off)+C	–	–	–	+ + + +	26
5	ADDC A,@EP	3	1	(A) ← (A)+((EP))+C	–	–	–	+ + + +	27
6	ADDCW A	3	1	(A) ← (A)+(T)+C	–	–	dH	+ + + +	23
7	ADDC A	2	1	(AL)← (AL)+(TL)+C	–	–	–	+ + + +	22
8	SUBC A,Ri	3	1	(A) ← (A)–(Ri)–C	–	–	–	+ + + +	38 to 3F
9	SUBC A,#d8	2	2	(A) ← (A)–d8–C	–	–	–	+ + + +	34
10	SUBC A,dir	3	2	(A) ← (A)–(dir)–C	–	–	–	+ + + +	35
11	SUBC A,@IX+off	4	2	(A) ← (A)-((IX)+off)–C	–	–	–	+ + + +	36
12	SUBC A,@EP	3	1	(A) ← (A)-((EP))+C	–	–	–	+ + + +	37
13	SUBCW A	3	1	(A) ← (T)-(A)–C	–	–	dH	+ + + +	33
14	SUBC A	2	1	(AL)← (TL)-(AL)–C	–	–	–	+ + + +	32
15	INC Ri	4	1	(Ri)← (Ri)+1	–	–	–	+ + + –	C8 to CF
16	INCW EP	3	1	(EP)← (EP)+1	–	–	–	– – – –	C3
17	INCW IX	3	1	(IX)← (IX)+1	–	–	–	– – – –	C2
18	INCW A	3	1	(A) ← (A)+1	–	–	dH	+ + – –	C0
19	DEC Ri	4	1	(Ri)← (Ri)–1	–	–	–	+ + + –	D8 to DF
20	DECW EP	3	1	(EP)← (EP)–1	–	–	–	– – – –	D3
21	DECW IX	3	1	(IX)← (IX)–1	–	–	–	– – – –	D2
22	DECW A	3	1	(A) ← (A)–1	–	–	dH	+ + – –	D0
23	MULU A	19	1	(A) ← (AL)*(TL)	–	–	dH	– – – –	01
24	DIVU A	21	1	(A) ← (T)/(AL), MOD→(T)	dL	00	00	– – – –	11
25	ANDW A	3	1	(A) ← (A) ∩(T)	–	–	dH	+ + R –	63
26	ORW A	3	1	(A) ← (A) ∪(T)	–	–	dH	+ + R –	73
27	XORW A	3	1	(A) ← (A) ⊕(T)	–	–	dH	+ + R –	53
28	CMP A	2	1	(TL)–(AL)	–	–	–	+ + + +	12
29	CMPW A	3	1	(T)–(A)	–	–	–	+ + + +	13
30	RORC A	2	1		–	–	–	+ + – +	03
31	ROLC A	2	1		–	–	–	+ + – +	02
32	CMP A,#d8	2	2	(A)–d8	–	–	–	+ + + +	14
33	CMP A,dir	3	2	(A)– dir)	–	–	–	+ + + +	15
34	CMP A,@EP	3	1	(A)–((EP))	–	–	–	+ + + +	17
35	CMP A,@IX+off	4	2	(A)–((IX)+off)	–	–	–	+ + + +	16
36	CMP A,Ri	3	1	(A)–(Ri)	–	–	–	+ + + +	18 to 1F
37	DAA	2	1	decimal adjust for addition	–	–	–	+ + + +	84
38	DAS	2	1	decimal adjust for subtraction	–	–	–	+ + + +	94
39	XOR A	2	1	(A) ← (AL) ⊕(TL)	–	–	–	+ + R –	52
40	XOR A,#d8	2	2	(A) ← (AL) ⊕d8	–	–	–	+ + R –	54
41	XOR A,dir	3	2	(A) ← (AL) ⊕ (dir)	–	–	–	+ + R –	55
42	XOR A,@EP	3	1	(A) ← (AL) ⊕ ((EP))	–	–	–	+ + R –	57
43	XOR A,@IX+off	4	2	(A) ← (AL) ⊕ ((IX)+off)	–	–	–	+ + R –	56
44	XOR A,Ri	3	1	(A) ← (AL) ⊕ (Ri)	–	–	–	+ + R –	58 to 5F
45	AND A	2	1	(A) ← (AL) ∩ (TL)	–	–	–	+ + R –	62
46	AND A,#d8	2	2	(A) ← (AL) ∩ d8	–	–	–	+ + R –	64
47	AND A,dir	3	2	(A) ← (AL) ∩(dir)	–	–	–	+ + R –	65
48	AND A,@EP	3	1	(A) ← (AL) ∩((EP))	–	–	–	+ + R –	67
49	AND A,@IX+off	4	2	(A) ← (AL) ∩ ((IX)+off)	–	–	–	+ + R –	66
50	AND A,Ri	3	1	(A) ← (AL) ∩ (Ri)	–	–	–	+ + R –	68 to 6F
51	OR A	2	1	(A) ← (AL) ∪ (TL)	–	–	–	+ + R –	72
52	OR A,#d8	2	2	(A) ← (AL) ∪ d8	–	–	–	+ + R –	74
53	OR A,dir	3	2	(A) ← (AL) ∪ (dir)	–	–	–	+ + R –	75
54	OR A,@EP	3	1	(A) ← (AL) ∪ ((EP))	–	–	–	+ + R –	77
55	OR A,@IX+off	4	2	(A) ← (AL) ∪ ((IX)+off)	–	–	–	+ + R –	76
56	OR A,Ri	3	1	(A) ← (AL) ∪ (Ri)	–	–	–	+ + R –	78 to 7F
57	CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
58	CMP @EP,#d8	4	2	((EP))– d8	–	–	–	+ + + +	97
59	CMP @IX+off,#d8	5	3	((IX)+off) – d8	–	–	–	+ + + +	96
60	CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
61	INCW SP	3	1	(SP)← (SP) + 1	–	–	–	– – – –	C1
62	DECW SP	3	1	(SP)← (SP) – 1	–	–	–	– – – –	D1

4.3 BRANCH INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	BZ/BEQ rel	3	2	if Z=1 then PC ←PC+rel	–	–	–	– – – –	FD
2	BNZ/BNE rel	3	2	if Z=0 then PC ←PC+rel	–	–	–	– – – –	FC
3	BC/BLO rel	3	2	if C=1 then PC ←PC+rel	–	–	–	– – – –	F9
4	BNC/BHS rel	3	2	if C=0 then PC ←PC+rel	–	–	–	– – – –	F8
5	BN rel	3	2	if N=1 then PC ←PC+rel	–	–	–	– – – –	FB
6	BP rel	3	2	if N=0 then PC ←PC+rel	–	–	–	– – – –	FA
7	BLT rel	3	2	if V⊕N=1 then PC←PC+rel	–	–	–	– – – –	FF
8	BGE rel	3	2	if V⊕N=0 then PC←PC+rel	–	–	–	– – – –	FE
9	BBC dir:b,rel	5	3	if (dir:b)=0 then PC←PC+rel	–	–	–	– + – –	B0 to B7
10	BBS dir:b,rel	5	3	if (dir:b)=1 then PC←PC+rel	–	–	–	– + – –	B8 to BF
11	JMP @A	2	1	(PC)←(A)	–	–	–	– – – –	E0
12	JMP ext	3	3	(PC)←ext	–	–	–	– – – –	21
13	CALLV #vct	6	1	vector call	–	–	–	– – – –	E8 to EF
14	CALL ext	6	3	subroutine call	–	–	–	– – – –	31
15	XCHW A,PC	3	1	(PC)←(A), (A)←(PC)+1	–	–	dH	– – – –	F4
16	RET	4	1	return from subroutine	–	–	–	– – – –	20
17	RETI	6	1	return from interrupt	–	–	–	restore	30

4.4 OTHER INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	PUSHW A	4	1	SP ← SP–2 (SP) ← A	–	–	–	– – – –	40
2	POPW A	4	1	A ← (SP) SP ← SP+2	–	–	dH	– – – –	50
3	PUSHW IX	4	1	SP ← SP–2 (SP) ← IX	–	–	–	– – – –	41
4	POPW IX	4	1	IX ← (SP) SP ← SP+2	–	–	–	– – – –	51
5	NOP	1	1	No operation	–	–	–	– – – –	00
6	CLRC	1	1	C ← 0	–	–	–	– – – R	81
7	SETC	1	1	C ← 1	–	–	–	– – – S	91
8	CLRI	1	1	C ← 0	–	–	–	– – – –	80
9	SETI	1	1	C ← 1	–	–	–	– – – –	90

4.5 F²MC-8L FAMILY INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir:0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir:1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir:2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir:3	BBC dir:3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#dB		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir:4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir:5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	MOV @IX+d,A	XOR A,@IX+d	AND A,@IX+d	OR A,@IX+d	MOV @IX+d,#d8	CMP @IX+d,#d8	CLRB dir:6	BBC dir:6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:7	BBC dir:7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir:0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir:1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir:2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir:3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir:4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir:5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir:6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir:7,rel	INC R7	DEC R7	CALLV #7	BLT rel

5. MASK OPTIONS

Table 5-1 Mask Options

No	Item \ Model	MB89PV140 –101	MB89PV140 –102	MB89144V1 MB89145V1 MB89146V1 MB89147V1	MB89144V2 MB89145V2 MB89146V2 MB89147V2	MB89P147V1 MB89W147V1	MB89P147V2 MB89W147V2
1	Power-on reset Available Unavailable	Available		Select when ordering mask		Select by EPROM writer	
2	Reset pin output Available Unavailable	Available		Select when ordering mask		Select by EPROM writer	
3	Clock mode selection Single-circuit clock mode Dual-circuit clock mode	Single	Dual	Select when ordering mask		Select by EPROM writer	
4	Pull-up resistor P14 to P17 P32 to P37	Unavailable		Select when ordering mask (Can be selected for each pin)		Select by EPROM writer (Can be selected for each pin)	
5	Pull-down resistor P47 to P40 P57 to P50 P67 to P60	Unavailable		Unavailable	Available for all pins	Unavailable	Available for all pins

Table 5-2 Model Specifications

Model	SH-DIP64	QFP64
MB89PV140-101	MB89PV140C-101-ES-SH	MB89PV140CF-101-ES
MB89PV140-102	MB89PV140C-102-ES-SH	MB89PV140CF-102-ES
MB89144V1	MB89144P-SH-V1	MB89144PF-BND-V1
MB89144V2	MB89144P-SH-V2	MB89144PF-BND-V2
MB89145V1	MB89145P-SH-V1	MB89145PF-BND-V1
MB89145V2	MB89145P-SH-V2	MB89145PF-BND-V2
MB89146V1	MB89146P-SH-V1	MB89146PF-BND-V1
MB89146V2	MB89146P-SH-V2	MB89146PF-BND-V2
MB89P147V1	MB89P147P-SH-V1	MB89P147PF-BND-V1
MB89P147V2	MB89P147P-SH-V2	MB89P147PF-BND-V2
MB89W147V1	MB89W147C-ES-V1	MB89W147CF-ES-V1
MB89W147V2	MB89W147C-ES-V2	MB89W147CF-ES-V2

APPENDIX

APPENDIX A I/O MAP

Addresses 00_H to 17_H

Address	Read/Write	Register	Initial value MSB ⇐ ⇒ LSB	Description of register
00_H	(R/W)	PDR0	XXXX XXXX	Port 0 data register
01_H	(W)	DDR0	0000 0000	Port 0 data direction register
02_H	(R/W)	PDR1	XXXX XXXX	Port 1 data register
03_H	(W)	DDR1	0000 0000	Port 1 data direction register
04_H	(R/W)	PDR2	- - - - 0000	Port 2 data register
05_H	Reserved	—	—	Access disable
06_H	Reserved	—	—	Access disable
07_H	(R/W)	SYCC	X - - 1 1111	System clock control register
08_H	(R/W)	STBC	00001 0 - - -	Standby control register
09_H	(R/W)	WDTC	000 - XXXX	Watchdog timer control register
$0A_H$	(R/W)	TBCR	00 - - - 000	Time-base timer control register
$0B_H$	(R/W)	WPCR	00 - - - 000	Watch prescaler control register
$0C_H$	(R/W)	PDR3	XXXX XXXX	Port 3 data register
$0D_H$	(W)	DDR3	0000 0000	Port 3 data direction register
$0E_H$	(R/W)	BUZR	- - - - - - 00	Buzzer register
$0F_H$	(R/W)	EIC	0000 0000	External interrupt control register
10_H	(R/W)	PDR4	0000 0000	Port 4 data register
11_H	(R/W)	PDR5	0000 0000	Port 5 data register
12_H	(R/W)	PDR6	0000 0000	Port 6 data register
13_H	(W)	PDR7	- - - - - - 00	Port 7 data register
14_H				
15_H				
16_H	(W)	COMR	XXXX XXXX	8-bit PWM timer compare register
17_H	(R/W)	CNTR	0 - 00 0000	8-bit PWM timer control register

See each section describing the block of the registers for each register function.

Address 18_H to $7F_H$

Address	Read/Write	Register	Initial value MSB ⇐ ⇒ LSB	Description of register
18_H	(R/W)	T3CR	X000 XXX0	Timer 3 control register
19_H	(R/W)	T2CR	X000 XXX0	Timer 2 control register
$1A_H$	(R/W)	T3DR	XXXX XXXX	Timer 3 data register
$1B_H$	(R/W)	T2DR	XXXX XXXX	Timer 2 data register
$1C_H$	(R/W)	SMR	0000 0000	Serial mode register
$1D_H$	(R/W)	SDR	XXXX XXXX	Serial data register
$1E_H$	(R/W)	ADC1	0000 0000	A/D control register 1
$1F_H$	(R/W)	ADC2	-000 0001	A/D control register 2
20_H	(R/W)	ADDH	0000 00XX	A/D data register (H)
21_H	(R/W)	ADDL	XXXX XXXX	A/D data register (L)
22_H	(W)	PCR0	0000 0000	Port input control register 0
23_H	(W)	PCR1	- - - - 0000	Port input control register 1
24_H	(R/W)	MCNT	0000 0000	MPG control register
25_H	(R/W)	INTSTR	0000 0000	MPG interrupt status register
26_H	(W)	CMCLBR(H)	- - - - 0000	MPG compare clear buffer register (H)
27_H	(W)	CMCLBR(L)	0000 0000	MPG compare clear buffer register (L)
28_H	(W)	OUTCBR(H)	- - - - 0000	MPG output buffer register (H)
29_H	(W)	OUTCBR(L)	0000 0000	MPG output buffer register (L)
$2A_H$				
$2B_H$				
$2C_H$	Reserved	—		(Access disable)
$2D_H$				
$2E_H$				
$2F_H$				
30_H to 77_H				
78_H				
79_H				
$7A_H$				
$7B_H$				
$7C_H$	(W)	ILR1	1111 1111	Interrupt level setting register 1
$7D_H$	(W)	ILR2	1111 1111	Interrupt level setting register 2
$7E_H$	(W)	ILR3	1111 1111	Interrupt level setting register 3
$7F_H$	Reserved	—		(Access disable)

Note: The value is undefined when the bit indicated by — in the register column.

See each section describing the block of the registers for each register function.

APPENDIX B EPROM SETTING FOR MB89P147

MB89P147 is provided with the function corresponding to MBM27C256A by EPROM setting. The setting can be performed by writing program data with general-purpose EPROM writer through adaptor for exclusive use .

• Setting

(1) Set the EPROM writer to MBM27C256A.

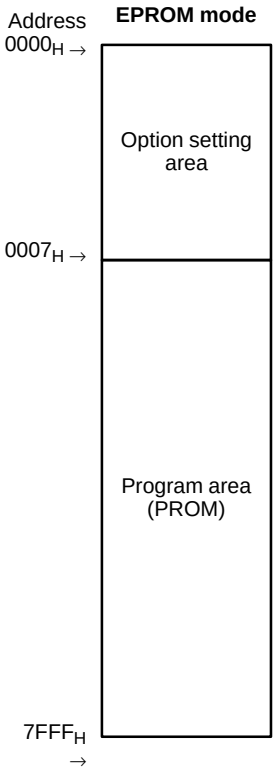
(2) Load the program data from address $\mathbf{0007_H}$ to address $\mathbf{7FFF_H}$ of EPROM writer.

(The data is loaded from address $\mathbf{8000_H}$ to address $\mathbf{0FFFF_H}$ in the operation mode, and from address $\mathbf{0000_H}$ to address $\mathbf{7FFF_H}$ in the EPROM mode.)

Load the option data at addresses $\mathbf{0000_H}$ to $\mathbf{0006_H}$ in the EPROM writer. (See the next Bit Map for the correspondence of each option.)

(3) Write the data with the EPROM writer.

The memory space in the EPROM mode is as follows:



Bit Map for PROM Option

	7	6	5	4	3	2	1	0
0000_H (8000_H)	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	<OP 4> Clock specification 1: Double 0: Single	<OP 3> Reset pin output 1:Available 0:Unavailable	<OP 2> Power-on reset 1:Available 0:Unavailable	Reserved (Write 1.)	Reserved (Write 1.)
0001_H (8001_H)	P17 Pull-up register 1:Available 0:Unavailable	P16 Pull-up register 1:Available 0:Unavailable	P15 Pull-up register 1:Available 0:Unavailable	P14 Pull-up register 1:Available 0:Unavailable	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible
0002_H (8002_H)	P37 Pull-up register 1:Available 0:Unavailable	P36 Pull-up register 1:Available 0:Unavailable	P35 Pull-up register 1:Available 0:Unavailable	P34 Pull-up register 1:Available 0:Unavailable	P33 Pull-up register 1:Available 0:Unavailable	P32 Pull-up register 1:Available 0:Unavailable	Empty Read/write possible	Empty Read/write possible
0003_H (8003_H)	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible
0004_H (8004_H)	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible
0005_H (8005_H)	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible
0006_H (8006_H)	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible	Empty Read/write possible

Note: The default of each bit is 1.

APPENDIX C LIST OF SYSTEM CLOCK CYCLE TIMES WHEN GEAR CHANGED (Source clock: 8 MHz, 4 MHz)

Number of system clocks	Setting of CS1 and CSO bits (system clock select bit) of SYCC register							
	CS1 = 1, CSO = 1		CS1 = 1, CSO = 0		CS1 = 0, CSO = 1		CS1 = 0, CSO = 0	
	8 MHz (µs)	4 MHz (µs)	8 MHz (µs)	4 MHz (µs)	8 MHz (µs)	4 MHz (µs)	8 MHz (µs)	4 MHz (µs)
1	0.5	1.0	1.0	2.0	2.0	4.0	8.0	16.0
2	1.0	2.0	2.0	4.0	4.0	8.0	16.0	32.0
4	2.0	4.0	4.0	8.0	8.0	16.0	32.0	64.0
8	4.0	8.0	8.0	16.0	16.0	32.0	64.0	128.0
16	8.0	16.0	16.0	32.0	32.0	64.0	128.0	256.0
32	16.0	32.0	32.0	64.0	64.0	128.0	256.0	512.0
64	32.0	64.0	64.0	128.0	128.0	256.0	512.0	1024.0

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