FUJITSU SEMICONDUCTOR
MICROCONTROLLER MANUAL

CM25-10128-2E

F²MC-8L FAMILY
8-BIT MICROCONTROLLER
MB89143A/4A SERIES
HARDWARE MANUAL

FUJITSU

Introduction

This specification uses the following terminology:

1. A "clock cycle" is one cycle of the source oscillator clock.
2. An "instruction cycle" is the minimum instruction execution time. The minimum instruction execution time is the resulting clock cycle after division by the gear function (see "2.1.5 Clock Controller"). (See "Instruction Cycle" in "6.4 AC Characteristics" and "Appendix 2 Quick Reference Table for the Instruction Cycle at Gear Change".)

CONTENTS

Chapter 1: Overview

The MB89143A/4A has been developed as a general-purpose version of the F^{2}MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers with ASIC (Application Specific IC) compatibility.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as two clock control systems, five operating speed control stages, timers, a serial interface, an A/D converter, a buzzer output, high-voltage drivers, a watch prescaler, and external interrupts. The device is suitable for a wide range of applications from consumer to industrial equipment.

*: F^{2}MC stands for FUJITSU Flexible Microcontroller.

1.1 Features

- Minimum execution time: 0.5 µs (at an 8.0-MHz source oscillator frequency)
- Interrupt processing time: 4.50 µs (at an 8.0-MHz source oscillator frequency)
- F^{2}MC-8L CPU core

  Instruction set optimized for controller applications
  - Multiplication and division instructions
  - 16-bit operations
  - Instruction test and branch instructions
  - Bit manipulation instruction, etc.

- Dual clock control
- High-voltage ports: 24 channels
- Dual timers
  - 8/16-bit timer/counter (can also be used as 2 × 8-bit timers)
  - 21-bit time-base counter
- 8-bit serial interface: 1 channel
  - Selectable transfer direction supports communications with a wide range of devices.
- A/D converter: 8 channels
  - Successive approximation A/D converter with 8-bit resolution
- External interrupts: 2 channels
  - Two channels are independent and capable of wake-up from low-power consumption mode. (can be selected to trigger on rising edges, falling edges, or both edges)
  - –0.3 V to 7.0 V can be applied to INT1 (N-ch open-drain).
- Low-power consumption modes
  - Sub mode (Halts the high speed clock and operates on the low speed clock.)
  - Watch mode (Halts all functions except the Watch prescaler.)
  - Stop mode (Halts the oscillation so that the device consumes almost no current.)
  - Sleep mode (Halts the CPU so that the device consumes approximately one third of the usual operating current.)
- Watch prescaler
- Buzzer output
- Watchdog reset, reset output, and power-on reset
- Mask option
  - Allows selection of single/dual clock system, presence/absence of pull-up resistor and reset output.
- Packages:
  - SDIP64 (Package code: DIP-64P-M01)
  - QFP64 (Package code: FPT-64P-M06) (Under development review)

1.2 Series Product Lineup

Table 1.2.1 lists the product lineup for the MB89143A/4A and MB89140 series.

Table 1.2.1 MB89143A/4A and MB89140 Series Product Lineup

Parameter \ Part number	MB89143A	MB89144A	MB89144, 5, 6	MB89P147	MB89PV140
Classification	Mass production products (mask ROM products)			OTPROM/EPROM products	Piggyback/evaluation product (for evaluation and development)
ROM size	8K × 8 bits	12K	12K, 16K, 24K × 8 bits	32K × 8-bit internal	32K × 8-bit external (piggy-back)
RAM size	256 × 8 bits		256, 512, 768 × 8 bits	1K × 8-bit internal	1K × 8-bit internal
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.5 µs/8 MHz to 8.0 µs/8 MHz, 61.0 µs/32 kHz Interrupt processing time: 4.5 µs/8 MHz to 72.0 µs/8 MHz, 562.5 µs/32 kHz Note: The above times change according to the gear function.				
Ports	High-voltage ports (P-ch open-drain): 24 (P40 to P47, P50 to P57, P60 to P67) Buzzer output (P-ch open-drain, high-voltage port): 1 Output ports (CMOS): 4 (P20 to P23) Input ports (CMOS): 2 (P70 and P71 are used as X0A and X1A pins when a dual clock is used.) I/O ports (CMOS): 23 (P00 to P07, P10 to P17, P30, P32 to P37) I/O ports (N-ch open-drain): 1 (P31) Total: 55				
Time-base timer	Support four interval times: 0.26 ms, 0.51 ms, 1.02 ms, and 0.524 s (for an 8.0-MHz source oscillation)				
8/16-bit timer/counter	8/16-bit timer operation (operating clock: internal clock, external trigger) 8/16-bit event counter operation (rising, falling, or both edges selectable)				
Serial I/O	8 bits, LSB-first or MSB-first selectability Transfer clock (external, 4, 8, or 16 system clock cycles)				
A/D converter	8-bit resolution × 8 channels A/D conversion mode (conversion time: 22 µs at 8 MHz with the gear function set at maximum speed) Supports repeated activation by an external trigger.		10-bit resolution × 12 channels A/D conversion mode (conversion time: 16.5 µs at 8 MHz with the gear function set at maximum speed) Sense mode (conversion time: 9.0 µs at 8 MHz with the gear function set at maximum speed) Supports repeated activation by an external trigger.		
External interrupts	Two independent channels (edge selection, interrupt vector, source flag) Rising, falling, or both edges can be selected. Internal analog noise filter Used for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)				
Buzzer output	Selectable output frequency (1.95 kHz or 3.91 kHz for an 8-MHz source oscillation). Output from a high-voltage pin.				
Watchdog reset	Generates an internal reset after 524 to 1049 ms (at an 8-MHz source oscillation) if program runaway occurs.				
8-bit PWM	No		Can operate as an 8-bit timer or as an 8-bit resolution PWM.		
12-bit MPG	No		Can operate as a 12-bit resolution PWM, reload timer, or PPG.		
Standby mode	Sleep mode, stop mode, and watch mode				
Process	CMOS				
Package	DIP-64P-M01		DIP-64P-M01/FPT-64P-M06		MDP-64C-P02/ MQP-64C-P01
Supported EPROM					MBM27C256A-20
Operating voltage	4.0 to 6.0 V		2.7 to 6.0 V		

*: See the MB89140 series specifications for further details of products other than the MB89143.

1.3 Block Diagram

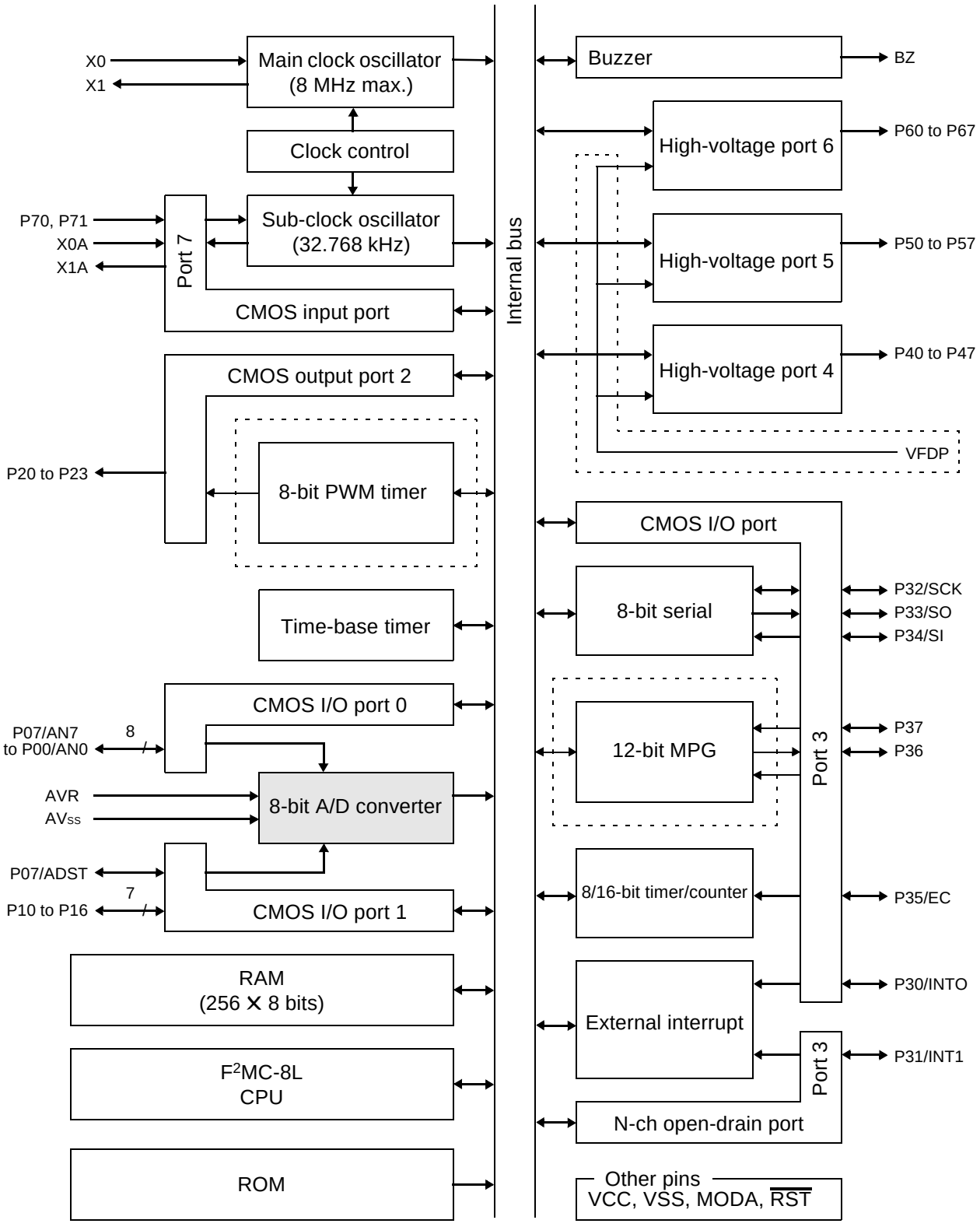
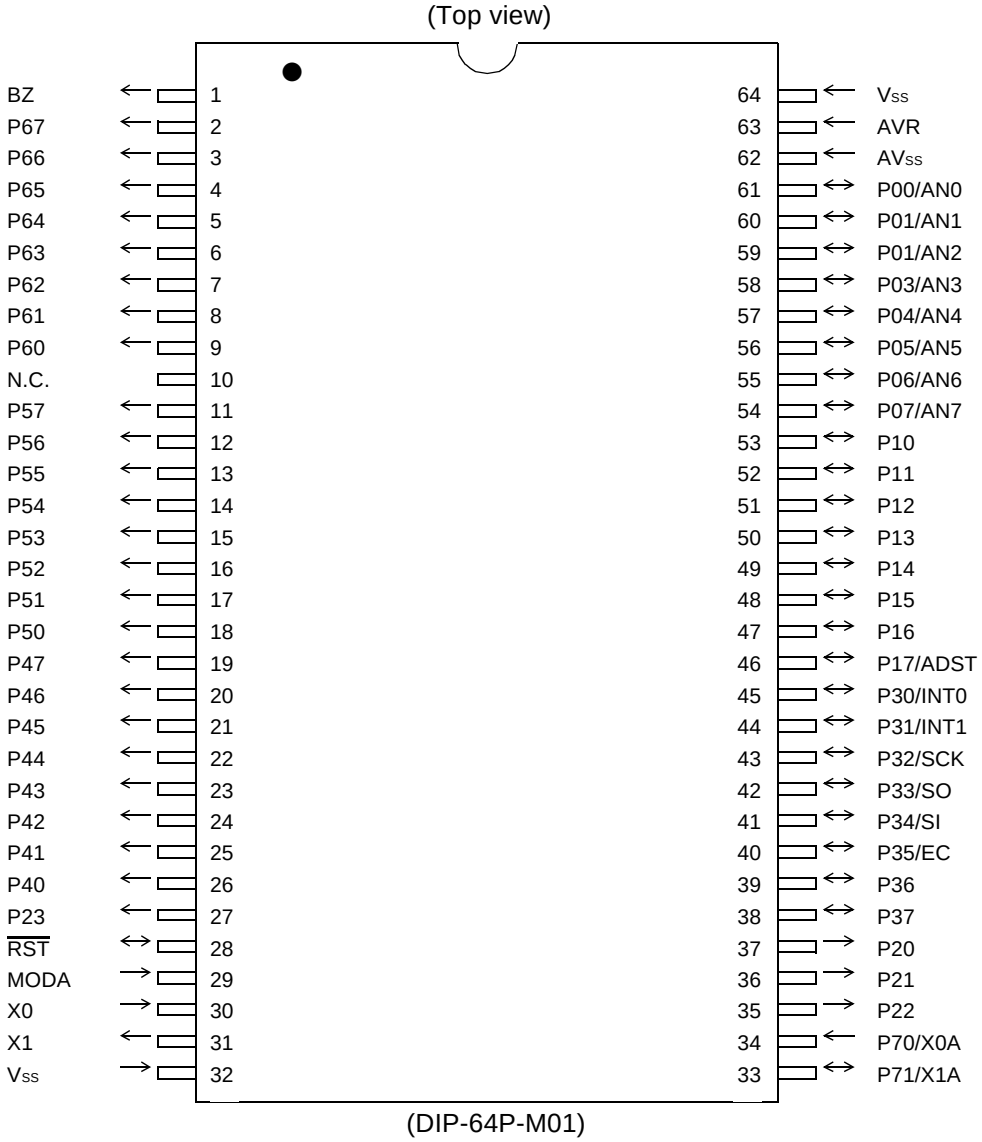


Figure 1.3.1 Overall Block Diagram (MB89143A/4A)

Note: The units enclosed in dotted lines are not provided on the MB89143A/4A. The A/D converter has 8-bit resolution × 8-bit channels.

1.4 Pin Assignment



(DIP-64P-M01)

- When used as general-purpose ports, P70/X0A and P71/X1A are input-only ports.
- P07 to P00 are initialized as analog inputs ports after a reset. P13 to P10 are initialized with a fixed "L" level input after a reset. To use as ports, always set "1" in the PCR1 and PCR0 registers.

Figure 1.4.1 Pin Assignment

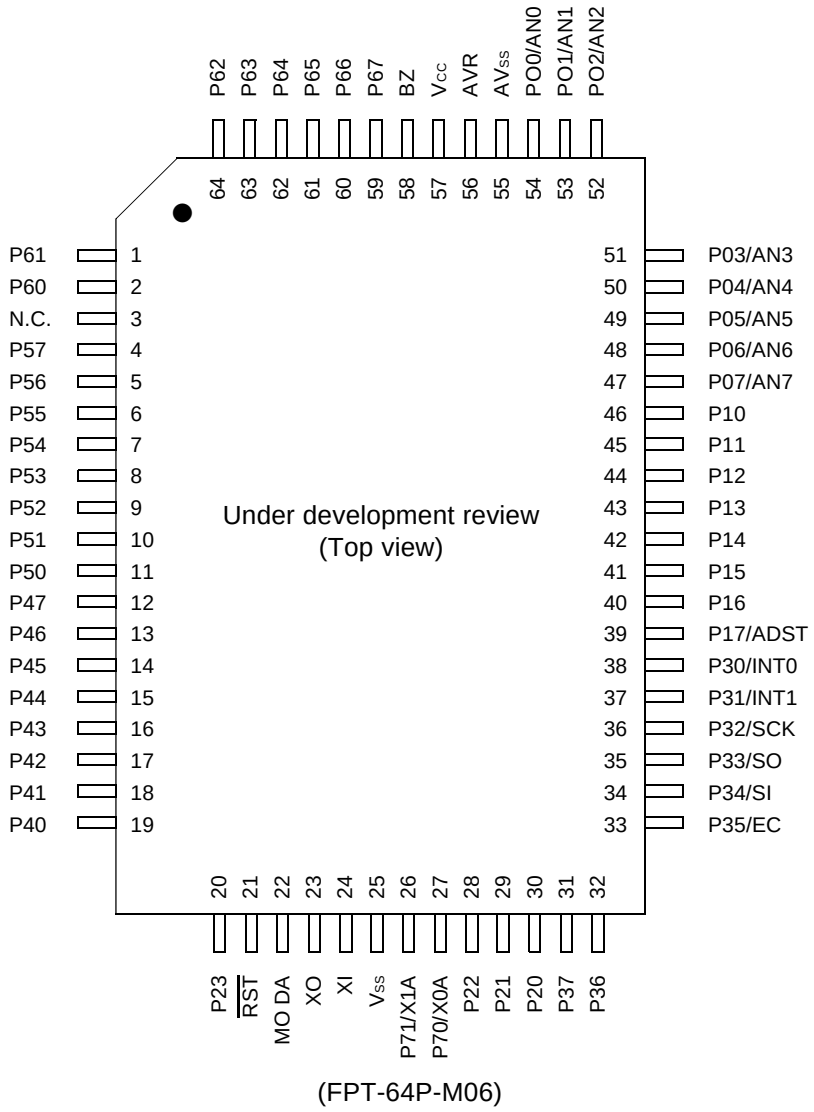
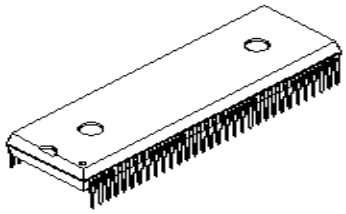


Figure 1.4.2 Pin Assignment

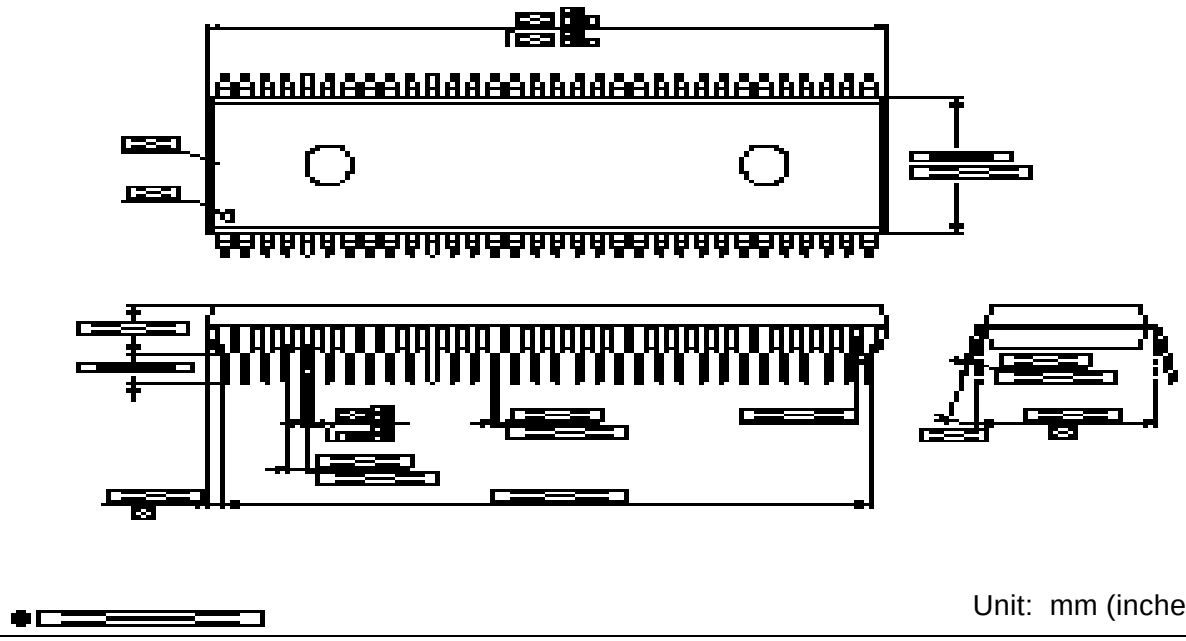
1.5 Package Dimensions

DIP-64P-M01

EIAJ code: SDIP064-P-0750-1

64-pin Plastic SH-DIP  (DIP-64P-M01)	Lead pitch	70 mil
	Row spacing	750 mil
	Sealing method	Plastic mold

64-pin Plastic SH-DIP
(DIP-64P-M01)



Unit: mm (inches)

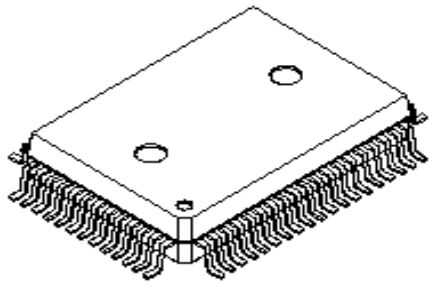
The package dimensions given in this document are for reference only. Obtain the dimensions of the regular version separately.

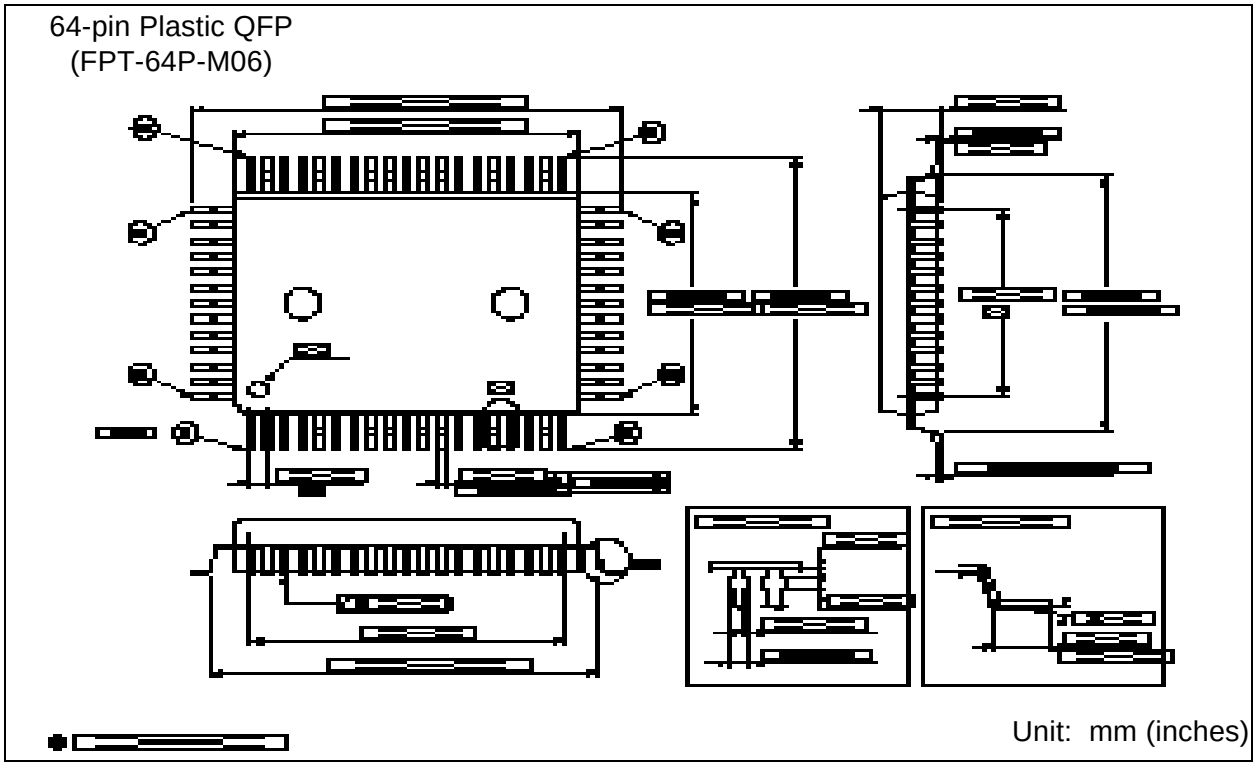
Figure 1.5.1 Package Dimensions

Under development review

FPT-64P-M06

EIAJ code: *QFP064-P-1420-3

64-pin Plastic QFP  FPT-64P-M06	Lead pitch	1.00 mm
	Package width × length	14 × 20 mm
	Lead shape	Gull-wing
	Sealing method	Plastic mold
	Length of flat section of pin	1.20 mm



The package dimensions given in this document are for reference only. Obtain the dimensions of the regular version separately.

Figure 1.5.2 Package Dimensions

1.6 Pin Description

Table 1.6.1 lists the pin functions and Figure 1.6.1 shows the I/O circuit types.

Table 1.6.1 Pin Description

Pin no.		Pin name	Circuit type	Function
SDIP*1	QFP*2			
30	23	X0	A	Main clock oscillator pins Use a crystal oscillator.
31	24	X1		
29	22	MODA	B	Input pin for setting the operating mode. Normally connect directly to Vss.
28	21	$\overline{\text{RST}}$	C	Reset I/O pin This port is a N-ch open-drain output type with pull-up resistor and a hysteresis input type. "L" is output from this pin by an internal source. The internal circuit is initialized by the input of "L". The pin has an internal noise canceller.
54 to 61	47 to 54	P07/AN7 to P00/AN0	F	General-purpose I/O ports These ports are a hysteresis input type. Also serve as analog inputs.
46	39	P17/ADST	H	General-purpose I/O port This port is a hysteresis input type. Also serve as the external activation pin for the A/D converter.
47 to 53	40 to 46	P16 to P10		General-purpose I/O ports These ports are a hysteresis input type.
34	27	P70/X0A	J	Can be selected (as a mask option) to function as either a general-purpose input port or as an oscillator sub-clock pin. When set as an input port, the pin is a hysteresis input.
33	26	P71/X1A		Can be selected (as a mask option) to function as either a general-purpose input port or as an oscillator sub-clock pin. When set as an input port, the pin is a hysteresis input.
27, 35 to 37	20, 28 to 30	P23, P22 to P20	D	General-purpose output ports
38, 39	31, 32	P37, P36	H	General-purpose I/O ports These ports are a hysteresis input type.
40	33	P35/EC		General-purpose I/O port This port is a hysteresis input type. Also serve as the external clock input for the 8/16-bit timer/counter.
41	34	P34/S1		General-purpose I/O port This port is a hysteresis input type. Also serve as the serial data input for the 8-bit serial interface.
42	35	P33/S0		General-purpose I/O port This port is a hysteresis input type. Also serve as the serial data output for the 8-bit serial interface.
43	36	P32/SCK		General-purpose I/O port This port is a hysteresis input type. Also serve as the serial transfer clock for the 8-bit serial interface.
44	37	P31/INT1	E	General-purpose I/O port This port is an N-ch open-drain output and a hysteresis input. Also serve as an external interrupt pin. When used as an interrupt, the pin is a hysteresis input and has an internal noise filter.
45	38	P30/INT0	I	General-purpose I/O port This port is a hysteresis input type. Also serve as an external interrupt pin. When used as an interrupt input, the pin is a hysteresis input and has an internal noise filter.
1	58	BZ	G	P-ch high-voltage open-drain output port Used as the buzzer output only.

*1 : DIP-64P-M01
*2 : FPT-64P-M06

Table 1.6.1 Pin Description *(Continued)*

Pin no.		Pin name	Circuit type	Function
SDIP*1	QFP*2			
19 to 26	12 to 19	P47 to p40	G	P-ch high-voltage open-drain output ports
11 to 18	4 to 11	P57 to P50		
2 to 9	59 to 2	P67 to P60		
10	3	N.C.	-	N.C. pin
64	57	V_{CC}	-	Power supply pin Also serve as the A/D converter AV_{CC} power supply pin.
32	25	V_{SS}	-	Power supply pin (GND).
63	56	AVR	-	A/D converter reference power supply pin
62	55	AV_{SS}	-	A/D converter power supply pin Use at the same voltage as V_{SS}.

*1 : DIP-64P-M01
*2 : FPT-64P-M06

Figure 1.6.1 I/O Circuit Type

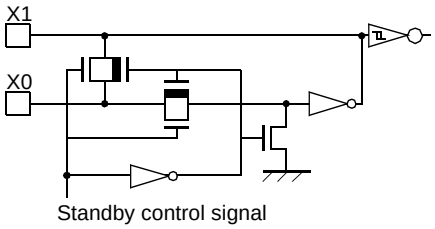
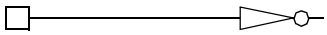
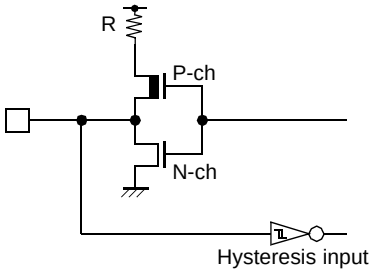
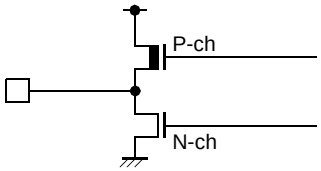
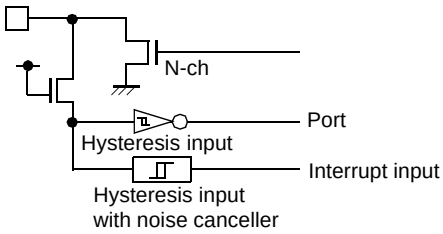
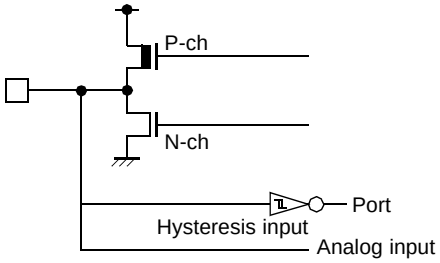
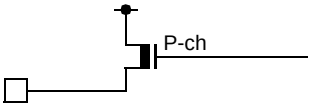
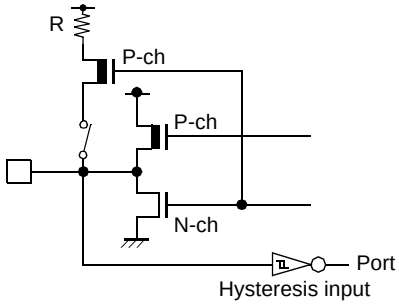
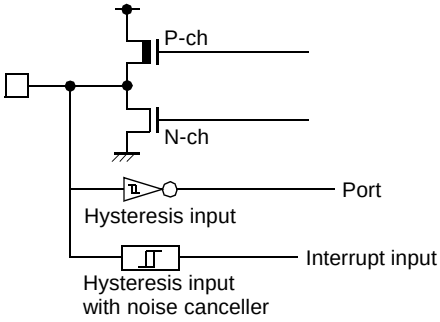
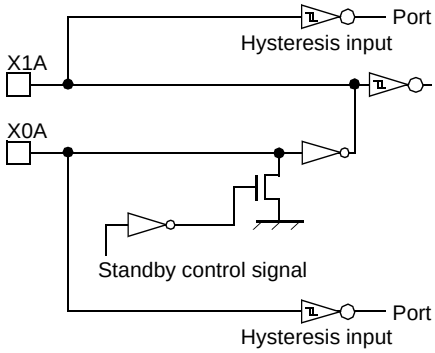
Type	Circuit	Remarks
A		• At an oscillation feedback resistor of approximately 1 MΩ/5 V
B		
C		• At a output pull-up resistor (P-ch) of approximately 50 kΩ/5 V • CMOS hysteresis input
D		• CMOS output
E		• N-ch open-drain output • CMOS hysteresis input • Hysteresis input is provided with noise canceller
F		• CMOS output • CMOS hysteresis input
G		• P-ch high-voltage open-drain output

Figure 1.6.1 I/O Circuit Type *(Continued)*

Type	Circuit	Remarks
H		• CMOS output • CMOS hysteresis input • Pull-up option (for P14 to P17 and P32 to P37 only)
I		• CMOS output • CMOS hysteresis input. • Hysteresis input is provided with noise canceller.
J		• No oscillation feedback resistor is provided internally. • Can be used as a CMOS hysteresis input when the sub-clock is not used.

1.7 Handling Devices

1. Preventing latch-up

Latchup may occur on CMOS ICs if voltage higher than Vcc or lower than Vss is applied to input and output pins other than medium- to high-voltage pins or higher than voltage which shows on "6.1 Absolute Maximum Ratings" in "Chapter 6 Electrical Characteristics" is applied between Vcc and Vss. (However, up to 7.0 V can be applied to the P31/INT pin, regardless of Vcc.)

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AVR) and analog input from exceeding the digital power supply (Vcc) when the analog system power supply is turned on and off.

2. Treatment of unused input pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down resistor.

3. Treatment of power supply pins on microcontrollers with A/D and D/A converters

Connect to be AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. pins

Be sure to leave (internally connected) N.C. pins open.

5. Power supply voltage fluctuations

Although Vcc power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that Vcc ripple fluctuations (P-P value) will be less than 10% of the standard Vcc value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions using an external clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and release from stop mode.

Chapter 2: Hardware Structure

2.1 CPU

2.1.1 Memory Space

The microcontrollers of MB89143A/4A offer a memory space of 64 Kbytes for storing I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided, into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the table of interrupt reset vectors and vector call instructions toward the highest address within the program area. Figure 2.1.1 shows the structure of the MB89143A/4A memory space.

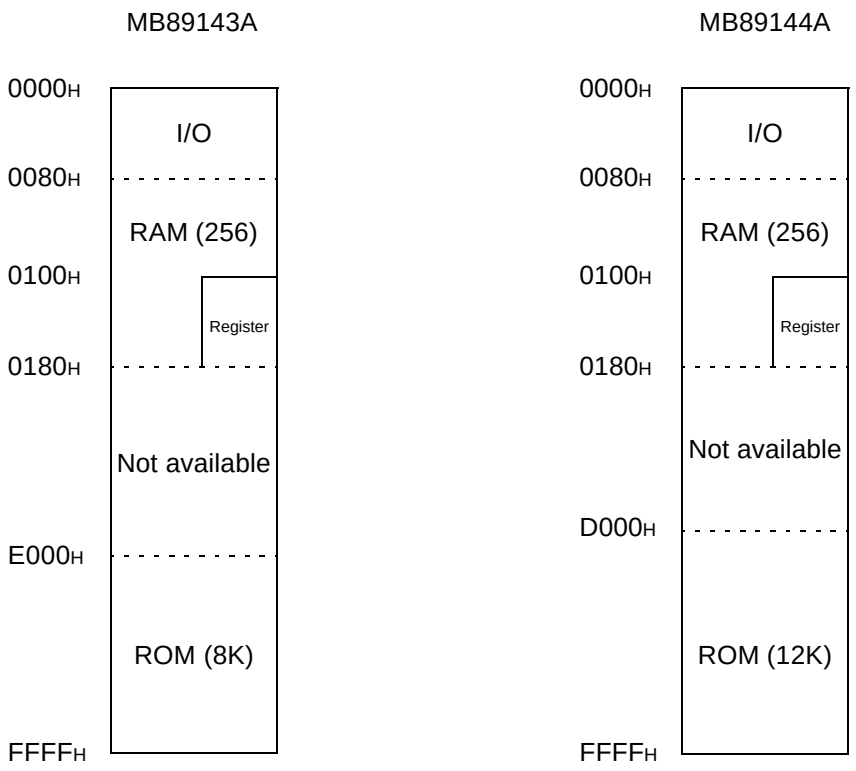


Figure 2.1.1 MB89143A/4A Memory Space

○ I/O area

Control registers and data registers for the peripheral functions are located in this area. Appendix 1 shows the memory map of the I/O area.

○ RAM area

The static RAM is located in this area. The addresses 0100H to 017FH are also used as the general-purpose register area.

○ ROM area

The internal ROM is located in this area. The addresses FFC0H to FFFFH are used for the interrupt, reset, and vector call instruction tables. Figure 2.1.2 shows the table addresses referenced by the MB89143A/4A for each interrupt number and reset.

	Table Address	
	Upper	Lower
Reset vector	FFFEH	FFFFH
Reset mode	- - - - -	FFFDH
Interrupt #0	FFFAH	FFFBH
Interrupt #1	FFF8H	FFF9H
Interrupt #2	FFF6H	FFF7H
Interrupt #3	FFF4H	FFF5H
Interrupt #4	FFF2H	FFF3H
Interrupt #5	FFF0H	FFF1H
Interrupt #6	FFEEH	FFEFH
Interrupt #7	FFECH	FFEDH
Interrupt #8	FFEAH	FFEBH
Interrupt #9	FFE8H	FFE9H
Interrupt #10	FFE6H	FFE7H
Interrupt #11	FFE4H	FFE5H

	Table Address	
	Upper	Lower
CALLV #7	FFCEH	FFCFH
CALLV #6	FFCCH	FFCDH
CALLV #5	FFCAH	FFCBH
CALLV #4	FFC8H	FFC9H
CALLV #3	FFC6H	FFC7H
CALLV #2	FFC4H	FFC5H
CALLV #1	FFC2H	FFC3H
CALLV #0	FFC0H	FFC1H

Note: FFFCH is reserved.

Figure 2.1.2 Reset and Interrupt Vector Table

2.1.2 Locating Memory Space in 16-Bit Data

Figure 2.1.3 shows how the MB89143A/4A handles 16-bit memory data. The data written to the lower address is the higher order byte and the data written to the next address is the lower order byte.

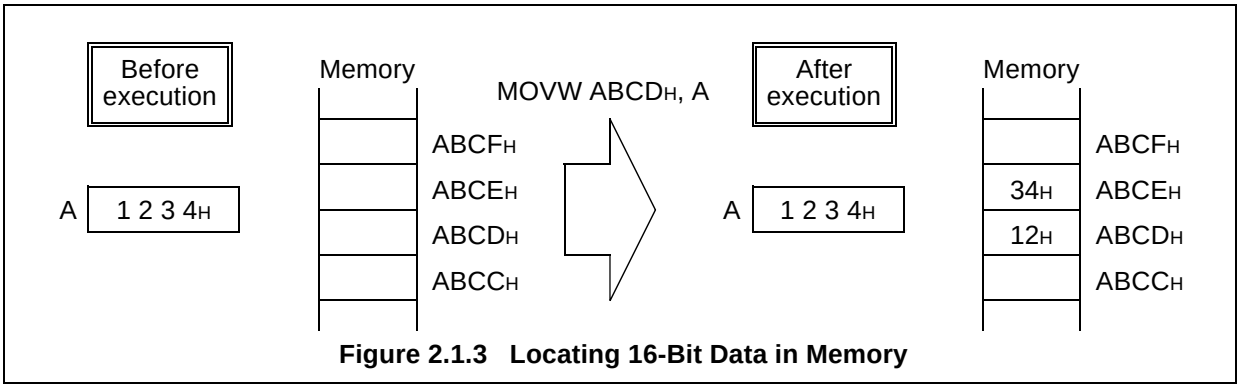


Figure 2.1.3 Locating 16-Bit Data in Memory

The same byte order applies when specifying a 16-bit operand in an instruction. The address following the OP code contains the upper byte and the next address contains the lower byte. The byte ordering applies to both 16-bit immediate data and operands that specify a memory address.

```
Example   MOV     A, 5678H      ;  Extended address
          MOVW    A, #1234H     ;  16-bit immediate data
                                   After assembly
                  ⋮
          XXXXH   XX    XX
          XXXXH   60    56    78    ;  Extended address
          XXXXH   E4    12    34    ;  16-bit immediate data
          XXXXH   XX
                  ⋮
```

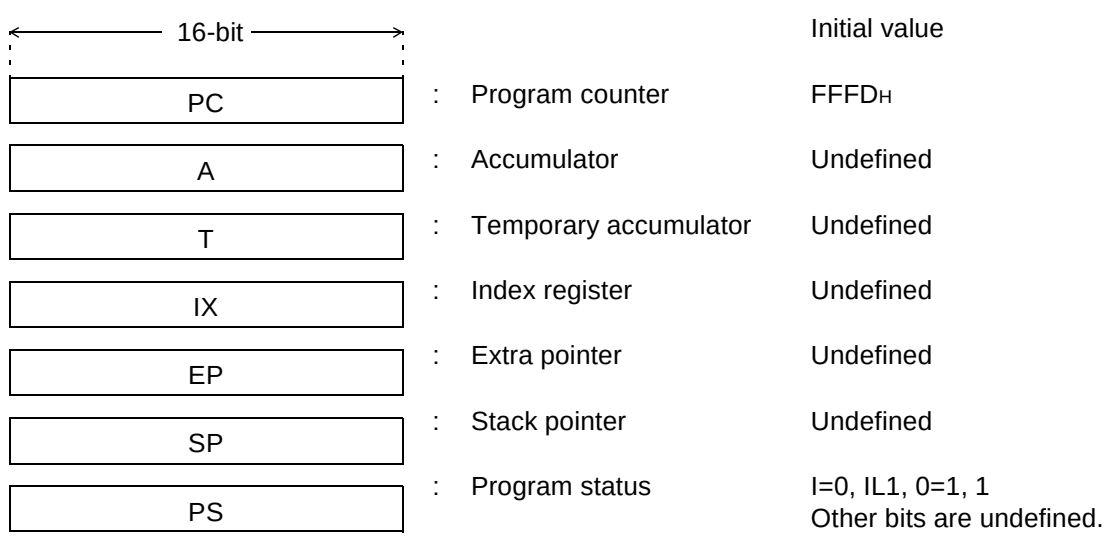
Figure 2.1.4 Byte Order of 16-Bit Data in Instructions

The same byte order applies when saving data on the stack during an interrupt or similar.

2.1.3 Registers

The MB89143A/4A has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

- Program counter (PC) : A 16-bit-long register for indicating instruction storage positions
- Accumulator (A) : A 16-bit-long temporary register for storing operation, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T) : A 16-bit-long register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Stack pointer (SP) : A 16-bit-long register for indicating a stack area
- Program status (PS) : A 16-bit-long register for storing a register pointer, a condition code
- Index register (IX) : A 16-bit-long register for index modification
- Extra pointer (EP) : A 16-bit-long pointer for indicating a memory address



The PS is divided into the upper 8 bits which hold the register bank pointer (RP) and the lower 8 bits which hold the condition code register (CCR). (Figure 2.1.5)

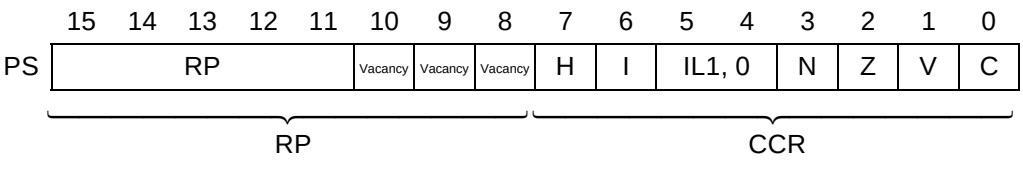


Figure 2.1.5 Structure of the Program Status Register

The RP indicates the address of the register bank currently in use. Figure 2.1.6 shows the relationship between the pointer contents and the actual address is based on the conversion rule.

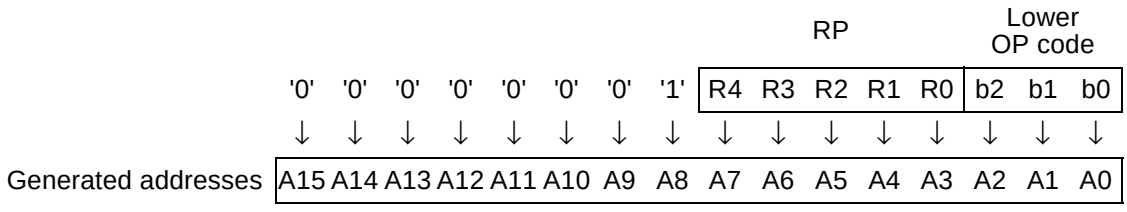


Figure 2.1.6 Rule for Conversion of Actual Addresses the General-purpose Register Area

The CCR consists of bits that indicating the results of arithmetic operations the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

○ H flag : Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared overwise. This flag is for decimal ajustment instructions.

○ I flag : Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0. Set to 0 when reset.

○ IL1, IL0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High ↕ Low = no interrupt
0	1		
1	0	2	
1	1	3	

○ N flag : Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

○ Z flag : Set when an arithmetic operation results in 0. Cleared otherwise.

○ V flag : Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

○ C flag : Set when a carry or borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided.

- General-purpose registers: An 8-bit-long register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank consists of 8 registers and up to a total of 16 banks can be used on the MB89143A/4A.

The bank currently in use is indicated by the register bank pointer (RP).

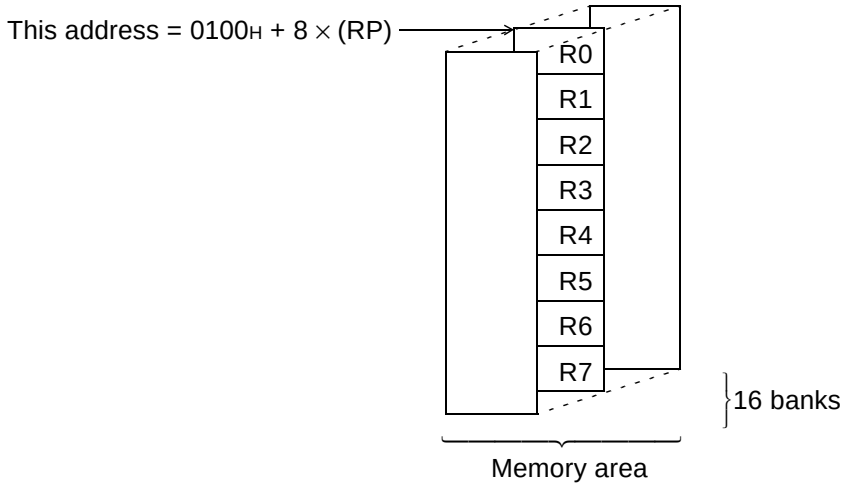


Figure 2.1.7 Register Bank Configuration

2.1.4 Operating Modes

Use the MB89143A/4A in single-chip mode.

The figure below shows the memory map.

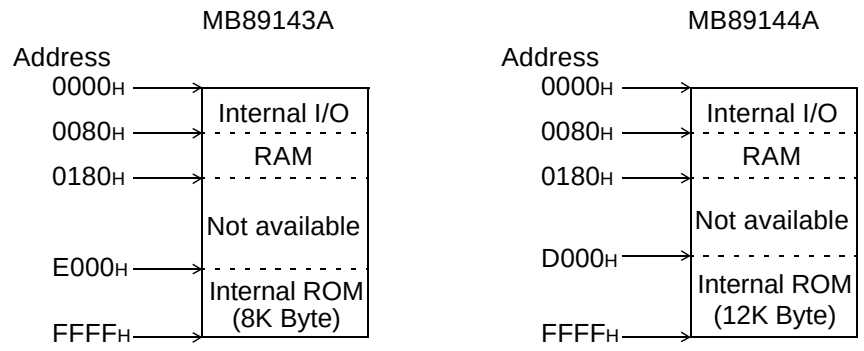
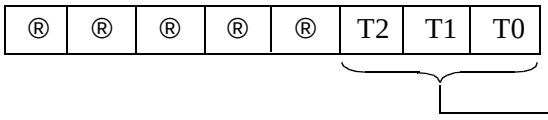


Figure 2.1.8 Memory Map

The level of the device mode pin and the mode data read during a reset determine how the device operates. The following shows the relationship between the level of the device mode pin and device operation.

MODA	Description
0	Read reset vector from internal ROM.
1	Write mode (for products with internal EPROM)

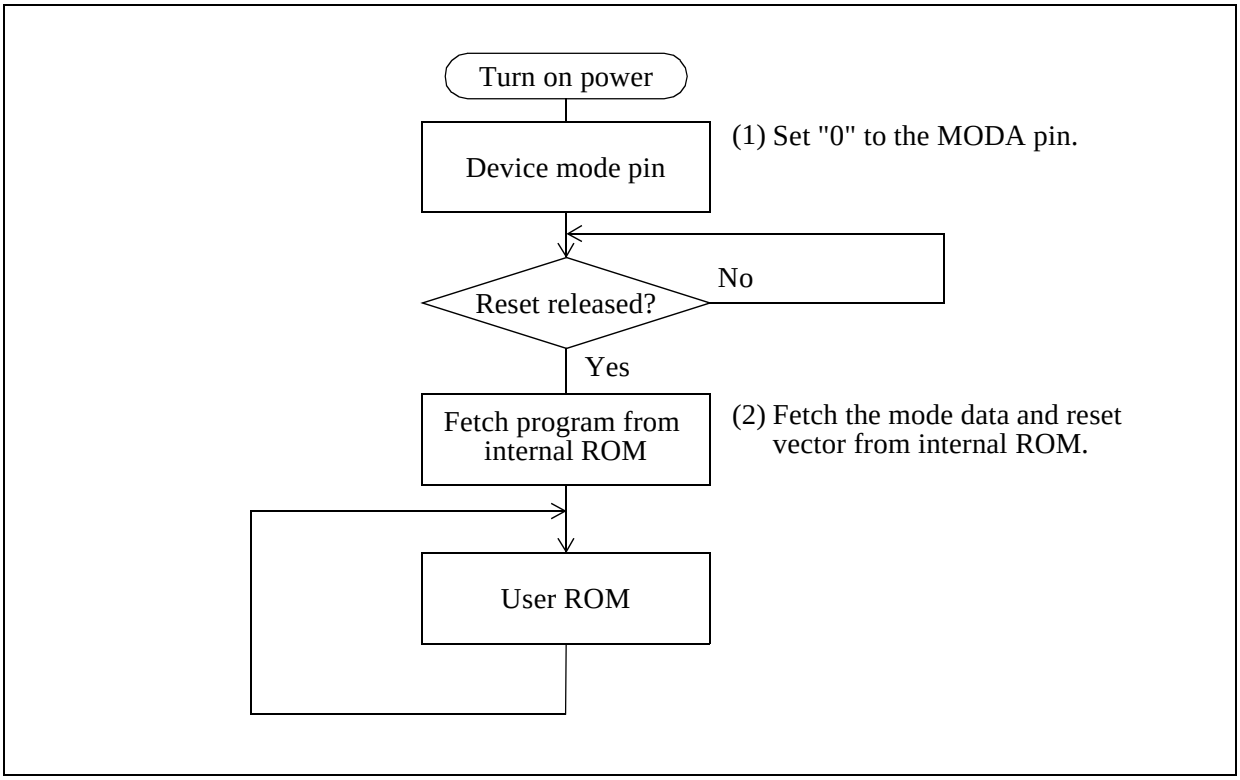
Set the mode data as follows.



T2	T1	T0	Operation
0	0	0	Single clip mode selection
Other			Reserved. Do not specify.

As shown in the flow chart below, single-chip mode is set by the level of the device mode pin and the mode data fetched during the reset sequence.

Setting procedure	Selected mode	Mode pin	Mode data
(1) → (2)	Single-chip mode	0	00000000



2.1.5 Clock Controller

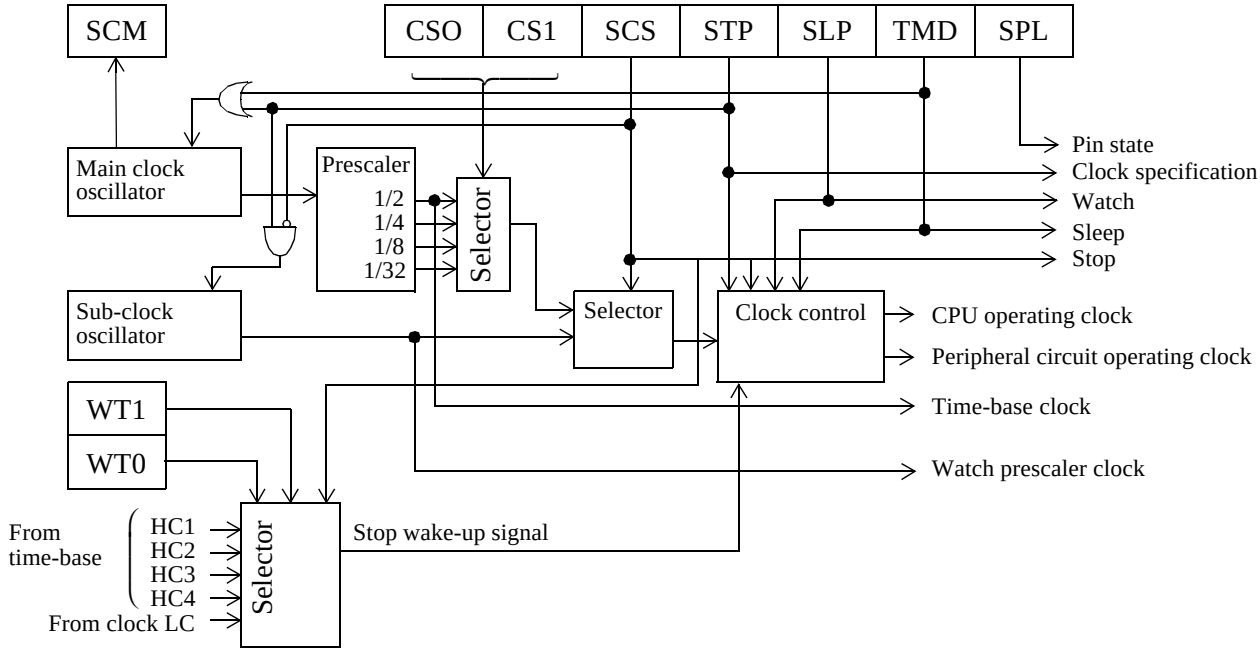
The functions of the clock controller block include standby operation, setting the oscillation stabilization delay time, generation of software resets, and clock switching.

(1) Registers

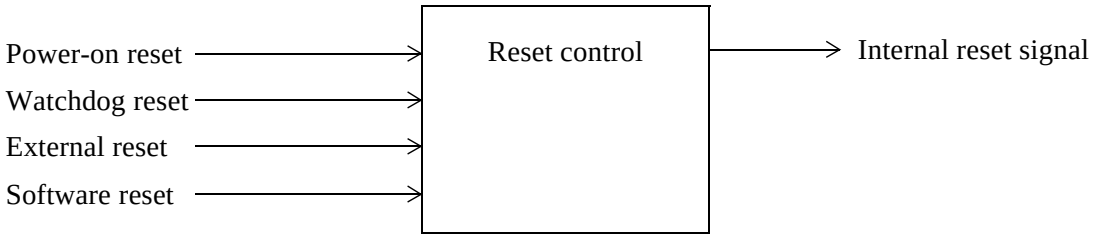
Bit	7	6	5	4	3	2	1	0	
Address: 0008H	STP	SLP	SPL	RST	TMD	—	—	—	Standby control register (STBC)
Address: 0007H	SCM	—	—	WT1	WT0	SCS	CS1	CS0	System clock control register (SYCC)

(2) Block Diagram

(a) Machine clock controller



(b) Reset controller



(3) Register Description

(3.1) STBC (Standby Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0008H	STP	SLP	SPL	RST	TMD	—	—	—	00010---B
	(W)	(W)	(R/W)	(W)	(W)				

[Bit 7] STP: Stop bit

Instructs the device to change to stop mode.

0	No operation
1	Stop mode

Cleared by a reset or by wake-up of stop mode.

Reading always returns "0".

[Bit 6] SLP: Sleep bit

Instructs the device to change to sleep mode.

0	No operation
1	Sleep mode

Cleared by a reset or by wake-up of sleep or stop mode.

Reading always returns "0".

[Bit 5] SPL: Pin state specification bit

Specifies the external pin states during stop mode.

0	Maintain states and levels immediately before entering stop mode.
1	High impedance

Cleared by a reset.

[Bit 4] RST: Software reset bit

Specifies a software reset.

0	Generate a reset signal for four instruction cycles.
1	No operation

Reading this bit returns "1".

If a software reset is triggered in sub operation mode, the device delays for the oscillation stabilization time then enters main mode. Therefore, the reset signal is output for the duration of the oscillation stabilization time.

[Bit 3] TMD: Timer bit

Instructs the device to change to watch mode.

0	Not applicable.
1	Watch mode

Writing to this bit is only allowed in sub mode (SCS = "0"). Reading always returns "0". Cleared by an interrupt request or reset.

(3.2) SYCC (System Clock Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0007H	SCM	—	—	WT1	WT0	SCS	CS1	CS0	X--11100B
	(R)			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] SCM: System clock monitor bit

This bit indicates whether the current system clock is the main clock or the sub-clock.

0	Sub clock (main clock halted or main clock oscillation stabilizing)
1	Main clock

[Bit 4, 3] WT1, WT0: Oscillation stabilization delay time selection bits

These bits select the oscillation stabilization delay time for the main clock.

WT1	WT0	Oscillation stabilization time	Oscillation stabilization time for an 8-MHz source oscillation
1	1	Approx. 2^{18}/FC	32.8 (ms)
1	0	Approx. 2^{17}/FC	16.4 (ms)
0	1	Approx. 2^{14}/FC	2.0 (ms)
0	0	Approx. 2^{4}/FC	0 (ms)

FC: Frequency of main clock oscillator

When the system clock select (SCS) bit specifies main mode, the device changes to main mode after the specified delay time.

The oscillation stabilization time after a reset depends on the initial value.

Do not write to this bit during the oscillation stabilization time. Also, do not write to this bit at the same time as changing from sub-clock to main clock mode.

The oscillation stabilization time for the main clock is derived from the main clock being divided. As the oscillation period is unstable immediately after the start of oscillation, the times listed above are an indication only.

[Bit 2] SCS: System clock select bit

Sets the system clock mode.

0	Selects sub-clock (32 kHz) mode
1	Selects main clock (8 MHz) mode

[Bit 1, 0] CS1, CS0: System clock selection bits (Gear function)

The table below lists the system operating clock speeds when the system clock select (SCS) bit specifies main mode.

CS1	CS0	Instruction cycle	Minimum instruction execution time at 8-MHz operation
0	0	64/FC	8.0 (μs)
0	1	16/FC	2.0 (μs)
1	0	8/FC	1.0 (μs)
1	1	4/FC	0.5 (μs)

FC: Frequency of main clock oscillator

(4) Operation

(4.1) Low-power Consumption Modes

To reduce power consumption, the MB89143A/4A supports three operating modes, the sleep and stop states. The table below lists the available modes. Also, four different system clocks are available in main mode, depending on the state of the system. This enables power consumption to be reduced to a minimum.

Table 2.1.1 Operation in Low-power Consumption Modes

Main operating mode	(CS1, CS0)	Operating mode	Clock generation		Operating clocks (for an 8-MHz main clock)				Wakeup factor for each mode
			Main	Sub	CPU	Time-base	Peripherals	Clock	
Main mode	(1, 1)	RUN	Operating	Operating	4 MHz	4 MHz	4 MHz	32 kHz	Any interrupt request
		Sleep			Halted				
		Stop	Halted			Halted	Halted		External interrupts
	(1, 0)	RUN	Operating	Operating	2.0 MHz	4 MHz	2.0 MHz	32 kHz	Any interrupt request
		Sleep			Halted				
		Stop	Halted			Halted	Halted		External interrupts
	(0, 1)	RUN	Operating	Operating	1.00 MHz	4 MHz	1.00 MHz	32 kHz	Any interrupt request
		Sleep			Halted				
		Stop	Halted			Halted	Halted		External interrupts
	(0, 0)	RUN	Operating	Operating	250.0 kHz	4 MHz	250.0 kHZ	32 kHz	Any interrupt request
		Sleep			Halted				
		Stop	Halted			Halted	Halted		External interrupts
Sub mode	—	RUN	Halted	Operating	32 kHz	Halted	32 kHz	32 kHz	Any interrupt request
		Sleep			Halted				
		Stop		Halted			Halted	Halted	External interrupts
Watch mode			Halted	Operating	Halted	Halted	Halted	32 kHz	External or timer interrupt

- The main clock oscillation halts in sub mode.
- Only the CPU operating clock halts in sleep mode, other clocks continue to operate.
- Other than a specific subset of resources, all functions halt in watch mode.
- Stop mode halts the oscillation. This mode maintains data with lowest power consumption.

(a) Watch mode

○ Changing to watch mode

- Writing "1" to the TMD bit in STBC changes to watch mode. However, the write is ignored if the SCS bit in SYCC is "1".
- Watch mode halts all chip functions except for the timer prescaler, external interrupts, and wakeup. Therefore, this mode maintains data with lowest power consumption.
- Also, the SPL bit in STBC controls the state of I/O and output pins during watch mode. Pins can be set to maintain their states prior to entering watch mode or to go to high impedance.
- If an interrupt request is present when "1" is written to the TMD bit, the device does not change to watch mode and instruction execution continues.
- In watch mode, registers and RAM maintain their values prior to entering watch mode.

○ Waking up from watch mode

- Wake-up from watch mode is either by an interrupt or input of a reset.
- If a reset is input during watch mode, the device changes to the reset state and wake up from watch mode.
- The device wakes up from watch mode if a peripheral circuit generates an interrupt request with a level higher than "11" during watch mode.
- Interrupt processing is executed after recovering from watch mode if the I flag and IL bits indicate that the interrupt can be accepted, in the same way as for normal interrupts. If the interrupt is not accepted, execution continues from the next instruction after the instruction that entered watch mode.
- On recovering from watch mode by a reset, the device first enters the oscillation stabilization delay state. The reset sequence does not execute until the oscillation stabilization delay is complete. The oscillation stabilization time is the oscillation stabilization time for the main clock specified by the WT1 and WT0 bits.

(b) Sleep mode

○ Changing to sleep mode

- Writing "1" to SLP (bit 6) in STBC changes to sleep mode.
- Sleep mode halts the CPU operating clock. The CPU halts but peripheral circuits continue to operate.
- If an interrupt request is present when "1" is written to SLP (bit 6), the device does not change to sleep mode and instruction execution continues.
- In sleep mode, registers and RAM maintain their values prior to entering sleep mode.

○ Waking up from sleep mode

- Wake-up from sleep mode is either by an interrupt or input of a reset.
- If a reset is input during sleep mode, the device changes to the reset state and wake up from sleep mode.
- The device wakes up from sleep mode if a peripheral circuit generates an interrupt request with a level higher than "11" during sleep mode.
- Interrupt processing is executed after recovering from sleep mode if the I flag and IL bits indicate that the interrupt can be accepted, in the same way as for normal interrupts. If the interrupt is not accepted, execution continues from the next instruction after the instruction that entered sleep mode.

(c) Stop mode

○ Changing to stop mode

- Writing "1" to STP (bit 7) in STBC changes to stop mode.
- The operation of stop mode depends on whether the device is operating on the main clock or sub-clock.

  When using the main clock : Operation of the main clock halts but the sub-clock does not halt. All chip functions other than the timer function halt.

  When using the sub-clock : Operation of both the main clock and sub-clock halts. All chip functions halt.
- Also, SPL (bit 5) in STBC controls the state of I/O and output pins during stop mode. Pins can be set to maintain their states prior to entering stop mode or to go to high impedance.
- If an interrupt request is present when "1" is written to STP (bit 7), the device does not change to stop mode and instruction execution continues.
- In stop mode, registers and RAM maintain their values prior to entering stop mode.

○ Waking up from stop mode

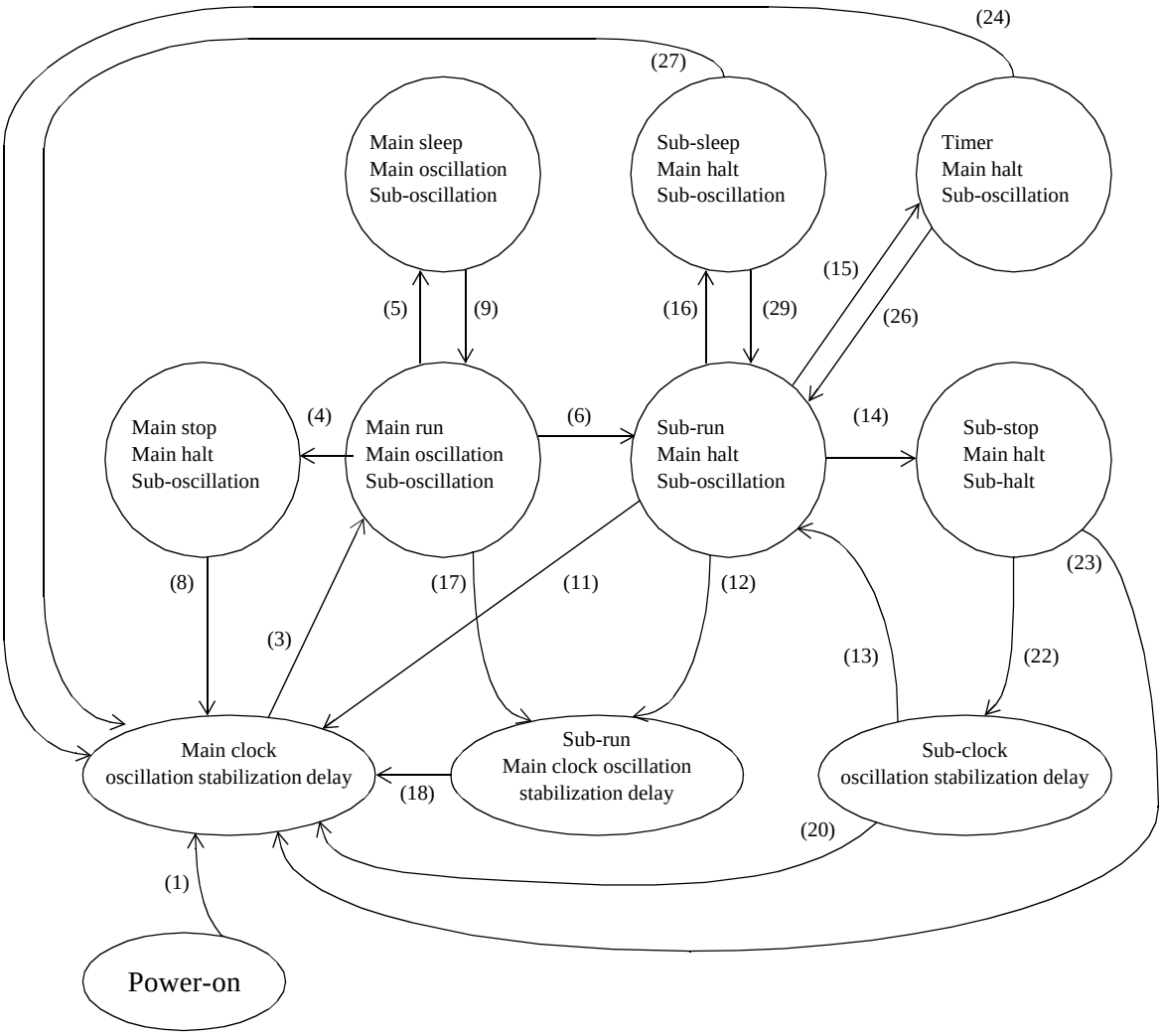
- Wake-up from stop mode is either by an interrupt or input of a reset.
- If a reset is input during stop mode, the device changes to the reset state and wake up from stop mode.
- The device wakes up from stop mode if an external interrupt circuit generates an interrupt request with a level higher than "11" during stop mode.
- Interrupt processing is executed after recovering from stop mode and after the oscillation stabilization delay time has passed if the I flag and IL bits indicate that the interrupt can be accepted, in the same way as for normal interrupts. If the interrupt is not accepted, execution continues from the next instruction after the instruction that entered stop mode.
- The oscillation stabilization time for the main clock is selected from four options by the WT1 and WT0 bits. The oscillation stabilization time for the sub-clock is fixed (2^{15}/FCL, FCL: Sub-clock frequency).
- On recovering from stop mode by a reset, the device first enters the oscillation stabilization delay state. The reset sequence does not execute until the oscillation stabilization delay is complete. The oscillation stabilization time is the oscillation stabilization time for the main clock specified by the WT1 and WT0 bits.

(d) Setting low-power modes

STBC Register			Mode
STP (bit7)	SLP (bit6)	TMD (bit3)	
0	0	0	Normal
0	0	1	Watch
0	1	0	Sleep
1	0	0	Stop
1	X	X	Prohibited

Precaution: Do not change to stop mode, sleep mode, or watch mode at the same time as switching from sub-clock to main clock mode. After changing the SCS bit of the SYCC register from "0" to "1", do not change to any of these modes until the SCM bit of the SYCC register goes to "1".

(4.2) State Transition Diagram



(1) Power-on

(3) After oscillation stabilization

(4) STP bit set to "1"

(5) SLP bit set to "1"

(6) SCS bit set to "0"

(8) External reset or external interrupt

(9) External reset or any interrupt

(11) External reset or other reset

(12) SCS bit set to "1"

(13) After oscillation stabilization

(14) STP bit set to "1"

(15) TMD bit set to "1"

(16) SLP bit set to "1"

(17) After oscillation stabilization

(18) External reset or other reset

(20) External reset

(22) External interrupt

(23) External reset

(24) External reset

(26) External interrupt or timer interrupt

(27) External reset

(29) Any interrupt

(4.3) Resets

Table 2.1.2 lists the four different types of reset.

Table 2.1.2 Factor of Resets

Reset	Description
External pin reset	Set the external reset pin to the "L" level.
Software reset	Write "0" to RST (bit 4) of STBC.
Watchdog reset	Watchdog timer overflow
Power-on reset	Turn on the power.

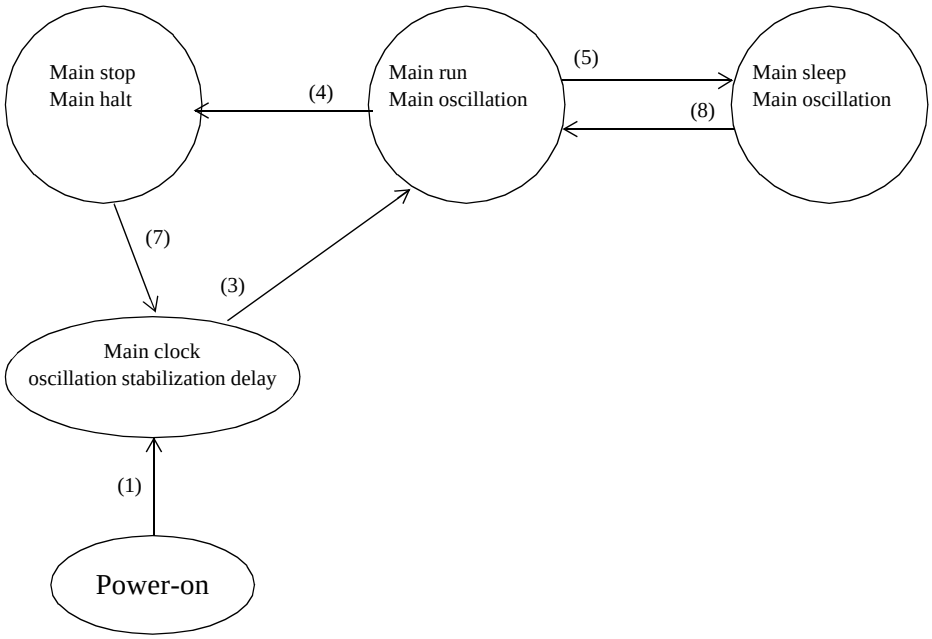
As the oscillator is halted when a power-on reset occurs or a reset occurs in stop mode, an oscillation stabilization time is required after the oscillator starts. The time-base timer or watch prescaler provides the stabilization time. Therefore, operation cannot restart immediately after a reset.

(5) Single Clock Operation

Single clock module can be selected as a mask option. So far, this section has described the functions of a dual clock system. However, apart from being unable to use sub-clock or watch mode, the operation of a single clock system is the same.

P71/X1A and P70/X0A function as input ports in single clock operation.

(5.1) State Transition Diagram



(1) Products that support the power-on reset

(3) After oscillation stabilization

(4) STP bit set to "1"

(5) SLP bit set to "1"

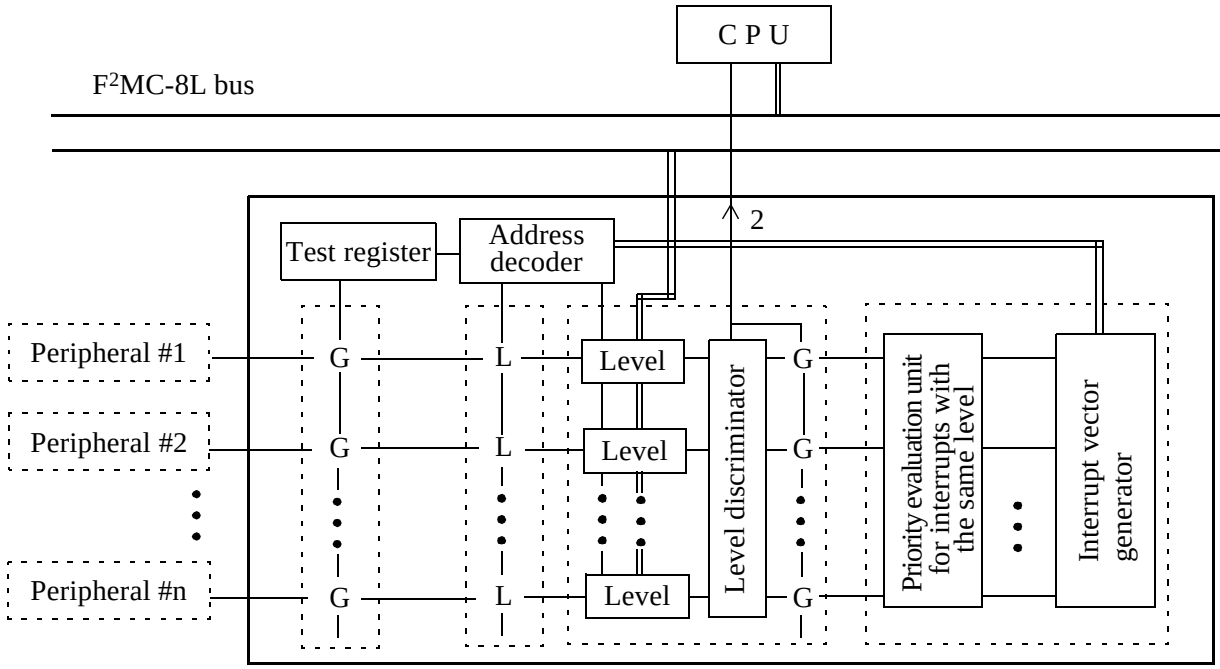
(7) External reset or interrupt

(8) External reset or interrupt

2.1.6 Interrupt Controller

The F²MC-8L interrupt controller is located between the F²MC-8L CPU and the various peripherals. The controller module receives interrupt requests from the peripherals, prioritizes, and then passes the interrupts to the CPU. The interrupt controller also determines the priority of interrupts with the same level.

(1) Block Diagram



(2) Registers

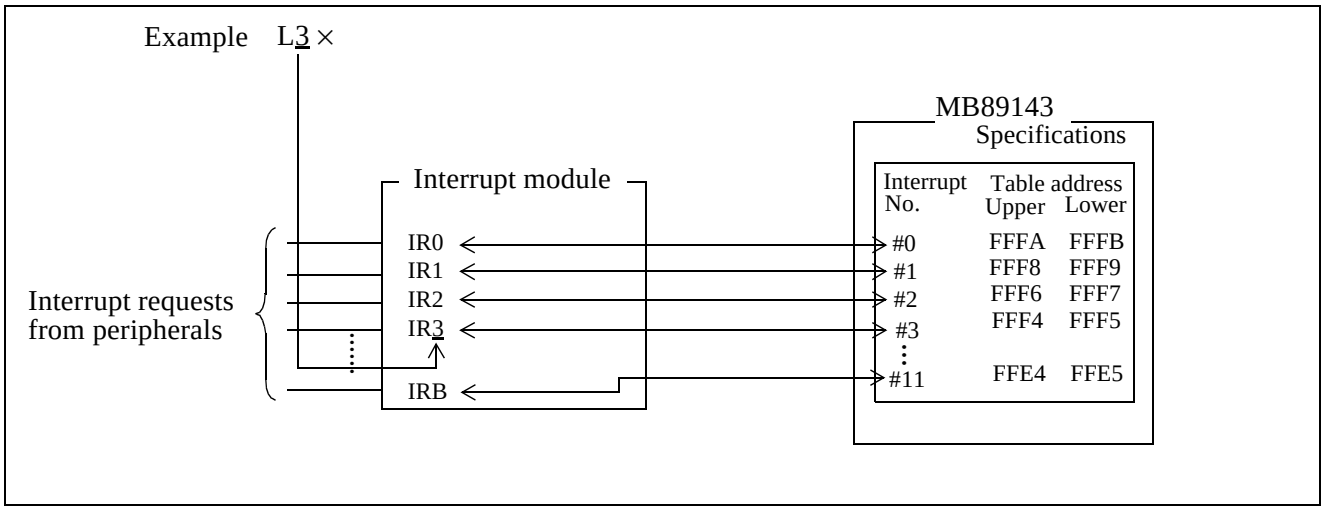
Address	7	6	5	4	3	2	1	0	Name (Abbreviation)	(Initial value)
007C$_H$	L31	L30	L21	L20	L11	L10	L01	L00	Interrupt level setting register #1 [ILR1]	(11111111)
007D$_H$	L71	L70	L61	L60	L51	L50	L41	L40	Interrupt level setting register #2 [ILR2]	(11111111)
007E$_H$	LB1	LB0	LA1	LA0	L91	L90	L81	L80	Interrupt level setting register #3 [ILR3]	(11111111)

(3) Register Description

(3.1) Interrupt Level Setting Registers (ILRx: Interrupt Level Register x)

	7							0		
ILR1	L31	L30	L21	L20	L11	L10	L01	L00	W	When reset (11111111)
ILR2	L71	L70	L61	L60	L51	L50	L41	L40	W	When reset (11111111)
ILR3	LB1	LB0	LA1	LA0	L91	L90	L81	L80	W	When reset (11111111)

The ILRx registers set the interrupt levels for each resource. The middle digit of each bit name indicates the interrupt number.



When an interrupt request is generated by a peripheral, the interrupt controller sends the interrupt level to the CPU based on the value set in the two ILRx bits for that interrupt. The following table shows the relationship between the two ILRx bits and the interrupt request level.

Lx1	Lx0	Interrupt Request Level
0	X	1
1	0	2
1	1	3 (No interrupt)

(4) Operation

(4.1) Interrupt Function

The MB89143A/4A has twelve interrupt request inputs from peripherals. The interrupt level for each input can be set in the corresponding 2-bit level register. When a peripheral generates an interrupt, the interrupt controller receives the interrupt and outputs the contents of the corresponding level register to the CPU. The following describes the overall interrupt processing for the device.

1. An interrupt source is generated in a peripheral.
2. The peripheral checks the interrupt enable bit and sends the interrupt request to the interrupt controller if the interrupt is enabled.
3. The interrupt controller receives the interrupt request, determines the priority of any other interrupt requests that have occurred simultaneously, then sends the interrupt level for the highest priority interrupt to the CPU.
4. The CPU compares the interrupt level of the request received from the interrupt controller with the IL bits in the program status register.
5. If the result of comparison is that the new interrupt has a higher priority than the current interrupt processing level, the CPU then checks the I flag in the program status register.
6. If the I flag indicates that interrupts are enabled, the CPU sets the level of the new request in the IL bits, then performs interrupt processing after the completion of the currently executing instruction and passes control to the interrupt processing routine.
7. Interrupt processing completes when the user interrupt processing routine clears the interrupt source that triggered the interrupt request in step 1.

Figure 2.1.9 shows a summary of MB89143A/4A interrupt operation.

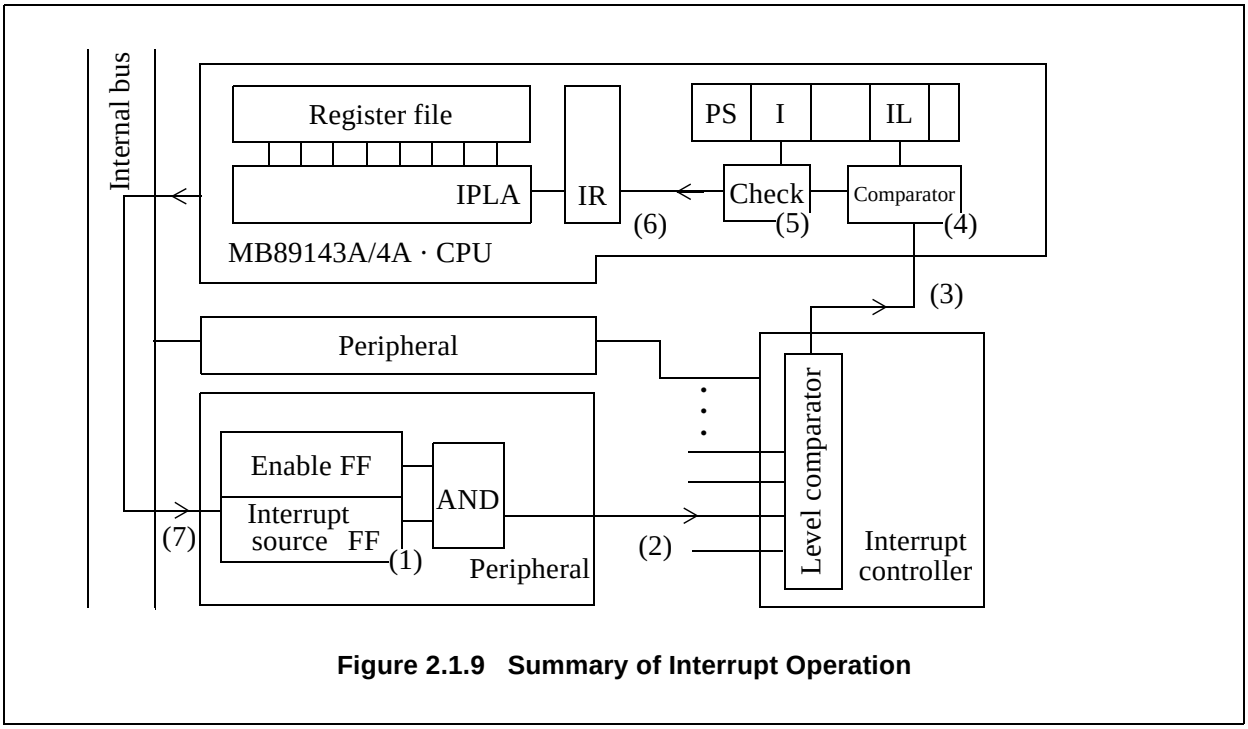


Figure 2.1.9 Summary of Interrupt Operation

2.2 Peripheral Functions

2.2.1 I/O Ports

- This series has eight parallel ports (55 pins, including the buzzer pin). Ports 0, 1, and 3 are CMOS I/O ports, port 2 is a CMOS output-only port, ports 4, 5, and 6 are P-ch open-drain high-voltage ports, and port 7 is an input-only port. The port 0 pins can also be used as analog input ports.
- Ports 0, 1, 2, and 3 also serve as a resource.
- The BZ pin is a P-ch open-drain high-voltage pin and is only used as the buzzer output.

Table 2.1.1 Port Functions

Pin	Input type	Output type	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
P00 to P07*2	CMOS (Hysteresis)	CMOS (Push-pull)	Parallel port 0	P07	P06	P05	P04	P03	P02	P01	P00
			Resource	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
P10 to P17	CMOS (Hysteresis)	CMOS (Push-pull)	Parallel port 1	P17	P16	P15	P14	P13	P12	P11	P10
			Resource	ADST	-	-	-	*3	*3	*3	*3
P20 to P23	-	CMOS (Push-pull)	Parallel port 2	-	-	-	-	P23	P22	P21	P20
P30 to P37	CMOS (Hysteresis)	CMOS (Push-pull)	Parallel port 3	P37	P36	P35	P34	P33	P32	-	P30
			Resource	-	-	EC	SI	SO	SCK	-	INT0
		N-ch open-drain	Parallel port 3	-	-	-	-	-	-	P31	-
			Resource	-	-	-	-	-	-	INT1	-
P40 to P47	-	P-ch open-drain high-voltage	Parallel port 4	P47	P46	P45	P44	P43	P42	P41	P40
P50 to P57	-	P-ch open-drain high-voltage	Parallel port 5	P57	P56	P55	P54	P53	P52	P51	P50
P60 to P67	-	P-ch open-drain high-voltage	Parallel port 6	P67	P66	P65	P64	P63	P62	P61	P60
P70 to P71	CMOS (Hysteresis)	-	Parallel port 7	-	-	-	-	-	-	P71*1	P70*1

*1: P71 and P70 become X1A and X0A respectively when the dual clock option is selected.

*2: After a reset, always declare P00 to P07 as general-purpose input ports in the PCR0 register if using these pins as input ports.

*3: After a reset, always declare P10 to P13 as general-purpose input ports in the PCR1 register if using these pins as input ports.

(1) Registers

Table 2.1.2 Port Registers

Register	Read/write	Address	Initial value
Port 0 data register (PDR0)	R/W	0000H	XXXXXXXXB
Port 0 data direction register (DDR0)	W	0001H	00000000B
Port 1 data register (PDR1)	R/W	0002H	XXXXXXXXB
Port 1 data direction register (DDR1)	W	0003H	00000000B
Port 2 data register (PDR2)	R/W	0004H	----0000B
Port 3 data register (PDR3)	R/W	000CH	XXXXXXXXB
Port 3 data direction register (DDR3)	W	000DH	00000000B
Port 4 data register (PDR4)	R/W	0010H	00000000B
Port 5 data register (PDR5)	R/W	0011H	00000000B
Port 6 data register (PDR6)	R/W	0012H	00000000B
Port 7 data register (PDR7)	R	0013H	------XXB

Precaution: The bit manipulation instructions (SETB and CLRB) cannot be used on the port data direction registers (DDR0, DDR1, and DDR3) as these registers are write-only.

(2) PCR0 and PCR1 (Port control registers).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0022H	P07	P06	P05	P04	P03	P02	P01	P00	00000000B
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0023H	—	—	—	—	P13	P12	P11	P10	----0000B
					(W)	(W)	(W)	(W)	

After a reset, general-purpose port input is disabled for ports P13 to P10 and P07 to P00. Therefore, write "1" to the corresponding register bits to use these pins as general-purpose port inputs. This enables the corresponding pins as port inputs.

As the registers are write-only, bit manipulation instructions (SETB and CLRB) cannot be used.

Register value	State
0	Operate as an analog input port.
1	Operate as a general-purpose input port.

Reading the PDR returns "0" when analog input port operation is specified. Do not use the pins as analog inputs when general-purpose port operation is specified.

(3) Function Description

P00 to P07 CMOS I/O ports (also serve as an analog input)

P10 to P13 CMOS I/O ports

- Switching between input and output

  DDR (data direction register) and PDR (port data register) bit are provided for each port bit, and each port bit can be set independently as either an input or output. Pins with DDR set to "1" operate as outputs and pins set to "0" operate as inputs.

- Output port (DDR = "1") operation

  Values written to the PDR are output directly to pins with DDR set to "1". Reading the PDR normally reads the pin value rather than the output latch value. However, read-modify-write instructions read the output latch value regardless of the DDR setting. Therefore, bit manipulation instructions can be used, even on ports that have both input and output pins. Data written to the PDR is stored in the output latch regardless of the DDR setting.

- Input port (DDR = "0") operation

  The pin output goes to high impedance and reading the PDR returns the pin value. However, if "0" is written to the PCR0 or PCR1 register, the corresponding pin value is read as "0" (see Figure 2.2.1).

- State during a reset

  A reset initializes the DDR to zero. This sets the output for all bits to high impedance. As the PDR is not initialized by a reset, set the PDR value before setting pins as outputs in the DDR. Also, port input is disabled after a reset, and port inputs are fixed at "L" (see Figure 2.2.1). Therefore, to specify pins as port inputs, write "1" to the corresponding bits in the PCR0 and PCR1 registers for the declaration of the use of port input.

- State during stop mode

  If the SPL bit in the standby control register is set to "1", all outputs go to high impedance during stop mode, regardless of the DDR setting.

- Analog inputs (P10 to P13 cannot be used as analog inputs)

  To use a pin as an analog input, set the corresponding DDR bit to "0". This turns off the output transistor. Also write "0" to any PCR0 register bits currently set to "1" that correspond to pins that you intend to use as analog inputs. This disables these pins from being used as general-purpose input ports. In this case, reading these port values always returns "0" (the port input level cannot be read).

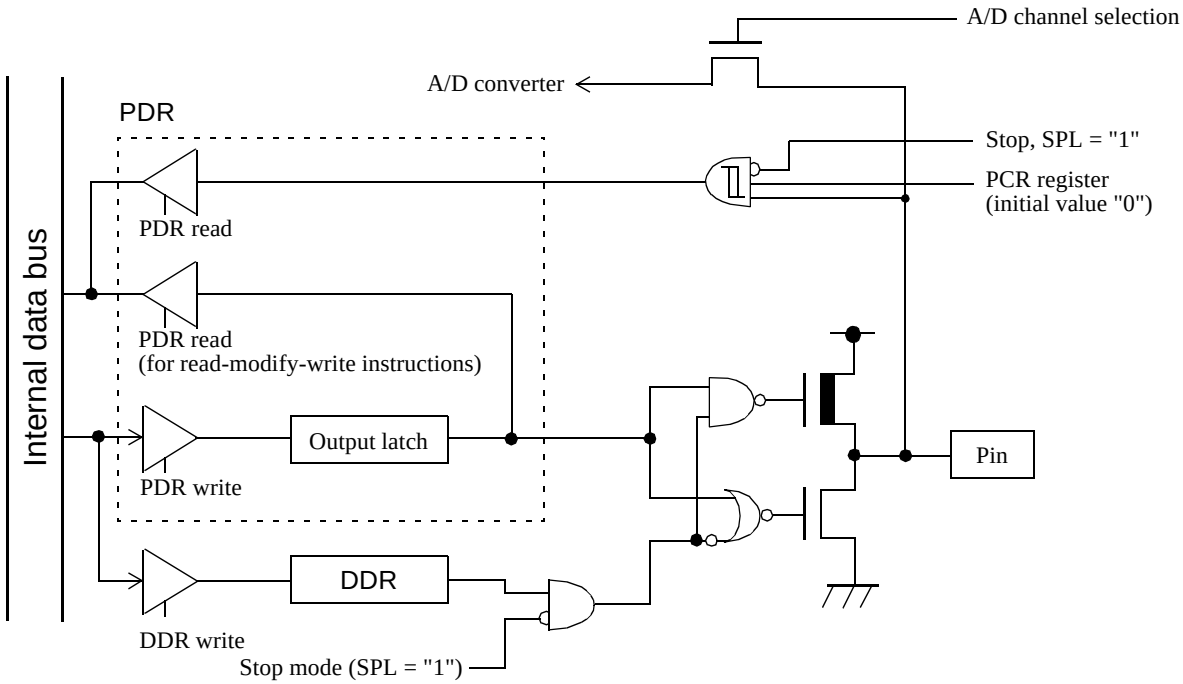


Figure 2.2.1 P00 to P07 and P10 to P13

P14 to P16 CMOS I/O ports

- Switching between input and output

  A DDR (data direction register) and PDR (port data register) bit are provided for each port bit, and each port bit can be set independently as either an input or output. Pins with DDR set to "1" operate as outputs and pins with DDR set to "0" operate as inputs.

- Output port (DDR = "1") operation

  Values written to the PDR are output directly to pins with DDR set to "1". Reading the PDR normally reads the pin value rather than the output latch value. However, read-modify-write instructions read the output latch value regardless of the DDR setting. Therefore, bit manipulation instructions can be used, even on ports that have both input and output pins. Data written to the PDR is stored in the output latch regardless of the DDR setting.

- Input port (DDR = "0") operation

  The pin output goes to high impedance and reading the PDR returns the pin value.

- State during a reset

  A reset initializes the DDR to zero. This sets the output for all bits to high impedance. As the PDR is not initialized by a reset, set the PDR value before setting pins as outputs in the DDR.

- State during stop mode

  If the SPL bit in the standby control register is set to "1", all outputs go to high impedance during stop mode, regardless of the DDR setting.

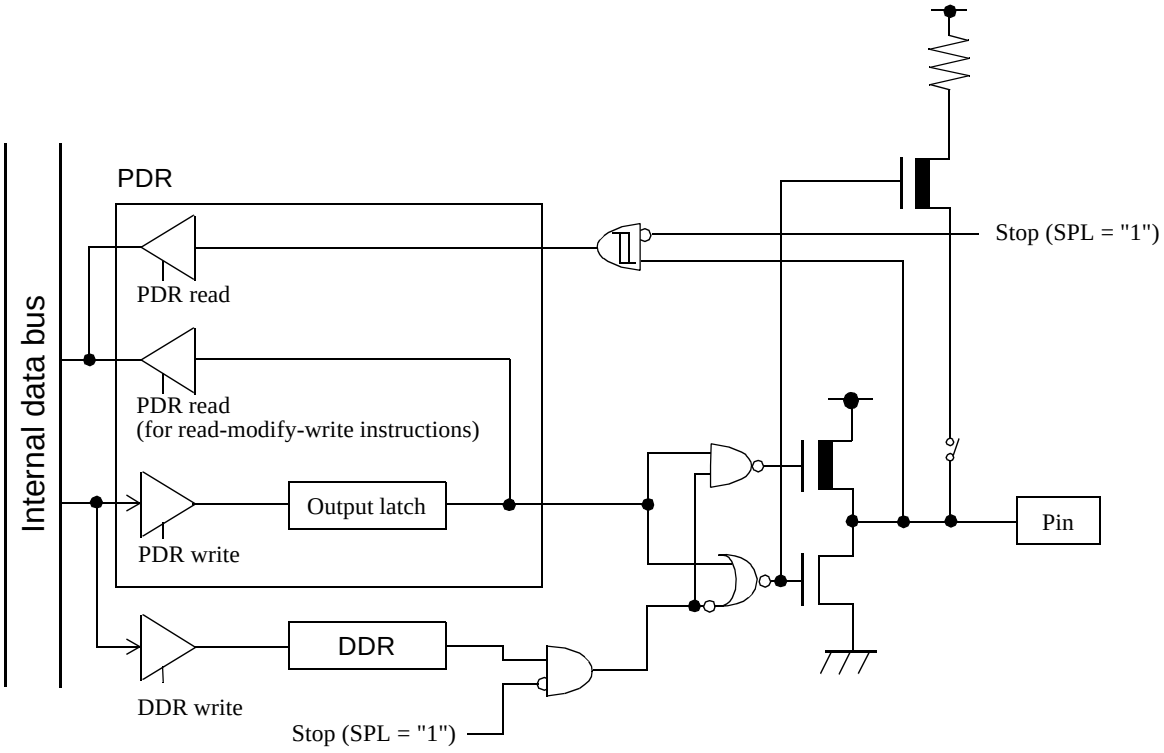


Figure 2.2.2 P14 to P16

P20 to P23 CMOS output ports

- Output port operation

  Values written to the PDR are output directly. As reading the PDR always reads the output latch value, bit manipulation instructions can be used, even if the output level varies due to the load.

- State during a reset

  A reset sets all pins to high impedance. Output port operation starts when port output is enabled at the vector fetch timing. The PDR is initialized to "0" by a reset. This sets all pins to the "L" level.

- State during stop mode

  If the SPL bit in the standby control register is set to "1", all outputs go to high impedance during stop mode, regardless of the PDR setting.

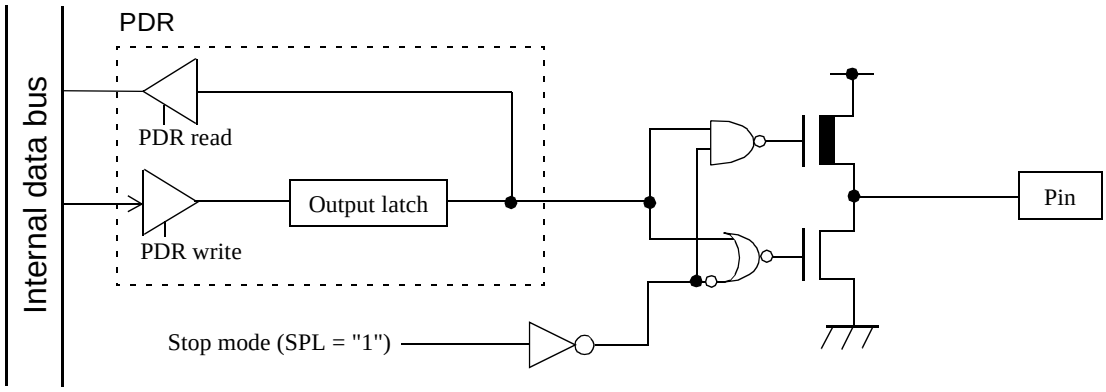


Figure 2.2.3 Port 2 (P20 to P23)

P71 and P70 CMOS input ports

- Input port operation

  The PDR is read only. Reading the PDR always returns the pin values. P71 and P70 function as X1A and X0A respectively if the dual clock option is selected.

- State during a reset

  The PDR is not initialized by a reset.

- State during stop mode

  Always fix the inputs at "L" or "H" when the single clock option is selected.

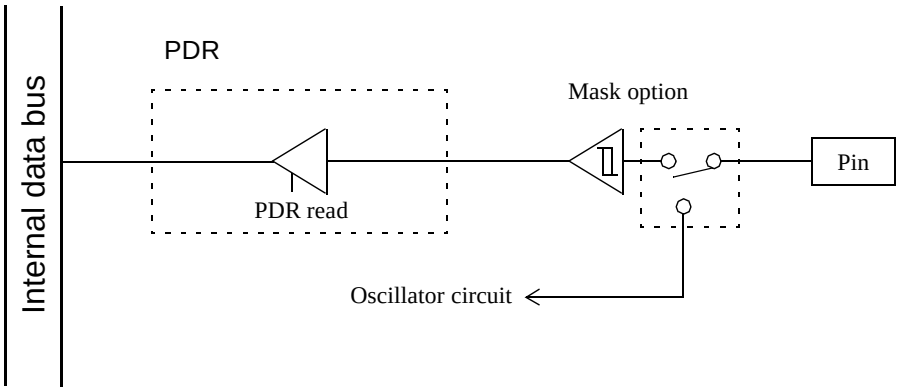


Figure 2.2.4 P71 and P70

P30, P32 to P37, and P17 CMOS I/O ports (also serve as a resource I/O)

- Switching between input and output

  DDR (data direction register) and PDR (port data register) bit are provided for each port bit, and each port bit can be set independently as either an input or output. Pins with DDR set to "1" operate as outputs and pins set to "0" operate as inputs.

- Output port (DDR = "1") operation

  Values written to the PDR are output directly to pins with DDR set to "1". Reading the PDR normally reads the pin value rather than the output latch value. However, read-modify-write instructions read the output latch value regardless of the DDR setting. Therefore, bit manipulation instructions can be used, even on ports that have both input and output pins. Data written to the PDR is stored in the output latch regardless of the DDR setting.

- Input port (DDR = "0") operation

  The pin output goes to high impedance and reading the PDR returns the pin value.

- Operation as a resource output

  To use a pin as a resource output, set the output enable bit in the resource. (See the description of each resource for details.) The output enable bit in the resource has priority when determining whether the pin is an input or output. Therefore, if output is enabled in the resource, the pin operates as a resource output even if the DDR bit is set to "0". Reading a parallel port remains a valid operation, even if the resource output is enabled. Consequently, the resource output value can be read.

- Operation as a resource input

  For ports that also serve as a resource input, the pin value is continuously input to the resource (regardless of the DDR or resource settings). To use the external signal in the resource, set the pin as an input in the DDR.

- State during a reset

  A reset initializes the DDR to zero. This sets the output for all bits to high impedance. As the PDR is not initialized by a reset, set the PDR value before setting pins as outputs in the DDR.

- State during stop mode

  If the SPL bit in the standby control register is set to "1", all outputs go to high impedance during stop mode, regardless of the DDR setting.

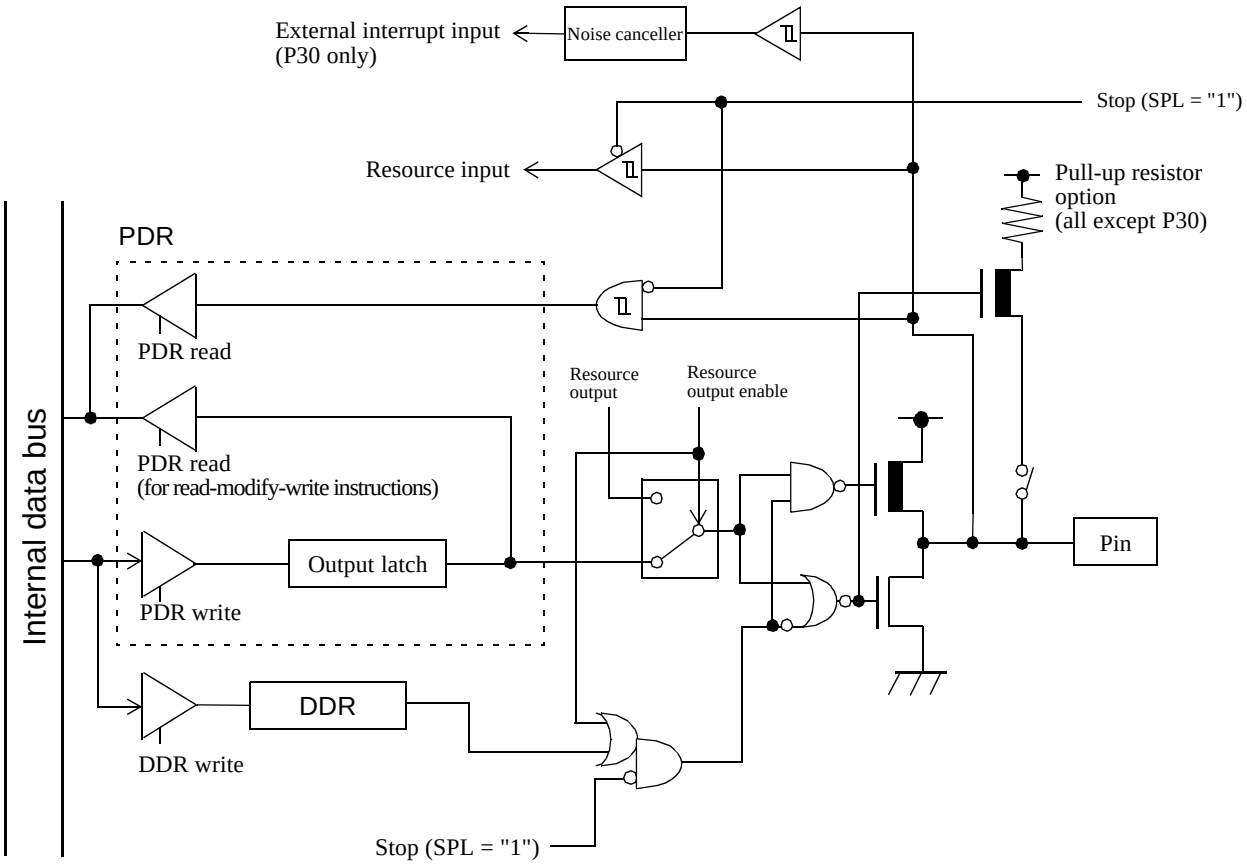


Figure 2.2.5 Port 3 (P30, P32 to P35, and P17)

P31 N-ch open-drain pin (shared with a resource input)

- Switching between input and output

  DDR (data direction register) and PDR (port data register) bit are provided for each port bit, and each port bit can be set independently as either an input or output. Pins with DDR set to "1" operate as outputs and pins with DDR set to "0" operate as inputs.

- Output port (DDR = "1") operation

  Values written to the PDR are output directly to pins with DDR set to "1". Reading the PDR normally reads the pin value rather than the output latch value. However, read-modify-write instructions read the output latch value regardless of the DDR setting. Therefore, bit manipulation instructions can be used, even on ports that have both input and output pins. Data written to the PDR is stored in the output latch regardless of the DDR setting.

- Input port (DDR = "0") operation

  The pin output goes to high impedance and reading the PDR returns the pin value.

- Operation as a resource input

  For ports that also serve as a resource input, the pin value is continuously input to the resource (regardless of the PDR or resource settings). To use the external signal in the resource, set the DDR bit to "0".

- State during a reset

  A reset initializes the DDR to zero. This sets the output for all bits to high impedance. As the PDR is not initialized by a reset, set the PDR value before setting pins as outputs in the DDR.

- State during stop mode

  If the SPL bit in the standby control register is set to "1", all outputs go to high impedance during stop mode, regardless of the DDR setting.

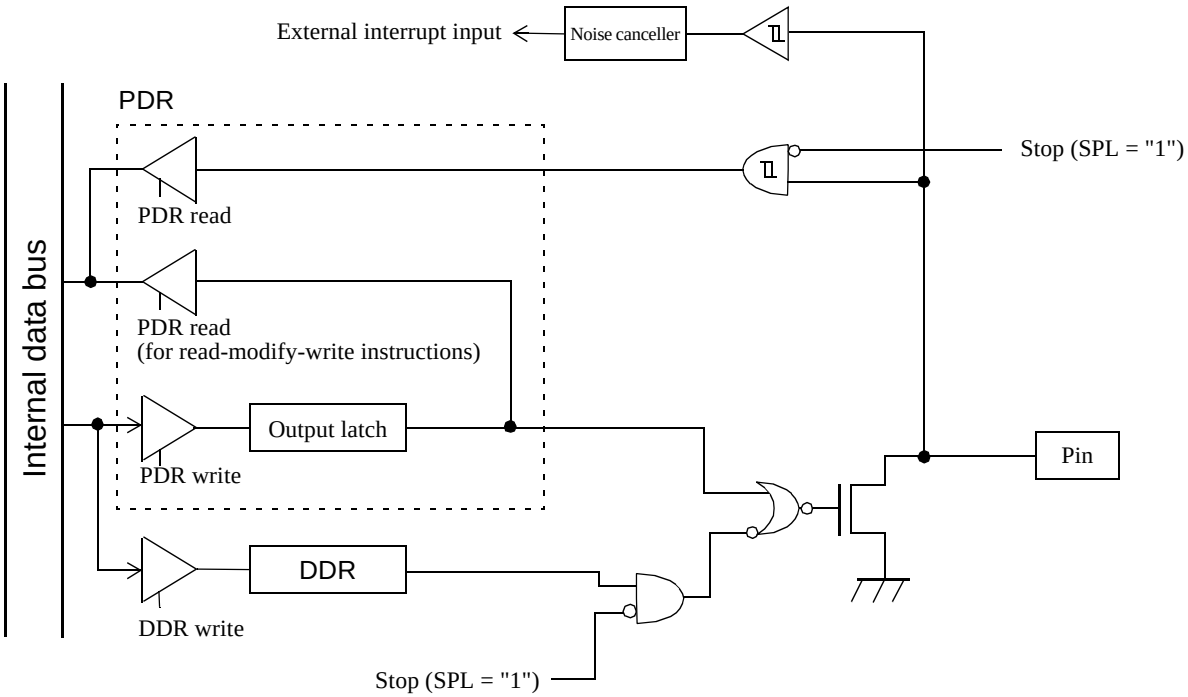


Figure 2.2.6 P31

P40 to P47 P-ch open-drain high-voltage output port

P50 to P57 P-ch open-drain high-voltage output port

P60 to P67 P-ch open-drain high-voltage output port

- Output port operation

  Values written to the PDR are output directly to the pins. As reading the PDR always reads the output latch value, it is not possible to read the pin state.

- State during a reset

  A reset initializes the PDR to zero. This turns the output transistor off for all bits.

- State during stop mode

  If the SPL bit in the standby control register is set to "1", all outputs go to high impedance during stop mode, regardless of the PDR setting.

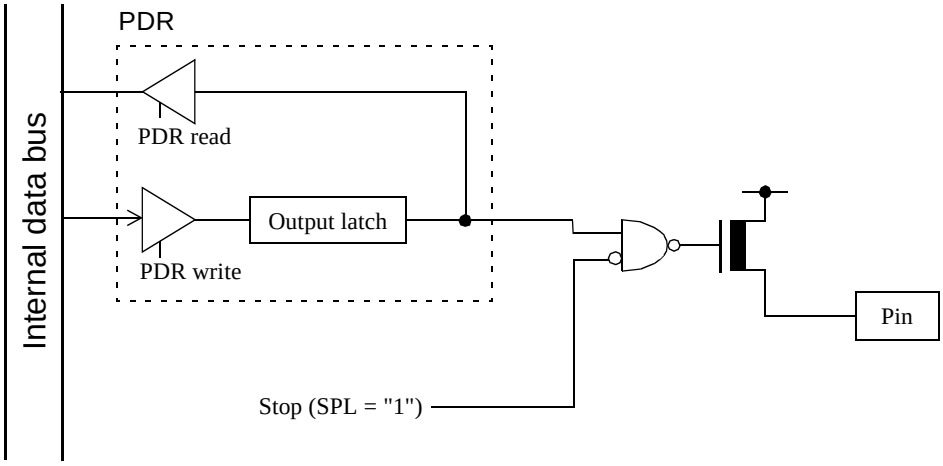


Figure 2.2.7 P40 to P47, P50 to P57, and P60 to P67

BZ P-ch open-drain high-voltage output

- Buzzer output operation

  Waveforms with the frequency specified by BUZR (the buzzer register) are output to the pin.

- State during a reset

  A reset initializes BUZR to zero. This sets the output to high impedance.

- State during stop mode

  If the SPL bit in the standby control register is set to "1", the output goes to high impedance during stop mode, regardless of the BUZR setting.

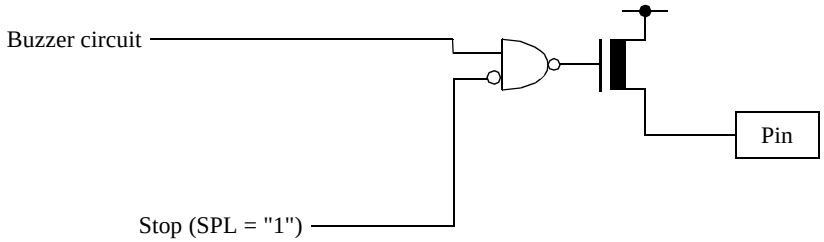


Figure 2.2.8 BZ

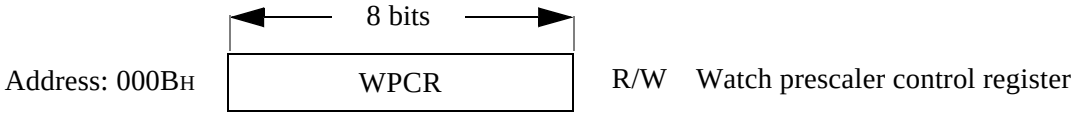
2.2.2 Watch Prescaler

◎ Incorporates a 15-bit binary counter.

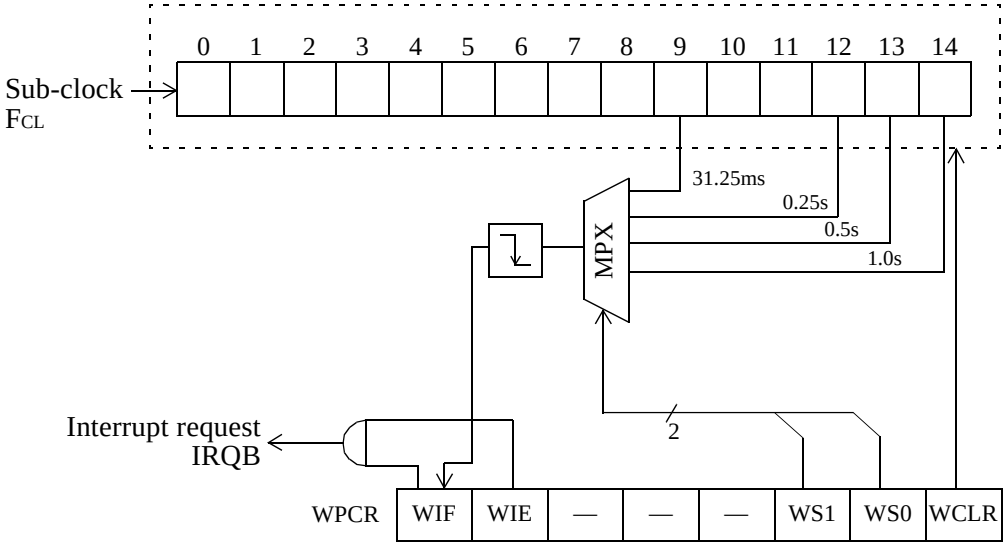
◎ Four different interval times available.

◎ This function is not available if the single clock mask option is selected.

(1) Register



(2) Block Diagram



(3) Register Description

WPCR (Watch Prescaler Control Register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 000B$_H$	WIF	WIE	—	—	—	WS1	WS0	WCLR	00---000$_B$
	(R/W)	(R/W)				(R/W)	(R/W)	(R/W)	

[Bit 7] WIF: Watch interrupt flag

Writing to this bit clears the watch interrupt flag.

0	Clear watch interrupt flag.
1	No operation

Reading this bit indicates whether a watch interrupt has occurred.

0	No watch interrupt
1	Watch interrupt occurred.

Read-modify-write instructions read this bit as "1".

An interrupt request is generated when the WIF bit goes to "1" if the WIE bit is "1".

Cleared by a reset.

[Bit 6] WIE: Watch interrupt enable bit

Enables watch interrupts.

0	Disable watch interrupts.
1	Enable watch interrupts.

[Bit 2, 1] WS1, WS0: Interval time setting bits for the watch interrupt

These bits specify the period of the watch interrupt.

WS1	WS0	Interrupt period	
0	0	31.25 [ms]	$2^{10}/F_{CL}$
0	1	0.25 [s]	$2^{13}/F_{CL}$
1	0	0.50 [s]	$2^{14}/F_{CL}$
1	1	1.00 [s]	$2^{15}/F_{CL}$

F_{CL}: Sub-clock oscillator frequency

[Bit 0] WCLR: Watch prescaler clear bit

This bit clears the watch prescaler.

0	Clear the watch prescaler.
1	No operation

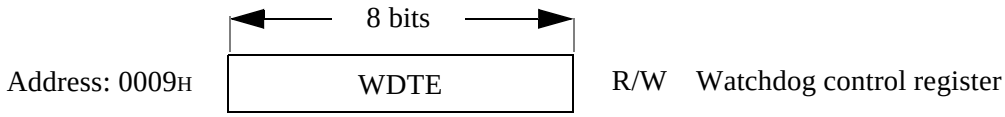
Reading this bit always returns "1".

2.2.3 Watchdog Reset

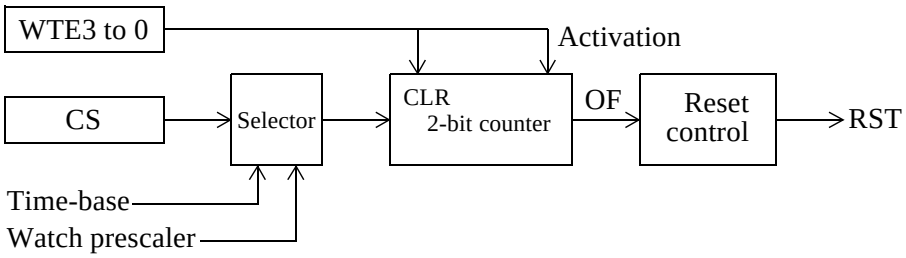
◎ Either the time-base timer or watch prescaler can be selected as the clock source.

◎ By repeatedly clearing the watchdog timer at fixed intervals, detection of an overflow on the watchdog timer can be used to detect program runaway.

(1) Register



(2) Block Diagram



(3) Register Description

(3.1) WDTE (Watchdog Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0009H	CS	—	—	—	WTE3	WTE2	WTE1	WTE0	0---XXXXB
	(R/W)				(W)	(W)	(W)	(W)	

[Bit 7] CS: Clock source selection bit

Selects the watch prescaler or time-base timer as the count clock.

0	Time-base timer Period $1/2^{22}$ FC
1	Watch prescaler Period $1/2^{14}$ FCL

FC: Main clock frequency

FCL: Sub-clock frequency

Notes: • Set this bit at the same time as starting the timer. Do not change the setting after the timer has started.

• Always select the watch prescaler if using sub mode.

• Do not select the watch prescaler on products using a single clock.

[Bits 3 to 0] WTE3 to WTE0: Watchdog control bits

The watchdog control bits

First write after a reset:

0101	Start watchdog timer.
Other than above	No operation

Second and subsequent writes after a reset:

0101	Clear the watchdog timer's counter.
Other than above	No operation

The watchdog timer can only be halted by a reset.

Reading these bits returns "1111".

(4) Operation

The watchdog timer function can detect program runaway.

○ Activation

Write "0101" to the watchdog control bits to start the timer.

○ Clearing the watchdog timer

Once started, writing "0101" to the watchdog control bits clears the watchdog timer.

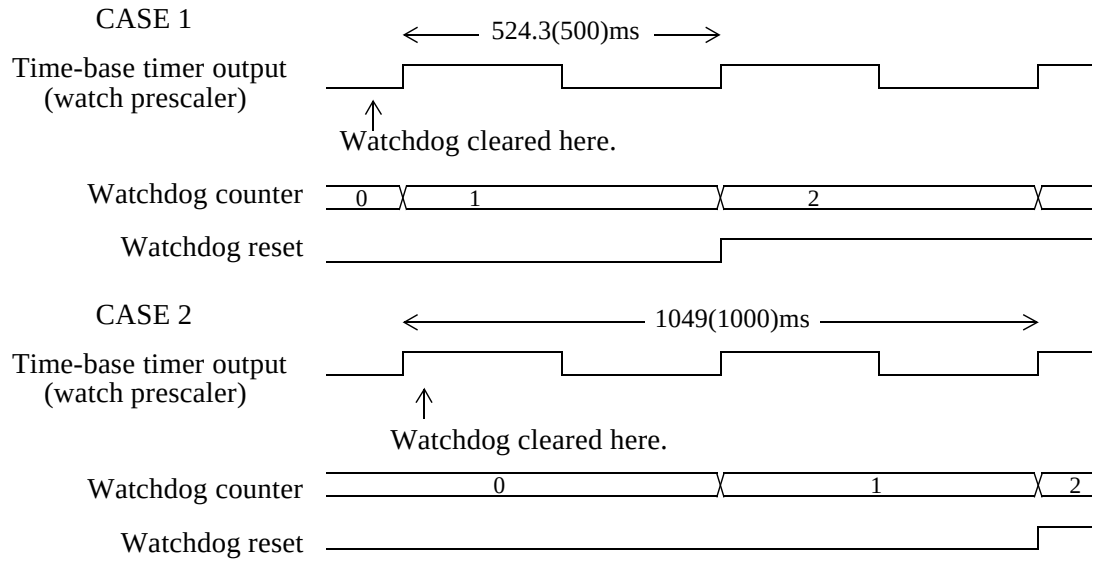
The counter of the watchdog timer is also cleared when the device changes to a standby state (stop, sleep, or watch mode).

○ Watchdog reset

A watchdog reset is generated and the chip is initialized if the watchdog timer is not cleared within the times specified in the table below.

	Clock source	
	8-MHz main clock time-base timer	32.768 kHz sub-clock watch prescaler
Minimum time	Approx. 524.3 ms	500 ms
Maximum time	Approx. 1049 ms	1000 ms

- The figure below shows the relationship between the time-base timer (or watch prescaler) and the 2-bit counter of the watchdog timer.



- As the above timing diagram shows, the watchdog interval time varies depending on when the watchdog timer is cleared.

○ Halting the watchdog timer

Once started, the watchdog timer does not halt until a reset occurs.

2.2.4 Time-base Timer

◎ Incorporates a 21-bit binary counter.

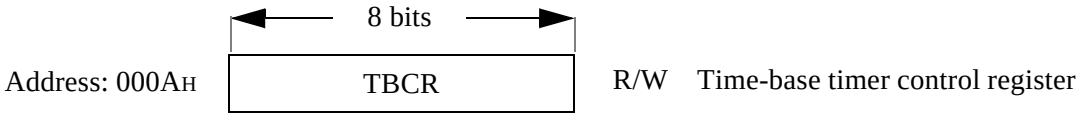
◎ Uses the main clock divided by 2 as the clock source.

◎ Four different selectable interval times

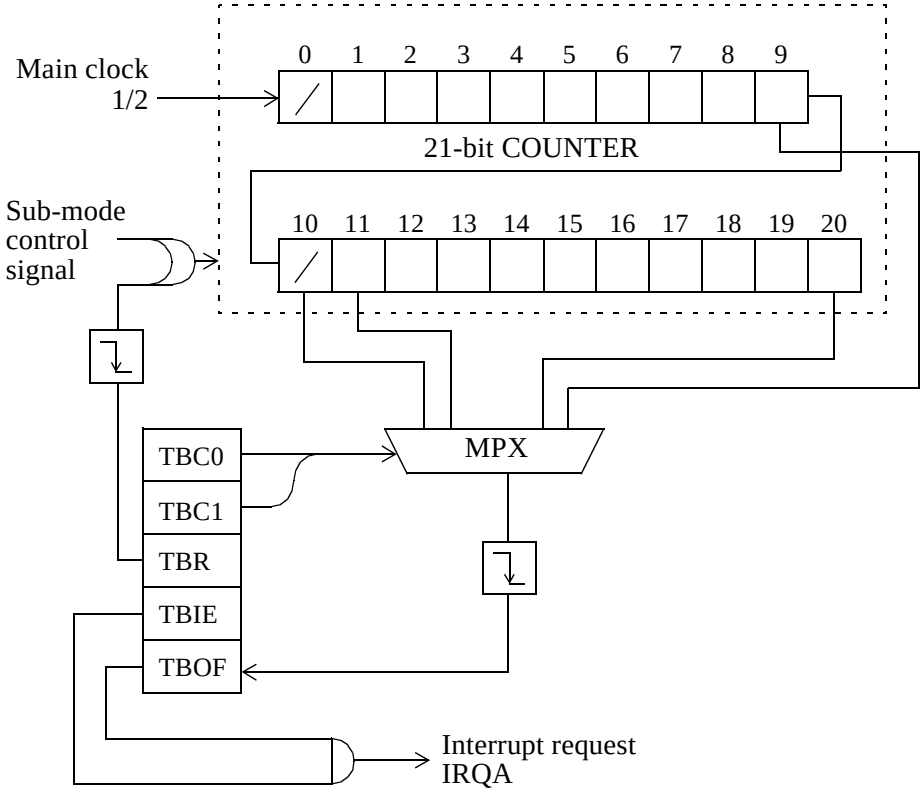
◎ Cannot be used when the main clock is halted.

◎ The timer clock source is not affected by changing the clock gear.

(1) Register



(2) Block Diagram



(3) Register Description

TBCR (Time-base timer control register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 000A$_H$	TBOF	TBIE	—	—	—	TBC1	TBC0	TBR	00---000$_B$
	(R/W)	(R/W)				(R/W)	(R/W)	(W)	

[Bit 7] TBOF: Interval timer overflow bit

Writing to this bit clears the interval timer overflow flag.

0	Clear the interval timer overflow flag.
1	No operation

Reading this bit indicates whether or not an interval timer overflow has occurred.

0	No interval timer overflow has occurred.
1	An interval timer overflow has occurred.

Read-modify-write instructions read the bit as "1".

If the TBIE bit is "1", an interrupt request is generated when the TBIF bit goes to "1".

Cleared by a reset.

[Bit 6] TBIE: Interval interrupt enable bit

Enables interval timer interrupts.

0	Disable interval interrupts.
1	Enable interval interrupts.

[Bit 2] TBC1: Interval time setting bit

[Bit 1] TBC0: Interval time setting bit

These bits set the period of the interval timer.

TBC1	TBC0	Interval time	For an 8-MHz source oscillation
0	0	$2^{11}F_C$	0.26 [ms]
0	1	$2^{12}F_C$	0.51 [ms]
1	0	$2^{13}F_C$	1.02 [ms]
1	1	$2^{22}F_C$	0.524 [s]

F$_C$: Main clock oscillation frequency

[Bit 0] TBR: Time-base timer clear bit

This bit clears the time-base timer.

0	Clear the time-base timer.
1	No operation

Reading this bit always returns "1".

2.2.5 8/16-Bit Timer/Counter (Timer 2 and Timer 3)

◎ The clock input can be selected from one external and three internal clocks.

◎ The external input can be selected to detect rising edges, falling edges, or both edges.

◎ Can operate in either 8 bits × 2 channel mode or 16 bits × 1 channel mode.

(1) Registers

	8 bits		
Address: 0018H	T3CR	R/W	Timer 3 control register
Address: 0019H	T2CR	R/W	Timer 2 control register
Address: 001AH	T3DR	R/W	Timer 3 data register
Address: 001BH	T2DR	R/W	Timer 2 data register

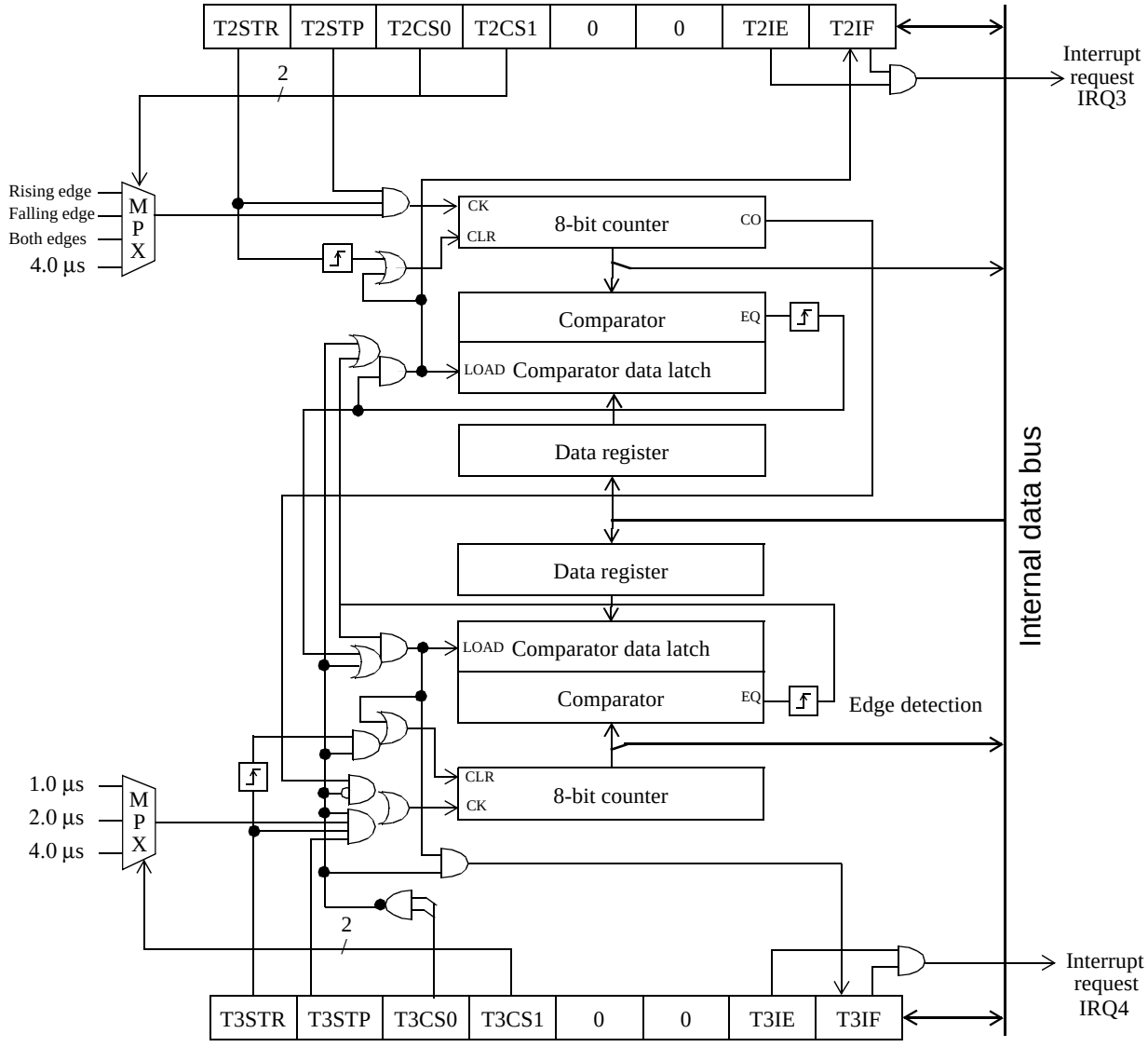


Figure 2.2.11 Block Diagram of the 8/16-Bit Timer/Counter

(2) Register Details

(2.1) Timer 2 Control Register (T2CR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0019H	T2IF	T2IE	0	0	T2CS1	T2CS0	T2STP	T2STR	X000 XXX0B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] T2IF: Interrupt request flag bit

The interrupt request flag bit.

(Write)

0	Clear interrupt request flag bit.
1	No operation

(Read)

0	No interrupt request
1	Interval interrupt request present

Read-modify-write instructions always read the bit as "1".

[Bit 6] T2IE: Interrupt enable bit

This bit specifies whether interrupts are enabled or disabled.

0	Disable interrupts
1	Enable interrupts

[Bit 5] RESERVE: Always write "0" to this bit.

[Bit 4] RESERVE: Always write "0" to this bit.

Note: Writing the values other than 0 to the bits 5 and 4 may cause errors.

[Bit 3] T2CS1: Clock source select bit

[Bit 2] T2CS0: Clock source select bit

These bits select the clock source for the timer.

T2CS1	T2CS0	Timer period (8 MHz with gear set to highest speed)	Instruction cycle
0	0	Rising edge of external clock	—
0	1	Falling edge of external clock	—
1	0	Both edges of external clock	—
1	1	4.00 [μs]	8 instruction cycles

Note: Even when the timer 3 is not being used, be sure to set the T3CR bits 3 and 2 (T3CS1, T3CS0) to the values other than ‘11’ to prevent errors.

[Bit 1] T2STP: Timer halt bit

The timer halt bit.

0	Continue operation without clearing the counter.
1	Temporarily halt count operation.

[Bit 0] T2STR: Timer start bit

The timer start bit.

0	Halt operation.
1	Clear counter then start operation.

(2.2) Timer 3 Control Register (T3CR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0018H	T3IF	T3IE	0	0	T3CS1	T3CS0	T3STP	T3STR	X000 XXX0B
	(R/W)	(R/W)			(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] T3IF: Interrupt request flag bit

The interrupt request flag bit.

(Write)

0	Clear interrupt request flag bit.
1	No operation

(Read)

0	No interrupt request
1	Interval interrupt request present

Read-modify-write instructions always read the bit as "1".

[Bit 6] T3IE: Interrupt enable bit

This bit specifies whether interrupts are enabled or disabled.

0	Disable interrupts
1	Enable interrupts

[Bit 5] RESERVE: Always write "0" to this bit.

[Bit 4] RESERVE: Always write "0" to this bit.

Note: Writing the values other than 0 to the bits 5 and 4 may cause errors.

[Bit 3] T3CS1: Clock source select bit

[Bit 2] T3CS0: Clock source select bit

These bits select the clock source for the timer.

T3CS1	T3CS0	Timer period (8 MHz with gear set to highest speed)	Instruction cycle
0	0	1.0 [μs]	2 instruction cycles
0	1	2.0 [μs]	4 instruction cycles
1	0	4.0 [μs]	8 instruction cycles
1	1	(16-bit mode)	—

Note: Always set these bits to other than "11" if using timer 2 only.

[Bit 1] T3STP: Timer halt bit

The timer halt bit.

0	Continue operation without clearing the counter.
1	Temporarily halt count.

[Bit 0] T3STR: Timer start bit

The timer start bit.

0	Halt operation.
1	Clear counter then start operation.

(2.3) Timer 2 and 3 Data Registers (T2DR, T3DR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 001B$_H$									XXXX XXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 001A$_H$									XXXX XXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Writing data sets the interval time. Reading data reads the current counter value.

(3) Operation

(3.1) 8-Bit Internal Clock Mode

In 8-bit internal clock mode, the clock source setting bits (T2CS1, T2CS0) and (T3CS1, T3CS0) in the timer control registers (T2CR and T3CR) select the internal clock for each channel and the timer data registers (T2DR and T3DR) set the interval times.

To start a timer, first set the interval time in the data register, then write "1" to the timer start bit (T2STR or T3STR) in the timer control register. This clears the counter to "00H" and loads the data register value to the compare latch. The count-up operation then starts.

The timer/counter sets the interval interrupt request flag bit (T2IF or T3IF) to "1" when the counter value matches the value set in the data register. At this time, the counter is cleared to "00H", the data register value is re-loaded into the compare latch, and the count operation continues. If the interrupt enable bit (T2IE and T3IE) is "1", an interrupt request is output to the CPU.

The interval time (T) is calculated as follows, where (n) is the value set in the data register and ϕ is the selected clock.

$$T = \phi \times (n + 1) \ [\mu s]$$

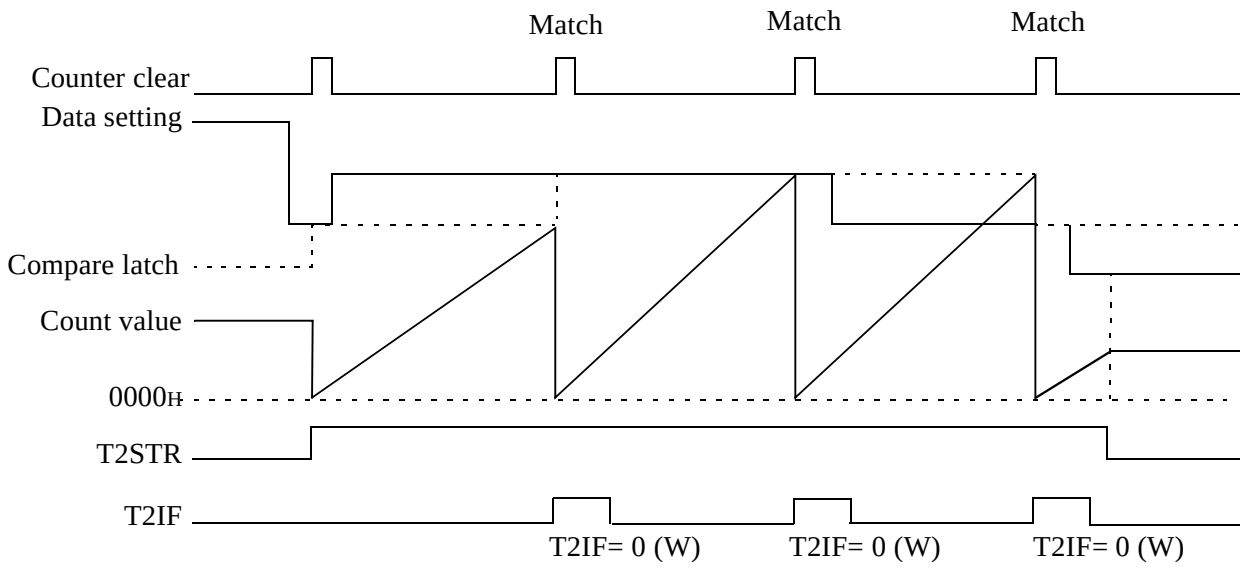


Figure 2.2.12 Internal Clock Mode Operation

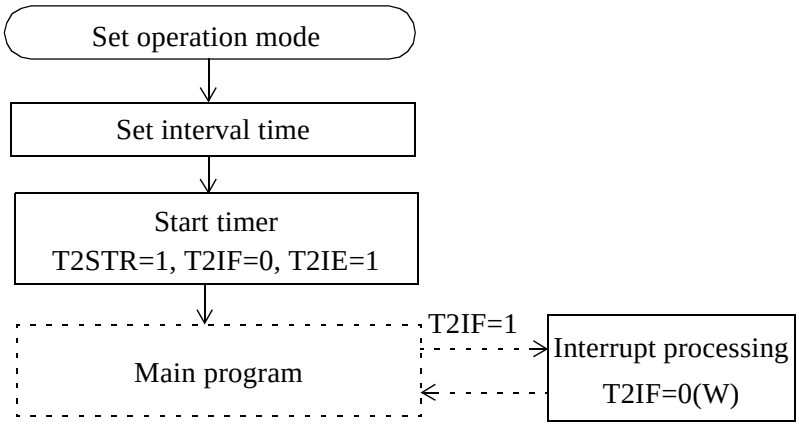


Figure 2.2.13 Timer Setting Flowchart

(3.2) 8-Bit External Clock Mode

In 8-bit external clock mode, the clock source select bits (T2CS1, T2CS0) in the timer 2 control register (T2CR) select one of the three types of external clock input.

To start a timer, write "1" to the timer start bit (T2STR) of T2CR. This clears the counter and starts counting up.

The timer/counter sets the interval interrupt request flag bit (T2IF) to "1" when the counter value matches the value set in the data register. If interrupts are enabled at this time (T2IE = "1"), an interrupt request is output to the CPU.

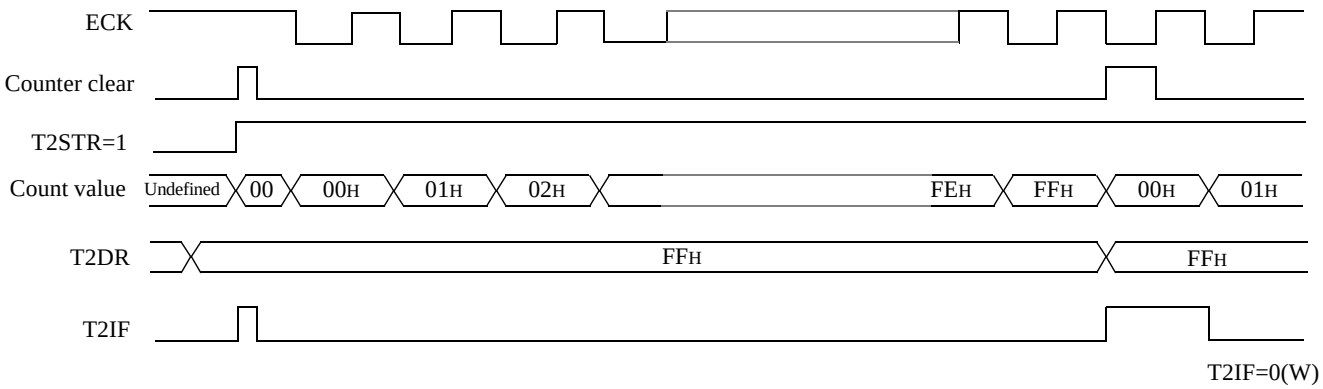


Figure 2.2.14 External Clock Mode Operation

(3.3) Cautions on Using the Timer Halt Bit

Figure 2.2.15 shows how the count value can advance by one when the timer is halted by the timer start bit after the timer has been temporarily halted by the timer halt bit. Whether or not the count advances by one depends on the state of the timer input clock (the count advances by one if the input clock level is "L", but not if the input level is "H".)

Therefore, when the timer is temporarily halted by the timer halt bit, read the counter before writing "0" to the start bit.

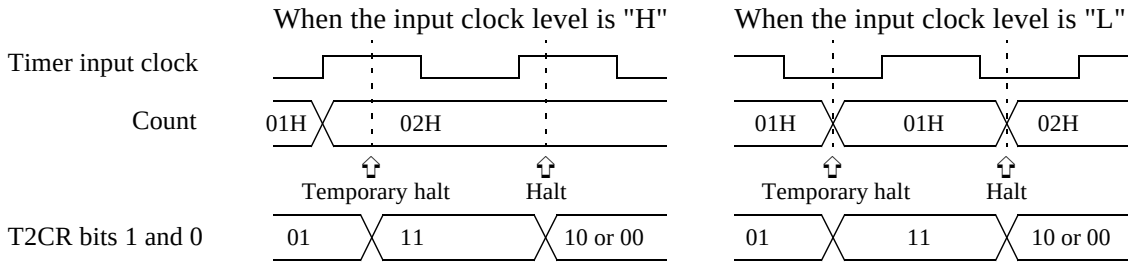


Figure 2.2.15 Timer Operation When Using the Timer Halt Bit

(3.4) 16-Bit Mode

The timer control register bits are set as follows in 16-bit mode.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0019H	T2IF	T2IE	—	—	T2CS1	T2CS0	T2STP	T2STR
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0018H	T3IF	T3IE	—	—	T3CS1	T3CS0	T3STP	T3STR
	No meaning		Set to "00"		Set to "11"		No meaning	

In 16-bit mode, set the T3CS1 and T3CS0 bits of T3CR to "11", and set bits 4 and 5 to "00".

In 16-bit mode, timer control is performed by T2CR. T3DR becomes the upper byte and T2DR the lower byte of the data register.

The T2CS1 and T2CS0 bits of T2CR select the clock source. To start the timer, write "1" to the T2STR bit in T2CR. This clears the counter then starts counting.

The timer/counter sets the T2IF bit to "1" when the counter value matches the value set in the data register. If the T2IE bit = "1" at this time, an interrupt request is output to the CPU.

Note: When reading the counter value in 16-bit mode, always read the counter twice and check the validity of the read value before using the data.

○ For a diagram of timer operation, see the operation diagrams for the 8-bit modes.

(3.5) Starting and Temporarily Halting the Timer

As the operation is the same for both timer 3 and timer 2, the following describes the operation for timer 2 only.

1. Starting the count after clearing the counter

   When the T2STR bit is "0", write "01" to the T2STP and T2STR bits. The timer clears the counter and starts counting when the T2STR bit changes from "0" to "1".

2. Restarting without clearing the counter when the timer is temporarily halted

   Write "11" to the T2STP and T2STR bits to temporarily halt the count. To restart the count after a temporary halt without clearing the counter, change the T2STP and T2STR bits from "11" to "01".

   The table below shows the timer states for each T2STP and T2STR bit setting, and the operation when the timer is started (T2STP and T2STR bits = "01") from each state.

T2STP	T2STR	Timer state	Timer operation when started (bit 1, 0 = "01") from this state
0	0	Count halted	Count starts after clearing the counter.
0	1	Count operating	Count continues.
1	0	Count halted	Count starts after clearing the counter.
1	1	Count temporarily halted	Count continues without clearing the counter.

2.2.6 A/D Converter

On being activated by software, the 8-bit successive approximation type A/D converter performs an 8-bit A/D conversion and stores the conversion result in the ADDH and ADDL registers.

The A/D converter has the following features.

◎ Conversion speed: 22 μs (for an 8-MHz source oscillation)

◎ Conversion completion can be detected by an interrupt or by software polling.

◎ Incorporates a sample/hold circuit.

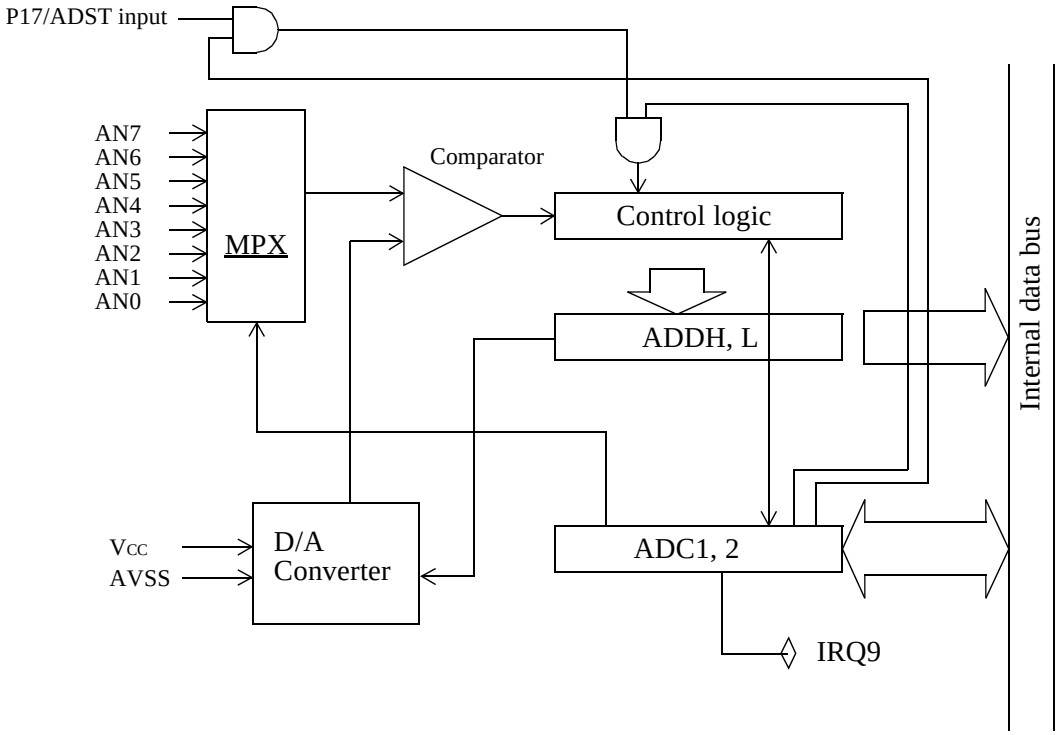
◎ Sense function (conversion speed = 6 μs) (for an 8-MHz source oscillation)

◎ Supports activation by an external input.

(1) Registers

	8 bits		
Address: 001EH	ADC1	R/W	AD control status register 1
Address: 001FH	ADC2	R/W	AD control status register 2
Address: 0020H	ADDH	R/W	ADC data register H
Address: 0021H	ADDL	R/W	ADC data register L

(2) Block Diagram



(3) Register Description

(3.1) ADC1 (A/D Converter Control Register 1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 001E$_H$	ANS3	ANS2	ANS1	ANS0	ADI	ADMV	SIFM	AD	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	(R/W)	

[Bits 7 to 4] ANS3 to ANS0: Analog input select bits

These four bits select the analog input. However, setting ANS3 to ANS0 to 1000$_B$ to 1111$_B$ is prohibited.

ANS3	ANS2	ANS2	ANS0	Selected channel	ANS3	ANS2	ANS1	ANS0	Selected channel
0	0	0	0	0	1	0	0	0	—
0	0	0	1	1	1	0	0	1	—
0	0	1	0	2	1	0	1	0	—
0	0	1	1	3	1	0	1	1	—
0	1	0	0	4	1	1	0	0	—
0	1	0	1	5	1	1	0	1	—
0	1	1	0	6	1	1	1	0	—
0	1	1	1	7	1	1	1	1	—

[Bit 3] ADI: Interrupt flag bit

This bit has the following meaning when read in A/D mode.

0	Conversion is not complete.
1	Conversion complete.

This bit has the following meaning when read in sense mode.

0	The condition specified by the SIFM bit is not satisfied.
1	The condition specified by the SIFM bit is satisfied.

An interrupt request is generated in both A/D and sense modes if this bit is set when ADIE (bit 3) of the ADC2 register is "1".

Writing to this bit has the following meaning in both A/D and sense modes.

0	Clear this bit.
1	No change. No effect on operation.

Read-modify-write instructions always read the bit as "1".

[Bit 2] ADMV: Conversion-in-progress flag

This flag indicates that A/D conversion is in progress.

0	No conversion in progress
1	Conversion in progress

[Bit 1] SIFM: Interrupt source setting bit

This bit sets the source for generating an interrupt in sense mode.

0	Generate an interrupt if (analog input voltage) < (data register value)
1	Generate an interrupt if (analog input voltage) > (data register value)

[Bit 0] AD: A/D conversion start bit

Writing "1" to this bit when EXT (bit 1) of the ADC2 register is "0" starts A/D conversion in both A/D and sense modes. Writing "0" to this bit has no meaning. Reading the bit always returns "0". Writing to the bit has the following meaning.

0	Halt A/D conversion.
1	Start A/D conversion (if EXT (bit 1) of ADC2 is "0").

(3.2) ADC2 (A/D Converter Control Register 2)

This register is used for status indication and control of the A/D converter.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 001F$_H$	—	—	—	ADCK	ADIE	ADMD	EXT	TEST	---00001$_B$
				(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 4] ADCK: A/D converter activation trigger bit

This bit selects the A/D converter activation trigger.

0	No change
1	Start conversion on the rising edge of the P17/ADST input.

To use P17 as an external input, set P17 as an input in the DDR.

[Bit 3] ADIE: Interrupt enable bit

This bit specifies whether interrupts are enabled or disabled.

0	Disable interrupts
1	Enable interrupts

[Bit 2] ADMD: Function selection bit

This bit switches between A/D mode and sense mode.

0	A/D mode
1	Sense mode

[Bit 1] EXT: Continuous conversion activation enable bit

This bit enables continuous conversion activation by the A/D converter clock.

0	Start by setting AD (bit 0) in ADC1.
1	Start on the rising edge of the clock specified by ADCK (bit 4) of ADC2.

[Bit 0] TEST: Test bit

This bit is only used for testing. Always write "1" to this bit. Reading the bit always returns "1".

(3.3) ADDH and ADDL (A/D Result Registers)

In A/D mode, these registers store the A/D conversion result.

In sense mode, write the compare value to these registers in advance.

ADDH contains the upper 2 bits and bits 7 to 2 of ADDL contain the lower 6 bits.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0020H	—	—	—	—	—	—	7	6	000000XXB
							(R/W)	(R/W)	

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0021H	5	4	3	2	1	0	—	—	XXXXXX00B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)			

In A/D mode, the A/D conversion result is stored in these registers when A/D conversion completes. As the register contents become undefined once A/D conversion starts, only read the registers after conversion completes.

In sense mode, the value written to these registers prior to starting the sense operation is used as the compare value. Reading the registers has no meaning.

Do not write to these registers while conversion is in progress in either A/D or sense mode.

(4) Operation

(4.1) A/D Mode

a. Activation

Write "0" to ADMD (bit 2) of the ADC2 register to set A/D mode, then write "1" to AD (Bit 0) of the ADC1 register to start conversion. If EXT (bit 1 of ADC2) is "1", conversion is activated on the rising edge on the clock selected by ADCK (bit 4 of ADC2).

b. Restarting

A/D conversion can be restarted, even if a conversion is already in progress through the activation.

c. Ending conversion

Provided that it is not restarted, A/D conversion completes 22 μs (44 instruction cycles with an 8-MHz source oscillation) after starting. On completion, ADI (bit 3) of ADC1 is set. An interrupt request is generated at this time if ADIE (bit 3 of ADC2) is "1".

(4.2) Sense Mode

Sense mode compares the analog voltage at the input port with the voltage value specified by the program.

a. Activation

Write "1" to ADMD (bit 2) of the ADC2 register to set sense mode, then write "1" to AD (Bit 0) of the ADC1 register to start conversion. If EXT (bit 1 of ADC2) is "1", conversion is activated on the rising edge on the clock selected by ADCK (bit 4 of ADC2).

b. Result

The A/D converter compares the analog voltage at the input port with the voltage value specified by the program and sets ADI (bit 3 of ADC1) if the condition specified by SIFM (bit 1 of ADC1) is satisfied. An interrupt request is generated at this time if ADIE (bit 3 of ADC2) is '1".

c. Ending conversion

In sense mode, the interrupt flag (ADI) is not set on completion. Whether or not the sense function has completed can be determined by checking whether ADMV (bit 2 of ADC1) is '0".

(5) Cautions on Using the A/D Converter

a. Clear the ADI interrupt flag (bit 3 of ADC1) when switching between A/D and sense mode.

b. Do not switch between A/D and sense mode when conversion is in progress.

c. In A/D mode, the contents of ADDL and ADDH become invalid immediately after starting A/D conversion. Therefore, take care not to read the register values during conversion. After conversion completes, ADDL and ADDH maintain their values until the next conversion is started.

d. Conversion cannot be activated by AD (bit 0 of ADC1) when EXT (bit 1 of ADC2) is set to "1" (continuous conversion enabled). Do not change the ADCK (bit 4 of ADC2) value when EXT (bit 1 of ADC2) is set to "1" (continuous conversion enabled).

e. A/D conversion halts and all registers are initialized when a reset or stop occurs.

f. Do not change the analog channel while conversion is in progress. In particular, when performing continuous conversion, disable continuous conversion (set EXT (bit 1 of ADC2) to "0") and wait until ADMV (bit 2 of ADC1) goes to "0" before changing the channel.

g. The analog channel can be changed at the same time as restarting conversion. (ANS2 to ANS0 can be changed when writing "1" to AD. However, do not do this when performing continuous conversion.)

h. Do not change SIFM while conversion is in progress. In particular, when performing continuous conversion, disable continuous conversion (set EXT to "0") and wait until ADMV goes to "0" before changing SIFM.

i. SIFM can be changed at the same time as restarting conversion using AD.

j. Use input pulses longer than 22 μs (44 instruction cycles with an 8 MHz source oscillation) when using the P17/ADST input as a continuous conversion trigger for the A/D converter.

(6) Cautions on Program Development

Take note of the following points when developing programs for the MB89143A/4A on the MB89PV140 or MB89P147.

a. The MB89143A/4A has 8-bit resolution but the MB89PV140 and MB89P147 have 10-bit resolution. A right shift operation is required to convert from 10-bit to 8-bit resolution.

b. Parameters such as sampling time can be set in a register in the MB89PV140 and MB89P147. This is not supported by the MB89143A/4A.

c. The sampling times for the MB89PV140, MB89P147, and MB89143A/4A are different. If you are using an interrupt, for example, to notify completion of A/D conversion, the interrupt generation timings will be different.

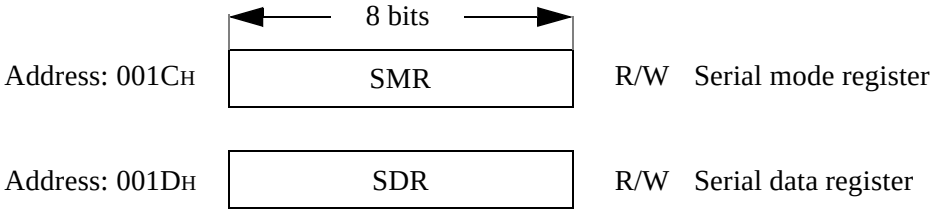
2.2.7 8-Bit Serial I/O

◎ Serial I/O supports clock synchronous 8-bit serial data transfer.

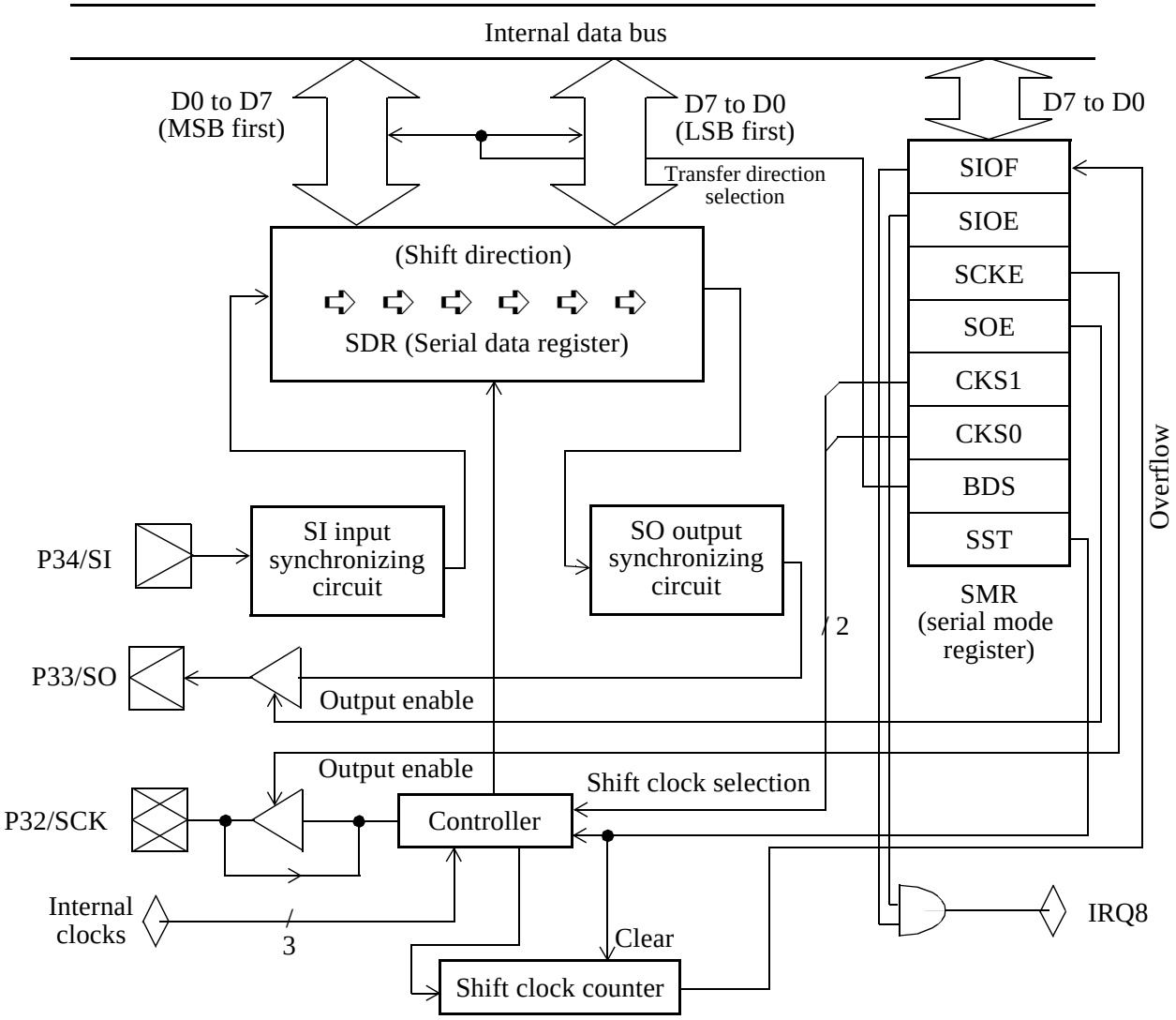
◎ LSB-first or MSB-first data transfer can be selected.

◎ Four different shift clock modes are available (three internal and one external).

(1) Registers



(2) Block Diagram



(3) Register Description

(3.1) SMR (Serial Mode Register)

The serial I/O control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 001C$_H$	SIOF	SIOE	SCKE	SOE	CKS1	CKS0	BDS	SST	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] SIOF: Serial I/O interrupt request flag

This flag indicates the state of serial I/O transfer. Reading has the following meaning.

0	Serial data transfer is not complete.
1	Serial data transfer is complete.

Read-modify-write instructions always read the bit as "1".

An interrupt request to the CPU is generated when this bit is set if interrupts are enabled (SIOE = "1").

Writing has the following meaning.

0	Clear this bit.
1	Does not change the bit. No effect on operation.

Either this bit or SST (bit 0 of SMR) can be used to determine when transfer is complete.

[Bit 6] SIOE: Serial I/O interrupt enable bit

Enables serial I/O interrupt requests.

0	Disable output of serial I/O interrupts.
1	Enable output of serial I/O interrupts.

[Bit 5] SCKE: Enable shift clock output bit

Controls the shift clock I/O pin.

0	General-purpose port (P32) or SCK input pin
1	SCK (shift clock) output pin

Always set P32/SCK as an input (set bit 2 of DDR3 to "0") if using the pin for the external clock.

[Bit 4] SOE: Serial data output enable bit

Controls the external serial I/O output pin.

0	General-purpose port pin (P33)
1	SO (serial data) output pin

Always set P34/SI as an input (set bit 4 of DDR3 to "0") if using the pin as the SI pin.

[Bits 3 and 2] CKS1, CKS0: Shift clock select bits

These bits select the serial shift clock mode.

CKS1	CKS0	Mode	SCK
0	0	Internal shift clock mode (4 instruction cycles)	Output
0	1	Internal shift clock mode (8 instruction cycles)	Output
1	0	Internal shift clock mode (16 instruction cycles)	Output
1	1	External shift clock mode (SCK)	Input

[Bit 1] BDS: Transfer direction select bit

This bit selects whether to transfer serial data with the least significant bit (LSB) first or most significant bit (MSB) first.

0	LSB-first
1	MSB-first

Note that changing this bit after writing data to SDR invalidates the data.

[Bit 0] SST: Serial I/O transfer start bit

The serial I/O transfer start bit. Automatically cleared to "0" when transfer is complete.

0	Halt serial I/O transfer.
1	Start serial I/O transfer.

Check that transfer has halted (SST = "0") before staring the next transfer.

(3.2) SDR (Serial Data Register)

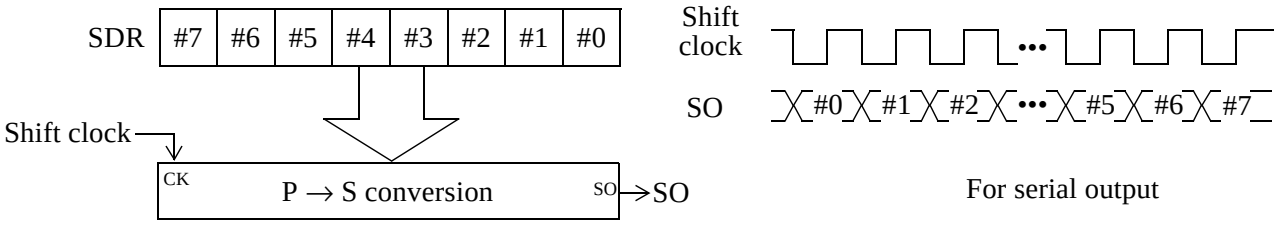
The 8-bit serial data register stores the serial I/O transfer data. Do not write to this register during serial I/O operation.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 001D$_H$									XXXXXXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

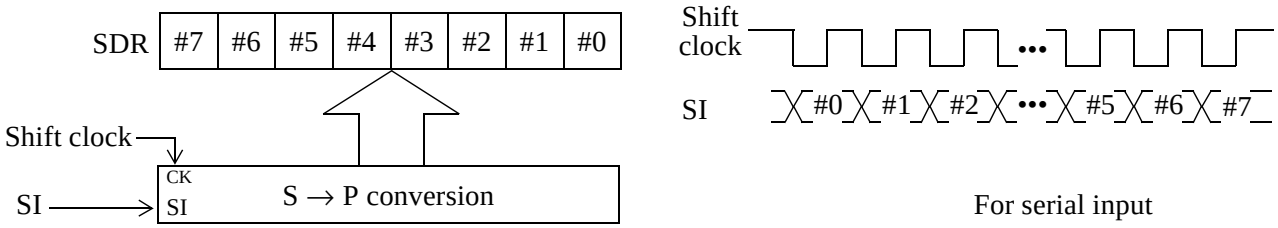
(4) Operation

(4.1) Overview

This module contains a serial mode register (SMR) and serial data register (SDR). For serial output, the SDR bits are sequentially output to the serial output pin (SO), synchronized with the falling edge of the serial shift clock generated from the internal or external clock. For serial input, bits are sequentially input from the serial input pin (SI) to the SDR on the rising edge of the serial shift clock.



For serial output



For serial input

(4.2) Operating Modes

The serial I/O operating mode is determined by the shift clock selection in the SMR. Three internal shift clock modes and one external shift clock mode are available. Change modes or perform clock selection only when the serial I/O is halted (SST (bit 0) of SMR = "0").

a. Internal shift clock mode

   Serial I/O operates using an internal clock and the shift clock is output from the SCK pin as the synchronous timing output. The clock output has a 50% duty ratio. One data bit is transferred for each clock cycle.

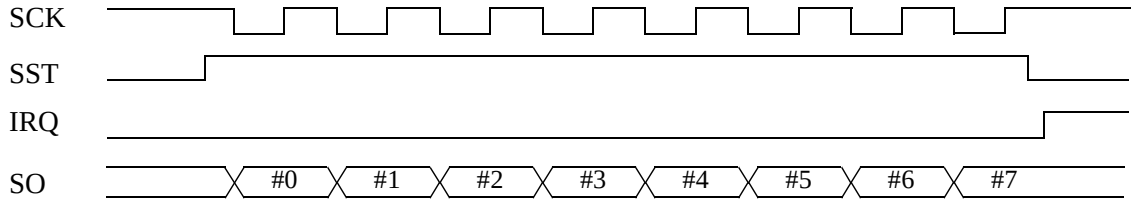
b. External shift clock mode

   One data bit is transferred for each clock cycle. Transfer is synchronized by the external shift clock input from the SCK pin. The transfer speed can range from DC to 8 clock cycles (1.00 MHz for an 8-MHz source oscillation).

   Whichever mode is used, do not write to SMR or SDR while serial I/O is operating.

(4.3) Interrupt Function

This module can generate interrupt requests to the CPU. An interrupt request is generated when the interrupt flag SIOF (bit 7) of SMR is set on completion of an 8-bit data transfer after interrupts have been enabled by setting SIOE (bit 6) of SMR to "1".

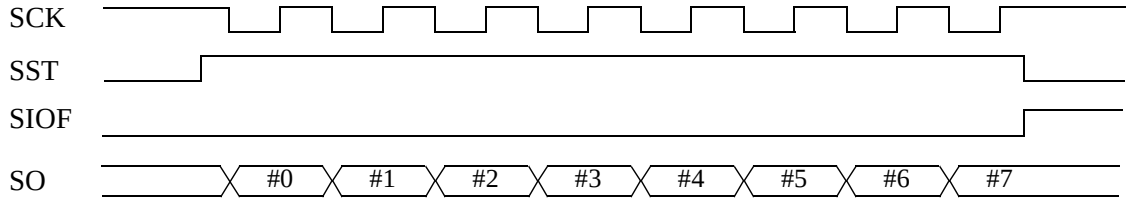


(4.4) Start and Stop Timing of the Shift Operation

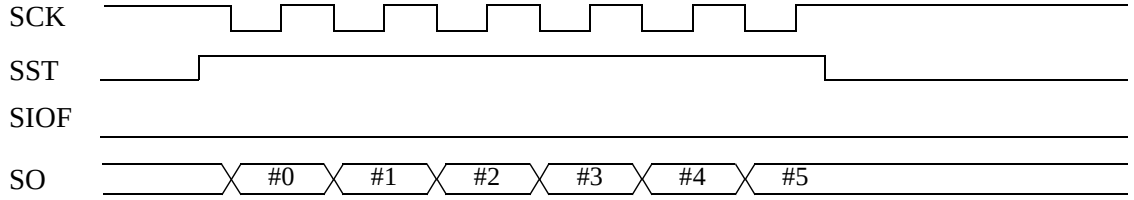
Writing "1" to SST (bit 0) of SMR starts transfer and writing "0" halts transfer. Also, SST is automatically cleared to "0" to halt the shift operation when data transfer completes.

a. Internal shift clock mode (LSB-first)

(When transfer completes)

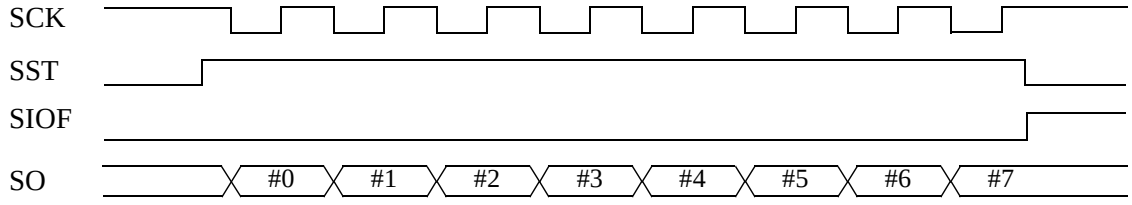


(When transfer is halted before completion)

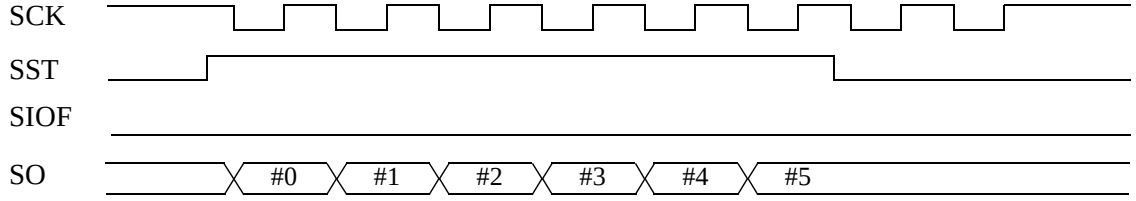


b. External shift clock mode (LSB-first)

(When transfer completes)



(When transfer is halted before completion)



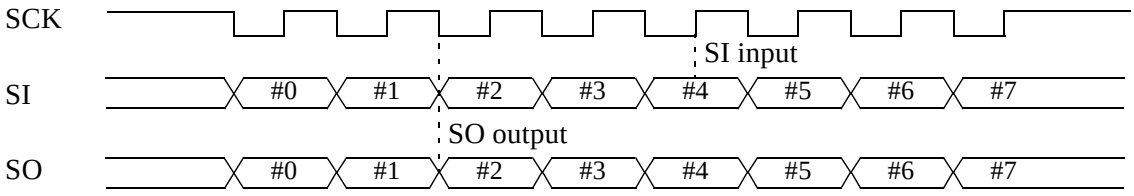
* However, if data is written to the SDR, the output data changes on the falling edge of the external clock.

Figure 2.2.23 Start and Stop Timing of the Shift Operation

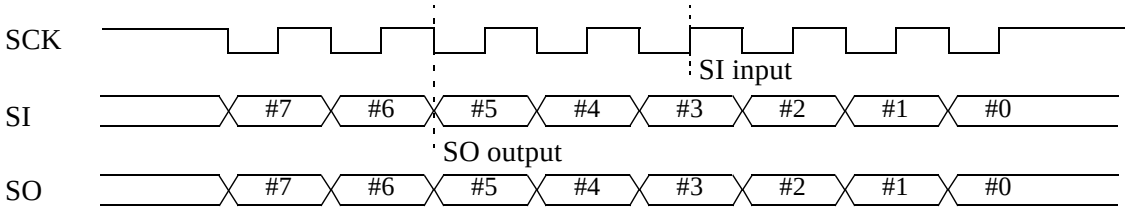
(4.5) Input and Output Shift Timing

Data is output from the serial output pin (SO) on the falling edge of the shift clock and data is input from the serial input pin (SI) on the rising edge of the shift clock.

a. LSB-first (BDS = "0")



b. MSB-first (BDS = "1")



DI7 to DI0 are input data and DO7 to DO0 are output data.

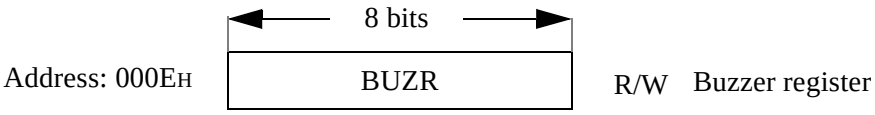
Figure 2.2.24 Input and Output Shift Timing

2.2.8 Buzzer Output

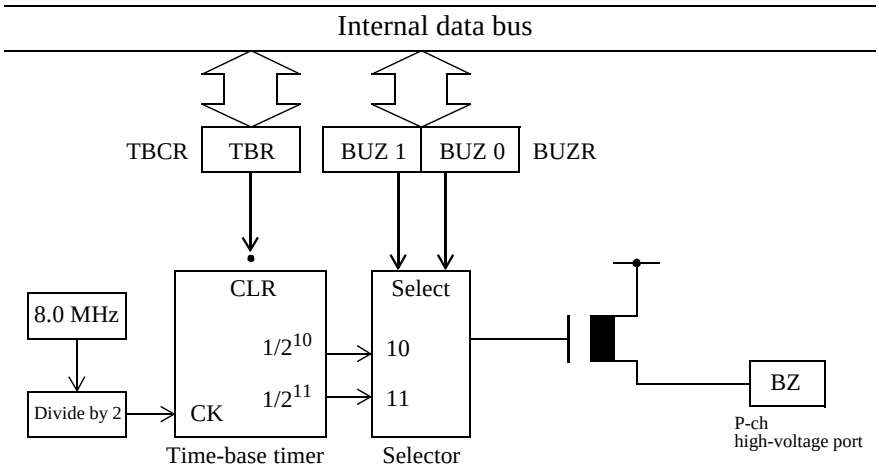
◎ Can be used for applications such as sounding a buzzer to confirm key input.

◎ Two different output frequencies are available via a register setting.

(1) Register



(2) Block Diagram



(3) Register Description

BUZR (Buzzer Register)

A 2-bit register that sets the output frequency and pin state for the buzzer pin.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 000EH	—	—	—	—	—	—	BUZ1	BUZ0	------00B
							(R/W)	(R/W)	

[Bit 1, Bit 0] BUZ1, BUZ0: Buzzer selection bits

These bits are used to both enable buzzer output and select the frequency. Setting the bits to "00" disables buzzer output. Other settings select the frequencies listed in the table below.

Table 2.1.4 Buzzer Output Frequency

BUZ1	BUZ0	Buzzer output frequency	For an 8-MHz source oscillation
0	0	High impedance	—
0	1	Set (H)	—
1	0	$F_C/2^{11}$	3.91 kHz
1	1	$F_C/2^{12}$	1.95 kHz

F_C: Main clock frequency

(4) Operation

The buzzer circuit outputs a signal that can be used for applications such as sounding a confirmation tone. The buzzer register enables buzzer output and sets the frequency.

Setting "00" to the BUZR register sets the output to "Hi-Z" and setting "01" sets the output to the "H" level. Setting the BUZR register to "10" or "11" outputs a square wave with the frequency listed in the above table.

When the buzzer output frequency set in the BUZR register is being output to the buzzer pin, switch settings when both the $F_C/2^{11}$ and $F_C/2^{12}$ outputs from the time-base timer are "L".

(5) Note on Using the Buzzer Output

As the buzzer output uses a signal from the time-base timer, clearing the time-base timer affects the buzzer output. Switching the buzzer output frequency is also affected by the time-base timer.

The buzzer output always starts from the "Hi-Z" state and ends in the "Hi-Z" state. Therefore, the result of changing the BUZR register is not reflected in the buzzer output pin immediately. This also applies in cases such as changing from buzzer output to "H" output or from "Hi-Z" output to "H" output.

A maximum of 384 μs (when operating at 8-MHz) can pass between setting the BUZR register and the actual change occurring in the buzzer output.

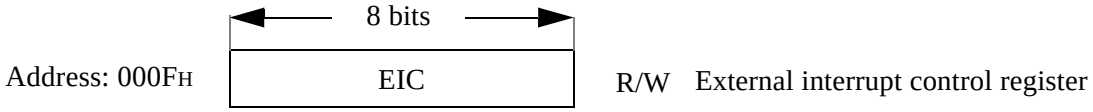
2.2.9 External Interrupt Circuit

◎ This circuit sets the corresponding flag when it detects an edge on one of the two external interrupt source (INT0 and INT1).

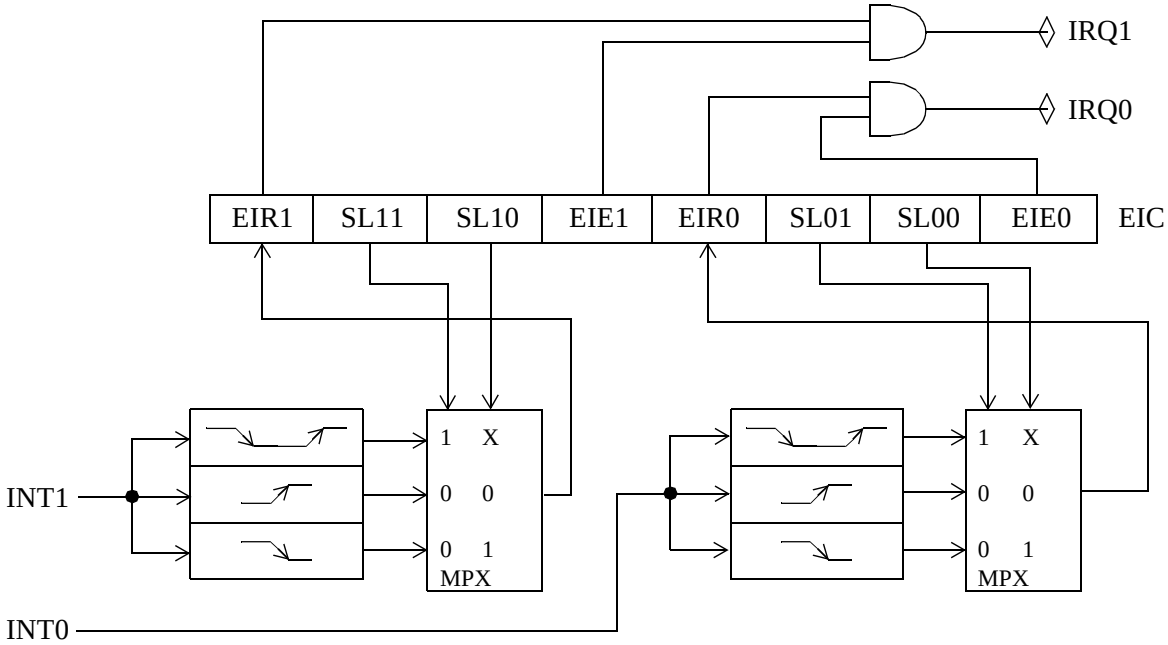
◎ An interrupt can be generated at the same time as the flag is set.

◎ Either of the two interrupts can be used to recover from stop or sleep mode.

(1) Register



(2) Block Diagram



(3) Register Description

(3.1) EIC (External Interrupt Control Register)

This register controls interrupts from the IRQ pins.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 000F$_H$	EIR1	SL11	SL10	EIE1	EIR0	SL01	SL00	EIE0	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] EIR1: External interrupt request flag

This bit is set to "1" if the edge specified by the SL10 and SL11 bits is input to the INT1 pin. An interrupt request (IRQ1) is generated if EIE1 is "1" when this bit is set. Reading the bit has the following meaning.

0	The specified edge has not been input to the INT1 pin.
1	The specified edge has been input to the INT1 pin (generate IRQ1).

Read-modify-write instructions always read the bit as "1".

Writing to the bit has the following meaning.

0	Clear this bit.
1	Does not change the bit. No effect on operation.

[Bits 6 and 5] SL11 and SL10: Edge polarity mode selection bits

SL10 and SL11 control the input edge polarity mode for the INT1 pin.

SL11	SL10	External interrupt active edge selection
1	×	Both edges mode
0	1	Falling edge
0	0	Rising edge

[Bit 4] EIE1: Interrupt enable bit

External interrupt request enable bit for the INT1 pin.

0	Disable interrupt requests.
1	Enable interrupt requests when EIR1 is set.

[Bit 3] EIR0: External interrupt request flag

This bit is set to "1" if the edge specified by the SL00 and SL01 bits is input to the INT0 pin. An interrupt request (IRQ0) is generated if EIE0 is "1" when this bit is set. Reading the bit has the following meaning.

0	The specified edge has not been input to the INT0 pin.
1	The specified edge has been input to the INT0 pin (generate IRQ0).

Read-modify-write instructions always read the bit as "1".

Writing to the bit has the following meaning.

0	Clear this bit.
1	Does not change the bit. No effect on operation.

[Bits 2 and 1] SL01 and SL00: Edge polarity mode selection bits

SL00 and SL01 control the input edge polarity mode for the INT0 pin.

SL01	SL00	External interrupt active edge selection
1	×	Both edges mode
0	1	Falling edge
0	0	Rising edge

[Bit 0] EIE0: Interrupt enable bit

External interrupt request enable bit for the INT0 pin.

0	Disable interrupt requests.
1	Enable interrupt requests when EIR0 is set.

(4) Notes on Using External Interrupts

When enabling an interrupt after wake-up from a reset, always clear the interrupt flag at the same time. (An interrupt request is generated immediately if the interrupt flag (EIR1 or EIR0) is "1" when the interrupt is enabled.)

Chapter 3: Operation

3.1 Clock Generator

The MB89143A/4A has an internal system clock generator circuit. The clock is generated by connecting a crystal oscillator to the X0 and X1 pins. The internal clock can also be supplied by inputting an externally generated clock to the X0 pin. In this case, leave the X1 pin open.

The X0A and X1A pins are used for the sub-clock and operate in the same way as the X0 and X1 pins.

If the single clock option is selected, X0A functions as the P70 pin and X1A as the P71 pin.

Insert a feedback resistor between X0A and X1A if using a crystal oscillator.

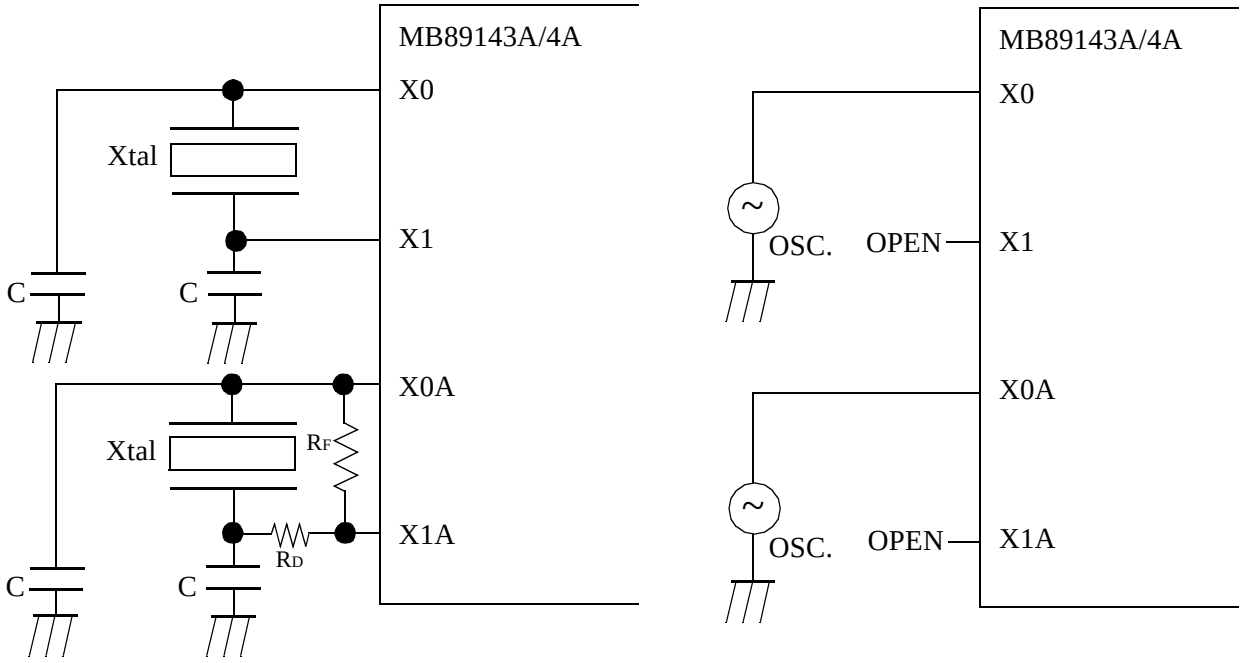


Figure 3.1.1 Clock Oscillator

3.2 Resets

3.2.1 Reset Operation

When a reset condition occurs, the MB89143A/4A aborts the currently executing instruction and changes to the reset state. The content of RAM does not change during a reset. However, if a reset occurs during writing of 16-bit data, it is possible that only the upper byte is written and the lower byte is lost. Also, if a reset occurs close to a write timing, the contents of the address being written to cannot be guaranteed.

The MB89143A/4A recovers from the reset when the reset condition is released. The MB89143A/4A reads the mode data from FFFDH, the upper byte of the reset vector from FFFEH, and the lower byte of the reset vector from FFFFH. After fetching the data in this order, the device starts operation. Figure 3.2.1 shows the flowchart.

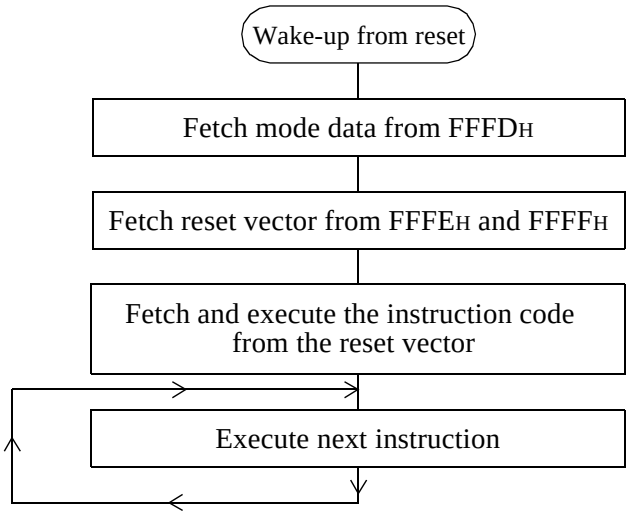
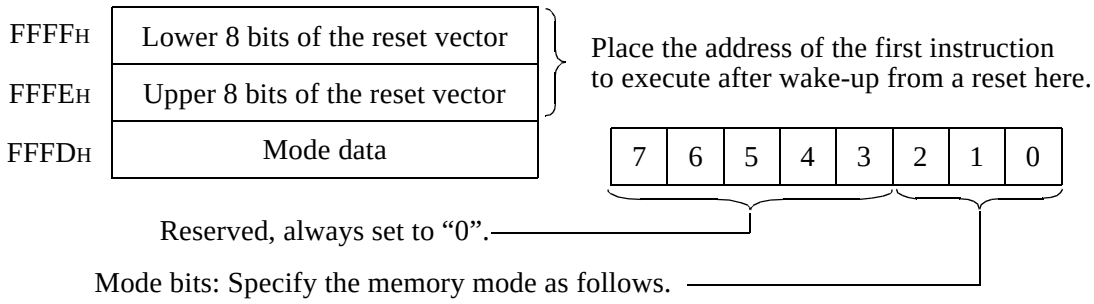


Figure 3.2.1 Summary of Reset Operation

Figure 3.2.2 shows the format of the data stored at FFFDH, FFFEH and FFFFH.



T2	T1	T0	Operation
0	0	0	External access prohibited (single-chip)
Other			Reserved. Do not use these settings.

Figure 3.2.2 Structure of the Reset Vector

3.2.2 Reset Conditions

The following conditions trigger a reset on the MB89143A/4A.

1. External pin reset : An "L" level applied to the $\overline{\text{RST}}$ pin.
2. Software reset : Writing "0" to the RST bit in the standby control register.
3. Turning on the power : Power-on reset
4. Reset triggered by the watchdog function : The watchdog function is enabled by the watchdog control register but the register is not accessed again within the specified time.

After a power-on reset or wake-up from a stop mode, operation does not start until after an oscillation stabilization time. See "(4.2) State Transition Diagram", "(4.3) Resets", or "(5.1) State Transition Diagram" in "2.1.5 Clock Controller" for details.

3.2.3 Cautions When Turning on the Power

Take note of the following points when turning on the power.

1. The state of the LSI (I/O ports, operating mode, etc.) is undefined immediately after applying the power supply and until the voltage rises to a sufficient level for the internal transistors to operate.
2. The state of the LSI (operating mode, etc.) is undefined immediately after applying the power supply and until the oscillation starts.
3. Hold the $\overline{\text{RST}}$ pin at the "L" level after applying the power supply and until the oscillation stabilizes (33 ms for 8-MHz operation). This keeps the device in the reset state.

Accordingly, if it is necessary to set the device to a fixed state with respect to the external system during this period, use an external circuit or similar to determine the state of the LSI.

3.2.4 Receiving an External Reset Signal

The $\overline{\text{RST}}$ pin has an internal analog noise filter to prevent misoperation due to noise. The reset signal output from the analog noise filter is sampled asynchronously when the signal inputs an "L" level. Sampling is synchronized with the internal clock when the signal inputs an "H" level.

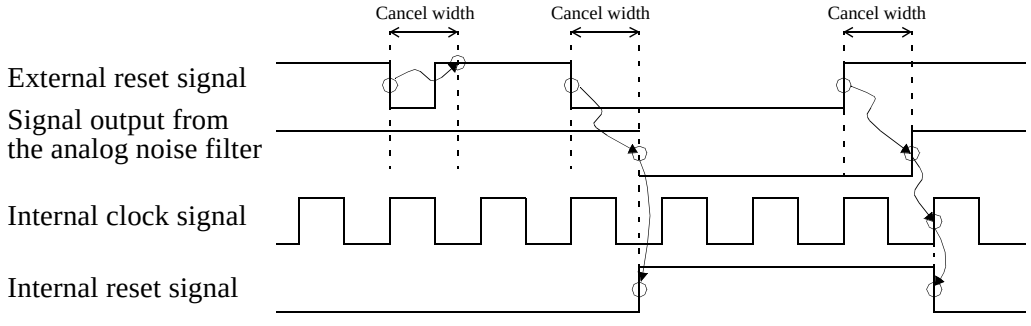


Figure 3.2.3 Receiving an External Reset Signal

3.3 Interrupts

When an interrupt request from an internal peripheral or external interrupt input occurs, the CPU temporarily halts operation for the currently executing instructions and executes the interrupt processing program if the interrupt controller and CPU are able to accept the interrupt. Figure 3.3.1 shows the flow of interrupt processing.

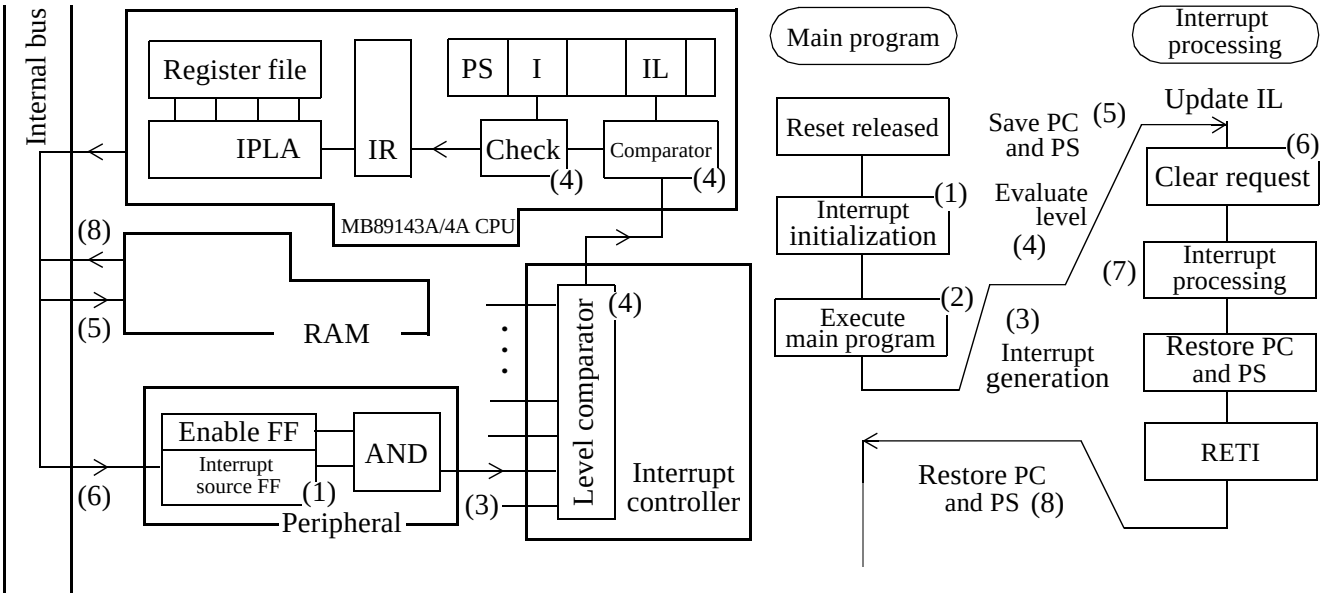


Figure 3.3.1 Flow of Interrupt Processing

As all interrupts are initially disabled, interrupts are first initialized in the main program (1). This initialization sets up each peripheral that generates an interrupt and sets the interrupt level registers (ILR1 to ILR3) in the interrupt controller corresponding to each interrupt. Using the interrupt level registers (ILR1 to ILR3) in the interrupt controller, an interrupt level can be set for each interrupt. The interrupt level can be set in the range 1 to 3, where level 1 is the highest priority and level 2 is the next highest priority. As level 3 indicates that the interrupt request is not generated, setting an interrupt to this level disables the interrupt request.

After setting up the peripheral, the main program executes the various control functions (2). If a peripheral generates an interrupt while the main program is executing (3), the interrupt controller identifies the highest priority interrupt of the interrupts generated at this timing and passes this interrupt to the CPU. The CPU receives the interrupt and checks the current interrupt level and I flag state (4), then starts interrupt processing.

CPU interrupt processing saves the current PC and PS contents on the stack (5), fetches the entry address for the interrupt processing program from the interrupt vector, updates the IL bits in the PS with the level of the current request, then starts execution of the interrupt processing routine.

The user interrupt processing routine clears the interrupt (6), performs the interrupt processing, then ends by executing the RETI instruction to restore the PC and PS contents from the stack (9). This returns execution to the interrupted instruction.

Note: Unlike the F^2MC-8, interrupts do not save A and T to the stack.

If interrupts with the same interrupt level occur simultaneously, the lower interrupt number (closest to IRQ0) has priority.

Table 3.3.1 lists the relationship between interrupt sources and interrupt vectors.

Table 3.3.1 Interrupt Sources and Interrupt Vectors

Interrupt source	Upper vector address	Lower vector address
IRQ0 (external interrupt 0)	FFFAH	FFFBH
IRQ1 (external interrupt 1)	FFF8H	FFF9H
IRQ2 (Unused)	FFF6H	FFF7H
IRQ3 (8/16-bit timer/counter)	FFF4H	FFF5H
IRQ4 (8/16-bit timer/counter)	FFF2H	FFF3H
IRQ5 (Unused)	FFF0H	FFF1H
IRQ6 (Unused)	FFEEH	FFEFH
IRQ7 (Unused)	FFECH	FFEDH
IRQ8 (8-bit serial I/O)	FFEAH	FFEBH
IRQ9 (A/D converter)	FFE8H	FFE9H
IRQA (Interval timer)	FFE6H	FFE7H
IRQB (Watch)	FFE4H	FFE5H

3.4 Low-power Consumption Modes

The MB89143A/4A has three standby modes for reducing current consumption: sleep mode, stop mode, and watch mode. The device changes to these modes by writing to the STBC (standby control register). See "2.1.5 Clock Controller" for details on setting and recovering from these modes.

The low-power consumption modes are different depending on which of the dual clock modes (main clock mode or sub-clock mode) is used on the MB89143A/4A. (See the state transition diagram in "2.1.5 Clock Controller" for details.)

The MB89143A/4A can operate as a single clock system if the single clock mask option is selected. However, the device cannot recover from sub-clock mode if only a single clock is used but the single clock mask option is not selected. Therefore, always select the single clock mask option if only using a single clock.

Table 3.4.1 Low-power Consumption Modes for Each Clock Mode

Function			Main Mode			Sub-Mode			
		Note	RUN	Sleep	Stop	RUN	Sleep	Stop	Watch
Main clock		—	Operating	Operating	Halted	Halted	Halted	Halted	Halted
Sub-clock		—	Operating	Operating	Operating	Operating	Operating	Halted	Operating
CPU	Instruction	○	Operating	Halted	Halted	Operating	Halted	Halted	Halted
	ROM	○	Operating	Hold	Hold	Operating	Hold	Hold	Hold
	RAM	○							
Peripherals	Ports	○	Operating	Hold	Hold	Operating	Hold	Hold	Hold
	Watch prescaler	×	Operating	Operating	Operating*1	Operating	Operating	Halted	Operating
	Time-base timer	×	Operating	Operating	Halted	Halted	Halted	Halted	Halted
	8/16-bit timer	○	Operating	Operating	Halted	Operating	Operating	Halted	Halted
	8-bit SIO	○	Operating	Operating	Halted	Operating	Operating	Halted	Halted
	8-bit A/DC	○	Operating	Operating	Halted	Operating*2	Operating*2	Halted	Halted
	External interrupts	○	Operating	Operating	Operating	Operating	Operating	Operating	Operating
	Buzzer output	×	Operating	Operating	Halted	Halted	Halted	Halted	Halted
	Watchdog	×	Operating	Halted	Halted	Operating*3	Halted	Halted	Halted

Notes: ○: Operating speed and related parameters depend on the clock mode (main or sub) and gear function.

×: Operating speed and related parameters are independent of the clock mode (main or sub) and gear function.

*1: The watch prescaler continues counting but does not generate watch interrupts.

*2: Can operate, but do not use.

*3: When the watch prescaler is used as the clock source.

3.5 Pin States during Sleep, Stop, Watch, and Reset Modes

The MB89143A/4A pins go to the following states during sleep, stop, watch, or reset mode.

1. Sleep mode : Pins set as port outputs maintain their states prior to entering sleep mode. The state of output pins used by resources depends on the resource setting. All input pins continue to function as inputs.
2. Stop mode : If bit 5 of STBC (standby control register) is set to "0" at the same time as entering stop mode, all output pins maintain their states prior to entering stop mode.

   If bit 5 of STBC (standby control register) is set to "1", output pins go to high impedance and pins with the pull-up option selected go to "H". Input pins maintain their states prior to entering stop mode or are tied to "L" internally.
3. Watch mode : If bit 5 of STBC (standby control register) is set to "0" at the same time as entering watch mode, all output pins maintain their states prior to entering watch mode. If bit 5 of STBC (standby control register) is set to "1", output pins go to high impedance and input pins maintain their states prior to entering watch mode or are tied to "L" internally.
4. Reset : In normal use, all I/O pins and resource pins go to high impedance.

The following page lists the pin states for each mode in detail.

Pin State Details

<table>
<tr><th rowspan="3">Pin name</th><th colspan="4">Main Mode</th><th colspan="4">Sub-Mode</th><th colspan="2" rowspan="2">Watch</th><th rowspan="3">During a Reset</th></tr>
<tr><th rowspan="2">RUN</th><th rowspan="2">Sleep</th><th colspan="2">Stop</th><th rowspan="2">RUN</th><th rowspan="2">Sleep</th><th colspan="2">Stop</th></tr>
<tr><th>SPL=0</th><th>SPL=1</th><th>SPL=0</th><th>SPL=1</th><th>SPL=0</th><th>SPL=1</th></tr>
<tr><td>X0</td><td colspan="2">Oscillator input</td><td colspan="6">High impedance*1</td><td>Oscillator input</td></tr>
<tr><td>X1</td><td colspan="2">Oscillator output</td><td colspan="6">"H" output</td><td>Oscillator output</td></tr>
<tr><td>X0A</td><td colspan="5">Oscillator input</td><td colspan="2">High impedance*1</td><td colspan="3">Oscillator input</td></tr>
<tr><td>X1A</td><td colspan="5">Oscillator output</td><td colspan="2">"H" output</td><td colspan="3">Oscillator output</td></tr>
<tr><td>MODA</td><td colspan="10">Mode input</td></tr>
<tr><td>$\overline{\text{RST}}$</td><td colspan="9">Reset input</td><td>Reset input*2</td></tr>
<tr><td rowspan="3">P37 to P30,
P17 to P10,
P07 to P00,
P23 to P20</td><td colspan="2">Port inputs</td><td colspan="2">Remain as inputs</td><td colspan="2">Port inputs</td><td colspan="4">Remain as inputs</td><td rowspan="3">High impedance</td></tr>
<tr><td>Port outputs</td><td>Maintain current output</td><td rowspan="2">Maintain current output</td><td rowspan="2">Output High impedance*1</td><td>Port outputs</td><td>Maintain current output</td><td rowspan="2">Maintain current output</td><td rowspan="2">Output High impedance*1</td><td rowspan="2">Maintain current output</td><td rowspan="2">Output High impedance*1</td></tr>
<tr><td colspan="2">Resource I/O</td><td colspan="2">Resource I/O</td></tr>
<tr><td rowspan="3">P31/INT1 to
P30/INT0</td><td colspan="2">Port inputs</td><td colspan="2">Remain as inputs</td><td colspan="2">Port inputs</td><td colspan="4">Remain as inputs</td><td rowspan="3">High impedance</td></tr>
<tr><td>Port outputs</td><td>Maintain current output</td><td>Maintain current output</td><td>Output High impedance*1</td><td>Port outputs</td><td>Maintain current output</td><td>Maintain current output</td><td>Output High impedance*1</td><td>Maintain current output</td><td>Output High impedance*1</td></tr>
<tr><td colspan="10">External interrupt inputs (resource inputs)*5</td></tr>
<tr><td>P47 to P40,
P57 to P50,
P67 to P60</td><td colspan="3">Port outputs</td><td>Output High impedance*1</td><td colspan="3">Port outputs</td><td>Output High impedance*1</td><td>Port outputs</td><td>Output High impedance*1</td><td>High impedance</td></tr>
<tr><td>P71, P70*3</td><td colspan="4">Port inputs*4</td><td colspan="6"></td><td>High impedance</td></tr>
<tr><td>BZ</td><td colspan="2">Buzzer output</td><td>Maintain current output</td><td>High impedance</td><td colspan="2">Buzzer output</td><td>Maintain current output</td><td>High impedance</td><td>Maintain current output</td><td>High impedance</td><td>High impedance</td></tr>
</table>

*1: The input level is fixed to prevent leakage due to the input being open.

*2: Outputs "L" during the oscillation stabilization time for a power-on reset.

*3: When the single clock option is selected. If the dual clock option is selected, these pins operate in the same way as X0 and X1.

*4: Fix the input to "H" or "L".

*5: Ensure that an intermediate level is not input to P30/INT0 and P31/INT1.

Chapter 4: Instructions

4.1 Instructions

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists the symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir : b	Bit direct address (8 : 3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of the accumulator A (8 bits)
AL	Lower 8 bits of the accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of the temporary accumulator T (8 bits)
TL	Lower 8 bits of the temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

Table 1 Instruction Symbols *(continued)*

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (3 bits, i = 1 to 7)
✕	Indicates that the very ✕ is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(✕)	Indicates that the contents of ✕ is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((✕))	The address indicated by the contents of ✕ is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembly notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, and AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "-" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

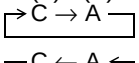
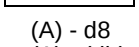
Example: 48 to 4F ← This indicates 48, 49, ..., 4F.

4.2 Transfer Instructions

No.	Mnemonic	~	#	Operation	TL	TH	AH	N	Z	V	C	OP code
1	MOV dir,A	3	2	(dir) ← (A)	-	-	-	-	-	-	-	45
2	MOV @IX+off,A	4	2	((IX)+off) ← (A)	-	-	-	-	-	-	-	46
3	MOV ext,A	4	3	(ext) ← (A)	-	-	-	-	-	-	-	61
4	MOV @EP,A	3	1	((EP)) ← (A)	-	-	-	-	-	-	-	47
5	MOV Ri,A	3	1	(Ri) ← (A)	-	-	-	-	-	-	-	48 to 4F
6	MOV A,#d8	2	2	(A) ← d8	AL	-	-	+	+	-	-	04
7	MOV A,dir	3	2	(A) ← dir	AL	-	-	+	+	-	-	05
8	MOV A,@IX+off	4	2	(A) ← ((IX)+off)	AL	-	-	+	+	-	-	06
9	MOV A,ext	4	3	(A) ← (ext)	AL	-	-	+	+	-	-	60
10	MOV A,@A	3	1	(A) ← ((A))	AL	-	-	+	+	-	-	92
11	MOV A,@EP	3	1	(A) ← ((EP))	AL	-	-	+	+	-	-	07
12	MOV A,Ri	3	1	(A) ← (Ri)	AL	-	-	+	+	-	-	08 to 0F
13	MOV dir,#d8	4	3	(dir) ← d8	-	-	-	-	-	-	-	85
14	MOV @IX+off,#d8	5	3	((IX)+off) ← d8	-	-	-	-	-	-	-	86
15	MOV @EP,#d8	4	2	((EP)) ← d8	-	-	-	-	-	-	-	87
16	MOV Ri,#d8	4	2	(Ri) ← d8	-	-	-	-	-	-	-	88 to 8F
17	MOVW dir,A	4	2	(dir)←(AH), (dir+1)←(AL)	-	-	-	-	-	-	-	D5
18	MOVW @IX+off,A	5	2	((IX)+off)←(AH), ((IX)+off+1)←(AL)	-	-	-	-	-	-	-	D6
19	MOVW ext,A	5	3	(ext)←(AH), (ext+1)←(AL)	-	-	-	-	-	-	-	D4
20	MOVW @EP,A	4	1	((EP))←(AH), ((EP)+1)←(AL)	-	-	-	-	-	-	-	D7
21	MOVW EP,A	2	1	(EP) ← A)	-	-	-	-	-	-	-	E3
22	MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+	+	-	-	E4
23	MOVW A,dir	4	2	(AH)←(dir), (AL)←(dir+1)	AL	AH	dH	+	+	-	-	C5
24	MOVW A, @IX+off	5	2	(AH)←((IX)+off), (AL)←((IX)+off+1)	AL	AH	dH	+	+	-	-	C6
25	MOVW A,ext	5	3	(AH)←(ext), (AL)←(ext+1)	AL	AH	dH	+	+	-	-	C4
26	MOVW A,@A	4	1	(AH)←((A)), (AL)←((A)+1)	AL	AH	dH	+	+	-	-	93
27	MOVW A,@EP	4	1	(AH)←((EP)), (AL)←((EP)+1)	AL	AH	dH	+	+	-	-	C7
28	MOVW A,EP	2	1	(A) ← (EP)	-	-	dH	-	-	-	-	F3
29	MOVW EP,#d16	3	3	(EP) ← d16	-	-	-	-	-	-	-	E7
30	MOVW IX,A	2	1	(IX) ← (A)	-	-	-	-	-	-	-	E2
31	MOVW A,IX	2	1	(A) ← (IX)	-	-	dH	-	-	-	-	F2
32	MOVW SP,A	2	1	(SP) ← (A)	-	-	-	-	-	-	-	E1
33	MOVW A,SP	2	1	(A) ← (SP)	-	-	dH	-	-	-	-	F1
34	MOV @A,T	3	1	((A)) ← (T)	-	-	-	-	-	-	-	82
35	MOVW @A,T	4	1	((A)) ← (TH), ((A)+1) ← (TL)	-	-	-	-	-	-	-	83
36	MOVW IX,#d16	3	3	(IX) ← d16	-	-	-	-	-	-	-	E6
37	MOVW A,PS	2	1	(A) ← (PS)	-	-	dH	-	-	-	-	70
38	MOVW PS,A	2	1	(PS) ← (A)	-	-	-	+	+	+	+	71
39	MOVW SP,#d16	3	3	(SP) ← d16	-	-	-	-	-	-	-	E5
40	SWAP	2	1	(AH) ←→ (AL)	-	-	AL	-	-	-	-	10
41	SETB dir:n	4	2	(dir):n ← 1	-	-	-	-	-	-	-	A8 to AF
42	CLRB dir:n	4	2	(dir):]n ← 0	-	-	-	-	-	-	-	A0 to A7
43	XCH A,T	2	1	(AL) ←→ (TL)	AL	-	-	-	-	-	-	42
44	XCHW A,T	3	1	(A) ←→ (T)	AL	AH	dH	-	-	-	-	43
45	XCHW A,EP	3	1	(A) ←→ (EP)	-	-	dH	-	-	-	-	F7
46	XCHW A,IX	3	1	(A) ←→ (IX)	-	-	dH	-	-	-	-	F6
47	XCHW A,SP	3	1	(A) ←→ (SP)	-	-	dH	-	-	-	-	F5
48	MOVW A,PC	2	1	(A) ← (PC)	-	-	dH	-	-	-	-	F0

Notes:
- During byte transfer to A, T ← A is restricted to low bytes.
- Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F^2MC-8 family)
- "~" indicates the number of instruction cycles and "#" indicates the number of instruction bytes.

4.3 Arithmetic Operation Instructions

No.	Mnemonic	~	#	Operation	TL	TH	AH	N	Z	V	C	OP code
1	ADDC A,Ri	3	1	(A) ← (A)+(Ri)+C	-	-	-	+	+	+	+	28 to 2F
2	ADDC A,#d8	2	2	(A) ← (A)+d8+C	-	-	-	+	+	+	+	24
3	ADDC A,dir	3	2	(A) ← (A)+(dir)+C	-	-	-	+	+	+	+	25
4	ADDC A,@IX+off	4	2	(A) ← (A)+((IX)+off)+C	-	-	-	+	+	+	+	26
5	ADDC A,@EP	3	1	(A) ← (A)+((EP))+C	-	-	-	+	+	+	+	27
6	ADDCW A	3	1	(A) ← (A)+(T)+C	-	-	dH	+	+	+	+	23
7	ADDC A	2	1	(AL) ← (AL)+(TL)+C	-	-	-	+	+	+	+	22
8	SUBC A,Ri	3	1	(A) ← (A)-(Ri)-C	-	-	-	+	+	+	+	38 to 3F
9	SUBC A,#d8	2	2	(A) ← (A)-d8-C	-	-	-	+	+	+	+	34
10	SUBC A,dir	3	2	(A) ← (A)-(dir)-C	-	-	-	+	+	+	+	35
11	SUBC A,@IX+off	4	2	(A) ← (A)-((IX)+off)-C	-	-	-	+	+	+	+	36
12	SUBC A,@EP	3	1	(A) ← (A)-((EP))-C	-	-	-	+	+	+	+	37
13	SUBCW A	3	1	(A) ← (T)-(A)-C	-	-	dH	+	+	+	+	33
14	SUBC A	2	1	(AL) ← (TL)-(AL)-C	-	-	-	+	+	+	+	32
15	INC Ri	4	1	(Ri) ← (Ri)+1	-	-	-	+	+	+	-	C8 to CF
16	INCW EP	3	1	(EP) ← (EP)+1	-	-	-	-	-	-	-	C3
17	INCW IX	3	1	(IX) ← (IX)+1	-	-	-	-	-	-	-	C2
18	INCW A	3	1	(A) ← (A)+1	-	-	dH	+	+	-	-	C0
19	DEC Ri	4	1	(Ri) ← (Ri)-1	-	-	-	+	+	+	-	D8 to DF
20	DECW EP	3	1	(EP) ← (EP)-1	-	-	-	-	-	-	-	D3
21	DECW IX	3	1	(IX) ← (IX)-1	-	-	-	-	-	-	-	D2
22	DECW A	3	1	(A) ← (A)-1	-	-	dH	+	+	-	-	D0
23	MULU A	19	1	(A) ← (AL)*(TL)	-	-	dH	-	-	-	-	01
24	DIVU A	21	1	(A) ← (T)/(AL), MOD → (T)	dL	00	00	-	-	-	-	11
25	ANDW A	3	1	(A) ← (A) ∧ (T)	-	-	dH	+	+	R	-	63
26	ORW A	3	1	(A) ← (A) ∨ (T)	-	-	dH	+	+	R	-	73
27	XORW A	3	1	(A) ← (A) ∀ (T)	-	-	dH	+	+	R	-	53
28	CMP A	2	1	(TL) - (AL)	-	-	-	+	+	+	+	12
29	CMPW A	3	1	(T) - (A)	-	-	-	+	+	+	+	13
30	RORC A	2	1		-	-	-	+	+	-	+	03
31	ROLC A	2	1		-	-	-	+	+	-	+	02
32	CMP A,#dB	2	2	(A) - d8	-	-	-	+	+	+	+	14
33	CMP A,dir	3	2	(A) - (dir)	-	-	-	+	+	+	+	15
34	CMP A,@EP	3	1	(A) - ((EP))	-	-	-	+	+	+	+	17
35	CMP A,@IX+off	4	2	(A) - ((IX)+off)	-	-	-	+	+	+	+	16
36	CMP A,Ri	3	1	(A) - (Ri)	-	-	-	+	+	+	+	18 to 1F
37	DAA	2	1	decimal adjust for addition	-	-	-	+	+	+	+	84
38	DAS	2	1	decimal adjust for subtraction	-	-	-	+	+	+	+	94
39	XOR A	2	1	(A) ← (AL) ∀ (TL)	-	-	-	+	+	R	-	52
40	XOR A,#d8	2	2	(A) ← (AL) ∀ d8	-	-	-	+	+	R	-	54
41	XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	-	-	-	+	+	R	-	55
42	XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	-	-	-	+	+	R	-	57
43	XOR A,@IX+off	4	2	(A) ← (AL) ∀ ((IX)+off)	-	-	-	+	+	R	-	56
44	XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	-	-	-	+	+	R	-	58 to 5F
45	AND A	2	1	(A) ← (AL) ∧ (TL)	-	-	-	+	+	R	-	62
46	AND A,#d8	2	2	(A) ← (AL) ∧ d8	-	-	-	+	+	R	-	64
47	AND A,dir	3	2	(A) ← (AL) ∧ (dir)	-	-	-	+	+	R	-	65
48	AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	-	-	-	+	+	R	-	67
49	AND A,@IX+off	4	2	(A) ← (AL) ∧ ((IX)+off)	-	-	-	+	+	R	-	66
50	AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	-	-	-	+	+	R	-	68 to 6F
51	OR A	2	1	(A) ← (AL) ∨ (TL)	-	-	-	+	+	R	-	72
52	OR A,#d8	2	2	(A) ← (AL) ∨ d8	-	-	-	+	+	R	-	74
53	OR A,dir	3	2	(A) ← (AL) ∨ (dir)	-	-	-	+	+	R	-	75
54	OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	-	-	-	+	+	R	-	77
55	OR A,@IX+off	4	2	(A) ← (AL) ∨ ((IX)+off)	-	-	-	+	+	R	-	76

No.	Mnemonic	~	#	Operation	TL	TH	AH	N	Z	V	C	OP code
56	OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	-	-	-	+	+	R	-	78 to 7F
57	CMP dir,#d8	5	3	(dir) - d8	-	-	-	+	+	+	+	95
58	CMP @EP,#d8	4	2	((EP)) - d8	-	-	-	+	+	+	+	97
59	CMP @IX+off,#d8	5	3	((IX)+off) - d8	-	-	-	+	+	+	+	96
60	CMP Ri,#d8	4	2	(Ri) - d8	-	-	-	+	+	+	+	98 to 9F
61	INCW SP	3	1	(SP) ← (SP) + 1	-	-	-	-	-	-	-	C1
62	DECW SP	3	1	(SP) ← (SP) - 1	-	-	-	-	-	-	-	D1

4.4 Branch Instructions

No.	Mnemonic	~	#	Operation	TL	TH	AH	N	Z	V	C	OP code
1	BZ/BEQ rel	3	2	if Z=1 then PC←PC+rel	-	-	-	-	-	-	-	FD
2	BNZ/BNE rel	3	2	if Z=0 then PC←PC+rel	-	-	-	-	-	-	-	FC
3	BC/BLO rel	3	2	if C=1 then PC←PC+rel	-	-	-	-	-	-	-	F9
4	BNC/BHS rel	3	2	if C=0 then PC←PC+rel	-	-	-	-	-	-	-	F8
5	BN rel	3	2	if N=1 then PC←PC+rel	-	-	-	-	-	-	-	FB
6	BP rel	3	2	if N=0 then PC←PC+rel	-	-	-	-	-	-	-	FA
7	BLT rel	3	2	if V∀N=1 then PC←PC+rel	-	-	-	-	-	-	-	FF
8	BGE rel	3	2	if V∀N=0 then PC←PC+rel	-	-	-	-	-	-	-	FE
9	BBC dir:b,rel	5	3	if (dir:b)=0 then PC←PC+rel	-	-	-	-	+	-	-	B0 to B7
10	BBS dir:b,rel	5	3	if (dir:b)=1 then PC←PC+rel	-	-	-	-	+	-	-	B8 to BF
11	JMP @A	2	1	(PC)←(A)	-	-	-	-	-	-	-	E0
12	JMP ext	3	3	(PC)←ext	-	-	-	-	-	-	-	21
13	CALLV #vct	6	1	vector call	-	-	-	-	-	-	-	E8 to EF
14	CALL ext	6	3	subroutine call	-	-	-	-	-	-	-	31
15	XCHW A,PC	3	1	(PC)←(A), (A)←(PC)+1	-	-	dH	-	-	-	-	F4
16	RET	4	1	return from subroutine	-	-	-	-	-	-	-	20
17	RETI	6	1	return from interrupt	-	-	-	restore				30

4.5 Other Instructions

No.	Mnemonic	~	#	Operation	TL	TH	AH	N	Z	V	C	OP code
1	PUSHW A	4	1		-	-	-	-	-	-	-	40
2	POPW A	4	1		-	-	dH	-	-	-	-	50
3	PUSHW IX	4	1		-	-	-	-	-	-	-	41
4	POPW IX	4	1		-	-	-	-	-	-	-	51
5	NOP	1	1		-	-	-	-	-	-	-	00
6	CLRC	1	1		-	-	-	-	-	-	R	81
7	SETC	1	1		-	-	-	-	-	-	S	91
8	CLRI	1	1		-	-	-	-	-	-	-	80
9	SETI	1	1		-	-	-	-	-	-	-	90

F^{2}MC-8L Instruction Map

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir :0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir :1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir :2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir:3	BBC dir :3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir :4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir :5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	MOV @IX+d,A	XOR A,@IX+d	AND A,@IX+d	OR A,@IX+d	MOV @IX+d,#d8	CMP @IX+d,#d8	CLRB dir:6	BBC dir :6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:7	BBC dir :7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir :0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir :1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir :2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir :3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir :4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir :5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir :6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir :7,rel	INC R7	DEC R7	CALLV #7	BLT rel

Chapter 5:
Mask Options

No.	Part number	MB89143A MB89144A	MB89PV140		MB89P147V1
	Specifying procedure	Specify when ordering masking	101	102	Set with EPROM
1	Clock mode selection (Single clock mode (Dual clock mode	Selectable	Single clock mode	Dual clock mode	Selectable
2	Pull-up resistors (P14 to P17 (P32 to P37	Specify by pin	No	No	Specify by pin
3	Power-on reset (Yes (No	Yes	Yes	Yes	Selectable
4	Reset pin output (Yes (No	Selectable	Yes	Yes	Selectable
4	Pull-down resistors (P40 to P47 P50 to P57 (P60 to P67	No	No	No	No

Part numbers

Part number	SH-DIP64	QFP64
MB89143A MB89144A	MB89143AP MB89144AP	MB89143APF MB89144APF

Appendix 1:
I/O Map

(1.1) Addresses 00H to 17H

Address	Read/write	Register name	Initial value MSB←→LSB	Register description
00H	(R/W)	PDR0	XXXX XXXX	Port 0 data register
01H	(W)	DDR0	0000 0000	Port 0 direction register
02H	(R/W)	PDR1	XXXX XXXX	Port 1 data register
03H	(W)	DDR1	0000 0000	Port 1 direction register
04H	(R/W)	PDR2	---- 0000	Port 2 data register
05H	Vacancy			
06H	Vacancy			
07H	(R/W)	SYCC	X--1 1100	System clock control register
08H	(R/W)	STBC	0001 0---	Standby control register
09H	(R/W)	WDTE	0--- XXXX	Watchdog control register
0AH	(R/W)	TBCR	00-- -000	Time-base timer control register
0BH	(R/W)	WPCR	00-- -000	Watch prescaler control register
0CH	(R/W)	PDR3	XXXX XXXX	Port 3 data register
0DH	(W)	DDR3	0000 0000	Port 3 direction register
0EH	(R/W)	BUZR	---- --00	Buzzer register
0FH	(R/W)	EIC	0000 0000	External interrupt control register
10H	(R/W)	PDR4	0000 0000	Port 4 data register
11H	(R/W)	PDR5	0000 0000	Port 5 data register
12H	(R/W)	PDR6	0000 0000	Port 6 data register
13H	(R)	PDR7	---- --XX	Port 7 data register
14H	Vacancy			
15H	Vacancy			
16H	Vacancy			
17H	Vacancy			

Notes:
- The read value of bits marked as "-" is undefined.
- Do not use vacancies.
- See "(3) Register Description" for details of register contents.
- Bit manipulation instructions cannot be used on write-only registers (DDR0, DDR1, and DDR3).

(1.2) Addresses 18H to 7FH

Address	Read/write	Register name	Initial value MSB←→LSB	Register description
18H	(R/W)	T3CR	X000 XXX0	Timer 3 control register
19H	(R/W)	T2CR	X000 XXX0	Timer 2 control register
1AH	(R/W)	T3DR	XXXX XXXX	Timer 3 data register
1BH	(R/W)	T2DR	XXXX XXXX	Timer 2 data register
1CH	(R/W)	SMR	0000 0000	Serial mode register
1DH	(R/W)	SDR	XXXX XXXX	Serial data register
1EH	(R/W)	ADC1	0000 0000	A/D control register 1
1FH	(R/W)	ADC2	---0 0001	A/D control register 2
20H	(R/W)	ADDH	0000 00XX	A/D data register (H)
21H	(R/W)	ADDL	XXXX XX00	A/D data register (L)
22H	(W)	PCR0	0000 0000	Port input control register 0
23H	(W)	PCR1	---- 0000	Port input control register 1
24H to 7BH	Vacancy			
7CH	(W)	ILR1	1111 1111	Interrupt level register 1
7DH	(W)	ILR2	1111 1111	Interrupt level register 2
7EH	(W)	ILR3	1111 1111	Interrupt level register 3
7FH	Vacancy			

Notes:
- The read value of bits marked as "-" is undefined.
- Do not use vacancies.
- See "(3) Register Description" for details of register contents.
- Bit manipulation instructions cannot be used on write-only registers (PCR0, PCR1, ILR1, ILR2, and ILR3).

Appendix 2:
Quick Reference Table for the Instruction Cycle at Gear Change

(For 8-MHz and 4-MHz source oscillations)

Number of Instruction Cycles	CS1 and CS0 bit (system clock selection bit) setting in the SYCC register							
	CS1=1,CS0=1		CS1=1, CS0=0		CS1=0,CS0=1		CS1=0,CS0=0	
	8 MHz (µs)	4 MHz (µs)	8 MHz (µs)	4 MHz (µs)	8 MHz (µs)	4 MHz (µs)	8 MHz (µs)	4 MHz (µs)
1	0.5	1.0	1.0	2.0	2.0	4.0	8.0	16.0
2	1.0	2.0	2.0	4.0	4.0	8.0	16.0	32.0
4	2.0	4.0	4.0	8.0	8.0	16.0	32.0	64.0
8	4.0	8.0	8.0	16.0	16.0	32.0	64.0	128.0
16	8.0	16.0	16.0	32.0	32.0	64.0	128.0	256.0
32	16.0	32.0	32.0	64.0	64.0	128.0	256.0	512.0
64	32.0	64.0	64.0	128.0	128.0	256.0	512.0	1024

Appendix 3: Differences between the MB89143A/4A and MB89140 Series

Parameter			MB89143A/4A	MB89PV140,P147V1
Absolute maximum ratings			ΣIoh = –100 mA ΣIol = 50 mA	ΣIoh = –120 mA ΣIol = 150 mA
ROM			8 Kbytes for MB89143A; 12 Kbytes for MB89144A	32 Kbytes (External on PV models)
RAM			256 bytes	1 Kbyte
High -voltage ports	P60 to P67 BZ		Voh = 3 V, Ioh = –10 mA	Voh = 3 V, Ioh = –20 mA
	Pull-down resistors		No	No (Available on the MB89P147V2, 144V2, 145V2, and 146V2)
Resources	8-bit PWM timer		No	1-ch
	12 bit MPG		No	1-ch
	AD con-verter	Conversion accuracy	8 bits	10 bits
		Number of channels	8-ch	12-ch
		Conversion time	22 µs at 8 MHz	16.5 µs at 8 MHz
Packages	SDIP 64		Yes	Yes
	QFP 64		No	No
Operating voltage	8 MHz/maximum gear speed		VCC = 4.0 V to 6.0 V	VCC = 2.7 V to 6.0 V
	Watch mode/Sub-RUN		VCC = 2.5 V to 6.0 V	VCC = 2.2 V to 6.0 V
Mask options	Clock single/dual		Selectable	Selectable
	Reset output		selectable	Yes (MB89PV140), Selectable (MB89P147)
	Power-on reset		Yes	Yes (MB89PV140), Selectable (MB89P147)
	Pull-up resistor		Selectable (P14 to P17, P32 to P37)	Selectable (P14 to P17, P32 to P37, MB89P147) No (MB89PV140)
Noise filter	External interrupts		Yes	Yes
	$\overline{\text{RST}}$		Yes	Yes
	General-purpose inputs (Ports 0, 1, 2, 3, and 7)		No	Yes

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MB89143A/4A
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