FUJITSU SEMICONDUCTOR
MICROCONTROLLER MANUAL

CM25–10114–1E

F²MC-8L FAMILY MICROCONTROLLERS

MB89150/150A SERIES HARDWARE MANUAL

FUJITSU

1. GENERAL

The MB89150 and MB89150A series microcontrollers contain various resources such as an LCD controller/driver, timers, serial interfaces, a remote-control carrier frequency generator, and external interrupts, including the compact instruction system.

1.1 Features

- CPU core common to MB89600 series
- Double-clock pulse control
- Maximum memory space: 64K bytes
- Minimum instruction execution time: 0.95 μs at 4.2 MHz
- I/O ports: Max. 43
- 21-bit time-base counter
- 8/16-bit PWM timer/counter: 1 channel
- 8-bit serial I/O: 1 channel
- External interrupt input: 4 pins (Edge selection enabled) + 8 pins (Level interrupt)
- Buzzer output
- 15-bit watch prescaler
- LCD controller/driver with 36 segment outputs x 4 common outputs (max. 144 pixels)
- Built-in reference voltage generator and booster for driving LCD
- Built-in remote-control carrier frequency generator
- Internal power-on reset
- Low-power consumption modes (stop mode, sleep mode and watch mode)
- Package: QFP-80, SQFP-80
- CMOS technology

1.2 Product Series

Table 1-1 lists the types and functions of the MB89150 series of microcontrollers.

Table 1-1 Types and Functions of MB89150 Series of Microcontrollers

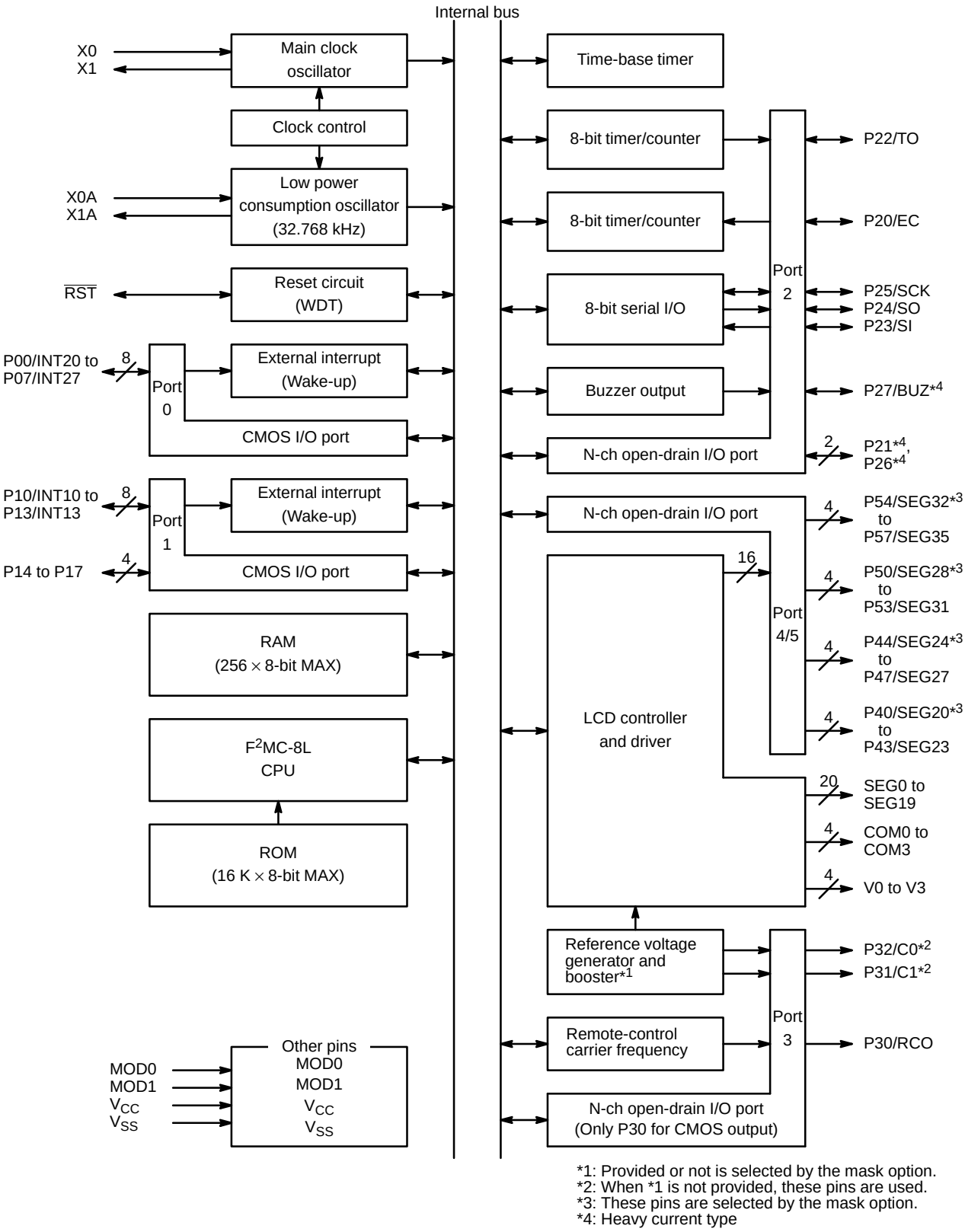
Model Name	MB89151/A	MB89152/A	MB89153/A	MB89154/A	MB89155/A	MB89P155/A	MB89PV150
Classification	Mass-produced product (mask ROM product)					Temporary product (small scale product)	Piggyback/ evaluation product (for development)
ROM capacity	4 K × 8 bits (Internal ROM)	6 K × 8 bits (Internal ROM)	8 K × 8 bits (Internal ROM)	12 K × 8 bits (Internal ROM)	16 K × 8 bits (Internal ROM)	16 K × 8 bits (Internal PROM, writable by general-purpose writer)	32 K × 8 bits (External ROM)
RAM capacity	128 × 8 bits	256 × 8 bits					512 × 8 bits
CPU functions	Number of basic instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum instruction execution time: 0.95 µs/4.2 MHz Interrupt processing time: 9 µs/4.2 MHz						
Port	I/O port (N-ch open drain): 8 (6 also used as resource pins, 3 used as heavy-current drive types) Output port (N-ch open drain): 18 (16 used as segment pins, 2 also used as boost capacitor connection pins)*3 I/O port (CMOS): 16 (12 also used as external interrupt pins) Output port (CMOS): 1 (also used as remote-control pin) Total: 43 (max.)						
Timer counter	2 channels for 8-bit timer counter or 1 channel for 16-bit event counter						
Serial I/O	8-bit length Selectable from least significant bit (LSB) first or most significant bit (MSB) first						
LCD controller and driver	Common output: 4 Segment output: 36*3 Biased power pin: 4 RAM capacity for LCD display: 36 × 4 bits Built-in reference voltage generator and booster for driving LCD (MB89150A only)*3 Built-in dividing resistor for driving LCD (selectable from external resistor)						Reference voltage generator and booster for driving LCD not built in
Number of external interrupts	4 (selectable from rising edge, falling edge, or both edges) 8 (interrupt for level only)						
Buzzer output	1 (7-type frequencies are programmable)						
Remote-control carrier frequency	1 (pulse width and cycle are programmable)						
Standby mode	Watch, sub, sleep, and stop modes						
Process	CMOS						
Package*1	QFP-80, SQFP-80						
Operating voltage*2	2.2 to 6.0 V					2.7 to 6.0 V	2.7 to 6.0 V
EMROM used	MBM27C256A-25 (LCC package)						

*1: Refer to the data sheet for the detail of each package

*2: Operating voltage varies depending to the condition such as frequency or others. Operation under 2.2 volt will be provided individually.

*3: Selected by the mask option.

1.3 Block Diagram



*1: Provided or not is selected by the mask option.
*2: When *1 is not provided, these pins are used.
*3: These pins are selected by the mask option.
*4: Heavy current type

Fig. 1.1 Block Diagram (Mass-produced product)

1.4 Pin Assignment

The production of this type is under consideration

Model with this pin assignment: MB8915X/P155

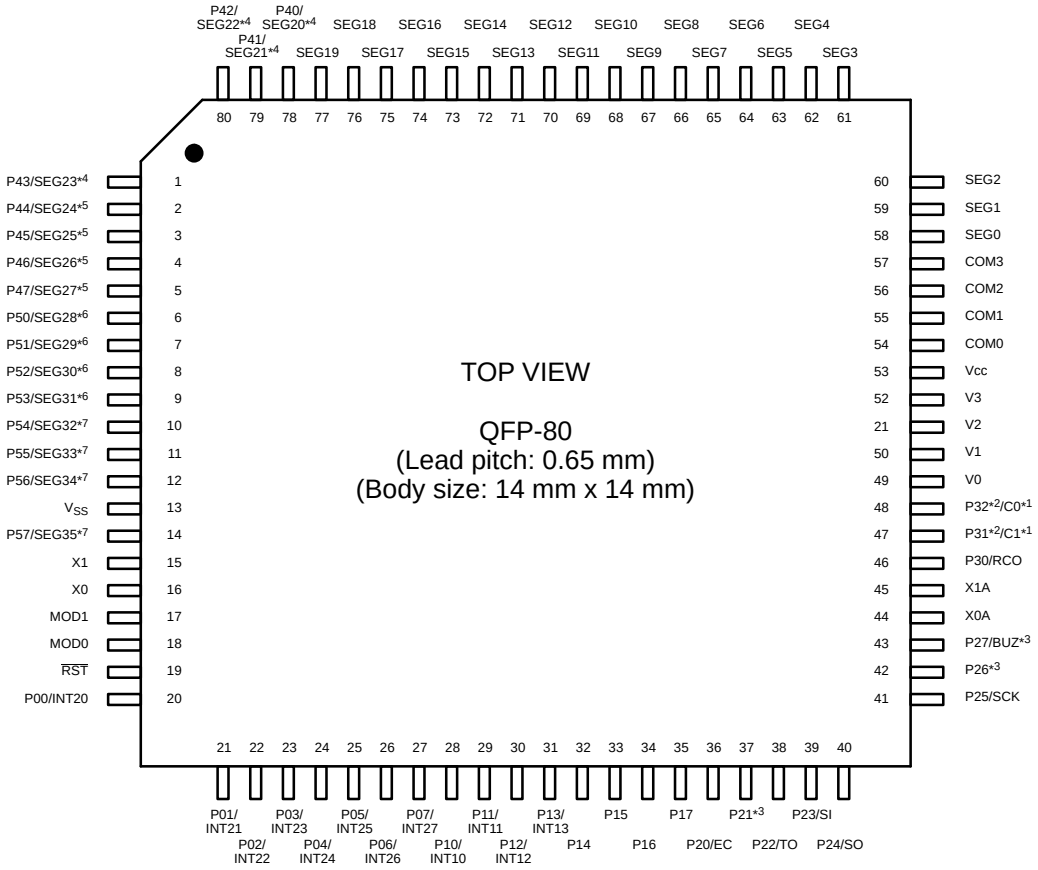


Fig. 1.2 Pin Assignment (FPT-80P-M11)

*1: Microcontrollers with built-in booster

*2: Microcontrollers without built-in booster

*3: N-ch open-drain heavy current type

*4 to *7: These pins are selected by the mask option at four pins.

Model with this pin assignment: MB8915X/P155

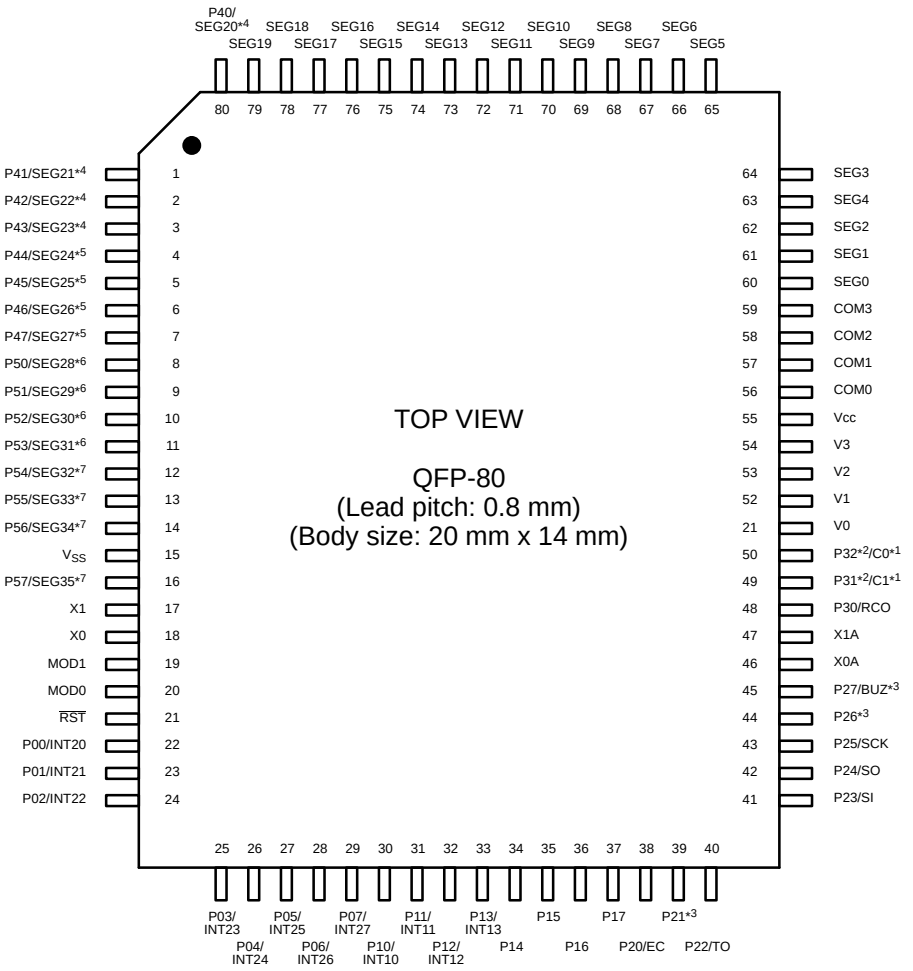


Fig. 1.3 Pin Assignment (FPT-80P-M06)

*1: Microcontrollers with built-in booster

*2: Microcontrollers without built-in booster

*3: N-ch open-drain heavy current type

*4 to *7: These pins are selected by the mask option at four pins.

Model with this pin assignment: MB8915X/P155

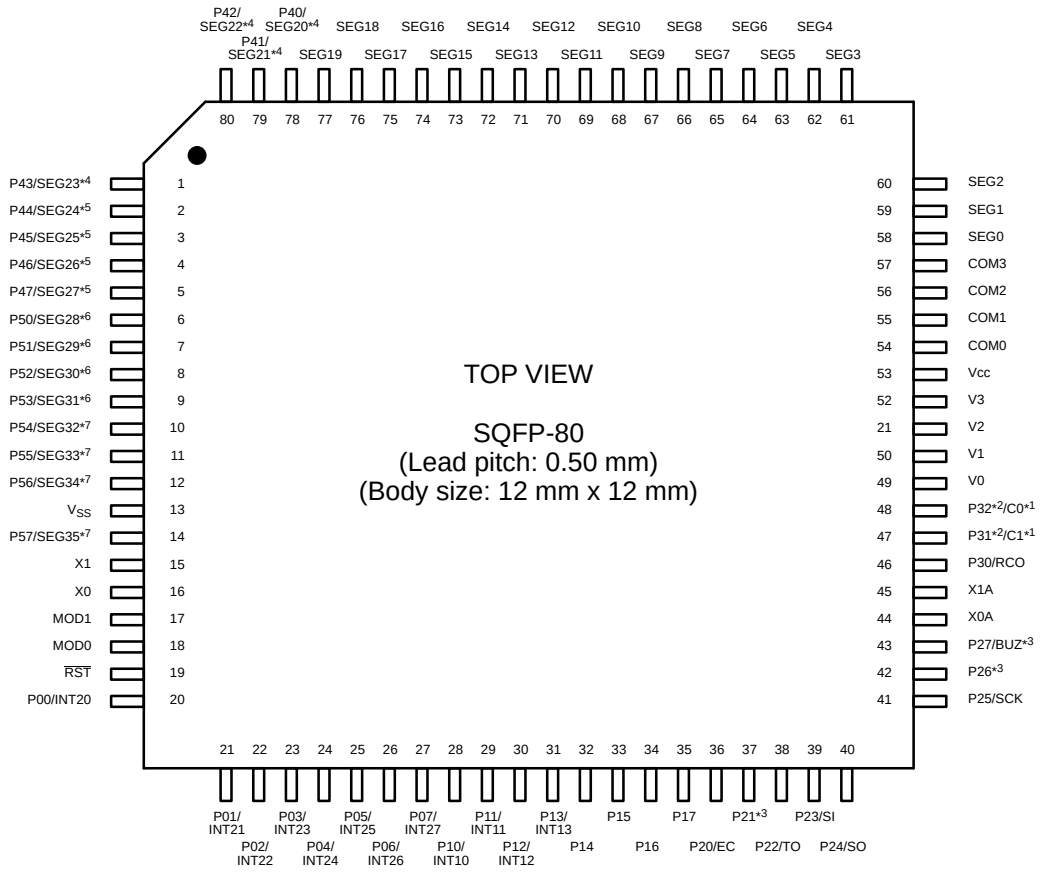


Fig. 1.4 Pin Assignment (FPT-80P-M05)

*1: Microcontrollers with built-in booster

*2: Microcontrollers without built-in booster

*3: N-ch open-drain heavy current type

*4 to *7: These pins are selected by the mask option at four pins.

Model with this pin assignment: MB8915X/P155

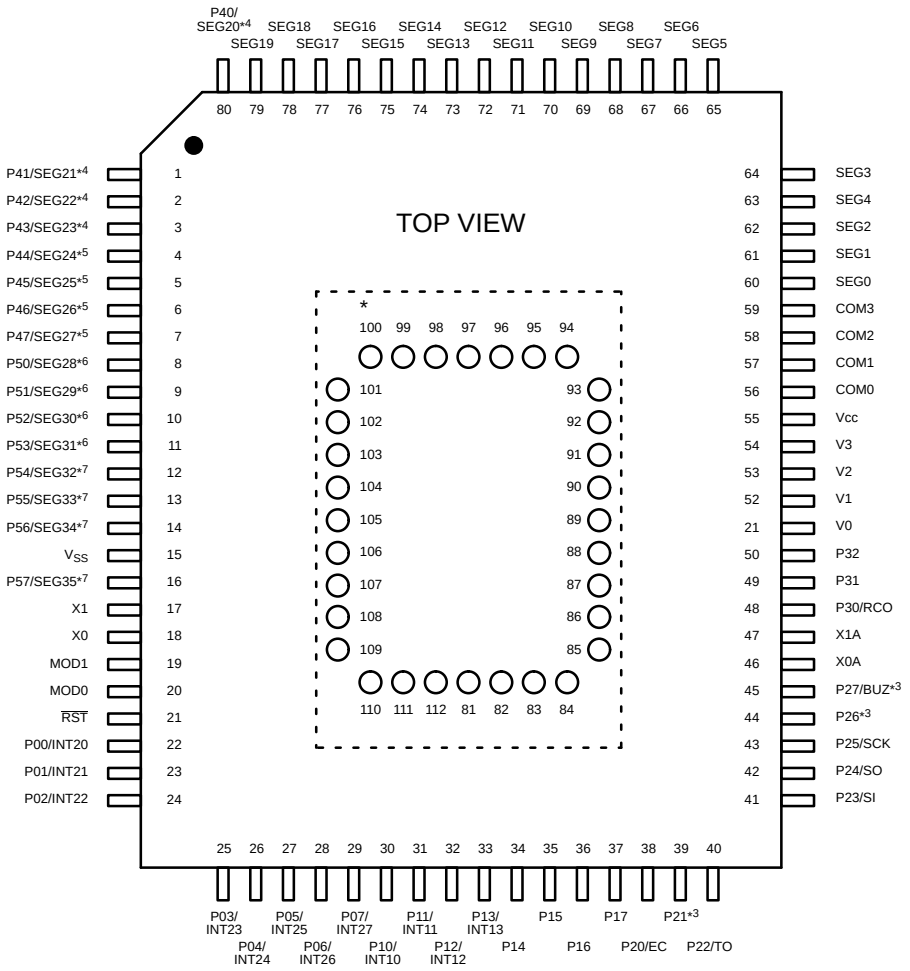


Fig. 1.5 Pin Assignment (MQP-80C-P01)

*3: N-ch open-drain heavy current type

*4 to *7: These pins are selected by the mask option at four pins.

1.5 Pin Function Description

Table 1-2 and Table 1-3 lists the pin function and Table 1-3 shows the input/output circuit configurations.

Table 1-2 Pin Function Description

Pin No.		Pin Name	Circuit type	Function
QFP 0.65	QFP 0.80			
16	18	X0	A	**Crystal oscillator pins for main clock (Max. 10 MHz)** CR oscillation available (only for mask product)
15	17	X1		
18	20	MOD0	B	**Operation-mode select pins** These pins are connected directly to V_{SS}.
17	19	MOD1		
19	21	$\overline{RSTX}$	C	**Reset I/O pin** This pin consists of an N-ch open-drain output with a pull-up resistor and hysteresis input. A Low level is output from this pin. The internal circuit is initialized at input of a Low level.
20 to 27	22 to 29	P00/INT20 to P07/INT27	D	**General-purpose I/O ports** These ports also serve as external interrupt 2 input (wake-up input) pins. Input is hysteresis type.
28 to 31	30 to 33	P10/INT10 to P13/INT13	D	**General-purpose I/O ports** These ports also serve as pins for input of external interrupt 1. Input of external interrupt 1 is hysteresis type.
32 to 35	34 to 37	P14 to P17	E	**General-purpose I/O port**
36	38	P20/EC	G	**N-ch open-drain type general-purpose I/O port** This port also serves as an external clock input pin for the timer. The resource is hysteresis input.
37	39	P21	H	**N-ch open-drain type general-purpose I/O port**
38	40	P22/TO	H	**N-ch open-drain type general-purpose I/O port** This port also serves as an timer output pin
39	41	P23/SI	G	**N-ch open-drain type general-purpose I/O port** This port also serves as an serial I/O data input pin. The resource is hysteresis input
40	42	P24/SO	H	**N-ch open-drain type general-purpose I/O port** This port also serves as an serial I/O data output pin.
41	43	P25/SCK	G	**N-ch open-drain type general-purpose I/O port** This port also serves as an serial I/O clock output pin. The resource is hysteresis input
42	44	P26	H	**N-ch open-drain type general-purpose I/O port**
43	45	P27/BUZ	H	**N-ch open-drain type general-purpose I/O port** This port also serves as an buzzer output pin
48	50	P32	I	This port serves as an N-ch open-drain type general-purpose output port only for microcontrollers without built-in booster.
		C0	—	This port serves as a capacitor connecting pin for microcontrollers with a built-in booster.
47	49	P31	I	This port serves as an N-ch open-drain type general-purpose output port only for microcontrollers without a built-in booster.
		C1	—	This port serves as a capacitor connecting pin for microcontrollers with a built-in booster.

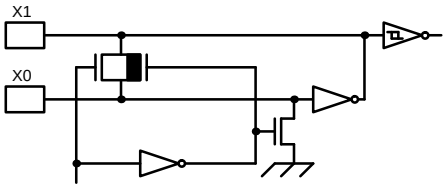
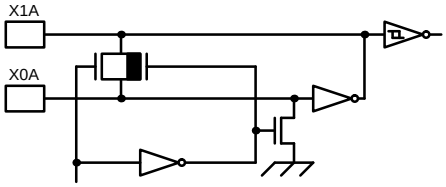
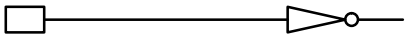
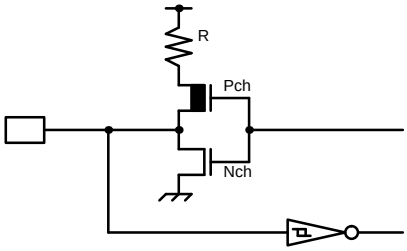
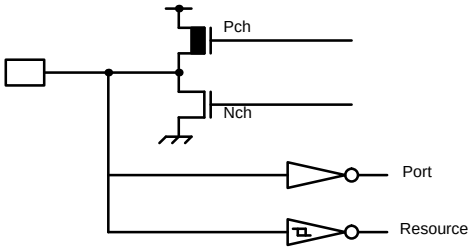
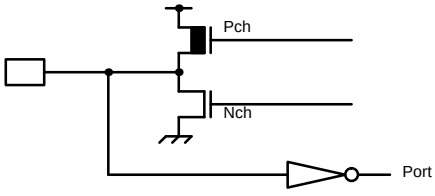
(Continued)

Pin No.		Pin Name	Circuit type	Function
QFP 0.65	QFP 0.80			
46	48	P30/RCO	F	**General-purpose output-only port** This port also serves as a remote-control carrier frequency output pin.
14 to 6	16 to 8	P57/SEG35 to P50/SEG28	I/J	**N-ch open-drain type general-purpose output ports** These ports also serve as LCDC segment output pins. They should be switched by the mask option.
5 to 78	7 to 80	P47/SEG27 to P40/SEG20	I/J	**N-ch open-drain type general-purpose output ports** These ports also serve as LCDC segment output pins. They should be switched by the mask option.
58 to 77	60 to 79	SEG0 to SEG19	J	**LCDC segment output-only pins**
57 56 55 54	59 58 57 56	COM3 COM2 COM1 COM0	J	**LCDC common output-only pins**
52 51 50 49	54 53 52 51	V3 V2 V1 V0	—	**Power pins for driving LCD**
44	46	X0A	A'	**Low-speed clock pulse oscillation pin (32 KHz)**
45	47	X1A		
53	55	V_{CC}	—	**Power pin**
13	15	V_{SS}	—	**Power (GND) pin**

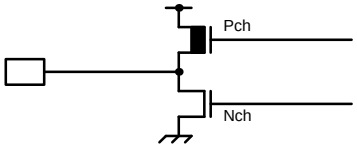
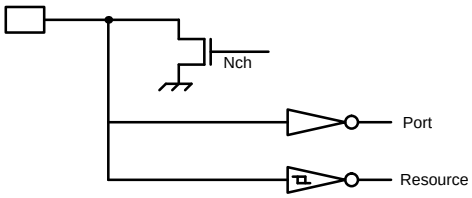
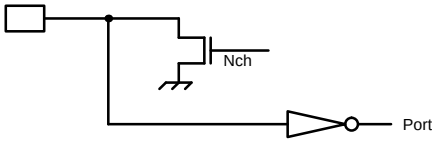
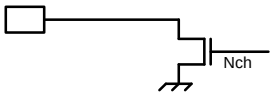
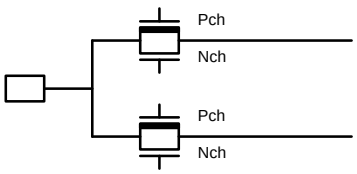
Table 1-3 Pins for External ROM

Pin No. QFP 0.80	Pin Name	Circuit type	Function
82	V_{PP}	Output	**High-level output pin**
83 84 85 86 87 88 89 90 91	A12 A7 A6 A5 A4 A3 A2 A1 A0	Output	**Address-output pins**
93 94 95	01 02 03	Input	**Data-input pins**
96	V_{SS}	Output	**Power (GND) pin**
98 99 100 101 102	04 05 06 07 08	Input	**Data-input pins**
103	CEX	Output	**Chip-enable pin for ROM** A High level is output in the standby mode.
104	A10	Output	**Address-output pin**
105	OEX	Output	**Output-enable pin for ROM** A Low level is always output.
107 108 109	A11 A9 A8	Output	**Address-output pins**
110	A13	Output	**Address-output pin**
111	A14	Output	**Address-output pin**
112	V_{CC}	Output	**Power pin for EPROM**
81 92 97 106	NC	—	**Internal-connection pins.** These pins must always be kept open.

Table 1-4 Input/Output Circuit Configurations

Classification	Circuit	Remarks
A	 Standby control signal	Used for high speed pulse • Feedback resistor: About 2 MΩ
A’	 Standby control signal	Used for low speed pulse
B		• Hysteresis input
C		• Output pull-up resistor (P-ch): About 50 kΩ (5 V) • Hysteresis input
D		• CMOS input/output • The resource is hysteresis input. • The pull-up resistor is available (not available for MB89PV150).
E		• CMOS input/output • The pull-up resistor is available (not available for MB89PV150).

(Continued)

Classification	Circuit	Remarks
F		• CMOS output • Pch is driven with heavy current
G		• N-ch open-drain input/output • CMOS input • The resource is hysteresis input. • The pull-up resistor is available (not available for MB89P155 and MB89PV150).
H		• N-ch open-drain input/output • CMOS input • P21, P26, and P27 are heavy-current drive type pins. • The pull-up resistor is available (not available for MB89P155 and MB89PV150).
I		• N-ch open-drain output • The pull-up resistor is available (not available for MB89P155 and MB89PV150). • P31 and P32 are not provided with a resistor.
J		• LCDC segment output

1.6 Handling Devices

(1) Preventing latch-up

Latch-up may occur if a voltage higher than V_{CC} or lower than Vss is applied to the input or output pins other than port 4, or if voltage exceeding the rated value is applied between V_{CC} and V_{SS}.
When latch-up occurs, the supply current increases rapidly, sometimes resulting in overheating and destruction. Therefore, no voltage exceeding the maximum ratings should be used.

(2) Handling unused input pins

Leaving unused input pins open may cause a malfunction. Therefore, these pins should be set to pull-up or pull-down.

(3) Always set NC (internal connections) open.

(4) Variations in supply voltage

Although the specified V_{CC} supply voltage operating range is assured, a sudden change in the supply voltage within the specified range may cause a malfunction. Therefore, the voltage supply to the IC should be kept as constant as possible. The V_{CC} ripple (P-P value) at the supply frequency (50 - 60 Hz) should be less than 10% of the typical V_{CC} value, or the coefficient of excessive variation should be 0.1 V/ms max. instantaneous change when the power supply is switched.

(5) Precautions for external clocks

It takes some time for oscillation to stabilize after changing the mode to power-on reset (option selection) and stop. Consequently, an external clock must be input.

2. HARDWARE CONFIGURATION

2.1 CPU

This section describes the CPU hardware composition. The CPU has the following six functions.

- Memory Space
- Arrangement of 16-bit Data in Memory
- Registers
- Operation Modes
- Clock Control Block
- Interrupt Controller

2.1.1 Memory space

The MB89150 series of microcontrollers have a memory area of 64K bytes. All I/O, data, and program areas are located in this space. The I/O area is near the lowest address and the data area is immediately above it. The data area may be divided into register, stack, and direct-address areas according to the applications. The program area is located near the highest address and the tables of interrupt and reset vectors and vector-call instructions are at the highest address. Figure 2.1 shows the structure of the memory space for the MB89150 series of microcontrollers.

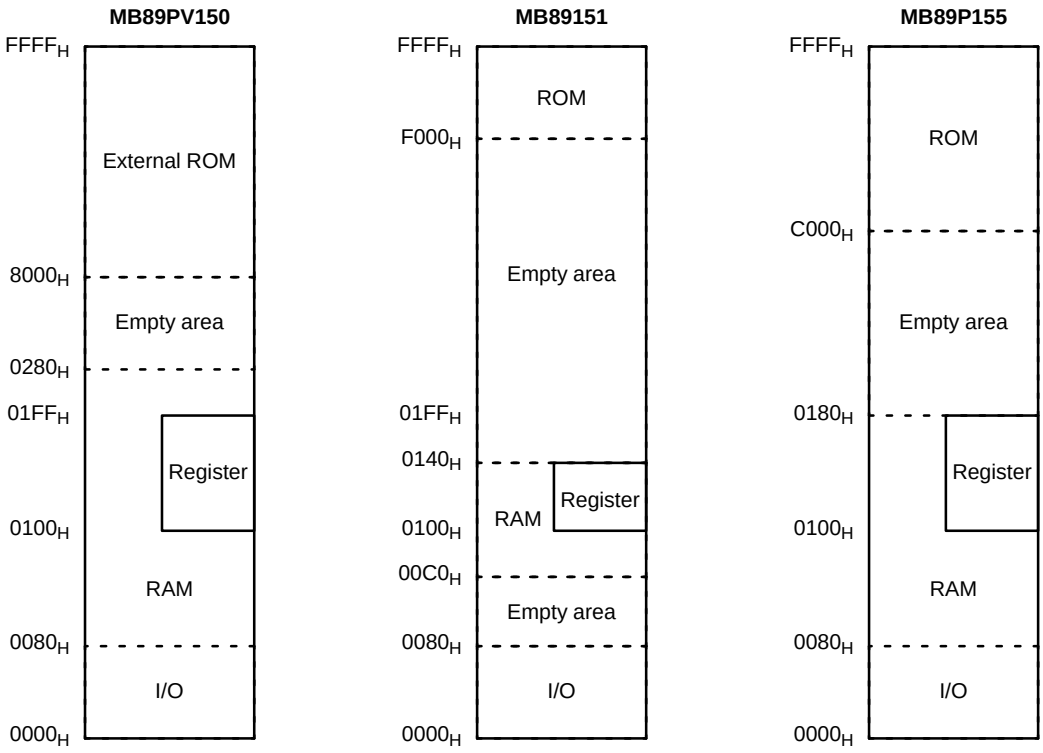


Fig. 2.1 Memory Space of MB89150 Series of Microcontrollers

(1) I/O area

This area is where various resources such as control and data registers are located. The memory map for the I/O area is given in APPENDIX A.

(2) RAM area

This area is where the static RAM is located. Addresses from 0100_H to $017F_H$ are also used as the general-purpose register area.

(3) ROM area

This area is where the internal ROM is located. Addresses from $FFD0_H$ to $FFFF_H$ are also used for the table of interrupt and reset and vector-call instructions. Fig. 2.2 shows the correspondence between each interrupt number or reset and the table addresses to be referenced for the MB89150 series of microcontrollers.

	Table address	
	Upper data	Lower data
CALLV #0	$FFC0_H$	$FFC1_H$
CALLV #1	$FFC2_H$	$FFC3_H$
CALLV #2	$FFC4_H$	$FFC5_H$
CALLV #3	$FFC6_H$	$FFC7_H$
CALLV #4	$FFC8_H$	$FFC9_H$
CALLV #5	$FFCA_H$	$FFCB_H$
CALLV #6	$FFCC_H$	$FFCD_H$
CALLV #7	$FFCE_H$	$FFCF_H$

	Table address	
	Upper data	Lower data
Interrupt #11	$FFE4_H$	$FFE5_H$
Interrupt #10	$FFE6_H$	$FFE7_H$
Interrupt #9	$FFE8_H$	$FFE9_H$
Interrupt #8	$FFEA_H$	$FFEB_H$
Interrupt #7	$FFEC_H$	$FFED_H$
Interrupt #6	$FFEE_H$	$FFEF_H$
Interrupt #5	$FFF0_H$	$FFF1_H$
Interrupt #4	$FFF2_H$	$FFF3_H$
Interrupt #3	$FFF4_H$	$FFF5_H$
Interrupt #2	$FFF6_H$	$FFF7_H$
Interrupt #1	$FFF8_H$	$FFF9_H$
Interrupt #0	$FFFA_H$	$FFFB_H$
Reset mode	-----	$FFFD_H$
Reset vector	$FFFE_H$	$FFFF_H$

Note: $FFFC_H$ is already reserved.

Fig. 2.2 Table of Reset and Interrupt Vectors

2.1.2 Arrangement of 16-bit data in memory

When the MB89150 series of microcontrollers handle 16-bit data, the data written at the lower address is treated as the upper data and that written at the next address is treated as the lower data as shown in Figure 2.3.

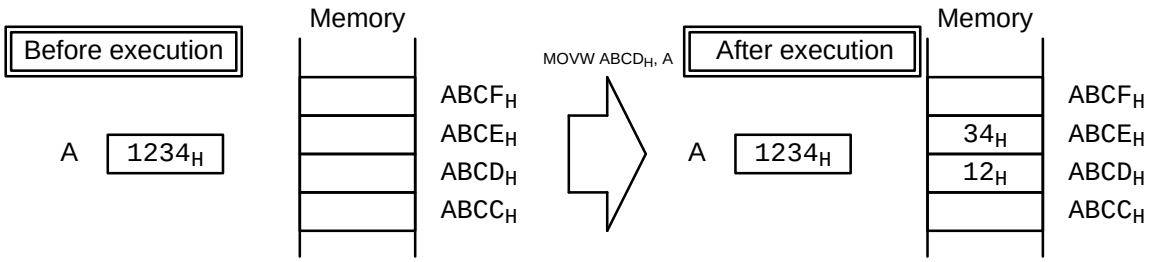


Fig. 2.3 Arrangement of 16-bit Data in Memory

This is the same as when 16 bits are specified by the operand during execution of an instruction. Bits closer to the OP code are treated as the upper byte and those next to it are treated as the lower byte. This is also the same when the memory address or 16-bit immediate data is specified by the operand.

[Example]

```
MOV A, 5678H      ; Extended address
MOV A, #1234H     ; 16-bit immediate data
```

Assemble

```
      ⋮
XXXXH XX XX
XXXXH 60 56 78 ; Extended address
XXXXH E4 12 34 ; 16-bit immediate data
XXXXH XX
      ⋮
```

Fig. 2.4 Arrangement of 16-bit Data during Execution of Instruction

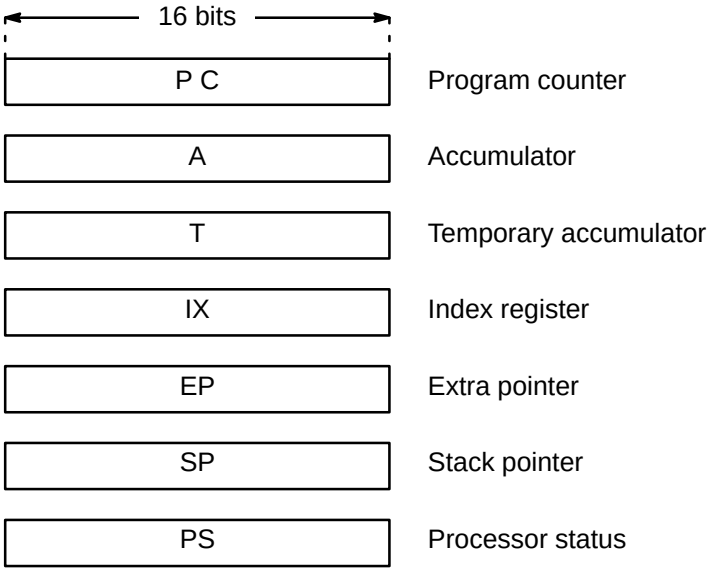
Data saved in the stack by an interrupt is also treated in the same manner.

2.1.3 Internal registers in CPU

The MB89150 series of microcontrollers have dedicated registers in the CPU and general-purpose registers in memory.

<Dedicated registers>

- Program counter (PC) — 16-bit long register indicating location where instructions stored
- Accumulator (A) — 16-bit long register where results of operations stored temporarily; the lower byte is used to execute 8-bit data processing instructions.
- Temporary accumulator (T) — 16-bit long register; the operations are performed between this register and the accumulator. The lower one byte is used to execute 8-bit data processing instructions
- Stack pointer (SP) — 16-bit long register indicating stack area
- Processor status (PS) — 16-bit long register where register pointers and condition codes stored
- Index register (IX) — 16-bit long register for index modification
- Extra pointer (EP) — 16-bit long register for memory addressing



The 16 bits of the program status (PS) can be divided into 8 upper bits for a register bank pointer (RP) and 8 lower bits for a condition code register (CCR). (See Figure 2.5.)

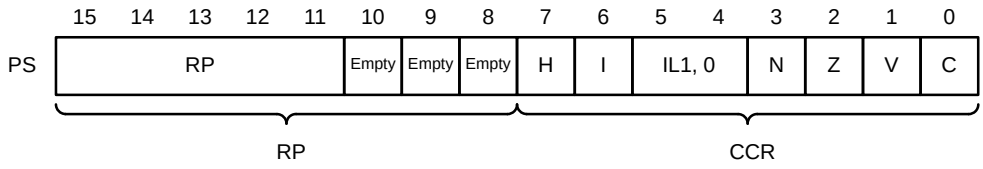


Fig. 2.5 Structure of Processor Status

The RP indicates the address of the current register bank and the contents of the RP; the real addresses are translated as shown in Figure 2.6.

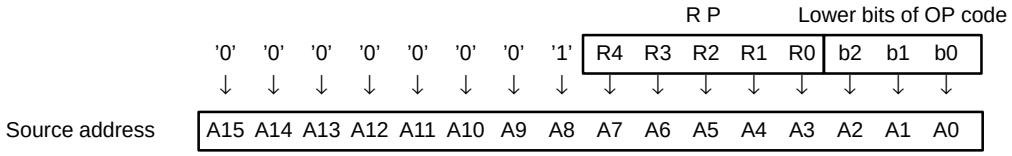


Fig. 2.6 Rule for Translating Real Addresses at General-purpose Register Area

The CCR has bits indicating the results of operations and transfer data contents, and bits controlling the CPU operation when an interrupt occurs.

- H-flag: H-flag is set when a carry or a borrow out of bit 3 into bit 4 is generated as a result of operations; it is cleared in other cases. This flag is used for decimal-correction instructions.
- I-flag: An interrupt is enabled when this flag is 1 and is disabled when it is 0. The I-flag is 0 at reset.
- IL1 and IL0: These bits indicate the level of the currently-enabled interrupt. The CPU executes interrupt processing only when an interrupt with a value smaller than the value indicated by this bit is requested.

IL1	IL0	Interrupt level	High and low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = No interrupt

- N-flag: The N-flag is set when the most significant bit is 1 as a result of operations; it is cleared when the MSB is 0.
- Z-flag: Z-flag is set when the bit is 0 as a result of operations; it is cleared in other cases.
- V-flag: V-flag is set when a two's complement overflow occurs as a result of operations; it is reset when an overflow does not occur.
- C-flag: C-flag is set when a carry or a borrow out of bit 7 is generated as a result of operations; it is cleared in other cases. When the shift instruction is executed, the value of the C-flag is shifted out.

<General-purpose registers>

General-purpose registers are 8-bit long registers for storing data.

The 8-bit long general-purpose registers are in the register banks in memory. One bank has eight registers and up to 32 banks are available for the MB89151 series of microcontrollers. The register bank pointer (RP) indicates the currently-used bank.

Note: The number of register banks used depends on the RAM capacity.

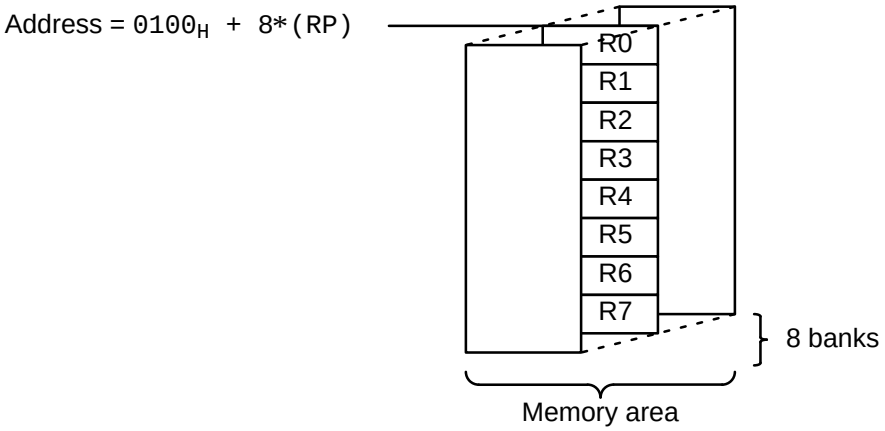


Fig. 2.7 Register Bank Configuration

2.1.4 Operation modes and external bus operation

The MB89150 series of microcontrollers have only single-chip mode.

The memory map is as follows:

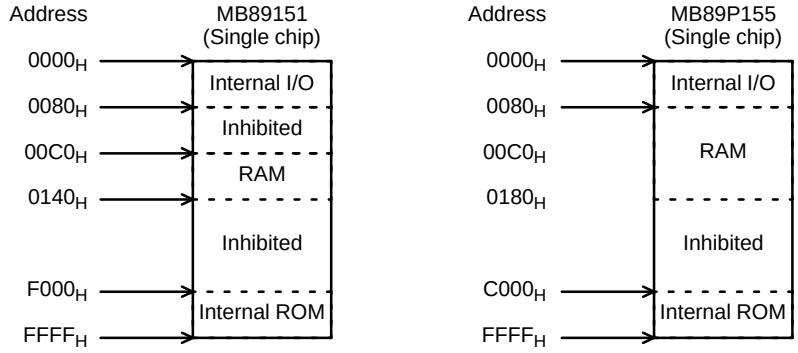


Fig. 2.8 Memory Maps in Various Modes

The relationship between the states and operations of the device-mode pins is shown below. (Only 00 can be set for MB89150.)

MOD1	MOD0	Description
0	0	Reset vectors are read from the internal ROM. The external access does not function.
1	1	Write mode for products containing EPROM.

The following functions are selected according to the mode-data setting conditions.

®	®	®	®	®	T2	T1	T0

®: Reserved: Specify 0.

Mode bits

T2	T1	T0	Operation
0	0	0	Select single-chip mode.
Other than above			Reserved. Do not set.

Note: Do not select the single-chip mode with the externally-fetched mode data.

2.1.5 Clock control block

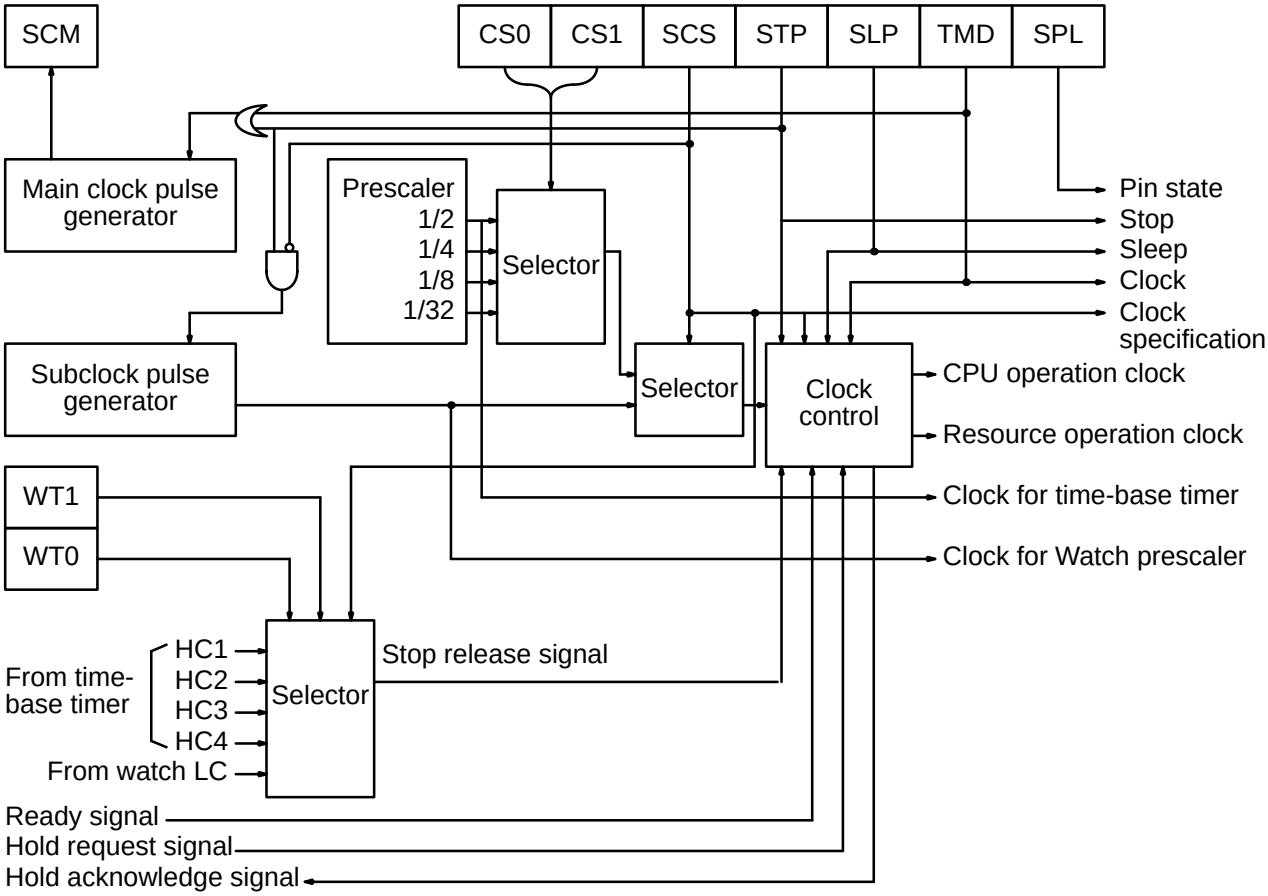
This block controls the standby operation, oscillation stabilization time, software reset, and clock switching.

(1) Register list

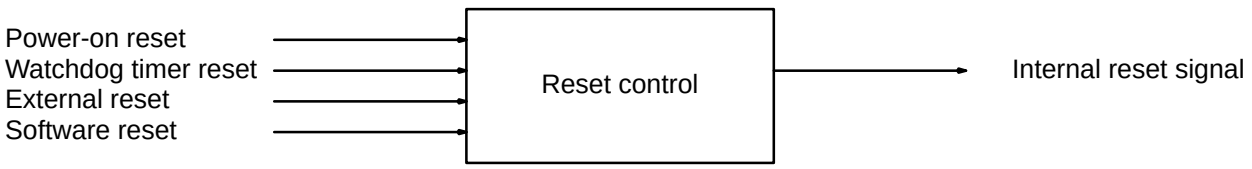
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Address: 0007_H	SCM	—	—	WT1	WT0	SCS	CS1	CS0	System clock control register (SYCC)
Address: 0008_H	STP	SLP	SPL	RST	TMD	—	—	—	Standby control register (STBC)

(2) Block diagram

(a) Machine clock control section



(b) Reset control section



(3) Description of registers

(a) STBC (Standby-conrol register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0008_H	STP	SLP	SPL	RST	TMD	—	—	—	$0001\ 0XXX_B$
	(W)	(W)	(R/W)	(W)	(W)				

[Bit 7] STP: Stop bit
Bit 7 specifies switching to the stop mode.

0	No operation
1	Stop mode

This bit is cleared at reset or stop cancellation.

0 is always read when this bit is read.

[Bit 6] SLP: Sleep bit
Bit 6 specifies switching to the sleep mode.

0	No operation
1	Sleep mode

This bit is cleared at reset or stop cancellation.

0 is always read when this bit is read.

[Bit 5] SPL: Pin state specifying bit
Bit 5 specifies the external pin state in the watch or stop mode.

0	Holds state and level immediately before watch or stop mode
1	High impedance

This bit is cleared at resetting.

[Bit 4] RST: Software reset bit
Bit 4 resets the software.

0	Generates 4-cycle reset signal
1	No operation

1 is always read when this bit is read.

If a software reset is performed during operation in a submode, one oscillation stabilization period is required to switch to the main mode. Therefore, a reset signal is output during the oscillation stabilization period.

[Bit 3] TMD: Watch bit

Bit 3 specifies switching to the watch mode.

0	No operation
1	Watch mode

Writing at this bit is possible only in the submode (SCS = 0). 0 is always read when this bit is read. This bit is cleared at an interrupt request or reset.

(b) System clock control register (SYCC)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0007_H	SCM	—	—	WT1	WT0	SCS	CS1	CS0	X--M M100$_B$
	(R)			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] SCM: System clock monitor bit

Bit 7 checks whether the current system clock is the main clock or subclock.

0	Subclock (Main clock is stopping or oscillation of main clock stable)
1	Main clock

[Bits 4 and 3] WT1 and WT0: Oscillation stabilization time select bits

Bits 4 and 3 select the oscillation stabilization wait time of the main clock.

WT1	WT0	Oscillation stabilization time	Oscillation stabilization time at original oscillation of 10 MHz
1	1	Approximate 2^{18}/fch	Approximate 87.4 (ms)
1	0	Approximate 2^{16}/fch	Approximate 21.8 (ms)
0	1	Approximate 2^{12}/fch	Approximate 1.4 (ms)
0	0	Approximate 2^{4}/fch	Approximate 0 (ms)

fch: Oscillation frequency of main clock

If the main mode is specified by the system clock select bit (SCS), the mode switches to main mode after the selected wait time has elapsed.

The initial value of this bit is determined by the mask option. Do not rewrite this bit during the oscillation stabilization period nor rewrite it concurrently with switching from low speed to high speed.

The oscillation stabilization time of the main clock is generated by dividing down the frequency of the main clock. Since the oscillation frequency is unstable immediately after oscillation starts, use the above table.

[Bit 2] SCS: System clock select bit

Bit 2 selects the system clock mode.

0	Selects subclock (32 kHz) mode
1	Selects main clock mode

[Bits 1 and 0] CS1 and CS0: System clock select bits

If the main mode is specified by the system clock select bit (SCS), the system clock is as given in the table below.

CS1	Cs0	Instruction cycle	Minimum instruction execution time at 10 MHz
0	0	64/fch	21.3 (µs)
0	1	16/fch	5.33 (µs)
1	0	8/fch	2.67 (µs)
1	1	4/fch	1.33 (µs)

fch: frequency of main clock

(4) Description of operation

(a) Low-power consumption mode

This chip has three operation modes. The sleep mode, and stop mode in the table below reduce the power consumption. In the main mode, four system clocks can be selected according to the system condition to minimize power consumption.

Table 2-1 Operating State of Low-power Consumption Modes

Main operation mode	(CS1, CS0)	Operation mode	Clock pulse generation		Each operating clock pulse (10 MHz main clock)				Wake-up source in each mode
			Main	Sub	CPU	Time-base timer	Each resource	Clock	
Main mode	(1, 1)	RUN	Oscillates	Oscillates	1.5 MHz	1.5 MHz	1.5 MHz	32 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP	Stops			Stops	Stops		External interrupt
	(1,0)	RUN	Oscillates	Oscillates	750 kHz	1.5 MHz	750 kHz	32 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP	Stops			Stops	Stops		External interrupt
	(0,1)	RUN	Oscillates	Oscillates	375 kHz	1.5 MHz	375 kHz	32 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP	Stops			Stops	Stops		External interrupt
	(0,0)	RUN	Oscillates	Oscillates	98.4 kHz	1.5 MHz	98.4 kHz	32 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP	Stops			Stops	Stops		External interrupt
Submode	—	RUN	Stops	Oscillates	32 kHz	Stops	32 kHz	32 kHz	Various interrupt requests
		SLEEP			Stops				
		STOP		Stops			Stops	Stops	External interrupt
CLOCK mode			Stops	Oscillates	Stops	Stops	Stops	32 kHz	Watch external interrupt

- The submode stops oscillation of the main clock.
- The SLEEP mode stops only the operating clock pulse of the CPU; other operations are continued.
- The WATCH mode stops the functions of all chips other than the special resources.
- The STOP mode stops the oscillation. Data can be held with the lowest power consumption in this mode.
- For microcontrollers with a built-in booster (MB89150A), the booster stops when the mode is switched from the subclock mode to the stop mode.

[1] WATCH mode

- Switching to WATCH mode
  - Writing 1 at the TMD bit (bit 3) of the STBC register switches the mode to WATCH mode. Writing is invalid if 1 is set at the SCS bit (bit 2) of the SYCC register.
  - The WATCH mode stops all chip functions except the watch prescaler, external interrupt, and wake-up functions. Therefore, data can be held with the lowest power consumption.
  - The input/output pins and output pins during the WATCH mode can be controlled by the SPL bit of the STBC register so that they are held in the state immediately before entering the WATCH mode or so that they enter the high-impedance state.
  - If an interrupt is requested when 1 is written at the TMD bit , instruction execution continues without switching to the WATCH mode.
  - In the WATCH mode, the values of registers and RAM immediately before entering the WATCH mode are held.
- Canceling WATCH mode
  - The WATCH mode is canceled by inputting the reset signal and requesting an interrupt.
  - When the reset signal is input during the WATCH mode, the CPU is switched to the reset state and the WATCH mode is canceled.
  - When an interrupt higher than level 11 is requested from a resource during the WATCH mode, the WATCH mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the WATCH mode.
  - If the WATCH mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Therefore, the reset sequence is not executed unless the oscillation stabilization time is elapsed. The oscillation stabilization time will be that of the main clock selected by the WT1 and WT0 bits. However, when Power-on Reset is not specified by the mask option, the CPU is not switched to the oscillation stabilization wait state, even if the WATCH mode is canceled by inputting the reset signal.

[2] SLEEP mode

- Switching to SLEEP mode
  - Writing 1 at the SLP bit (bit 6) of the STBC register switches the mode to SLEEP mode.
  - The SLEEP mode stops the CPU operating clock pulse; only the CPU stops and the resources continue to operate.
  - If an interrupt is requested when 1 is written at the SLP bit (bit 6), instruction execution continues without switching to the SLEEP mode. In the SLEEP mode,the values of registers and RAM immediately before entering the SLEEP mode are held.
- Canceling SLEEP mode
  - The SLEEP mode is canceled by inputting the reset signal and requesting an interrupt.
  - When the reset signal is input during the SLEEP mode, the CPU is switched to the reset state and the SLEEP mode is canceled.
  - When an interrupt higher than level 11 is requested from a resource during the SLEEP mode, the SLEEP mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the SLEEP mode.

[3] STOP mode

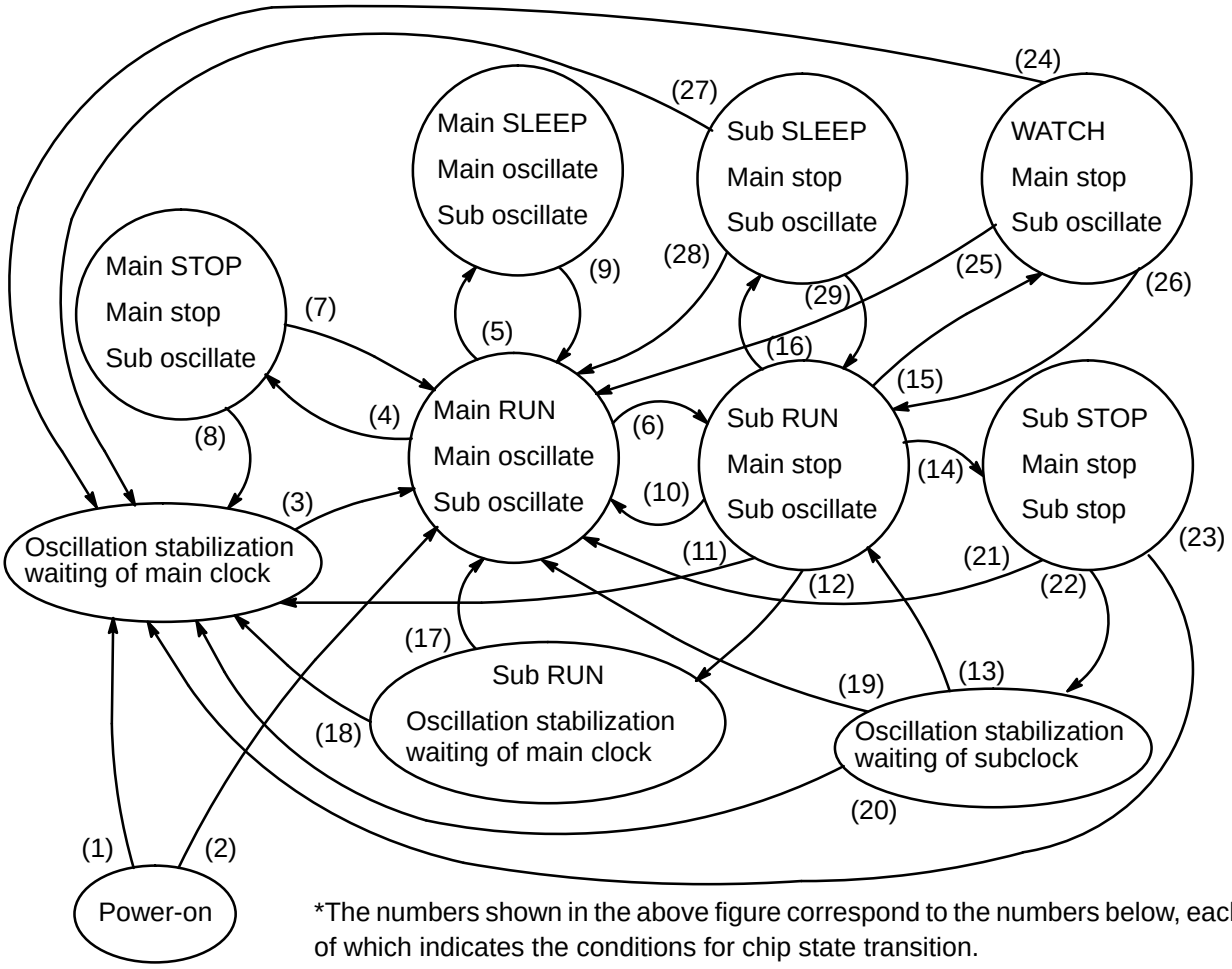
- Switching to STOP mode
  - Writing 1 at the STP bit (bit 7) of the STBC register switches the mode to STOP mode.
  - The STOP mode varies when the main clock is operating and when the subclock is operating.
    When the main clock is operating: The main clock stops but the subclock does not stop. All chip functions except the watch function stop.
    When subclock is operating: Both the main clock and subclock stop. All chip functions stop.
  - The input/output pins and output pins during the STOP mode can be controlled by the SPL bit (bit 5) of the STBC register so that they are held in the state immediately before entering the STOP mode, or so that they enter in the high-impedance state.
  - If an interrupt is requested when 1 is written at the STP bit (bit 7), instruction execution continues without switching to the STOP mode.
  - In the STOP mode, the values of registers and RAM immediately before entering the STOP mode are held.
- Canceling STOP mode
  - The STOP mode is canceled either by inputting the reset signal or by requesting an interrupt.
  - When the reset signal is input during the STOP mode, the CPU is switched to the reset state and the STOP mode is canceled.
  - When an interrupt higher than level 11 is requested from the external interrupt circuit during the STOP mode, the STOP mode is canceled.
  - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the STOP mode.
  - Four oscillation stabilization times of the main clock can be selected by the WT1 and WT0 bits. The oscillation stabilization time of the subclock is fixed (at 2^{15}/fcl -- fcl: frequency of subclock).
  - If the STOP mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Therefore, the reset sequence is not executed unless the oscillation stabilization time is elapsed. The oscillation stabilization time corresponds to the oscillation stabilization time of the main clock selected by the WT1 and WT0 bits. However, when Power-on Reset is not specified by the mask option, the CPU is not switched to the oscillation stabilization wait state even if the STOP mode is canceled by inputting the reset signal.

[4] Setting low power consumption mode

STBC Register			Mode
STP (Bit 7)	SLP (Bit 6)	TMD (Bit 3)	
0	0	0	Normal
0	0	1	WATCH
0	1	0	SLEEP
1	0	0	STOP
1	×	×	Disable

Note: When the mode is switched from the subclock mode to the main clock mode, do not set the stop, sleep, and watch modes. If the SCS bit of the SYCC register is rewritten from 0 to 1, set the above modes after the SCM bit of the SYCC register has been set to 1.
For microcontrollers with a built-in booster (MB89150A), the booster stops when the mode is switched from the subclock mode to the stop mode.

(b) State transition diagram



*The numbers shown in the above figure correspond to the numbers below, each of which indicates the conditions for chip state transition.

(1) When power-on reset option is selected
(2) When power-on reset option is not selected
(3) After oscillation stabilized
(4) Set STP bit to 1.
(5) Set SLP bit to 1.
(6) Set SCS bit to 0.
(7) External reset when power-on reset option not selected
(8) External reset or interrupt when power-on reset option selected
(9) External reset or interrupt
(10) External reset when power-on reset option not selected
(11) External reset or other reset when power-on reset option selected
(12) Set SCS bit to 1.
(13) After oscillation stabilized
(14) Set STP bit to 1.
(15) Set TMD bit to 1.
(16) Set SLP bit to 1.
(17) External reset after oscillation stabilized or when power-on reset option not selected
(18) External reset or other reset when power-on reset option selected
(19) External reset after oscillation is stabilized or when power-on reset option not selected
(20) External reset when power-on reset option selected
(21) External reset when power-on reset option not selected
(22) Interrupt
(23) External reset when power-on reset option selected
(24) External reset when power-on reset option selected
(25) External reset when power-on reset option not selected
(26) Interrupt
(27) External reset when power-on reset option selected
(28) External reset when power-on reset option not selected
(29) Interrupt

(d) Reset

There are four types of resets as shown in Table 2-2.

Table 2-2 Sources of Reset

Reset name	Description
External-pin reset	Sets external-reset pin to Low
Software reset	Writes 0 at RST (bit 4) of STBC
Watchdog reset	Overflows watchdog timer
Power-on reset	Turns power on

When the power-on reset and reset during the stop mode are used, the oscillation stabilization time is needed after the oscillator operates. The time-base timer or watch prescaler controls this stabilization time. Consequently, the operation does not start immediately even after canceling the reset.

However, if Power-on Reset Disabled is selected by the mask option, no oscillation stabilization time is required in any state after external pins have been released from the reset.

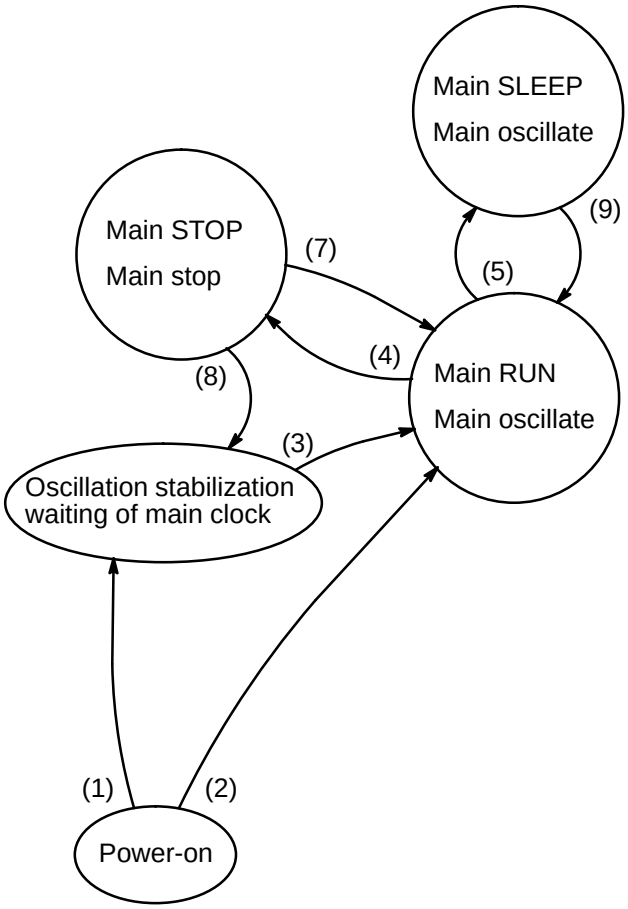
Note: If Power-on Reset Disabled is selected, the RST pin must be kept Low until the oscillation stabilization time selected by the option has elapsed after power on.

(5) Single clock

The single clock module can be selected by the mask option. In the single clock operation, the functions are the same as those of the double clock module except that the subclock mode cannot be set. Therefore, the input pin X0A of the subclock should be connected to GND. The X1A pin must be kept open.

Note: For microcontrollers with a built-in booster (MB89150A), do not select the single clock module. The double-clock module should be used.

(a) State transition diagram

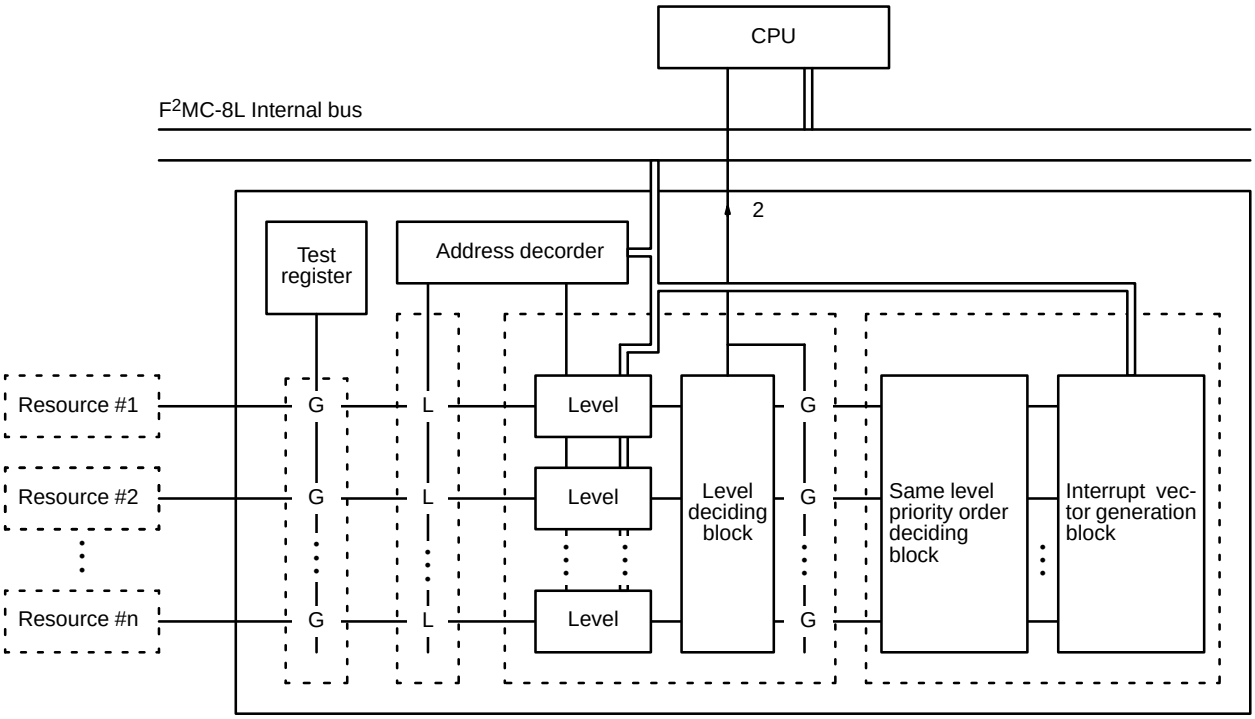


(1) When power-on reset option selected
(2) When power-on reset option not selected
(3) After oscillation stabilized
(4) Set STP bit to 1.
(5) Set SLP bit to 1.
(7) External reset when power-on reset option not selected
(8) External reset or interrupt when power-on reset option selected
(9) External reset or interrupt

2.1.6 Interrupt controller

The interrupt controller for the F^{2}MC-8L is located between the CPU and each resource. This controller receives interrupt requests from the resources, assigns priority to them, and transfers the priority to the CPU; it also decides the priority of same-level interrupts.

(1) Block diagram



(2) Register list

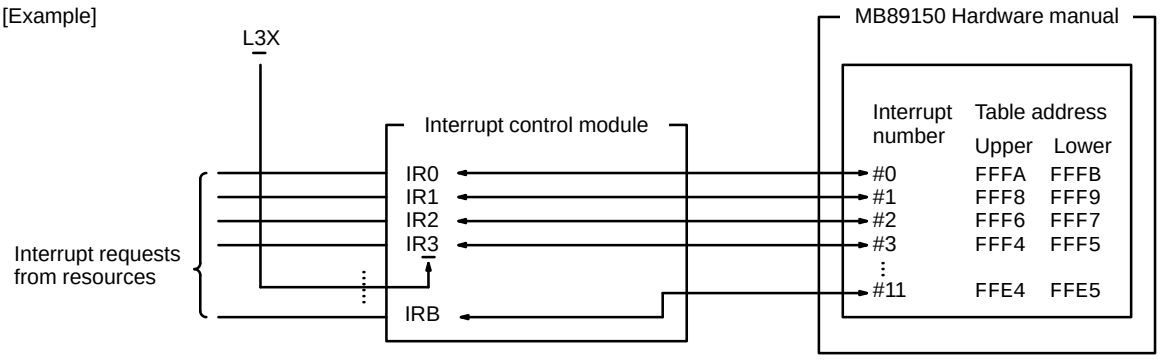
Address	7 6	5 4	3 2	1 0	Name	[Abbreviation]	(Initial value)
007C$_H$	L31 L30	L21 L20	L11 L10	L01 L00	Interrupt-level register #1	[ILR1]	(1111 1111)
007D$_H$	L71 L70	L61 L60	L51 L50	L41 L40	Interrupt-level register #2	[ILR2]	(1111 1111)
007E$_H$	LB1 LB0	LA1 LA0	L91 L90	L81 L80	Interrupt-level register #3	[ILR3]	(1111 1111)
007F$_H$	— —	— —	— —	EV EN	Interrupt-test register	[ITR]	(---- --00)

(2) Description of registers

- Interrupt level register (ILRX: Interrupt Level Register X)

	7	6	5	4	3	2	1	0		
1LR1	L31	L30	L21	L20	L11	L10	L01	L00	W	When reset (11111111)
1LR2	L71	L70	L61	L60	L51	L50	L41	L40	W	When reset (11111111)
1LR3	LB1	LB0	LA1	LA0	L91	L90	L81	L80	W	When reset (11111111)

The ILRx sets the interrupt level of each resource. The digits in the center of each bit correspond to the interrupt numbers.



When an interrupt is requested from a resource, the interrupt controller transfers the interrupt level based on the value set at the 2 bits of the ILRX corresponding to the interrupt to the CPU. The relationship between the 2 bits of the ILRX and the required interrupt levels is as follows:

Lx1	Lx0	Required interrupt level
0	X	1
1	0	2
1	1	3 (None)

- Interrupt test register (ITR)

	7							0	
ITR	---	---	---	---	---	---	※	※	–

The ITR is used for testing. Do not access it.

(4) Description of operation

• Interrupt functions

The MB89150 series of microcontrollers have 12 inputs for interrupt requests from each resource. The interrupt level is set by 2-bit registers corresponding to each input. When an interrupt is requested from a resource, the interrupt controller receives it and transfers the contents of the corresponding register to the CPU. The interrupt to the device is processed as follows:

(1) An interrupt source is generated inside each resource.

(2) If an interrupt is enabled, an interrupt request is output from each resource to the interrupt controller by referring to the interrupt-enable bit inside each resource.

(3) After receiving this interrupt request, the interrupt controller determines the priority of simultaneously-requested interrupts and then transfers the interrupt level for the applicable interrupt to the CPU.

(4) The CPU compares the interrupt level requested from the interrupt controller with the IL bit in the processor status register.

(5) As a result of the comparison, if the priority of the interrupt level is higher than that of the current interrupt processing level, the contents of the I-flag in the same processor status register are checked.

(6) As a result of the check in step (5), if the I-flag is enabled for an interrupt, the contents of the IL bit are set to the required level. As soon as the currently-executing instruction is terminated, the CPU performs the interrupt processing and transfers control to the interrupt-processing routine.

(7) When an interrupt source is cleared by software in the user's interrupt processing routine, the CPU terminates the interrupt processing.

Figure 2.9 outlines the interrupt operation for the MB89150 series of microcontrollers.

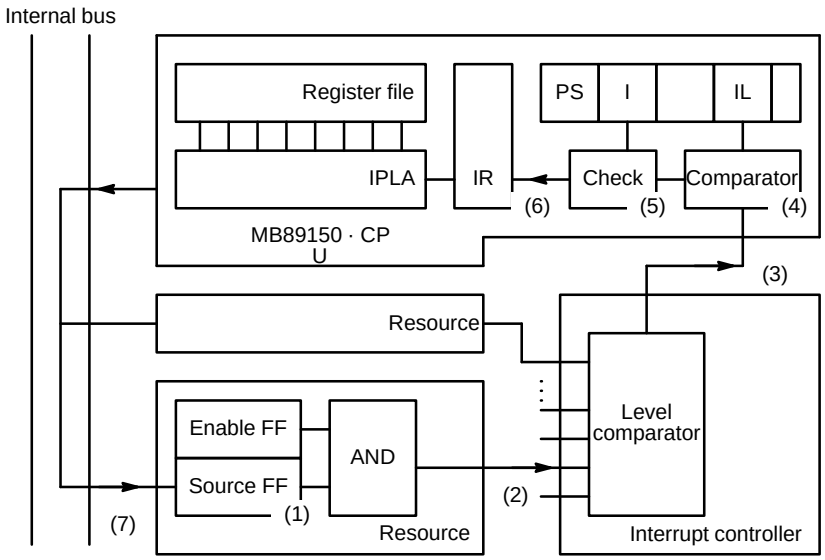


Fig. 2.9 Interrupt-processing Flowchart

2.2 Resource Functions

2.2.1 I/O ports

- The MB89150 series of microcontrollers have six parallel ports (43 ports). Ports 0, 1, and 2 serve as 8-bit I/O ports; ports 4 and 5 serve as 8-bit output-only ports; and port 3 serves as a 3-bit output-only port.
- Each port is also used as the I/O pin for the resource.

(1) List of port functions

Table 2-3 List of Port Functions

Pin name	Input type	Output type	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
P00 to P07	CMOS	CMOS push-pull	Parallel port 0	P07	P06	P05	P04	P03	P02	P01	P00
	Hysteresis		Resource	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20
P10 to P17	CMOS	CMOS push-pull	Parallel port 1	P17	P16	P15	P14	P13	P12	P11	P10
	Hysteresis		Resource					INT13	INT12	INT11	INT10
P20 to P27	CMOS	N-ch open drain	Parallel port 2	P27	P26	P25	P24	P23	P22	P21	P20
	Hysteresis		Resource	BUZ		SCK	SO	SI	TO		EC
P30 to P32	—	CMOS push-pull	Parallel port 3						P32	P31	P30
			Resource						C0	C1	RCO
P40 to P47	—	N-ch open drain	Parallel port 4	P47	P46	P45	P44	P43	P42	P41	P40
			Resource	SEG27	SEG26	SEG25	SEG24	SEG23	SEG22	SEG21	SEG20
P50 to P57	—	N-ch open drain	Parallel port 5	P57	P56	P55	P54	P53	P52	P51	P50
			Resource	SEG35	SEG34	SEG33	SEG32	SEG31	SEG30	SEG29	SEG28

Notes:

1. Ports 4 and 5 serve as output ports only when they are selected by the mask option for use as ports.
2. Ports 3 (excluding port 30) serves as an output ports only for microcontrollers without a built-in booster.

(2) Port registers

Table 2-4 Port Registers

Register name	Read/Write	Address	Initial value
Port-0 data register (PDR0)	R/W	0000_H	$XXXXXXXX_B$
Port-0 data direction register (DDR0)	W	0001_H	00000000_B
Port-1 data register (PDR1)	R/W	0002_H	$XXXXXXXX_B$
Port-1 data direction register (DDR1)	W	0003_H	00000000_B
Port-2 data register (PDR2)	R/W	0004_H	$XXXXXXXX_B$
Port-2 data direction register (DDR2)	W	0005_H	00000000_B
Port-3 data register (PDR3)	R/W	$000C_H$	$XXXXX111_B$
Port-4 data register (PDR4)	W	$000E_H$	11111111_B
Port-5 data register (PDR5)	R/W	$000F_H$	11111111_B

(3) Description of functions

P00 to P07 CMOS-type I/O ports

P10 to P17 CMOS-type I/O ports

- Switching input and output

These ports have a data-direction register (DDR) and port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input.

- Operation for output port (DDR = 1)

The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

- Operation for input port (DDR = 0)

When settings the input, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

- State when reset

The DDR is initialized to 0 by resetting and the output impedance goes High at all bits. The PDR is not initialized by resetting. Therefore, set the value of the PDR before setting the DDR to output.

• State in watch and stop modes

With the SPL bit of the standby-control register set to 1, in the watch or stop mode, the output impedance goes High irrespective of the value of the DDR.

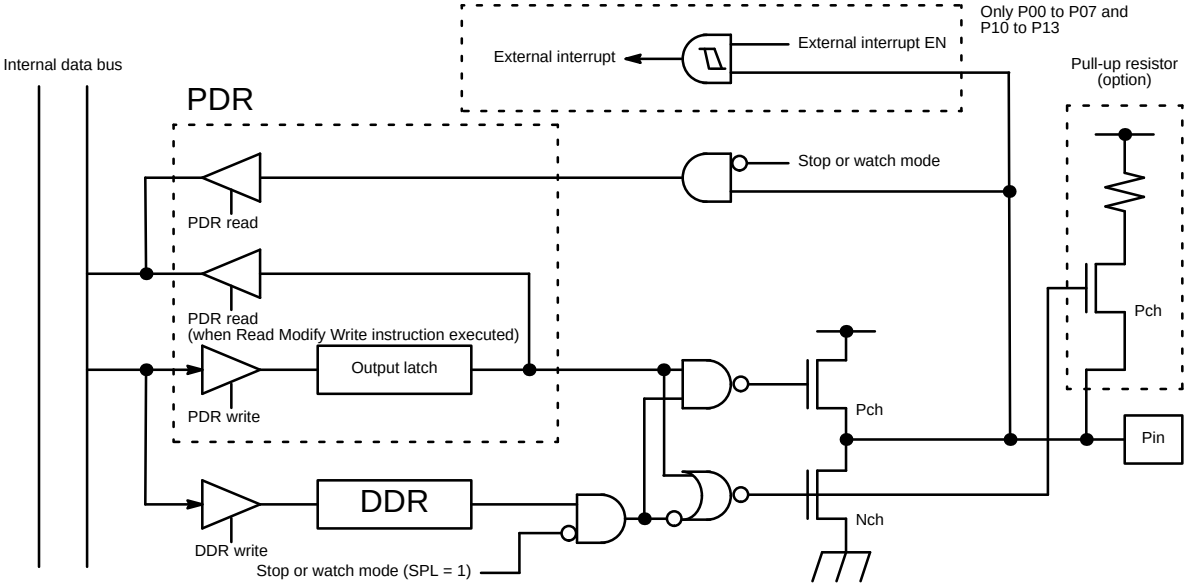


Fig. 2.10 Ports 0 and 1

P20 to P27 N-ch open-drain type I/O ports (also used as resource input/output)

- Switching input and output

This port has a data-direction register (DDR) and a port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input.

- Operation for output port (DDR = 1)

The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

- Resource output operation (DDR = 1)

When using as the resource output, setting is performed by the resource output enable bit. (See the description of each resource.) Even if the output from each resource is enabled, the read value of the port is effective except when the Read Modify Write instruction is read, so the pin state can be checked.

- Operation for input port (DDR = 0)

When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

When the DDR is initialized to 0 by reset, the output impedance of all bits goes High. Since the PDR is not initialized by reset, set the value before setting the DDR to output.

- State when reset

When reset, the DDR is initialized to 0 and the output impedance goes High at all bits. When reset, the PDR is not initialized. Therefore, set the value of the PDR before setting the DDR to output.

- State in watch and stop modes

With the SPL bit of the standby-control register set to 1, in the watch or stop mode, the output impedance goes High irrespective of the value of the DDR.

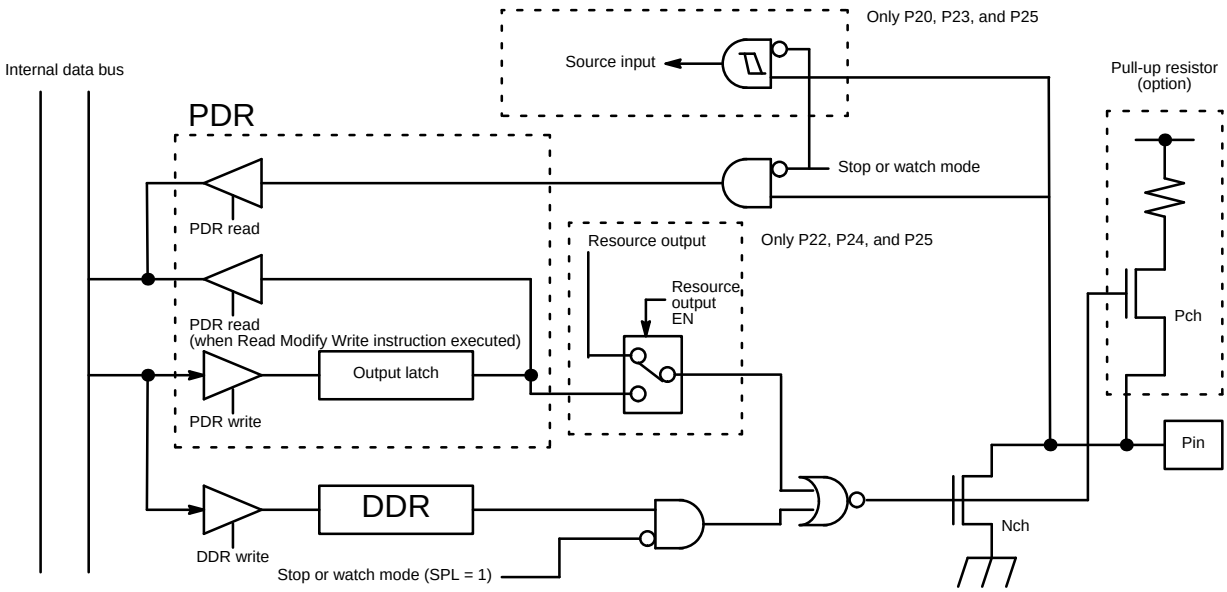


Fig. 2.11 Port 2

P30/RCO CMOS type output-only ports (also used as resource output)

- Operation for output port

The value written at the PDR is output to the pin. When the PDR is read at this port, the contents of the output latch can always be read instead of the pin state.

- Operation for resource output

When using as the resource output, setting is performed by the resource output enable bit. (See the description of each resource.) Even if the output from each resource is enabled, the read value of the port is effective except when the Read Modify Write instruction is read, so the pin state can be checked.

- State when reset

At reset, the PDR is initialized to 1 and the output transistors of all bits are turned off.

- State in stop mode

When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

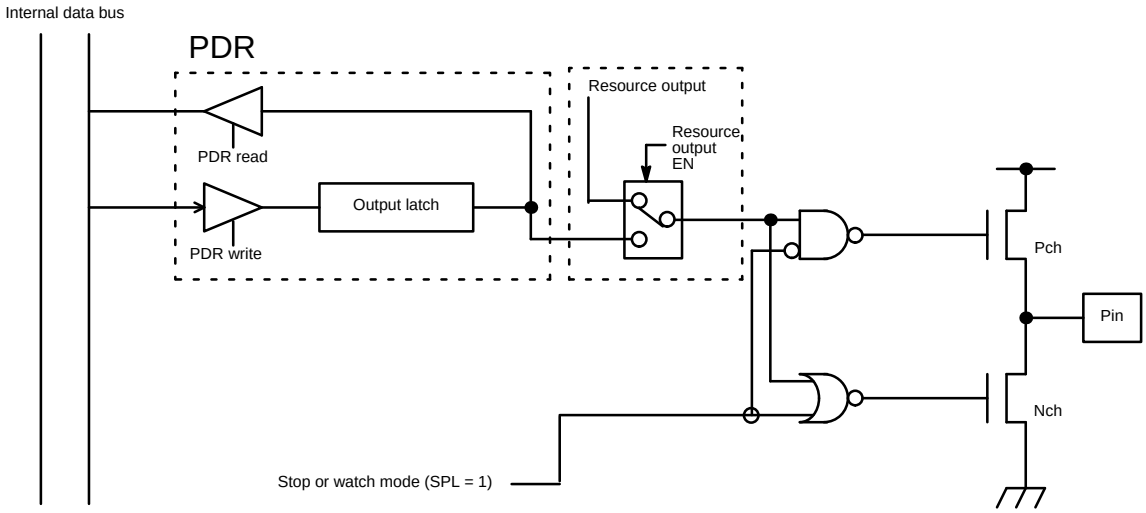


Fig. 2.12 P30

P31 and 32 N-ch open-drain type output ports (used as pins for connecting capacitors C0 and C1 when selected by mask option)
P40 to P47 N-ch open-drain-type output-only ports (also used as segment output)
P50 to P57 N-ch open-drain-type output-only ports (also used as segment output)

- Operation for output port

The value written at the PDR is output to the pin. When the PDR is read in this port, usually, the contents of the output latch is read instead of the value of the pin.

- Segment output

When selected by the mask option for use as segment pins, ports 4 and 5 serve as segment outputs. In this case, they cannot be used as output ports.

P31 and P32 serve as capacitor connection pins for microcontrollers with a built-in booster (MB89150A). They cannot be used as output ports. P31 and P32 are not available for selection of a pull-up resistor.

- State when reset

The PDR is initialized to 1 at reset, so the output register is turned off at all bits.

- State in stop mode

When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

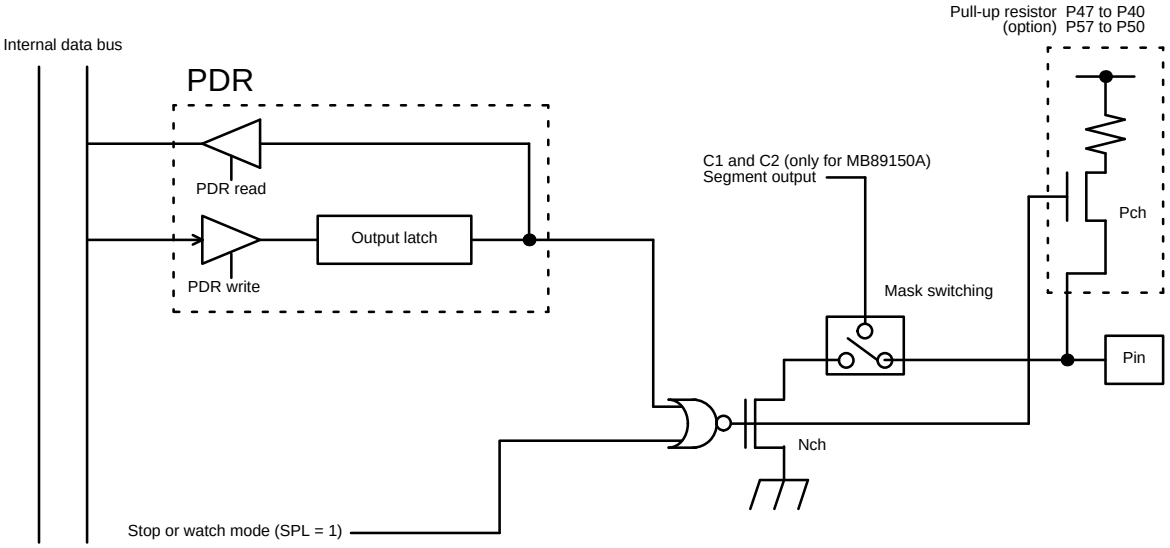


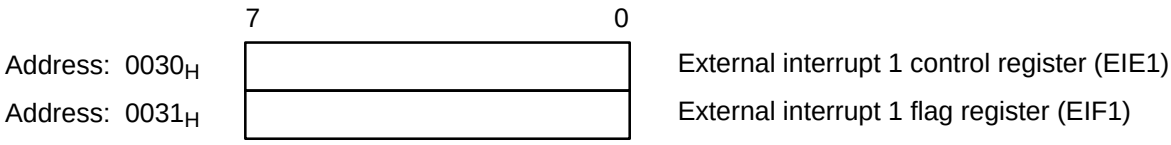
Fig. 2.13 P31, P32, Port 4, and Port 5

2.2.2 External interrupt 1

The external interrupt 1 is controlled by the external interrupt control and external interrupt flag registers.

- Four external interrupt inputs
- An interrupt request is output at the falling edge of the input signal.
- Inverting an input signal outputs an interrupt request at the rising edge.
- Usable as wake-up input

(1) Registers



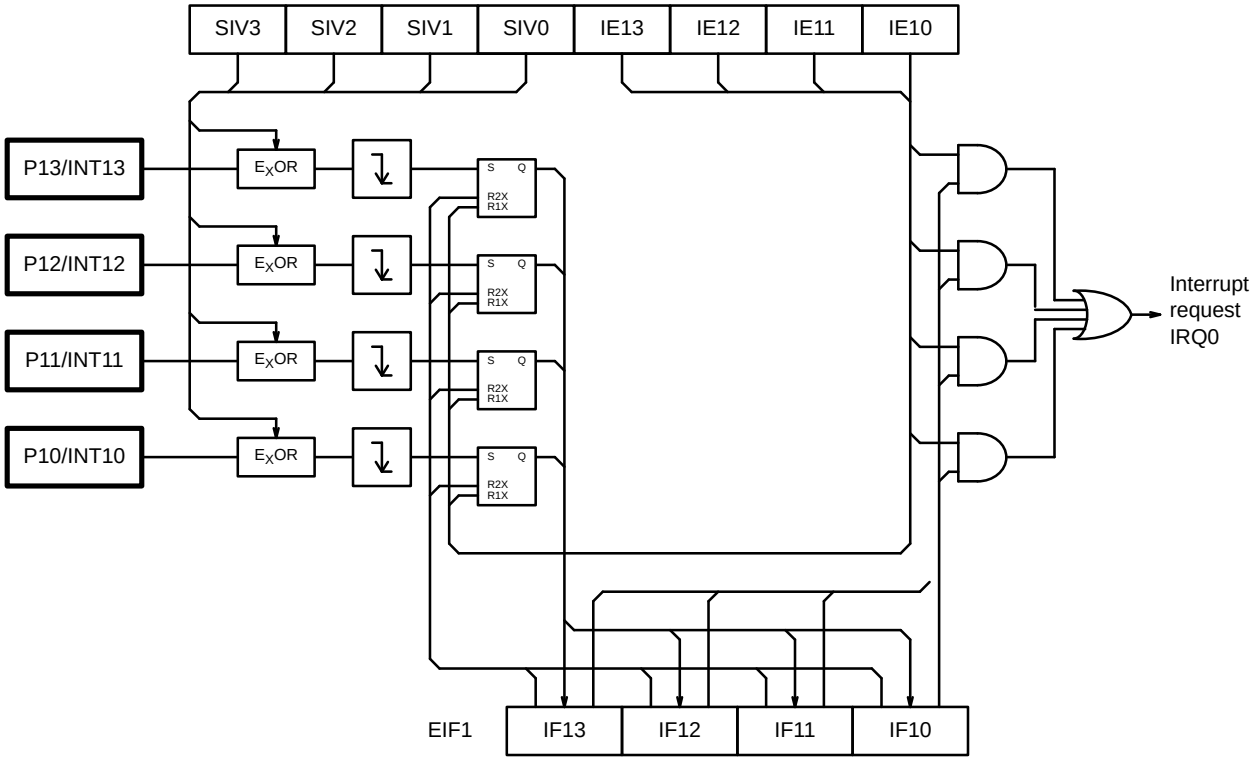


Fig. 2.14 External Interrupt 1 Block Diagram

(2) Description of registers

(a) External-interrupt 1 control register (EIE1)

Address: 0030_H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Initial value
SIV3	SIV2	SIV1	SIV0	IE13	IE12	IE11	IE10	0000 0000B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7]: SIV3
[Bit 6]: SIV2
[Bit 5]: SIV1
[Bit 4]: SIV0
These bits are used to invert external interrupts EI13 to EI10.

0	External interrupt signal not inverted
1	External interrupt signal inverted

[Bit 3]: IE13
[Bit 2]: IE12
[Bit 1]: IE11
[Bit 0]: IE10
These bits are used to enable external interrupts EI13 to EI10.

0	External interrupt disabled (edge detect flag initialized)
1	External interrupt enabled

Note: The interrupt flag may be turned on immediately after an interrupt is enabled or an interrupt input is inverted.

(b) External interrupt 1 flag register (EIF1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0031_H	—	—	—	—	IE13	IE12	IE11	IE10	---- 0000_B
					(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 3]: IF13
[Bit 2]: IF12
[Bit 1]: IF11
[Bit 0]: IF10
These bits are used to detect the falling edges of EI13 to EI10.

(When write)

0	Falling edge detect flag cleared
1	No operation

(When read)

0	Falling edge not detected
1	Falling edge detected

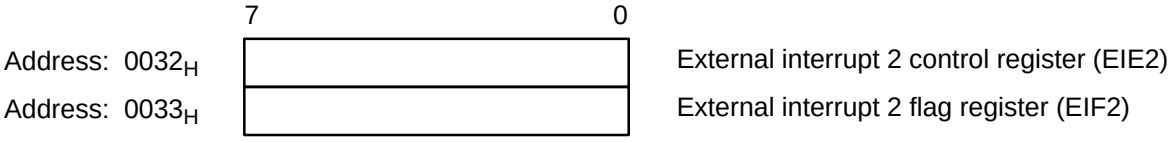
If the interrupt enable bits (IE13 to IE10) of the external interrupt 1 control register (EIE1) are 1, an interrupt request is output to the CPU when the corresponding falling edge detect flag bits (IF13 to IF10) are set to 1.

2.2.3 External interrupt 2

External interrupt 2 is controlled by the external interrupt control and external interrupt flag registers.

- Eight external interrupt input pins
- An interrupt request is output by Low-level input signals.
- Also usable as wake-up input

(1) Registers



(2) Block diagram

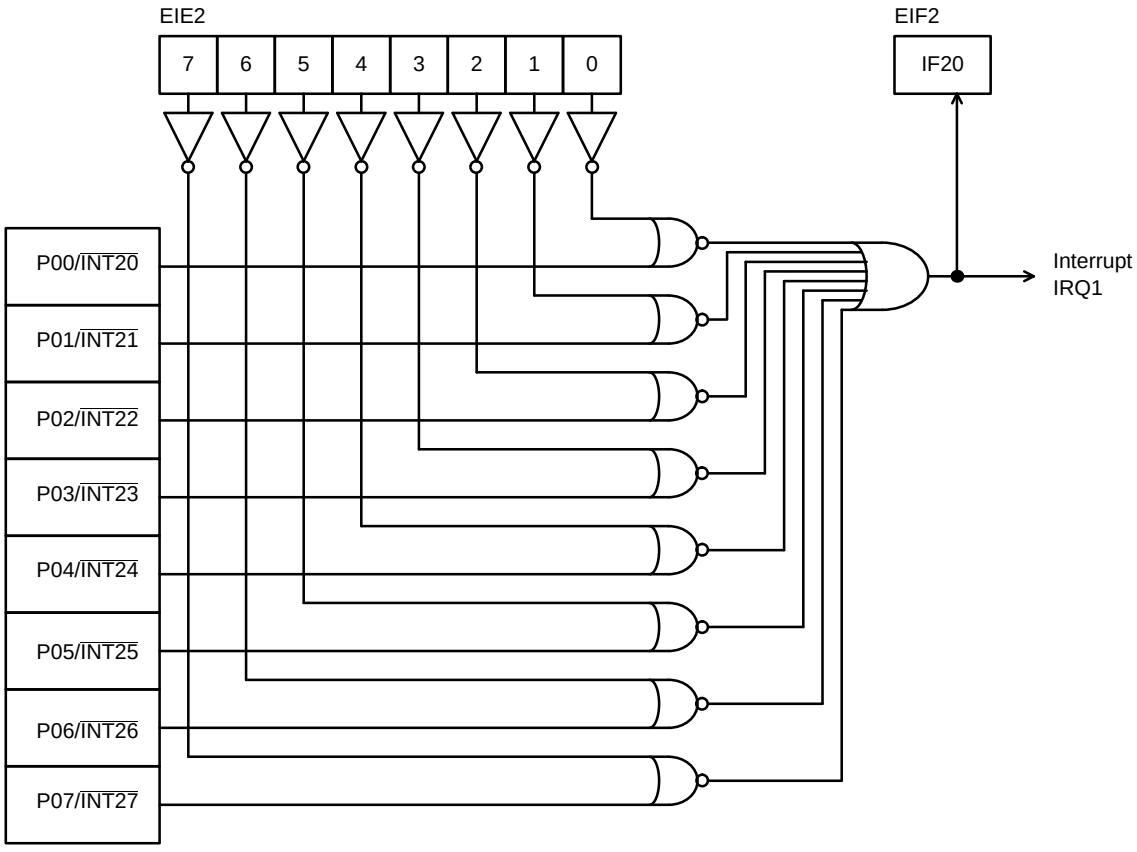


Fig. 2.15 External Interrupt 2 Block Diagram

(2) Description of registers

(a) External interrupt 2 control register (EIE2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address:	IE27	IE26	IE25	IE24	IE23	IE22	IE21	IE20	$0000\ 0000_B$
0032_H	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7]: IE27
[Bit 6]: IE26
[Bit 5]: IE25
[Bit 4]: IE24
[Bit 3]: IE23
[Bit 2]: IE22
[Bit 1]: IE21
[Bit 0]: IE20
These bits are used to enable external interrupt of INT27 to INT20.

0	External interrupt disabled
1	External interrupt enabled

(b) External interrupt 2 flag register (EIF2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0033_H	—	—	—	—	—	—	—	IF20	$---- ---0_B$
	—	—	—	—	—	—	—	(R/W)	

[Bit 0]: IF20
This bit is used to detect LOW level.

(When write)

0	Clears flag for detecting LOW level
1	No operation

(When read)

0	No LOW level input
1	LOW level input detected

If the interrupt enable bits (IE27 to IE20) of the external interrupt 2 control register (EIE2) are 1, the Low-level detect flag bit (IF20) is set to 1 and an interrupt request is output to the CPU when a Low level is input to the port corresponding to this bit.

Note: Unlike other resources, even if the external interrupt 2 control register is disabled for an interrupt, it keeps generating interrupts until the interrupt source is cleared. Therefore, always clear the interrupt source after disabling an interrupt.

2.2.4 8/16-bit timer (timer 1 and timer 2)

- Three internal clock pulses and one external clock pulse can be selected.
- Operation in 8-bit 2-ch mode or 16-bit 1-ch mode can be selected.
- A square-wave output function is included.

(1) Registers

	7	0	
Address: 0018_H	T2CR #2		Timer-2 control register (T2CR)
Address: 0019_H	T1CR #1		Timer-1 control register (T1CR)
Address: $001A_H$	T2DR #2		Timer-2 data register (T2DR)
Address: $001B_H$	T1DR #1		Timer-1 data register (T1DR)

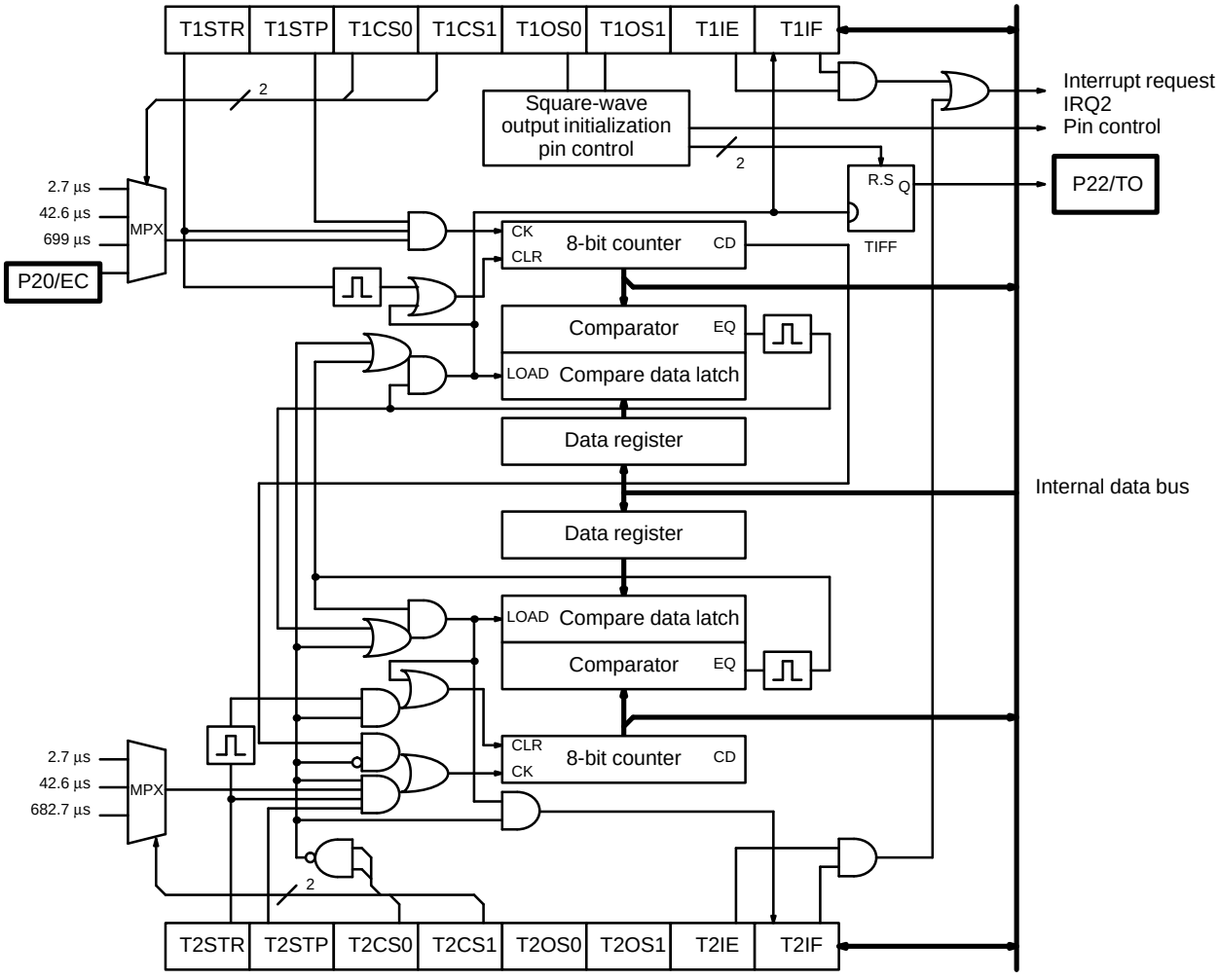


Fig. 2.16 8/16-bit Timer Block Diagram

(2) Description of registers

(a) Timer 1 control register (T1CR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0019_H	T1IF	T1IE	T1OS1	T1OS0	T1CS1	T1CS0	S1STP	S1STR	$X000\ XXX0_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7]: T1IF
This bit is used for the flag requesting an interrupt.

(When write)

0	Interrupt request flag clear
1	No operation

(When read)

0	No interrupt request
1	Interval interrupt request

1 is always read when the Read Modify Write instruction is executed.

[Bit 6]: T1IE
This bit is used to enable an interrupt.

0	Interrupt disabled
1	Interrupt enabled

[Bit 5]: T1OS1
[Bit 4]: T1OS0
These bits are used to control the square-wave output when the timer stops. See page 2-37 for the setting of the square-wave output.

T1OS1	T1OS0	
0	0	The output port [P22 (TO)] serves as a general-purpose port.
0	1	Set the initial value of the timer square wave output to Low.
1	0	Set the initial value of the timer square wave output to High.
1	1	Set the square wave output pin of the timer to the set data value.

The square-wave output is set to the set data value when STR1 is 0.

[Bit 3]: T1CS1
[Bit 2]: T1CS2
These bits are used to select clock source.

T1CS1	T1CS0	Clock cycle time (When 1/2 of 3 MHz is selected)		
0	0	Internal clock	2 instruction cycle	2.7 [µs]
0	1		32 instruction cycle	42.6 [µs]
1	0		512 instruction cycle	682.7 [µs]
1	1	External clock	—	

[Bit 1]: T1STP
This bit is used to stop the timer.

0	Continue counting without clearing the counter.
1	Suspend counting.

[Bit 0]: T1STR
This bit is used to start the timer.

0	Stop counting.
1	Clear the counter to start counting.

Note: When using the timer 1 in the 8-bit 1-ch mode, set bits 3 and 2 of the timer-2 control register to a value other than 11. Use of the timer without setting this register causes a malfunction.

(b) Timer-2 control register (T2CR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0018_H	T2IF	T2IE	T2OS1	T1OS0	T2CS1	T2CS0	T2STP	T2STR	$X000\ XXX0_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7]: T2IF
This bit is used for the flag requesting an interrupt.

(When write)

0	Interrupt request flag cleared
1	No operation

(When read)

0	No interrupt request
1	Interval interrupt request

1 is always read when the Read Modify Write instruction is executed.

[Bit 6]: T21E
This bit is used to enable interrupt.

0	Interrupt disabled
1	Interrupt enabled

[Bit 5]: T2OS1
[Bit 4]: T2OS0
These are empty bits. Always write 0.

[Bit 3]: T2CS1
[Bit 2]: T2CS0
These bits are used to select timer clock source.

T2CS1	T2CS0	Clock cycle time (When 1/2 of 3 MHz is selected)		
0	0	Internal clock	2 instruction cycle	2.7 [µs]
0	1		32 instruction cycle	42.6 [µs]
1	0		512 instruction cycle	682.7 [µs]
1	1	16-bit mode	—	

[bit 1]: T2STP
This bit is used to stop the timer.

0	Counting is continued without clearing the counter.
1	Counting is suspended

[Bit 0]: T2STR
This bit is used to start the timer.

0	Counting is stopped
1	The counter is cleared to start counting.

(c) Timer-1 and timer-2 data registers (T1DR, T2DR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $001B_H$									XXXX XXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $001A_H$									XXXX XXXX$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

The write data is used as the set value of the interval time, and the read data is used as the value of the counter.

(3) Description of operation

(a) 8-bit internal clock mode

In the 8-bit internal clock mode, three internal clock pulses can be selected by setting the clock source specifying bits (T1CS1 and T1CS0) and (T2CS1 and T2CS0) of the timer control registers (T1CR and T2CR). The timer data registers (T1DR and T2DR) are used to set the interval time. To start the timer, set the interval time at the timer data register, write 1 at the timer start bits (T1STR and T2STR) of the timer control register to clear the counter to 00H , and load the value of the timer data register into the compare latch. Then, counting up is started.

When the value of the counter agrees with that of the timer data register, the interval interrupt request flag bits (T1IF and T2IF) are set to 1. At this time, the counter is cleared to 00H and the value of the timer data register is reloaded into the compare latch. Then, counting up is continued. If the interrupt enable bits (T1IE and T2IE) are 1, an interrupt request is output to the CPU.

Assuming the set value is n and the selected clock pulse is F, the interval time (T) can be calculated by the following equation:

$T = \phi \times (n + 1)$ [μs]

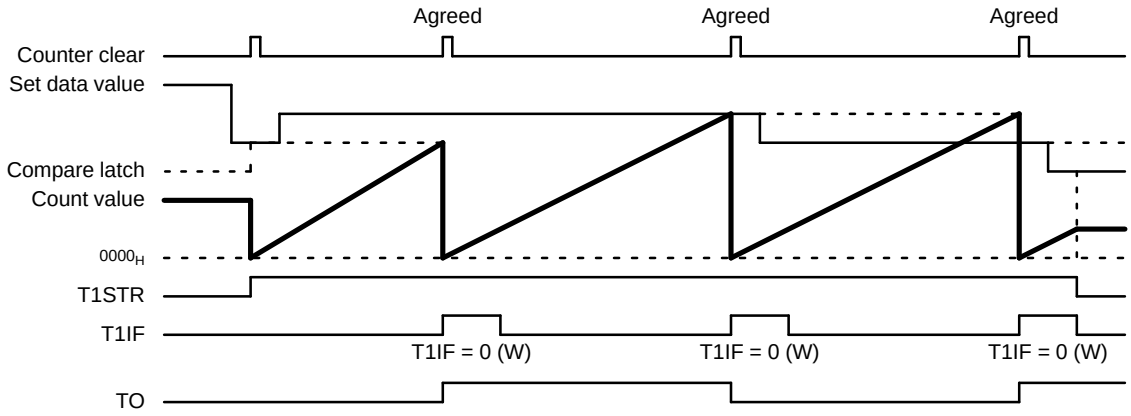


Fig. 2.17 Internal Clock Mode Operation Description Diagram

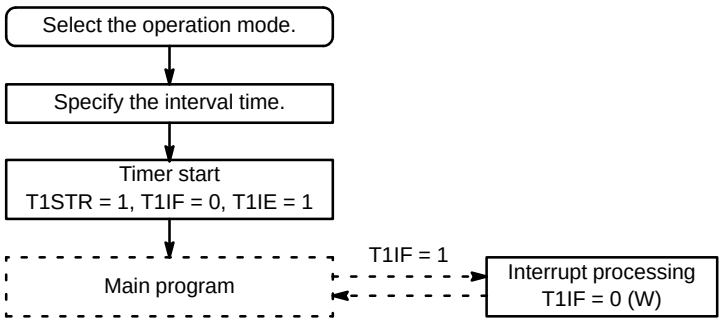


Fig. 2.18 Timer Setting Flow

(b) Initializing square-wave output

The square-wave output can be set to any value only when the timer stops (T1STR = 0).

To set, proceed as follows:

1. Write the set values (01 and 10) at the initialize bits (T1OS1 and T1OS0) of the square wave output. The values are held in the level latch shown in the figure below and not output to the pin. (Note that the previous square wave state is output to the pin.)
2. Write 11 at the same bits. This initializes the square wave output to the set value. If the T1STR bit is set to 0, the square wave output of the pin is set to the set value in 1 during this write cycle. The pin state of the square wave output in 1 and 2 is shown below.
3. Start the timer when the T1STR bit is 1.

These initialize bits can be set by the bit manipulation instruction.

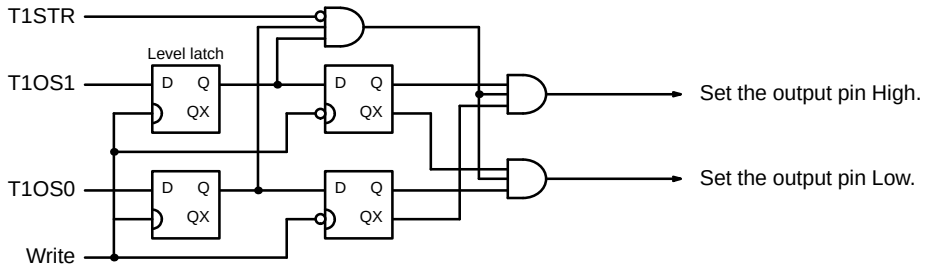
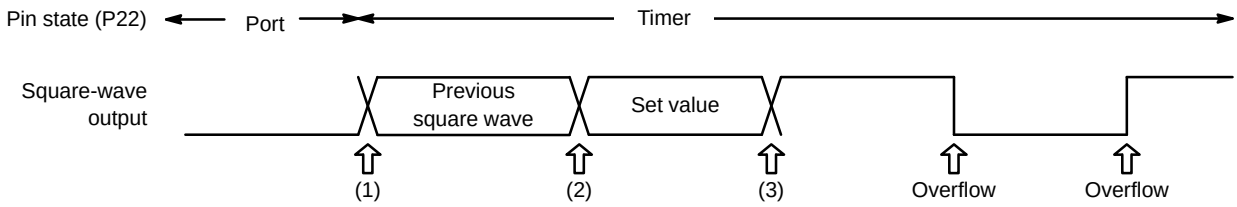


Fig. 2.19 Initialization of Equivalent Circuit



(c) 8-bit external clock mode

In the 8-bit external clock mode, the external clock input can be selected by setting the clock source select bits (T1CS1 and T1CS0) of the timer 1 control register (T1CR). External clock input pin of timer 1 is P20 (EC).

To start the timer, write 1 at the timer start bit (T1STR) of the T1CR to clear the counter.

When the value of the counter agrees with that of the timer data register, the interval interrupt request flag bit (T1IF) is set to 1. At this time, if an interrupt is enabled (T1IE = 1), an interrupt request is output to the CPU.

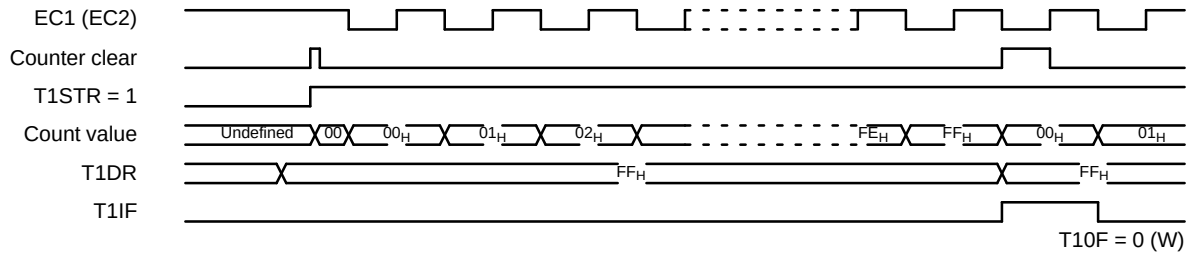


Fig. 2.20 External Cock Mode Operation Description Diagram

(d) Precautions for use of timer stop bit

If the timer is stopped by the timer start bit after being suspended by the timer stop bit, the input clock pulse to the timer may increment the count value by 1 as shown in Figure 2.20 (the count value is not incremented when the input clock pulse is High but incremented when it is Low). Therefore, if the timer is suspended by the timer stop bit, read the counter and then write 0 at the timer start bit.

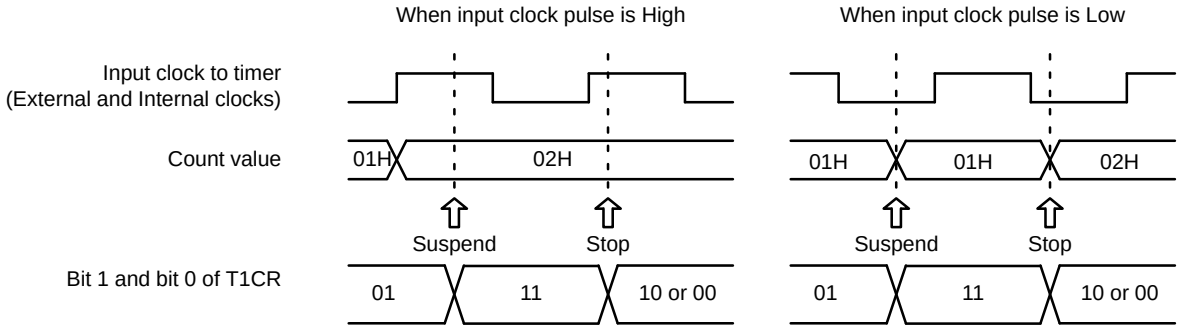


Fig. 2.21 Operation Diagram when Timer Stop Bit is Used

(e) 16-bit mode

In the 16-bit mode, each bit of the timer control registers is as shown below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0019_H	T1IF	T1IE	T1OS1	T1OS0	T1CS1	T1CS0	T1STP	T1STR
Address: 0018_H	T2IF	T2IE	T2OS1	T2OS0	T2CS1	T2CS0	T2STP	T2STR
	No operation		Set to 00		Set to 11		No operation	

In the 16-bit mode, write 11 at the T2CS1 and T2CS0 bits of the T2CR and set 0 at the T2OS1 and T2OS0 bits.

When in the 16-bit mode, the timer is controlled by the T1CR. The timer data registers T2DR and T1DR use the upper and lower bytes, respectively.

The clock source is selected by the T1CS1 and T1CS0 bits of the T1CR. To start the timer, write 1 at the T1STR bit of the T1CR to clear the counter.

If the value of the counter agrees with that of the timer data register, the T1IF bit is set to 1. At this time, an interrupt request is output to the CPU if the T1IE bit is 1.

Note: To read the value of the counter in the 16-bit mode, always read the value twice to check that it is valid and use the data.

(f) Starting and suspending timer

The timer 2 is the same as timer 1. Therefore, an explanation is given using timer 1.

(1) Clearing counter to start counting

When the T1STR bit is 0, write 01 at the T1STP and T1STR bits, respectively. The timer is cleared at the edge where the T1STR bit is set from 0 to 1 to start counting.

(2) Suspending timer to start counting without clearing counter

To suspend counting, set the T1STP and T1STR bits to 11. To start counting from the suspended state without clearing the counter, set the T1STP and T1STR bits from 11 to 01.

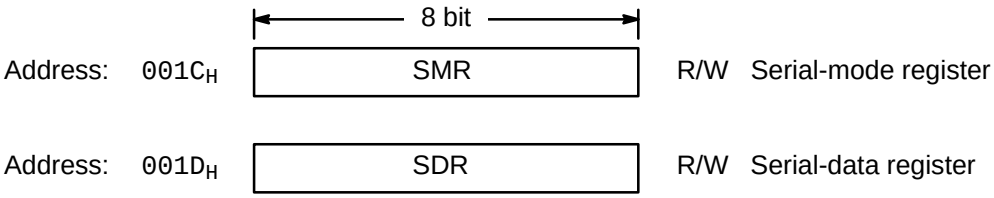
The state of the timer according to the setting conditions of T1STP and T1STR bits and the operation of the timer when started from the suspended state (when T1STP and T1STR bits = 01) are as follows.

T1STP	T1STR	Timer state setting	Operation of timer when started from timer state setting (bits 1 and 0 = 01)
0	0	Counting is stopped	Counter is cleared to start counting.
0	1	Counting is started	Counting is continued
1	0	Counting is stopped	Counter is cleared to start counting.
1	1	Counting is suspended	Counting is continued without clearing counter.

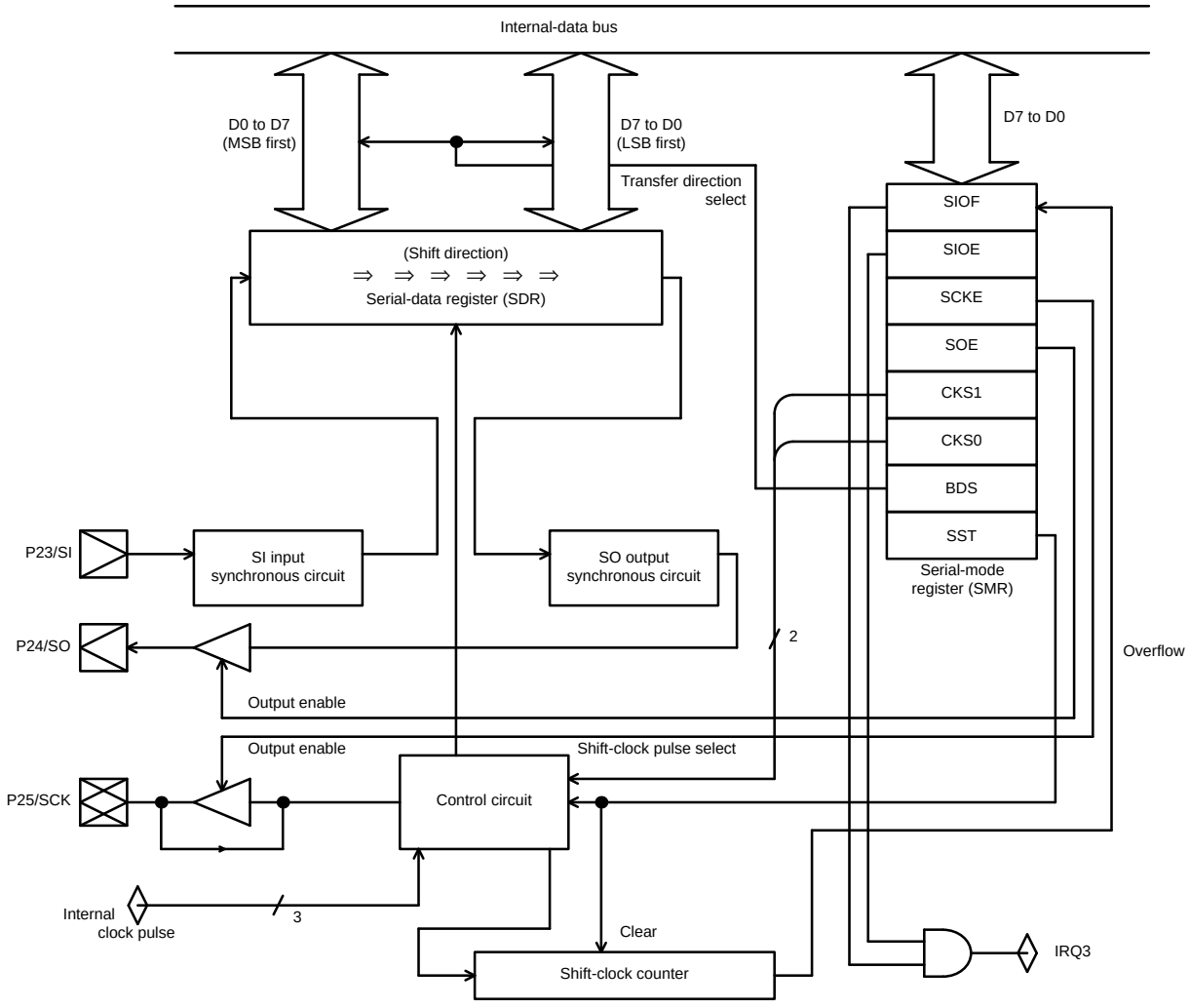
2.2.5 8-bit serial I/O

- 8-bit serial data transfer is possible by the clock synchronous method.
- LSB first or MSB first can be selected for data transfer.
- Four shift-clock modes (three internal and one external) can be selected.

(1) Registers



(2) Block diagram



(3) Description of registers

(a) Serial-mode register (SMR)

The SMR is used to control serial I/O.

Address: $001C_H$

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
SIOF	SIOE	SCKE	SOE	CKS1	CKS0	BDS	SST	$0000\ 0000_B$
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] SIOF: Serial I/O interrupt-request flag
Bit 7 indicates the serial I/O transfer state.
The meaning of each bit when reading is as follows:

0	Serial data transfer not terminated
1	Serial data transfer terminated

Note that 1 is always read when the Read Modify Write instruction is read. If this bit is set when an interrupt is enabled (SIOE = 1), an interrupt request is output to the CPU.
The meaning of each bit when writing is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

The end-of-transfer decision may be made by either the SST bit (bit 0) of the SMR or by this bit.

[Bit 6] SIOE: Serial I/O interrupt-enable bit
Bit 6 is used to enable a serial I/O interrupt request.

0	Serial I/O interrupt-output disable
1	Serial I/O interrupt-output enable

[Bit 5] SCKE: Shift-clock output-enable bit
Bit 5 is used to control the shift-clock I/O pins.

0	General-purpose port pin (P25) or SCK input pin
1	SCK (shift clock) output pin

When using the P25/SCK pin as an external clock, always set the DDR to input (bit 5 of PDR2 = 0).

[Bit 4] SOE: Serial-data output-enable bit
Bit 4 is used to control the output pin for serial I/O.

0	General-purpose port pin (P24)
1	SO (serial data) output pin

When using P23/SI pin for the external clock, always set the DDR to input (bit 3 of DDR2 = 0).

[Bits 3 and 2] CKS1 and CKS0: Shift-clock select bits
Bits 3 and 2 are used to select the serial shift-clock modes.

CKS1	CKS0	Mode	(Clock rate)	SCK
0	0	Internal shift-clock mode	(instruction cycle) × 2	Output
0	1	Internal shift-clock mode	(instruction cycle) × 8	Output
1	0	Internal shift-clock mode	(instruction cycle) × 32	Output
1	1	External shift-clock mode	SCK	Input

[Bit 1] BDS: Transfer direction select bit
At serial data transfer, Bit 1 is used to select whether data transfer is performed from the least significant bit first (LSB first) or from the most significant bit first (MSB first).

0	LSB first
1	MSB first

Note that when this bit is rewritten after writing data to the SDR, the data become invalid.

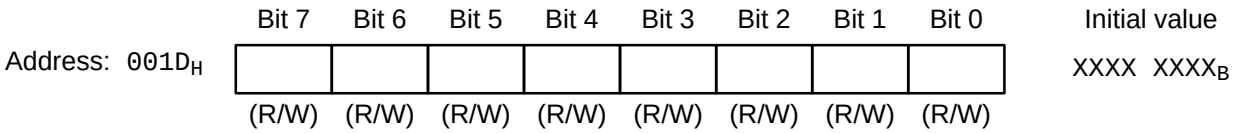
[Bit 0] SST: Serial I/O transfer-start bit
Bit 0 is used to start serial I/O transfer. The bit is automatically cleared to 0 when transfer is terminated.

0	Serial I/O transfer stop
1	Serial I/O transfer start

Before starting transfer, ensure that transfer is stopped (SST = 0).

(b) Serial-data register (SDR)

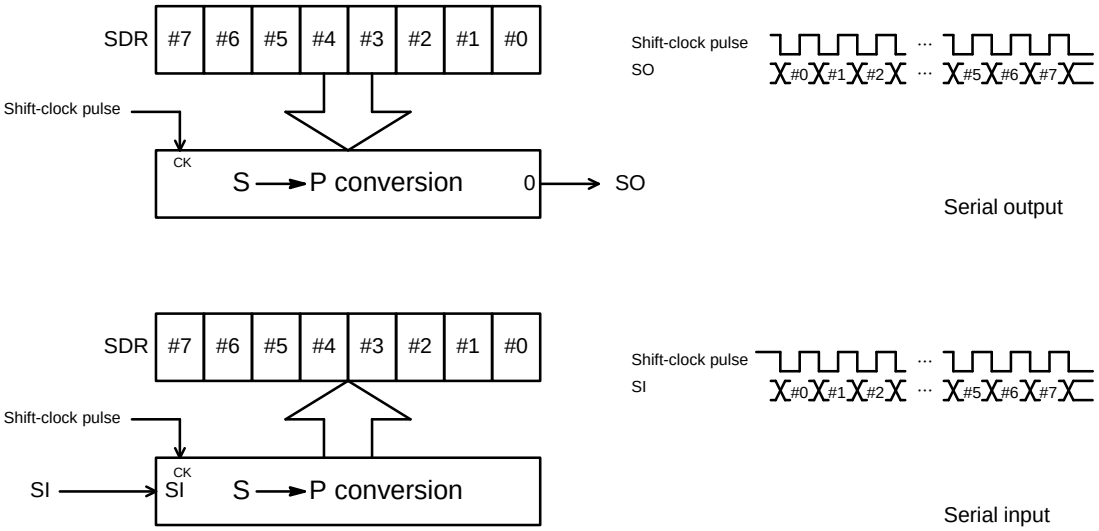
This 8-bit register is used to hold serial I/O transfer data. Do not write data to this register during the serial I/O operation.



(4) Description of operation

(a) Outline

This module consists of the serial-mode register (SMR) and serial-data register (SDR). At serial output, data in the SDR is output in bit serial to the serial output pin (SO) in synchronization with the falling edge of a serial shift-clock pulse generated from the internal or external clock. At serial input, data is input in bit serial from the serial input pin (SI) to the SDR at the rising edge of a serial shift-clock pulse.



(b) Operation modes

The serial I/O has three internal shift-clock modes and one external shift-clock mode, which are specified by the SMR. Mode switching or clock selection should be made with serial I/O stopped (SST bit (bit 0) of SMR = 0).

(1) Internal shift-clock mode

Operation is performed by the internal clock. A shift-clock pulse with a duty of 50% is output from the SCK pin as a synchronous timing output. Data is transferred bit-by-bit at every clock pulse.

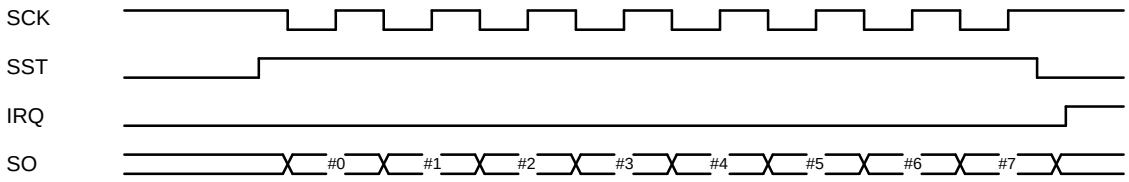
(2) External shift-clock mode

Data is transferred bit-by-bit at every clock pulse in synchronization with the external shift-clock pulse input from the SCK pin. The transfer speed can be from DC to 1/2 oscillation (two instruction cycles). When one instruction cycle is 2.0 μs (at 2 MHz oscillation), the transfer speed can be up to 0.25 MHz.

Do not write data to the SMR and SDR during the serial I/O operation in either mode.

(c) Interrupt functions

This module can output an interrupt request to the CPU. To output an interrupt request, set the SIOE bit (bit 6) of the SMR to 1 to enable an interrupt and then set the interrupt flag SIOF (bit 7) of SMR after 8-bit data transfer is terminated.

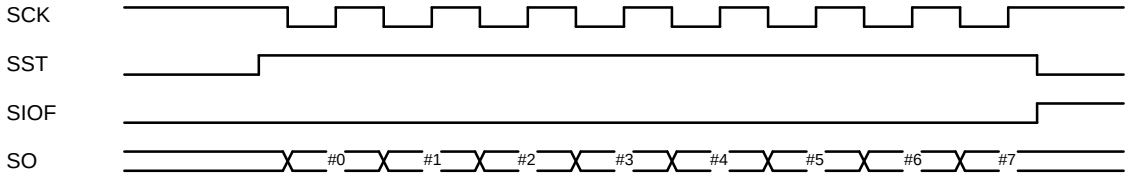


(d) Shift start/stop timing

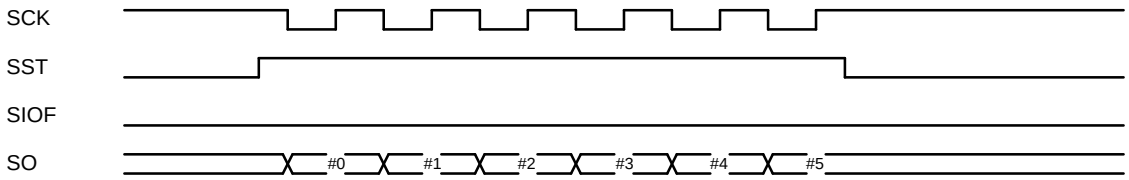
Data transfer starts when 1 is written at the SST bit (bit 0) of the SMR, and stops when 0 is written. When data transfer is terminated, the SST bit is automatically cleared to 0, which stops the operation.

(1) Internal shift-clock mode (LSB first)

[When transfer terminated]

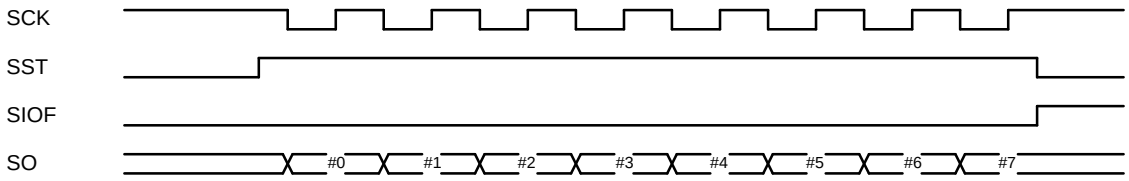


[When transfer suspended]

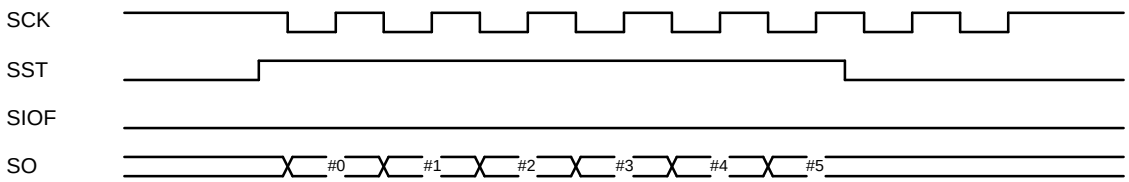


(2) External shift-clock mode (LSB first)

[When transfer terminated]



[When transfer suspended]



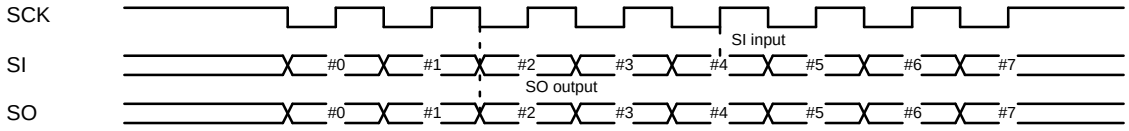
Note: When data is written at the SDR, the output data changes at the falling edge of the external-clock pulse.

Fig. 2.22 Shift Start/Stop Timing

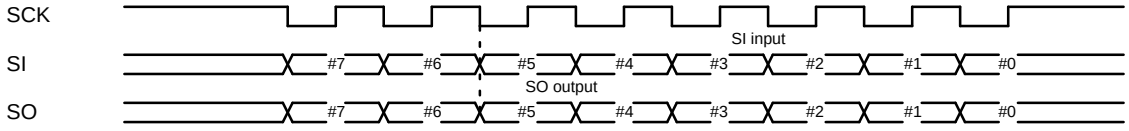
(e) Input/output shift timing

Data is output from the serial output pin (SO) at the falling edge of the shift-clock pulse, and is input from the serial input pin (SI) to the SDR at the rising edge of the shift-clock pulse.

(1) LSB first (BDS = 0)



(2) MSB first (BDS = 1)



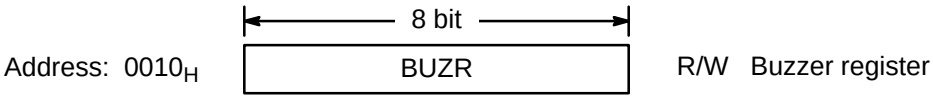
DI7 to DI0 indicate input data, and DO7 to DO0 indicate output data.

Fig. 2.23 Input/Output Shift Timing

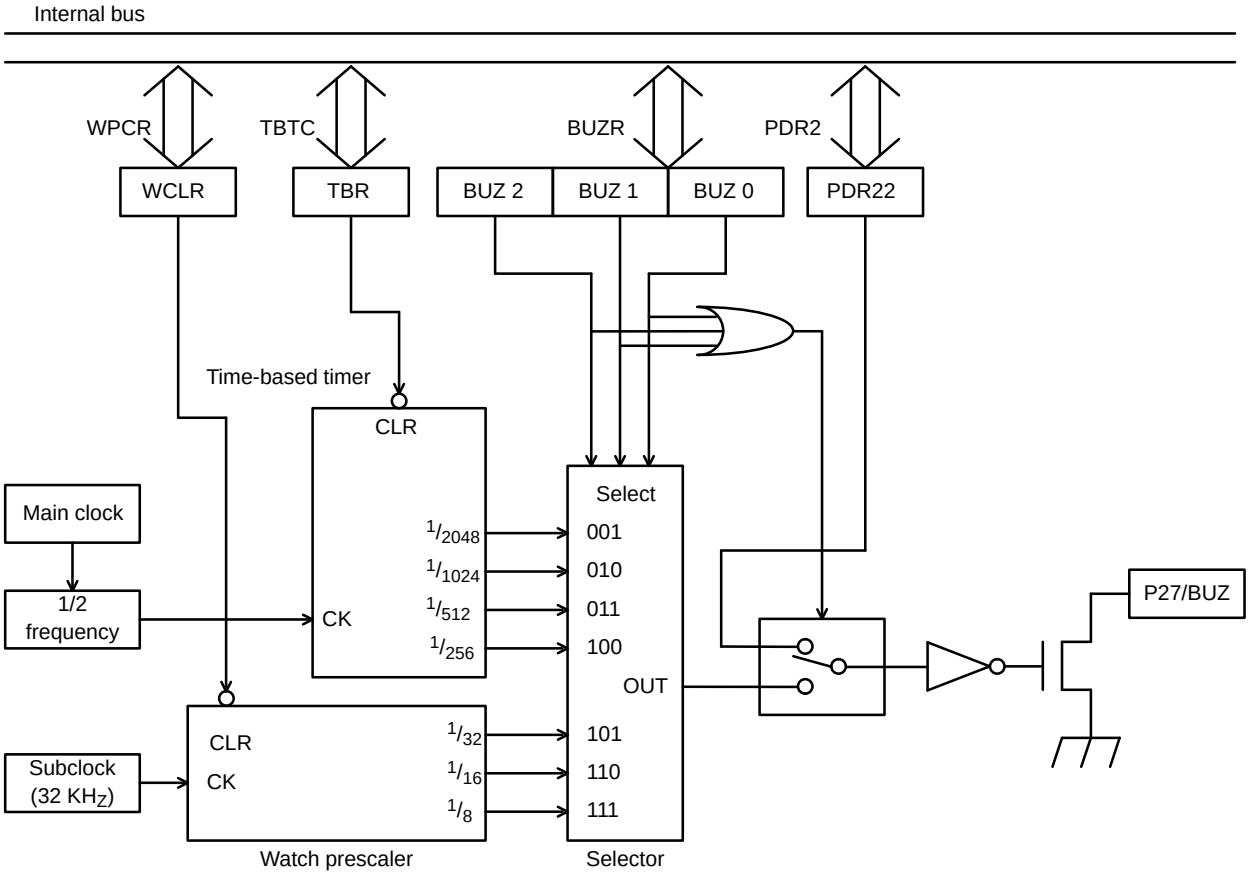
2.2.6 Buzzer output circuit

- The buzzer output sound for checking key input can be output from port 27.
- Seven frequencies can be output by setting the registers.

(1) Registers



(2) Block diagram



(3) Detailed description of registers

(a) Buzzer register (BUZR)

This 3-bit register enables buzzer output and selects the frequency.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $00F_H$	—	—	—	—	—	BUZ2	BUZ1	BUZ0	XXXX $X000_B$
						(R/W)	(R/W)	(R/W)	

[Bits 2, 1, and 0] BUZ2, BUZ1 and BUZ0: Buzzer-select bits

Bits 2, 1, and 0 are used to enable buzzer output and select the frequency. The buzzer output function is disabled by 000 and the port operates normally. In other cases, the frequencies listed in the table below are selected.

Table 2-5 Buzzer Output Frequencies (at fch = 3 MH_Z and fcl = 32 kHz)

BUZ2	BUZ1	BUZ0	Buzzer output frequency
0	0	0	General-purpose port operation
0	0	1	732 Hz
0	1	0	1465 Hz
0	1	1	2930 Hz
1	0	0	5859 Hz
1	0	1	1024 Hz
1	1	0	2048 Hz
1	1	1	4096 Hz

fch: Main clock frequency
fcl: Subclock frequency

(4) Description of operation

This circuit outputs a signal for use as a check sound. The buzzer register is used to enable buzzer output and select the frequency. When values other than 000 are set at the BUZR register, the square wave of the set frequency is output at the port.

(5) Precautions for buzzer output circuit

Part of the time-base timer or watch prescaler is used as the buzzer output. Therefore, each setting condition of the time-base timer or watch prescaler affects the circuit.

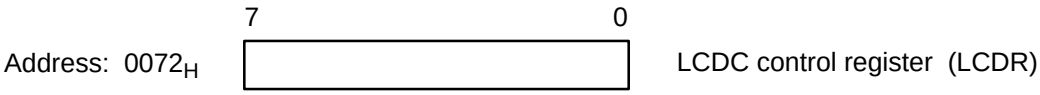
2.2.7 LCD controller/driver

The LCD controller/driver consists of the display controller that generates segment and common signals according to the display data and memory data, and the segment and common drivers that can drive the LCD panel directly.

Its main functions an features are as follows:

1. Direct LCD driving
2. Built-in reference voltage generator and booster for driving LCD (option)
3. Built-in dividing resistor for driving LCD (option)
4. Four common outputs (COM0 to COM3) and 36 segment outputs (SEG0 to SEG35)
5. 18-byte display data memory
6. 1/2, 1/3, or 1/4 selected as duty.
7. Main clock and subclock (32 kHz) selected as drive clock source.
8. SEG20 to SEG35 used as general-purpose ports (option).

(1) Registers



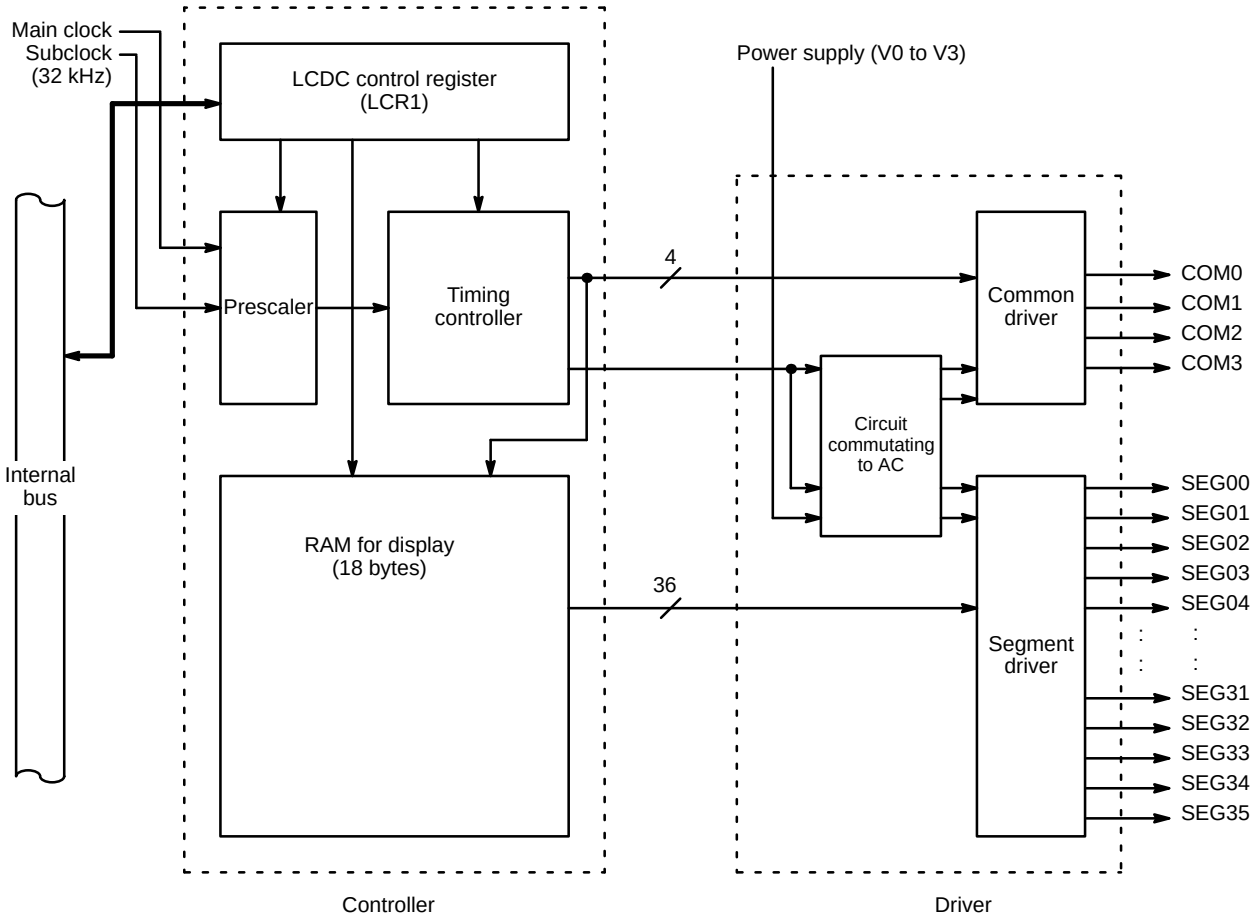


Fig. 2.24 LCDC Block Diagram

(2) Description of registers

LCDC control register 1 (LCDR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0072_H	CSS	LCEN	VSEL	BK	MS1	MS0	FP1	FP0	$0001\ 0000_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7]: Clock Source Select (CSS)
Bit 7 is a frame cycle generation clock select bit.

0	Main clock
1	Subclock

[Bit 6]: LCEN
Bit 6 is a LCD controller/driver operation enable bit at watch mode

0	Terminates the operation at watch mode
1	Executes operation at watch mode

[Bit 5]: VSEL
<<Microcontrollers without built-in booster>>
Bit 5 is a LCD drive power control bit.

0	Connection of internal resistor for divided voltage enters off state
1	Connection of internal resistor for divided voltage enters on state

<<Microcontrollers with built-in booster (MB89150A)>>
This bit is used to control the reference voltage generator.

0	The reference voltage generator and booster starts operation.
1	The reference voltage generator and booster stops operation (power-down mode).

[Bit 4]: Blanking (BK)
Bit 4 selects display or display blanking. The segment output in display blanking is an non-conforming waveform.

0	Display
1	Display blanking

[Bit 3]: MS1

[Bit 2]: MS0 (Mode Select 1 to 0)

Bit 3 and 2 select display mode. The mode is set according to the following table.

MS1	MS0	Display mode	Number of time divisions: N
0	0	LCD operation stop	—
0	1	1/2 duty output mode	2
1	0	1/3 duty output mode	3
1	1	1/4 duty output mode	4

[Bit 1]: FP1

[Bit 0]: FP0 (Frame Period 1 to 0)

Bits 1 and 0 select the LCD clock cycle. The frame frequency is shown below. Calculate the optimum frame frequency and set the register according to the LCD module.

FP1	FP0	Frame frequency (at fch = 3 MHz and fcl = 32 kHz)			
		CSS = 0		CSS = 1	
0	0	fch/($2^{12} \times$ N)	183 Hz (N = 4)	fch/($2^{5} \times$ N)	256 Hz (N = 4)
0	1	fch/($2^{13} \times$ N)	92 Hz (N = 4)	fch/($2^{6} \times$ N)	128 Hz (N = 4)
1	0	fch/($2^{14} \times$ N)	46 Hz (N = 4)	fch/($2^{7} \times$ N)	64 Hz (N = 4)
1	1	fch/($2^{15} \times$ N)	23 Hz (N = 4)	fch/($2^{8} \times$ N)	32 Hz (N = 4)

N: Number of time divisions
fch: Main clock frequency
fcl: Subclock frequency

(3) RAM for display

The LCD controller/driver contains the 18 x 8-bit RAM for generating a segment output signal. The value of this RAM is automatically read in synchronization with the common signal select timing and the waveform corresponding to this value is output from the segment output pin.

Thirty-six segment signals correspond to 18 locations of the display RAM. Each location bit is in synchronization with the common signal select timing: bits 0 and 4 with COM0, bits 1 and 5 with COM1, bits 2 and 6 with COM2, and bits 3 and 7 with COM3. If the value of each bit is 1, the signal is converted to LCD voltage and if it is 0, the signal is converted to non-LCD and is not output. However, at reset, COM0 to COM3 and SEG0 to SEG36 go Low to provide no LCD display.

The waveform is output from the segment pins in synchronization with the common signal select timing, irrespective of the CPU operation. Therefore, reading and writing from and to the display RAM are possible in any timing.

When using SEG20 to SEG35 as general-purpose output ports, the 8 upper bytes are usually used as RAM. When the external reset signal is input, the impedance of ports 4 and 5 goes High.

Address	COM3	COM2	COM1	COM0	
060_H	b3	b2	b1	b0	SEG00
	b7	b6	b5	b4	SEG01
061_H	b3	b2	b1	b0	SEG02
	b7	b6	b5	b4	SEG03
062_H	b3	b2	b1	b0	SEG04
	b7	b6	b5	b4	SEG05
:	:	:	:	:	
:	:	:	:	:	
068_H	b3	b2	b1	b0	SEG16
	b7	b6	b5	b4	SEG17
069_H	b3	b2	b1	b0	SEG18
	b7	b6	b5	b4	SEG19
$06A_H$	b3	b2	b1	b0	SEG20
:	b7	b6	b5	b4	SEG21
$06B_H$	b3	b2	b1	b0	SEG22
	b7	b6	b5	b4	SEG23
$06C_H$	b3	b2	b1	b0	SEG24
	b7	b6	b5	b4	SEG25
$06D_H$	b3	b2	b1	b0	SEG26
	b7	b6	b5	b4	SEG27
$06E_H$	b3	b2	b1	b0	SEG28
	b7	b6	b5	b4	SEG29
$06F_H$	b3	b2	b1	b0	SEG30
	b7	b6	b5	b4	SEG31
070_H	b3	b2	b1	b0	SEG32
	b7	b6	b5	b4	SEG33
071_H	b3	b2	b1	b0	SEG34
	b7	b6	b5	b4	SEG35

SEG20 to SEG27: Multiplexed with port 4.

SEG28 to SEG35: Multiplexed with port 5.

(4) Operation

First, write the data to be displayed by display RAM. Then, set the value corresponding to the LCD panel to be used to LCR (LCD control register). The, LCD drive waveform is output according to the data in the display RAM, When the clock pulse is supplied. A high-speed clock or watch clock can be selected as clock source. The clock source can be switched during the LCD display. However, the display tends to flicker by switching. Therefore, it is best to stop the display by blanking, etc. before switching the clock.

The display drive output has a 2-frame AC waveform. The combination of bias and duty shown below may be possible, but do not use 1/2 bias. Examples of waveforms are shown in the following pages.

<Combination of biases and duties of microcontrollers without built-in booster>

	1/2 duty	**1/3 duty**	**1/4 duty**
1/2 bias	◎	×	×
1/3 bias	×	◎	◎

◎ : Recommended mode
× : Application disabled

<Combination of biases and duties of microcontrollers with built-in booster>

	1/2 duty	**1/3 duty**	**1/4 duty**
1/2 bias	×	×	×
1/3 bias	×	◎	◎

Note: Do not select the single-clock module for microcontrollers with a built-in booster (MB89150A).

The COM2 and COM3 output waveforms are non-conforming waveforms in the 1/2 duty mode. The COM3 output waveform is also a non-conforming waveform at 1/3 duty.

When LCD operation is terminated, both common and segment output waveforms at L level. However, when SEG20 to SEG 35 are specified as general-purpose port by the mask option, segment data are not output.

(5) LCD drive output waveform

(a) Waveform at 1/2 bias and 1/2 duty

COM3	COM2	COM1	COM0	
—	—	0	0	SG_n
—	—	0	1	SG_{n+1}

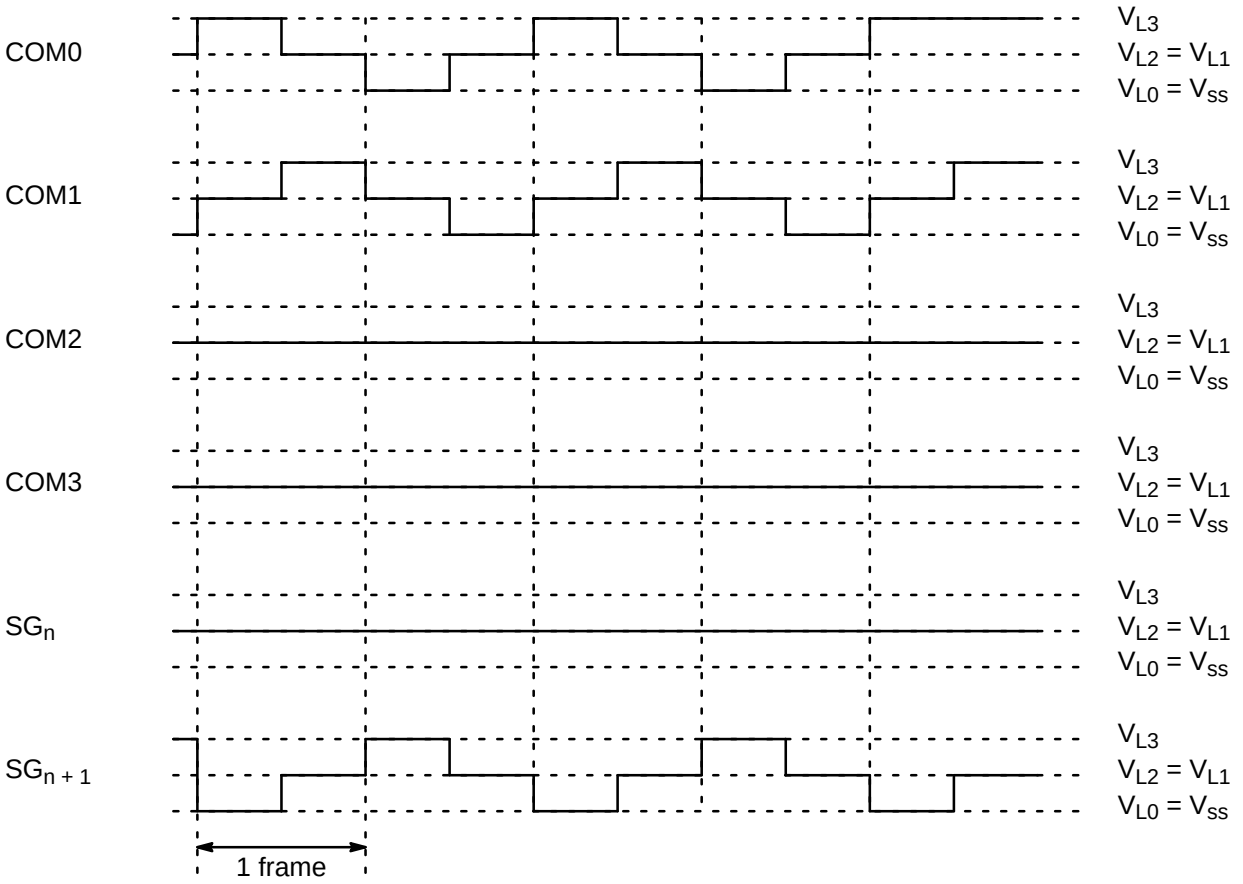


Fig. 2.25 Example of Waveform at Pin Corresponding to the RAM Data for Display

(b) Waveform at 1/3 bias and 1/3 duty

COM3	COM2	COM1	COM0	
—	1	0	0	SG_n
—	1	0	1	SG_{n+1}

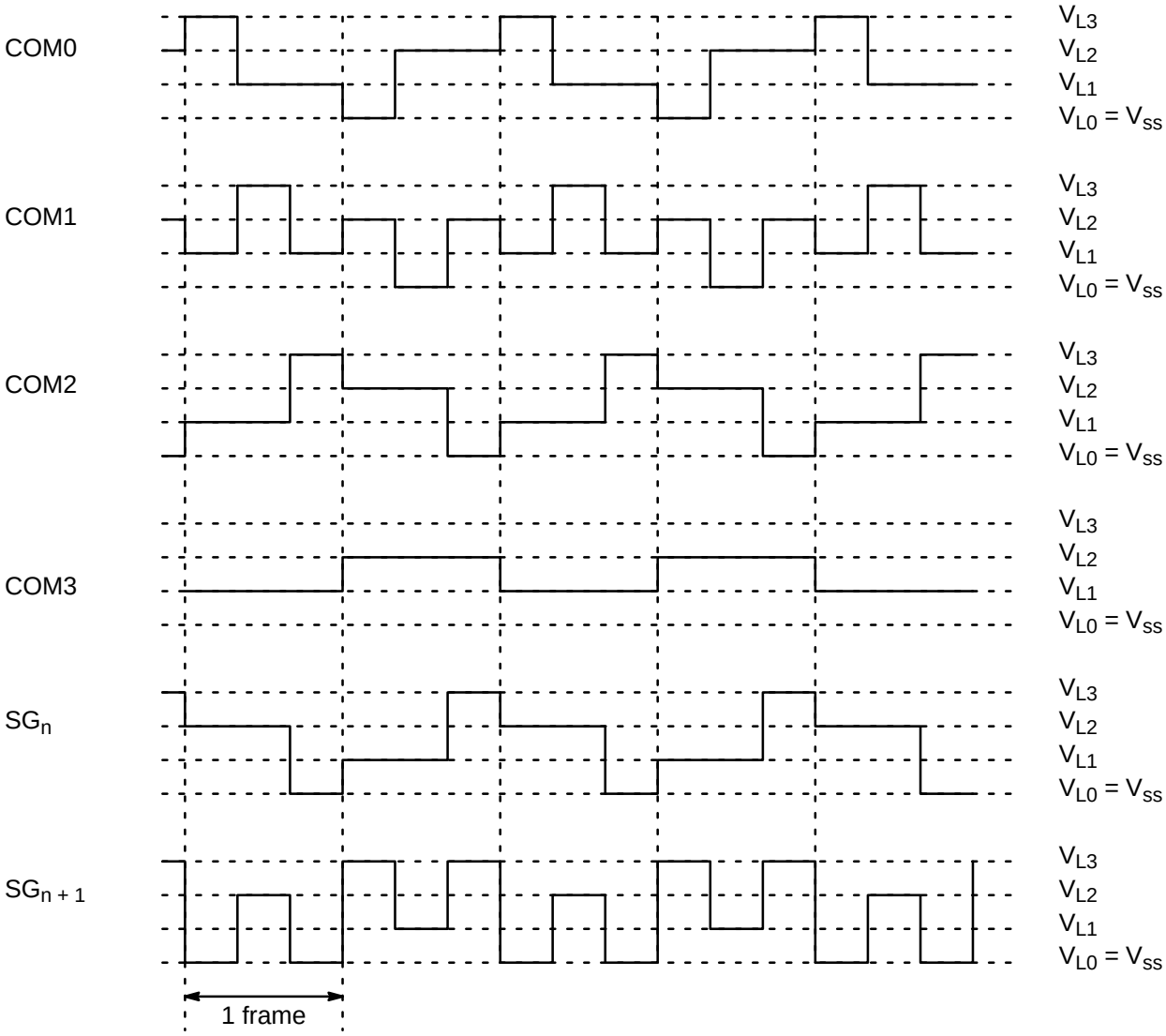


Fig. 2.26 Example of Waveform at Pin Corresponding to the RAM Data for Display

(c) Waveform at 1/3 bias and 1/4 duty

COM3	COM2	COM1	COM0	
0	1	0	0	SG_n
0	1	0	1	SG_{n+1}

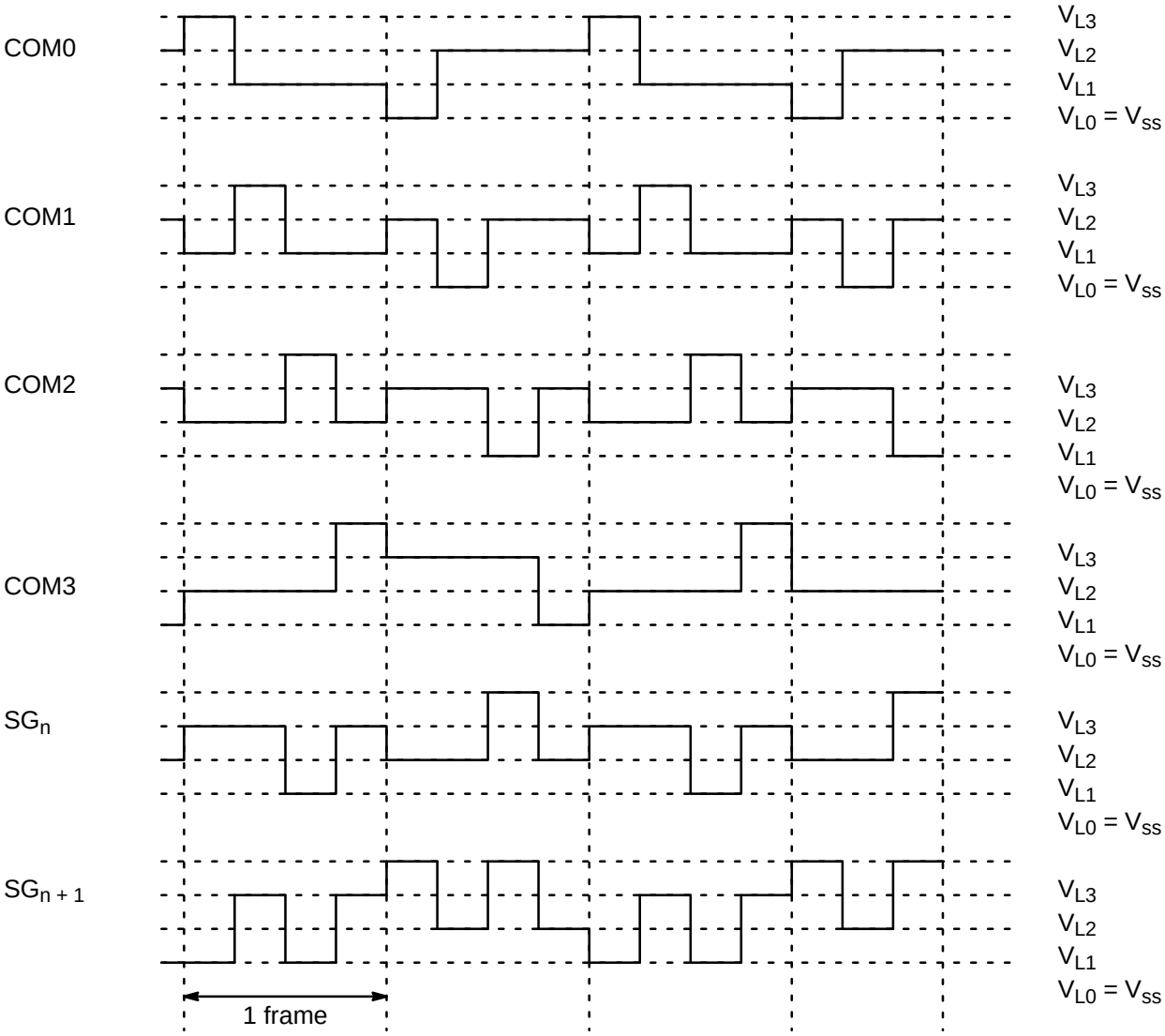


Fig. 2.27 Example of Waveform at Pin Corresponding to the RAM Data for Display

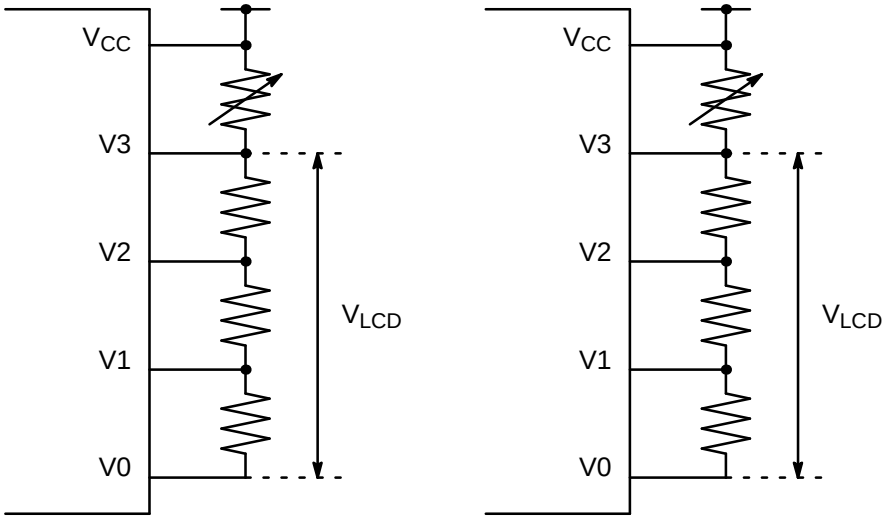
(6) Voltage setting at power pins (V_3, V_2, V_1, and V_0) for driving LCD

Set the voltages at the LCD power pins (V_3, V_2, V_1, and V_0) as shown below.

	V3	V2	V1	V0
1/2 bias	V_{LCD}	1/2 V_{LCD}	1/2 V_{LCD}	GND
1/3 bias	V_{LCD}	2/3 V_{LCD}	1/3 V_{LCD}	GND

V_{LCD}: LCD operating voltage

A connection example for supplying power to drive the LCD is shown below.



1/2 bias 1/3 bias

Notes:

1. To set a 1/2 duty when using the external dividing resistor, short-circuit the pins V2 and V1.
2. For microcontrollers with a built-in booster (MB89150A), the above pins serve as the external capacitor connection pins (Figure 2.22).

Built-in voltage dividing resistor

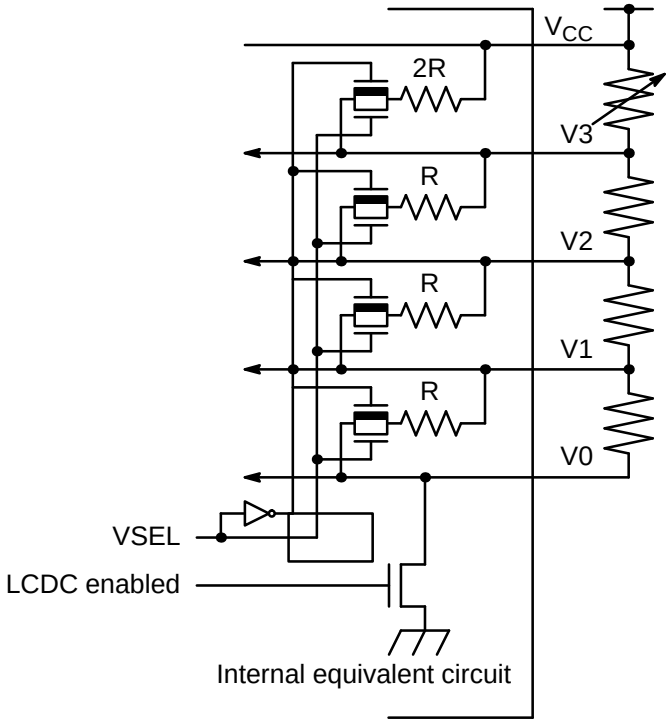
The built-in voltage dividing resistors are connected as shown in the next figure.

Writing 1 at the VSEL bit connects the built-in voltage dividing resistors. Therefore, write 1 at the VSEL bit to connect the resistors and set 0 to disconnect the resistors.

The V0 pin is connected to the V_{SS} through the transistor within chip. Therefore, when using the external resistance divider, connecting V_{SS} only to the V0 pin cut the current flowing into the resistor when the LCDC stops.

In the figure, the LCDC enable bit becomes inactive in the LCD stop and WATCH modes (LCEN = 0).

Microcontrollers with a built-in booster (MB89150A) do not contain a dividing resistor.



(7) Reference voltage generator and booster for doubling and tripling the voltage
(only for microcontrollers with built-in booster (MB89150A))

The reference voltage generator generates the reference voltage of 1.5 V without being affected by fluctuations in the operating voltage. The booster can be used solely without using the internal reference voltage generator by applying an external reference voltage to the V1 pin. This arrangement is optional.

The booster can be connected as shown in the figure below to generate a double or triple reference voltage from 32 kHz input clock pulses and the reference voltage.

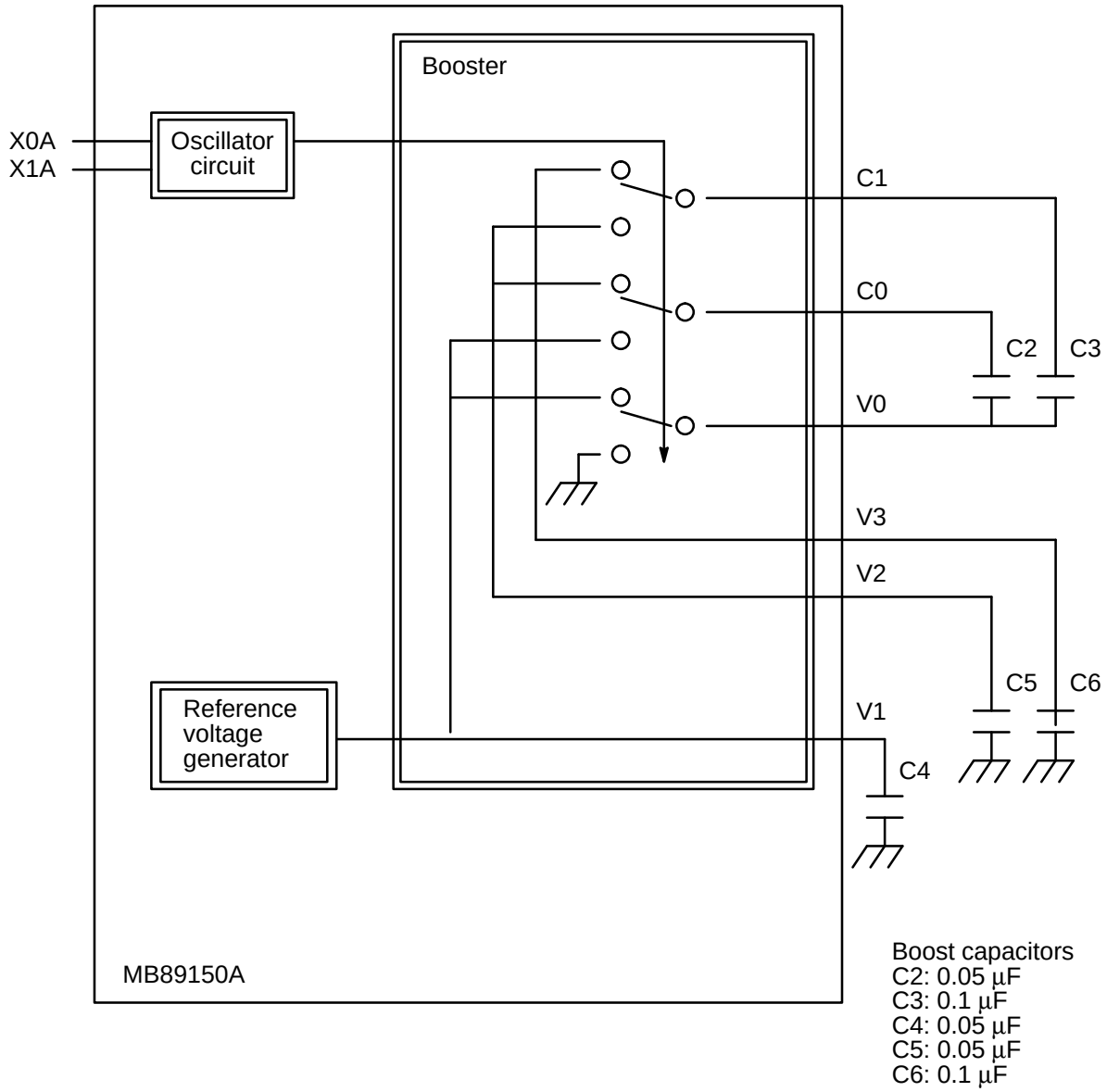


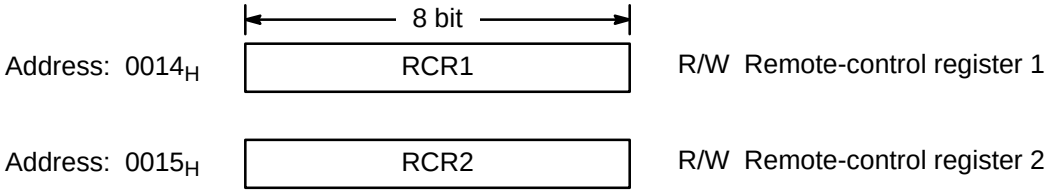
Fig. 2.28 External Connection Diagram of Reference Voltage Generator and Booster

Note: The reference voltage generator and booster function only when microcontrollers with built-in booster (MB89150A) are selected. When microcontrollers without built-in booster are selected, pins V3 to V0 serve as division resistor connection pins. Capacitors C0 and C1 serve as general-purpose output ports (P31 and P32).

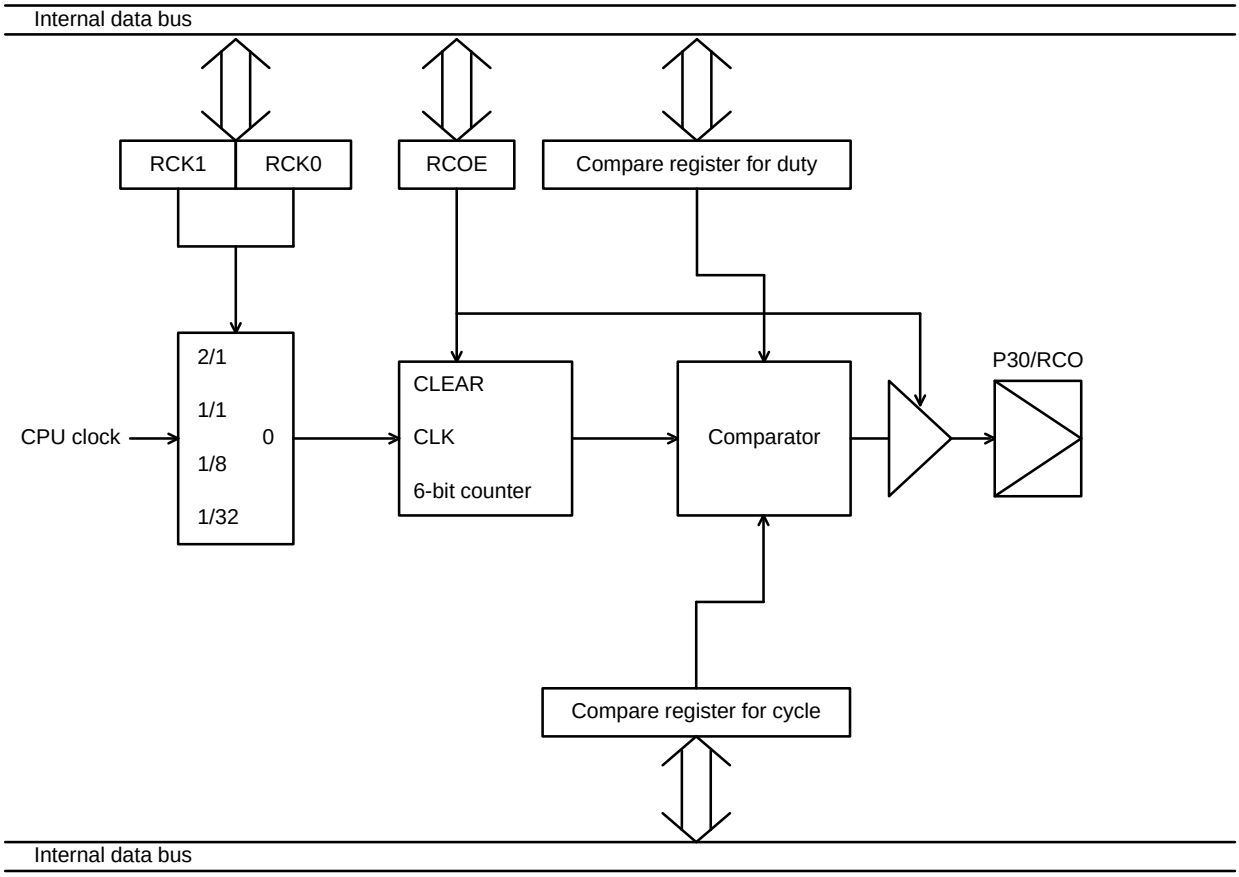
2.2.8 Remote-control carrier frequency generator

- This generator is a remote-control circuit for generating remote-control carrier frequencies.
- The 6-bit binary counter is built in.
- Four internal clock pulses can be selected to set a duty and cycle.

(1) Registers



(2) Block diagram



(3) Description of registers

(a) Remote-control register 1 (RCR1)

This register is used to select the reference clock and set the duty of remote-control carrier frequency.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0014_H	RCK1	RCK0	HSC5	HSC4	HSC3	HSC2	HSC1	HSC0	$0000\ 0000_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bits 7 and 6] RCK1 and RCK0: Bits for selecting clock source for remote-control carrier frequency
These bits are used to select the clock source for the remote-control carrier frequency.

RCK1	RCK0	Reference clock	Reference clock at fch = 3 MHz
0	0	(Instruction cycle time) × 1/2	0.67 μs
0	1	(Instruction cycle time) × 1	1.33 μs
1	0	(Instruction cycle time) × 8	10.33 μs
1	1	(Instruction cycle time) × 32	42.56 μs

Instruction cycle: Selectable from 1/4 to 1/64 oscillations of main clock by setting system clock control register (SYCC).

fch: Oscillation frequency of main clock

[Bits 5 to 0] HSC5 to HSC0: Bits for setting duty of remote-control carrier frequency

These bits are used for the 6-bit compare register to set the duty of the remote-control carrier frequency. To set the duty of the remote-control carrier frequency, set the value calculated from the clock source in binary at these bits. For example, to set a duty of 26 μs, select clock source = instruction x 1 and set 010100 (1/20 oscillation) at these 6 bits. This enables the selection of any duty.

(b) Remote-control register 2 (RCR2)

This register is used to enable the output and set the cycle of remote-control carrier frequency.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0015_H	RCEN	—	SCL5	SCL4	SCL3	SCL2	SCL1	SCL0	$0000\ 0000_B$
	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] RCEN: Bit for enabling output of remote-control carrier frequency

This bit is used to enable the output of remote-control carrier frequency to the P30/RCO pin. Setting this bit to 0 enables clearing of the 6-bit counter.

[Bits 5 to 0] SCL5 to SCL0: Bits for setting cycle of remote-control carrier frequency

These bits are used for the 6-bit compare register to set the cycle of the remote-control carrier frequency. To set the cycle of the remote-control carrier frequency, set the value calculated from the clock source in binary at these bits. For example, to set a cycle of 66 μs, select reference clock = instruction x 1 and set 110010 (1/50 oscillation) at these 6 bits. This enables selection of a cycle of 66.5 μs.

(4) Description of operation

Remote-control registers 1 and 2 (RCR1 and RCR2) control a 6-bit counter to output the remote-control carrier frequency to the P30/RCO pin.

A usage example is given below.

<Example>

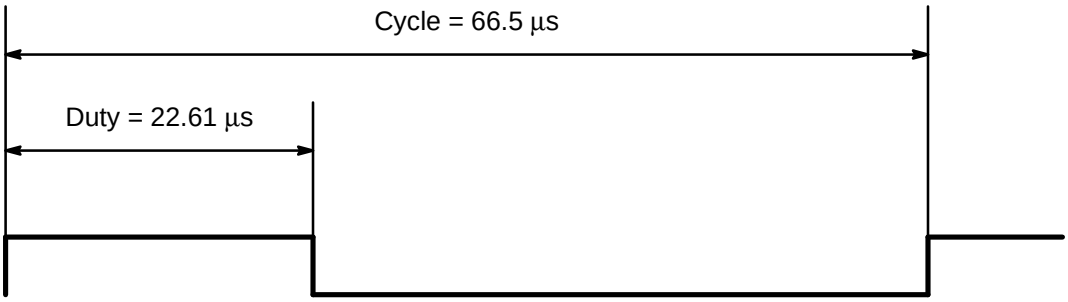
Cycle: 15 kHz

Duty: 1/3

Reference clock: instruction cycle X1

RCR1 set value: 01 010001
- 010001 — Duty set value (1/17 oscillation)
- 01 — Reference clock set value

RCR2 set value: 1X 110010
- 110010 — Cycle set value (1/50 oscillation)
- 1X — Output enable

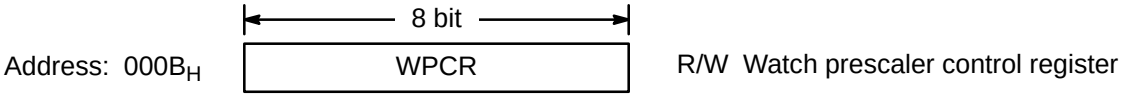


Note: To set the duty and cycle, the cycle set value must always be greater than the set duty value.

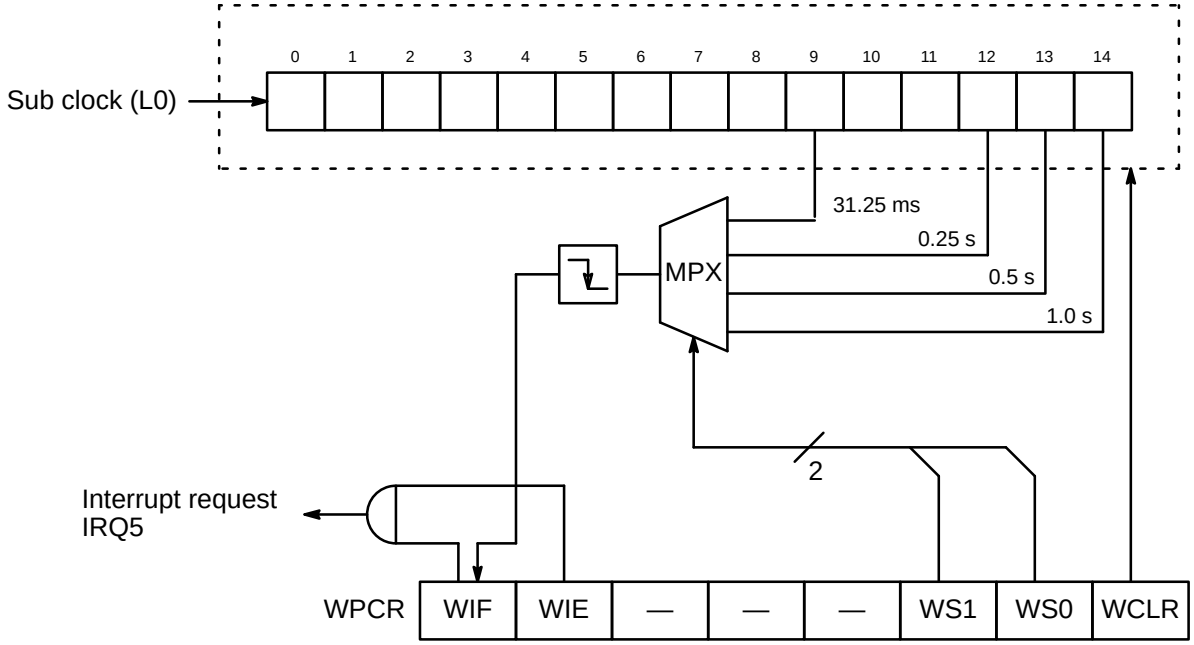
2.2.9 Watch prescaler

- This prescaler has a 15-bit binary counter
- Four interval times and three clock pulses can be selected.
- This function cannot be used when the single clock module is selected by the mask option.

(1) Registers



(2) Block diagram



(3) Description of registers

(a) Watch prescaler control register (WPCR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $000B_H$	WIF	WIE	—	—	—	WS1	WS0	WCLR	$00XX\ X000_B$
	(R/W)	(R/W)				(R/W)	(R/W)	(R/W)	

[Bit 7] WIF: Watch interrupt flag
When writing, this bit is used to clear the watch interrupt flag.

0	Clears watch interrupt flag
1	No operation

When reading, this bit indicates that the watch interrupt has occurred.

0	Watch interrupt not occurred
1	Watch interrupt occurred

1 is read when the Read Modify Write instruction is read. If the WIF bit is set to 1 when the WIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 6] WIE: Watch interrupt enable bit
This bit is used to enable an interrupt by the watch.

0	Interrupt by watch disabled
1	Interrupt by watch enabled

[Bit 2] WS1: Interrupt interval time specification bit by watch
[Bit 1] WS0: Interrupt interval time specification bit by watch
These bits are used to specify the interrupt cycles.

WS1	WS0	Interrupt cycle	Interrupt cycle at fcl = 32 KHz
0	0	2^{10}/fcl	31.25 [ms]
0	1	2^{13}/fcl	0.25 [s]
1	0	2^{14}/fcl	0.50 [s]
1	1	2^{15}/fcl	1.00 [s]

/fcl: Subclock oscillation frequency

[Bit 0] WCLR: Bit clearing watch prescaler
This bit is used to clear the watch prescaler.

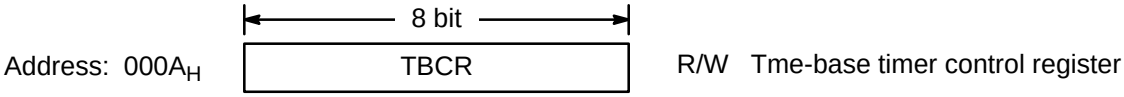
0	Watch prescaler cleared
1	No operation

1 is always read when this bit is read.

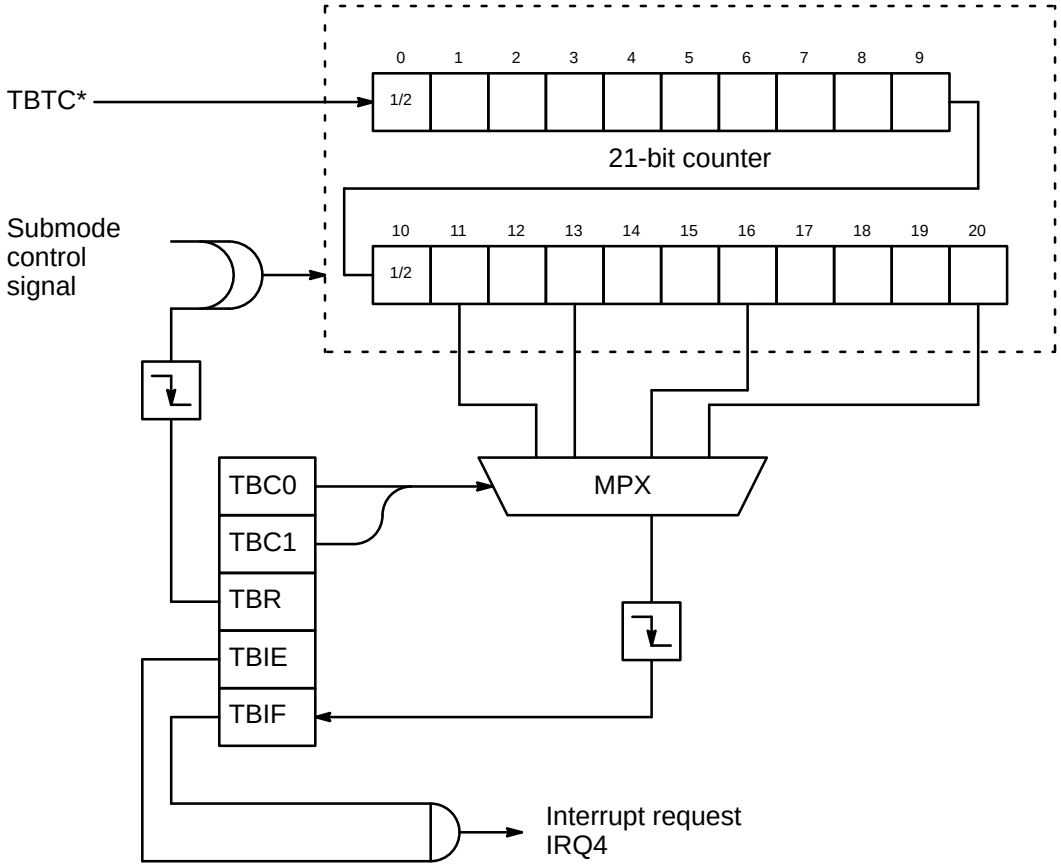
2.2.10 Time-base timer

- This timer has a 21-bit binary counter and uses a clock pulse with 1/2 oscillation of the main clock.
- Four interval times can be selected.
- This function cannot be used when the main clock is stopped.

(1) Registers



(2) Block diagram



*TBTC is a clock pulse with 1/2 oscillation of the main clock.

(3) Description of registers

(a) Time-base timer control register (TBCR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: $000A_H$	TBOF	TBIE	—	—	—	TBC1	TBC0	TBR	$00XX\ X000_B$
	(R/W)	(R/W)				(R/W)	(R/W)	(W)	

[Bit 7] TBOF: Interval timer overflow bit
When writing, this bit is used to clear the interval timer overflow flag.

0	Interval timer overflow flag cleared
1	No operation

When reading, this bit indicates that an interval timer overflow has occurred.

0	Interval timer overflow not occurred
1	Interval timer overflow occurred

1 is read when the Read Modify Write instruction is read. If the TBIF bit is set to 1 when the TBIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 6] TBIE: Interval-timer interrupt enable bit
This bit is used to enable an interrupt by the interval timer.

0	Interval interrupt disabled
1	Interval interrupt enabled

[Bit 2] TBC1: Interval time specification bit
[Bit 1] TBC2: Interval time specification bit
Bits 1 and 2 are used to specify interval timer cycle.

TBC1	TBC0	Interval time	Interval time at fch = 3 MHz
0	0	2^{13}/fch	2.73 [ms]
0	1	2^{15}/fch	10.92 [ms]
1	0	2^{18}/fch	87.38 [ms]
1	1	2^{22}/fch	1398.10 [ms]

/fch: main clock frequency

[Bit 0] TBR: Time-base timer clear bit
This bit is used to clear time-base timer.

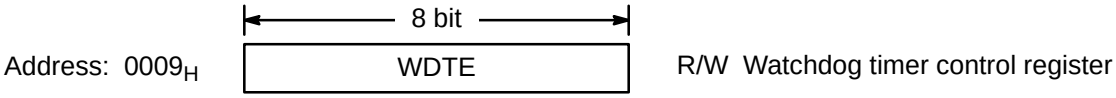
0	Time-base timer cleared
1	No operation

1 is always read when this bit is read.

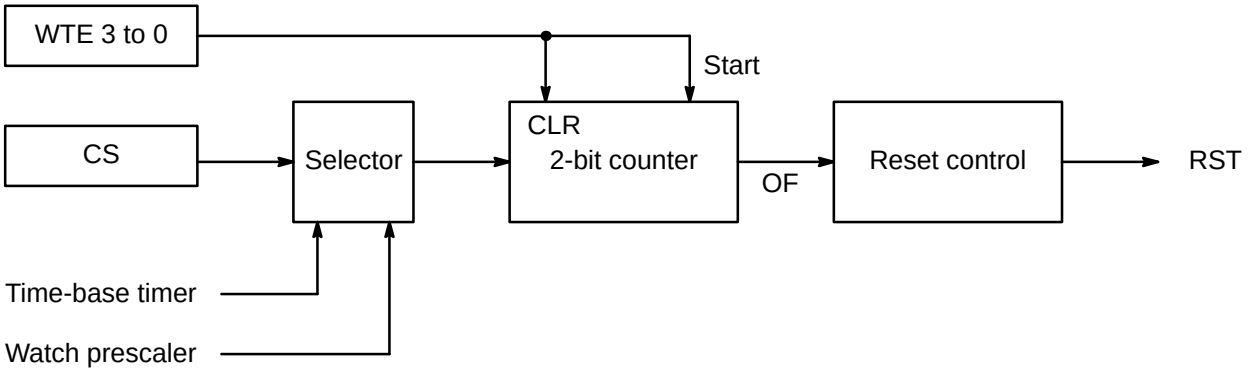
2.2.11 Watchdog timer reset

Either of a signal output from the time-base timer for counting with the main clock or a signal output from the watch prescaler for counting with the subclock can be selected as a clock.

(1) Registers



(2) Block diagram



(3) Description of register

• Watchdog timer control register (WDTE)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0009H	CS	—	—	—	WTE3	WTE2	WTE1	WTE0	0XXX XXXXB
	(R/W)				(W)	(W)	(W)	(W)	

[Bit 7] CS: Clock source switching bit

Bit 7 is used to select a count clock from either the watch prescaler or time-base timer.

0	Time-base timer Cycle = 2^{22} /fch
1	Watch prescaler Cycle = 2^{14} /fcl

fch: Main clock frequency
fcl: Subclock frequency

Set this bit as soon as the watchdog timer is started. Do not change the bit after the timer is started. When using the submode, always select the watch prescaler.

[Bits 3 to 0] WTE3 to WTE0: Watchdog timer control bit
Bits 3 to 0 control the watchdog timer.

First write only after reset

0101	Watchdog timer started
Other than the above	No operation

Second and later write

0101	Watchdog timer counter cleared
Other than the above	No operation

The watchdog timer can be stopped only by reset. 1111 is read when these bit are read.

(4) Description of operation

The watchdog timer enables detection of a program nullfunction.

- Starting watchdog timer
  The watchdog timer starts when 0101 is written at the watchdog timer control bits.
- Clearing watchdog timer
  When 0101 is written at the watchdog timer control bits after start, the watchdog timer is cleared. The counter of the watchdog timer is cleared when changing to the standby mode (STOP, SLEEP, CLOCK) or hold mode.
- Watchdog timer reset
  If the watchdog timer is not cleared within the time given in the table below, a watchdog timer reset occurs to reset the chip internally.

	Clock source		
	Time-based timer	**Watch prescaler**	
Minimum time	Approx. 1398.1 ms	Approx. 512 ms	at high-speed 3 MHz clock
Maximum time	Approx. 2796.2 ms	Approx. 1024 ms	at low-speed 32 kHz clock

- Stopping watchdog timer
  Once started, the watchdog timer will not stop until a reset occurs.

3. OPERATION

3.1 Clock Pulse Generator

The MB89150 series of microcontrollers incorporate the system clock pulse generator. The crystal oscillator is connected to the X0 and X1 pins to generate clock pulses. Clock pulses can also be supplied internally by inputting externally-generated clock pulses to the X0 pin. The X1 pin should be kept open.

The X0A and X1A pins are used for the subclock and function in the same manner as the X0 and X1 pins.

When the single clock module is selected by the option, the X0A pin should be connected to GND and the X1A pin should be kept open.

For microcontrollers with built-in booster, the single clock module cannot be selected by the option. The double-clock module should be used.

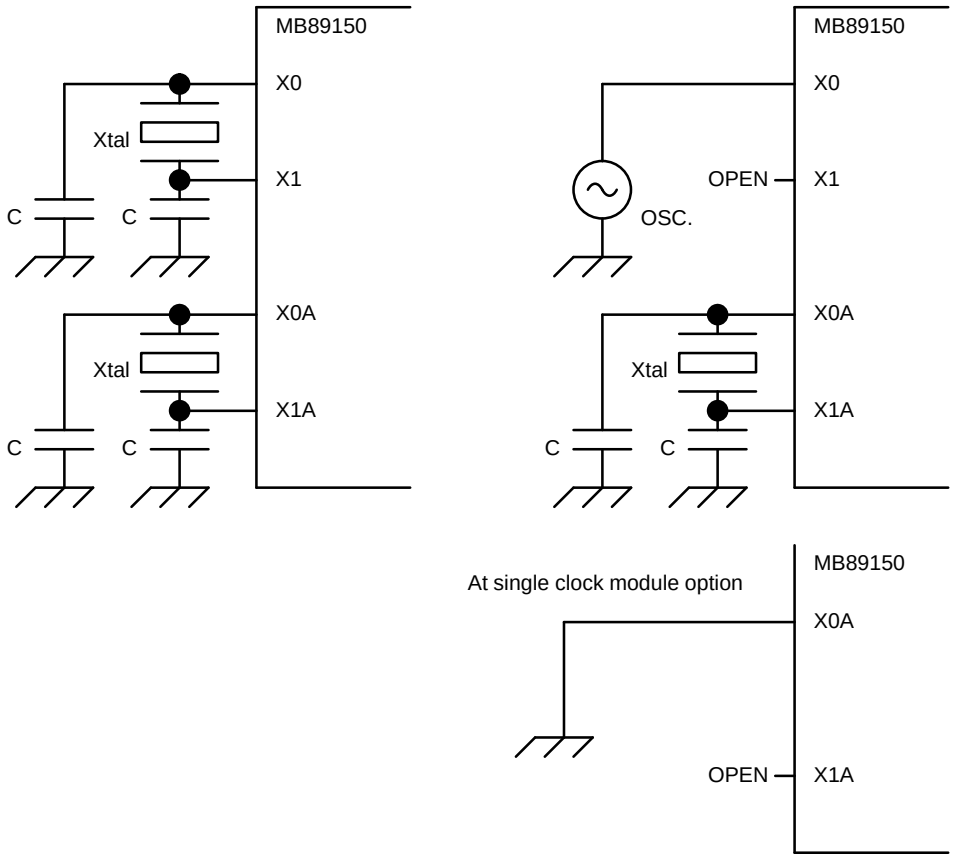


Fig. 3.1 Clock Pulse Generator

3.2 Reset

3.2.1 Reset operation

When reset conditions occur, the MB89150 series of microcontrollers suspend the currently-executing instruction to enter the reset state. The contents written at the RAM do not change before and after reset. However, if a reset occurs during writing of 16-bit long data, data is written to the upper bytes and may not be written to lower bytes. If a reset occurs around write timing, the contents of the addresses being written are not assured.

When the reset conditions are cleared, the MB89150 series of microcontrollers are released from the reset state and start operation after fetching the mode data from address $FFFD_H$, the upper bytes of the reset vectors from address $FFFE_H$, and the lower bytes from address $FFFF_H$, in that order. Figure 3.2 shows the flowchart for the reset operation.

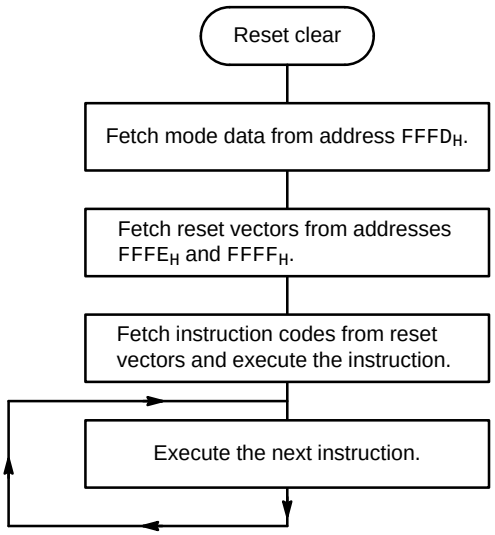
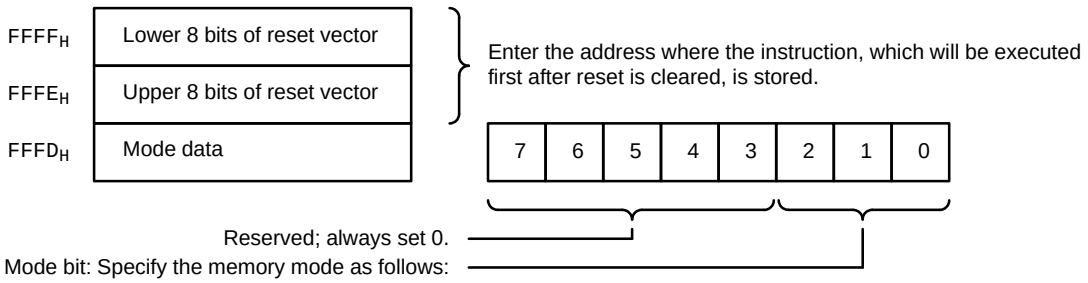


Fig. 3.2 Outline of Reset Operation

Figure 3.3 indicates the structure of data to be stored in addresses $FFFD_H$, $FFFE_H$, and $FFFF_H$.



T2	T1	T0	Operation
0	0	0	External-access disable (single chip)
Other than above			Reserved; do not set.

Fig. 3.3 Reset Vector Structure

3.2.2 Reset sources

The MB89150 series of microcontrollers have the following reset sources.

(1) External pin	A Low level is input to the RSTX pin.
(2) Specification by software	0 is written at the RST bit of the standby-control register.
(3) Power-on	The power is turned on when the power-on reset option is selected.
(4) Watchdog function	The watchdog function is enabled by the watchdog-control register and reaccess to this register is not obtained within the specified time.

When the stop mode is cleared by reset or power-on reset (option selected), operation is started after elapse of the oscillation stabilization time.

For details, see pages 2-16 to 2-18.

3.3 Interrupt

If the interrupt controller and CPU are ready to accept interrupts when an interrupt request is output from the internal resources or by an external-interrupt input, the CPU temporarily suspends the currently-executing instruction and executes the interrupt-processing program. Figure 3.4 shows the interrupt-processing flowchart.

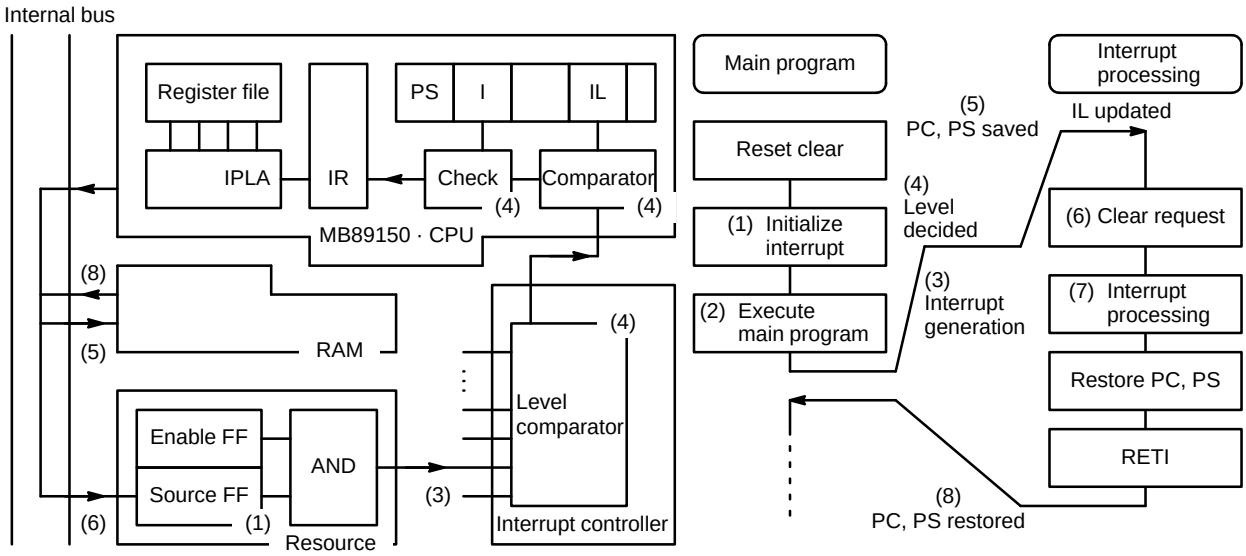


Fig. 3.4 Interrupt-processing Flowchart

All interrupts are disabled after a reset is cleared. Therefore, initialize interrupts in the main program (1). Each resource generating interrupts and the interrupt-level-setting registers (ILR1 to ILR3) in the interrupt controller corresponding to these interrupts are to be initialized. The levels of all interrupts can be set by the interrupt-level-setting registers (ILR1 to ILR3) in the interrupt controller. The interrupt level can be set from 1 to 3, where 1 indicates the highest level, and 2 the second highest level. Level 3 indicates that no interrupt occurs. The interrupt request of this level cannot be accepted. After initializing the registers, the main program executes various controls (2). Interrupts are generated from the resources (3). The highest-priority interrupt requests are identified from those occurring at the same time by the interrupt controller and are transferred to the CPU. The CPU then checks the current interrupt level and the status of the I-flag (4), and starts the interrupt processing.

The CPU performs the interrupt processing to save the contents of the current PC and PS in the stack (5) and fetches the entry addresses of the interrupt program from the interrupt vectors. After updating the IL value in the PS to the required one, the CPU starts executing the interrupt-processing routine.

Clear the interrupt sources (6) and process the interrupts in the user's interrupt-processing routine. Finally, restore the PC and PS values saved by the RETI instruction in the stack (8) to return to the interrupted instruction.

Note: Unlike the F^2MC-8, A and T are not saved in the stack at the interrupt time.

Table 3-1 lists the relationships between each interrupt source and interrupt vector.

Table 3-1 Interrupt Sources and Interrupt Vectors

Interrupt source	Upper vector address	Lower vector address
IRQ0 (External interrupt 1)	$FFFA_H$	$FFFB_H$
IRQ1 (External interrupt 2)	$FFF8_H$	$FFF9_H$
IRQ2 (16-bit timer counter)	$FFF6_H$	$FFF7_H$
IRQ3 (8-bit serial I/O)	$FFF4_H$	$FFF5_H$
IRQ4 (Interval timer)	$FFF2_H$	$FFF3_H$
IRQ5 (Watch)	$FFF0_H$	$FFF1_H$

3.4 Low-power Consumption Modes

The MB89150 series of microcontrollers have three standby modes: sleep, stop, and watch to reduce the power consumption. Writing to the standby control register (STBC) switches to these three standby modes. See 2.1.5 for setting and releasing each mode.

The MB89150 series of microcontrollers have a double clock module, and the low-power consumption modes vary with the main clock and subclock modes. Whether or not an oscillation stabilization period is required at release from each low-power consumption mode depends on the mask option of the power-on reset (See pages 2-16 to 2-18).

If the single clock module is specified with the mask option, the MB89150 series of microcontrollers can be used as single clocks. If the microcontrollers are used as single clocks without specifying the single clock module with the mask option, once the subclock mode is entered, it cannot be released. Therefore, when using these controllers as a single clock, specify the single clock module with the mask option.

Table 3-2 Low-power Consumption Mode at Each Clock Mode

Function		Note	Main mode			Sub mode			
			RUN	SLEEP	STOP	RUN	SLEEP	STOP	Watch
Main clock		—	Operate	Operate	Stop	Stop	Stop	Stop	Stop
Subclock		—	Operate	Operate	Operate	Operate	Operate	Stop	Operate
CPU	Instruction	—	Operate	Stop	Stop	Operate	Stop	Stop	Stop
	ROM	—	Operate	Hold	Hold	Operate	Hold	Hold	Hold
	RAM	—							
Re-source	I/O	○	Operate	Hold	Hold	Operate	Hold	Hold	Hold
	Watch prescaler	×	Operate	Operate	Operate*1	Operate	Operate	Stop	Operate
	Time-base timer	×	Operate	Operate	Stop	Stop	Stop	Stop	Stop
	16-bit timer	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	8-bit SIO	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	Remote-control carry	○	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	LCDC	○	Operate	Operate	Stop	Operate	Operate	Stop*3	Operate*2
	External interrupt	○	Operate	Operate	Operate	Operate	Operate	Operate	Operate
	Buzzer output	×	Operate	Operate	Operate*2	Operate*2	Operate*2	Stop	Operate*2
	Watchdog timer	×	Operate	Stop	Stop	Operate*2	Stop	Stop	Stop

Notes

○: Clock mode (main mode or submode)does not affects the operation speed or others.

×: Clock mode (main mode or submode)does not affects the operation speed or others.

*1: Watch prescaler can operate counting but watch interrupt cannot be operated.

*2: When clock source is used as watch prescaler.

*3: For microcontrollers with built-in booster (MB89150A), the booster stops.

3.5 Pin States for Sleep, Stop, and Reset

The state of each pin of the MB89150 series of microcontrollers at sleep, stop, and reset is as follows:

(1) Sleep — The pin state immediately before the sleep state is held.

(2) Stop — The pin state immediately before the stop state is held when the stop mode is started and bit 5 of the standby-control register (STBC) is set to 0; the impedance of the output and input/output pins goes High when the bit is set to 1.

(3) Reset — When the MOD pin is 00, the impedance of all I/O and resource pins (excluding pins for pull-up option) goes High.

The detailed pin state in each mode is described on the following pages.

Normal Pins for MB89150 Series of Microcontrollers (in Single-Chip Mode)

Pin name	Normal	Sleep	Stop SPL = 0	Stop SPL = 1	Reset
P07/INT27 to P00/INT20	Port input/output	Previous state	Previous state	High impedance Resource input	High impedance
P17 to P14	Port input/output	Previous state	Previous state	High impedance	High impedance
P13/INT13 to P10/INT10	Port input/output	Previous state	Previous state	High impedance Resource input	High impedance
X0, X0A	Input for oscillation	Input for oscillation	High impedance	High impedance	Input for oscillation
X1, X1A	Output for oscillation	Output for oscillation	H output	H output	Output for oscillation
MOD0 MOD1	Mode input	Mode input	Mode input	Mode input	Mode input
RSTX	Reset input	Reset input	Reset input	Reset input	Reset input *1
P27/BUZ	Port output	Previous state	Previous state	High impedance	High impedance
P26	Port output	Previous state	Previous state	High impedance	High impedance
P25/SCK	Port output	Previous state	Previous state	High impedance	High impedance
P24/SO	Port output	Previous state	Previous state	High impedance	High impedance
P23/SI	Port output	Previous state	Previous state	High impedance	High impedance
P22/TO	Port output	Previous state	Previous state	High impedance	High impedance
P21	Port output	Previous state	Previous state	High impedance	High impedance
P20/EC	Port output	Previous state	Previous state	High impedance	High impedance
P32/C0*2	Port output	Previous state	Previous state	High impedance	High impedance
P31/C1*2	Port output	Previous state	Previous state	High impedance	High impedance
P30/RCO	Port output	Previous state	Previous state	High impedance	H output
P47/P40*3	Port output	Previous state	Previous state	High impedance	High impedance
P57/P50*3	Port output	Previous state	Previous state	High impedance	High impedance
COM0 to COM3	Common output	Previous state	Previous state	Previous state	L output
SEG35 to SEG0	Segment output	Previous state	Previous state	Previous state	L output

*1: The reset pin is used as output pin according to the option setting.
*2: For microcontrollers with a built-in booster (MB89150A), these pins serve as capacitor connecting pins and not as ports.
*3: If segment output is selected, these pins serve as SEG35 to SEG0.

4. COMMAND

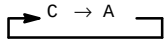
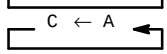
4.1 Transfer Instructions

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
2	MOV @IX+off,A	4	2	((IX)+off) ← (A)	–	–	–	– – – –	46
3	MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
4	MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
5	MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
6	MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
7	MOV A,dir	3	2	(A) ← dir	AL	–	–	+ + – –	05
8	MOV A,@IX+off	4	2	(A) ← ((IX)+off)	AL	–	–	+ + – –	06
9	MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
10	MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
11	MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
12	MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
13	MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
14	MOV @IX+off,#d8	5	3	((IX)+off)← d8	–	–	–	– – – –	86
15	MOV @EP,#d8	4	2	((EP))← d8	–	–	–	– – – –	87
16	MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
17	MOVW dir,A	4	2	(dir) ←(AH),(dir+1)← (AL)	–	–	–	– – – –	D5
18	MOVW @IX+off,A	5	2	((IX)+off)←(AH),((IX)+off+1)←(AL)	–	–	–	– – – –	D6
19	MOVW ext,A	5	3	(ext) ← (AH),(ext+1)←(AL)	–	–	–	– – – –	D4
20	MOVW @EP,A	4	1	((EP)) ← (AH),((EP)+1)← (AL)	–	–	–	– – – –	D7
21	MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
22	MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
23	MOVW A,dir	4	2	(AH)←(dir),(AL)←(dir+1)	AL	AH	dH	+ + – –	C5
24	MOVW A,@IX+off	5	2	(AH)←((IX)+off),(AL)←((IX)+off+1)	AL	AH	dH	+ + – –	C6
25	MOVW A,ext	5	3	(AH)←(ext),(AL)←(ext+1)	AL	AH	dH	+ + – –	C4
26	MOVW A,@A	4	1	(AH)←((A)),(AL)← ((A)+1)	AL	AH	dH	+ + – –	93
27	MOVW A,@EP	4	1	(AH)←((EP)),(AL) ←((EP)+1)	AL	AH	dH	+ + – –	C7
28	MOVH A,EP	2	1	(A) ←(EP)	–	–	dH	– – – –	F3
29	MOVW EP,#d16	3	3	(EP)←d16	–	–	–	– – – –	E7
30	MOVW IX,A	2	1	(IX)←(A)	–	–	–	– – – –	E2
31	MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
32	MOVW SP,A	2	1	(SP)← (A)	–	–	–	– – – –	E1
33	MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
34	MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
35	MOVW @A,T	4	1	((A)) ← (TH),((A)+1) ← (TL)	–	–	–	– – – –	83
36	MOVW IX,#d16	3	3	(IX)← d16	–	–	–	– – – –	E6
37	MOVW A,SP	2	1	(A) ← (PS)	–	–	dH	– – – –	70
38	MOVW PS,A	2	1	(PS)← (A)	–	–	–	+ + + +	71
39	MOVW SP,#d16	3	3	(SP)← d16	–	–	–	– – – –	E5
40	SWAP	2	1	(AH) ⇔ (AL)	–	–	AL	– – – –	10
41	SETB dir:n	4	2	(dir):n ← 1	–	–	–	– – – –	A8 to AF
42	CLRB dir:n	4	2	(dir):n ← 0	–	–	–	– – – –	A0 to A7
43	XCH A,T	2	1	(AL) ⇔ (TL)	AL	–	–	– – – –	42
44	XCHW A,T	3	1	(A) ⇔ (T)	AL	AH	dH	– – – –	43
45	XCHW A,EP	3	1	(A) ⇔ (EP)	–	–	dH	– – – –	F7
46	XCHW A,IX	3	1	(A) ⇔ (IX)	–	–	dH	– – – –	F6
47	XCHW A,SP	3	1	(A) ⇔ (SP)	–	–	dH	– – – –	F5
48	MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes

1. In byte transfer to A, T ← A is only for low bytes.
2. Operands for two or more operand instructions should be stored in the order designated in MNEMONIC (Opposite order to F^{2}MC-8 family).

4.2 Operation Instructions

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	ADDC A,Ri	3	1	(A) ← (A)+(Ri)+C	–	–	–	+ + + +	28 to 2F
2	ADDC A,#d8	2	2	(A) ← (A)+d8+C	–	–	–	+ + + +	24
3	ADDC A,dir	3	2	(A) ← (A)+(dir)+C	–	–	–	+ + + +	25
4	ADDC A,@IX+off	4	2	(A) ← (A)+((IX)+off)+C	–	–	–	+ + + +	26
5	ADDC A,@EP	3	1	(A) ← (A)+((EP))+C	–	–	–	+ + + +	27
6	ADDCW A	3	1	(A) ← (A)+(T)+C	–	–	dH	+ + + +	23
7	ADDC A	2	1	(AL)← (AL)+(TL)+C	–	–	–	+ + + +	22
8	SUBC A,Ri	3	1	(A) ← (A)–(Ri)–C	–	–	–	+ + + +	38 to 3F
9	SUBC A,#d8	2	2	(A) ← (A)–d8–C	–	–	–	+ + + +	34
10	SUBC A,dir	3	2	(A) ← (A)–(dir)–C	–	–	–	+ + + +	35
11	SUBC A,@IX+off	4	2	(A) ← (A)-((IX)+off)–C	–	–	–	+ + + +	36
12	SUBC A,@EP	3	1	(A) ← (A)-((EP))+C	–	–	–	+ + + +	37
13	SUBCW A	3	1	(A) ← (T)-(A)–C	–	–	dH	+ + + +	33
14	SUBC A	2	1	(AL)← (TL)-(AL)–C	–	–	–	+ + + +	32
15	INC Ri	4	1	(Ri)← (Ri)+1	–	–	–	+ + + –	C8 to CF
16	INCW EP	3	1	(EP)← (EP)+1	–	–	–	– – – –	C3
17	INCW IX	3	1	(IX)← (IX)+1	–	–	–	– – – –	C2
18	INCW A	3	1	(A) ← (A)+1	–	–	dH	+ + – –	C0
19	DEC Ri	4	1	(Ri)← (Ri)–1	–	–	–	+ + + –	D8 to DF
20	DECW EP	3	1	(EP)← (EP)–1	–	–	–	– – – –	D3
21	DECW IX	3	1	(IX)← (IX)–1	–	–	–	– – – –	D2
22	DECW A	3	1	(A) ← (A)–1	–	–	dH	+ + – –	D0
23	MULU A	19	1	(A) ← (AL)*(TL)	–	–	dH	– – – –	01
24	DIVU A	21	1	(A) ← (T)/(AL), MOD→(T)	dL	00	00	– – – –	11
25	ANDW A	3	1	(A) ← (A)∧(T)	–	–	dH	+ + R –	63
26	ORW A	3	1	(A) ← (A)∨(T)	–	–	dH	+ + R –	73
27	XORW A	3	1	(A) ← (A)∀(T)	–	–	dH	+ + R –	53
28	CMP A	2	1	(TL)–(AL)	–	–	–	+ + + +	12
29	CMPW A	3	1	(T)–(A)	–	–	–	+ + + +	13
30	RORC A	2	1		–	–	–	+ + – +	03
31	ROLC A	2	1		–	–	–	+ + – +	02
32	CMP A,#d8	2	2	(A)– d8	–	–	–	+ + + +	14
33	CMP A,dir	3	2	(A)– (dir)	–	–	–	+ + + +	15
34	CMP A,@EP	3	1	(A)– ((EP))	–	–	–	+ + + +	17
35	CMP A,@IX+off	4	2	(A)– ((IX)+off)	–	–	–	+ + + +	16
36	CMP A,Ri	3	1	(A)– (Ri)	–	–	–	+ + + +	18 to 1F
37	DAA	2	1	decimal adjust for addition	–	–	–	+ + + +	84
38	DAS	2	1	decimal adjust for subtraction	–	–	–	+ + + +	94
39	XOR A	2	1	(A) ← (AL) ∀(TL)	–	–	–	+ + R –	52
40	XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
41	XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
42	XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
43	XOR A,@IX+off	4	2	(A) ← (AL) ∀ ((IX)+off)	–	–	–	+ + R –	56
44	XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
45	AND A	2	1	(A) ← (AL)∧ (TL)	–	–	–	+ + R –	62
46	AND A,#d8	2	2	(A) ← (AL)∧ d8	–	–	–	+ + R –	64
47	AND A,dir	3	2	(A) ← (AL)∧(dir)	–	–	–	+ + R –	65
48	AND A,@EP	3	1	(A) ← (AL)∧((EP))	–	–	–	+ + R –	67
49	AND A,@IX+off	4	2	(A) ← (AL)∧((IX)+off)	–	–	–	+ + R –	66
50	AND A,Ri	3	1	(A) ← (AL)∧(Ri)	–	–	–	+ + R –	68 to 6F
51	OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
52	OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
53	OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
54	OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
55	OR A,@IX+off	4	2	(A) ← (AL) ∨ ((IX)+off)	–	–	–	+ + R –	76
56	OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
57	CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
58	CMP @EP,#d8	4	2	((EP))– d8	–	–	–	+ + + +	97
59	CMP @IX+off,#d8	5	3	((IX)+off) – d8	–	–	–	+ + + +	96
60	CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
61	INCW SP	3	1	(SP)← (SP) + 1	–	–	–	– – – –	C1
62	DECW SP	3	1	(SP)← (SP) – 1	–	–	–	– – – –	D1

4.3 Branch Instructions

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	BZ/BEQ rel	3	2	if Z=1 then PC ←PC+rel	–	–	–	– – – –	FD
2	BNZ/BNE rel	3	2	if Z=0 then PC ←PC+rel	–	–	–	– – – –	FC
3	BC/BLO rel	3	2	if C=1 then PC ←PC+rel	–	–	–	– – – –	F9
4	BNC/BHS rel	3	2	if C=0 then PC ←PC+rel	–	–	–	– – – –	F8
5	BN rel	3	2	if N=1 then PC ←PC+rel	–	–	–	– – – –	FB
6	BP rel	3	2	if N=0 then PC ←PC+rel	–	–	–	– – – –	FA
7	BLT rel	3	2	if V∀N=1 then PC←PC+rel	–	–	–	– – – –	FF
8	BGE rel	3	2	if V∀N=0 then PC←PC+rel	–	–	–	– – – –	FE
9	BBC dir:b,rel	5	3	if (dir:b)=0 then PC←PC+rel	–	–	–	– + – –	B0 to B7
10	BBS dir:b,rel	5	3	if (dir:b)=1 then PC←PC+rel	–	–	–	– + – –	B8 to BF
11	JMP @A	2	1	(PC)←(A)	–	–	–	– – – –	E0
12	JMP ext	3	3	(PC)←ext	–	–	–	– – – –	21
13	CALLV #vct	6	1	vector call	–	–	–	– – – –	E8 to EF
14	CALL ext	6	3	subroutine call	–	–	–	– – – –	31
15	XCHW A,PC	3	1	(PC)←(A), (A)←(PC)+1	–	–	dH	– – – –	F4
16	RET	4	1	return from subroutine	–	–	–	– – – –	20
17	RETI	6	1	return from interrupt	–	–	–	restore	30

4.4 Other Instructions

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	PUSHW A	4	1		–	–	–	– – – –	40
2	POPW A	4	1		–	–	dH	– – – –	50
3	PUSHW IX	4	1		–	–	–	– – – –	41
4	POPW IX	4	1		–	–	–	– – – –	51
5	NOP	1	1		–	–	–	– – – –	00
6	CLRC	1	1		–	–	–	– – – R	81
7	SETC	1	1		–	–	–	– – – S	91
8	CLRI	1	1		–	–	–	– – – –	80
9	SETI	1	1		–	–	–	– – – –	90

4.5 F^{2}MC-8L Instruction Map

5. MASK OPTIONS

Table 5-1 Mask Options

NO	Type	MB8915X/A	MB89P155	MB89PV150
	Specification method	**Select when ordering mask**	**Set by EPROM writer**	**Cannot be set**
1	Pull-up resistor { P00 to P07, P10 to P17 P20 to P27, P40 to P47 P50 to P57	Can be selected for each pin. However, P40 to 47 and P50 to P57 are specified only when segment output is not selected	P00 to P07 and P10 to P17 can be selected for each pin (Only P40 to P47, P50 to P57 and P20 to P27 do not have pull-up resistor.)	Pull-up resistor not provided
2	Power-on reset { Power-on reset available Power-on reset not available	Can be selected	Can be set	Power-on reset available
3	Oscillation stabilization time • Initial value of oscillation stabilization time of main clock can be set by selecting the values of WTM1 and WTM0 shown in the light columns	Can be selected WTM1 WTM0 0 0 : 2^2/f 0 1 : 2^{12}/f 1 0 : 2^{16}/f 1 1 : 2^{18}/f	Can be set WTM1 WTM0 0 0 : 2^2/f 0 1 : 2^{12}/f 1 0 : 2^{16}/f 1 1 : 2^{18}/f	Oscillation stabilization: 2^{16}/f
4	Types of main clock oscillation { Crystal or ceramic oscillator CR	Can be selected	Only crystal or ceramic oscillator	Only crystal or ceramic oscillator
5	Reset pin output { Reset output available Reset output not available	Can be selected	Can be set	Reset output available
6	Clock mode selection { Double clock mode Single clock mode	Can be selected	Can be set	Double clock mode
7	Selection of reference voltage supply method { Internally generated voltage Externally input voltage Selectable only for MB89150A	Can be selected	Can be set	—

Table 5-1 Mask Options (continued)

NO	Type	MB89151	MB89P155	MB89PV150
	Specification method	**Select when ordering mask**	**Selected by version number**	**Selected by version number**
8	Segment output switching selection 36: Port unselected 32: P57 to P54 selected 28: P57 to P50 selected 24: P57 to P50, P47 to P43 selected 20: P57 to P50, P47 to P40 selected	Selectable Select by number of segments	–101: 36 –102: 32 –103: 28 –104: 24 –105: 20	

Table 5-2 Configuration of Product Series

Product series	Temporary product	Piggyback/evaluation product	Number of segments	Booster
MB89150A	MB89P155-201 MB89P155-202 MB89P155-203 MB89P155-204 MB89P155-205	—	36 32 28 24 20	Provided
MB89150	MB89P155-101 MB89P155-102 MB89P155-103 MB89P155-104 MB89P155-105	MB89PV150-101 MB89PV150-102 MB89PV150-103 MB89PV150-104 MB89PV150-105	36 32 28 24 20	Unprovided

APPENDIX

APPENDIX A I/O MAP

Addresses 00_H – 17_H

Address	Read/Write	Register	Description of register
00_H	(R/W)	PDR0	Port-0 data register
01_H	(W)	DDR0	Port-0 direction register
02_H	(R/W)	PDR1	Port-1 data register
03_H	(W)	DDR1	Port-1 direction register
04_H	(R/W)	PDR2	Port-2 data register
05_H	(R/W)	DDR2	Port-2 direction register
06_H	—	—	—
07_H	(R/W)	SYCC	System clock control register
08_H	(R/W)	STBC	Standby-control register
09_H	(R/W)	WDTC	Watchdog-timer control register
$0A_H$	(R/W)	TBTC	Time-base timer control register
$0B_H$	(R/W)	WPCR	Watch prescaler control register
$0C_H$	(R/W)	PDR3	Port-3 data register
$0D_H$	—	—	—
$0E_H$	(R/W)	PDR4	Port-4 data register
$0F_H$	(R/W)	PDR5	Port-5 data register
10_H	(R/W)	BZCR	Buzzer register
11_H	—	—	—
12_H	—	—	—
13_H	—	—	—
14_H	(R/W)	RCR1	Remote-control register 1
15_H	(R/W)	RCR2	Remote-control register 2
16_H	—	—	—
17_H	—	—	—

Address 18_H – $7F_H$

Address	Read/Write	Register	Description of register
18_H	(R/W)	T2CR	Timer 2 control register
19_H	(R/W)	T1CR	Timer 1 control register
$1A_H$	(R/W)	T2DR	Timer 2 data register
$1B_H$	(R/W)	T1DR	Timer 1 data register
$1C_H$	(R/W)	SMR1	Serial mode register
$1D_H$	(R/W)	SDR1	Serial data register
$1E_H$ to $2F_H$	—	—	—
30_H	(R/W)	EIE1	External interrupt 1 control register 1
31_H	(R/W)	EIF1	External interrupt 1 flag register 1
32_H	(R/W)	EIE2	External interrupt 2 control register 2
33_H	(R/W)	EIF2	External interrupt 2 flag register 2
34_H to $5F_H$	—	—	—
60_H to 71_H	(R/W)	VRAM	RAM for displaying data
72_H	(R/W)	LCR1	LCDC control register 1
73_H to $7B_H$	—	—	—
$7C_H$	(W)	ILR1	Interrupt-level register 1
$7D_H$	(W)	ILR2	Interrupt-level register 2
$7E_H$	(W)	ILR3	Interrupt-level register 3
$7F_H$	Access disable	ITR	Interrupt-test register

APPENDIX B EPROM SETTING FOR MB89P155

MB89P155 is provided with the function corresponding to MBM27C256A by EPROM setting. The setting can be performed by writing program data with general-purpose EPROM writer through adaptor for exclusive use .

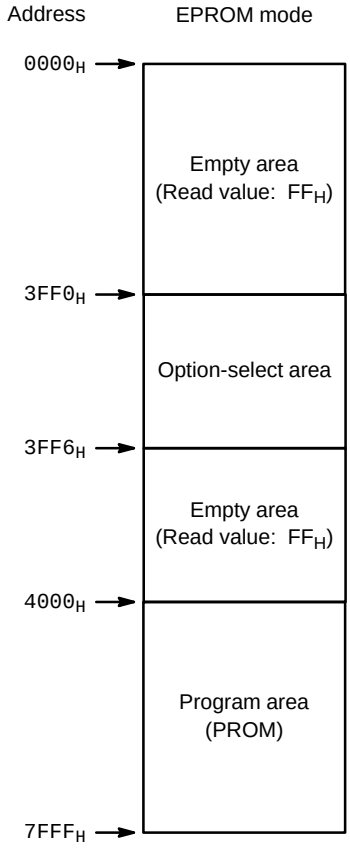
- Setting

  (1) Set the EPROM writer to MBM27C256A.

  (2) Load the program data from address 4000_H to address $7FFF_H$ of EPROM writer.
  (The data is loaded from address 8000_H to address $0FFFF_H$ in the operation mode, and from address 4000_H to address $7FFF_H$ in the EPROM mode.)
  Load the option information from address $3FF0_H$ to address $3FF6_H$ of the EPROM writer.
  (For the correspondence between the addresses and options, see the Bit Map on the next page.)

  (3) Write the data with the EPROM writer.

The memory space in the EPROM mode is as follows:



• Bit Map for PROM Option

	7	6	5	4	3	2	1	0
$3FF0_H$	Empty reset Readable	Empty Readable	Oscillation stabilization time WTM1 | WTM0 See Mask option list		Empty Readable	Reset pin 1: Available 0: Unavailable	Clock mode Output 1: Double 0: Single	Poewr-on selection 1: Available 0: Unavailable
$3FF1_H$	P07 Pull-up register 1: Unavailable 0: Available	P06 Pull-up register 1: Unavailable 0: Available	P05 Pull-up register 1: Unavailable 0: Available	P04 Pull-up register 1: Unavailable 0: Available	P03 Pull-up register 1: Unavailable 0: Available	P02 Pull-up register 1: Unavailable 0: Available	P01 Pull-up register 1: Unavailable 0: Available	P00 Pull-up register 1: Unavailable 0: Available
$3FF2_H$	P17 Pull-up register 1: Unavailable 0: Available	P16 Pull-up register 1: Unavailable 0: Available	P15 Pull-up register 1: Unavailable 0: Available	P14 Pull-up register 1: Unavailable 0: Available	P13 Pull-up register 1: Unavailable 0: Available	P12 Pull-up register 1: Unavailable 0: Available	P11 Pull-up register 1: Unavailable 0: Available	P10 Pull-up register 1: Unavailable 0: Available
$3FF3_H$	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable
$3FF4_H$	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable
$3FF5_H$	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable

Notes:
1. The initial value of each bit is 1.
2. Do not set 0 at empty bits.
   The read value of each empty bit is 1 unless 0 is set.

APPENDIX C ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

(V_{SS} = 0.0 V)

Parameter	Symbol	Requirements		Unit	Remarks
		Min.	Max.		
Supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
Supply voltage for LCD	V0 to V3	V_{SS} – 0.3	V_{SS} + 7.0	V	V0, V2 and V3 cannot exceed Vcc.
Supply voltage for EPROM program	V_{PP}	V_{SS} – 0.3	V_{CC} + 15.0	V	Applicable to MOD1 pin of MB89P155/A
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	All the pins must not exceed Vss + 7.0 V, excluding P20 to P27 without a pull-up resistor
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	Applicable to P20 to P27 without a pull-up resistor
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	All the pins must not exceed Vss + 7.0 V, excluding P20 to P27, P31 to P32, P40 to 47, and P50 to P57 without a pull-up resistor
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	Applicable to P20 to P27, P31 to P32, P40 to P47, and P50 to P57 without a pull-up resistor
Output current (L level)	I_{OL1}	—	10	mA	Applicable to all pins excluding P21, P26, and P27, and power supply pins
	I_{OL2}	—	20	mA	Applicable to P21, P26, and P27
Average output current (L level)	I_{OLAV1}	—	4	mA	Specified as average value in 1 hour. Applicable to all pins excluding, P21, P26, P27, and power pins.
	I_{OLAV2}	—	8	mA	Specified as the average value in 1 hour. Applicable to P21, P26, and P27.
Total output maximum current (L level)	ΣI_{OL}	—	40	mA	
Output current (H level)	I_{OH1}	—	–5	mA	Applicable to all pins excluding, P30 and power pins.
	I_{OH2}	—	–10	mA	Applicable to P30
Average output current (H level)	I_{OHAV1}	—	–2	mA	Specified as the average value in 1 hour. Applicable to P30 and power pins
	I_{OHAV2}	—	–4	mA	Specified as the average value in 1 hour. Applicable to P30
Total output maximum current (H level)	ΣI_{OH}	—	–10	mA	
Power consumption	P_d	—	300	mW	
Operation temperature	Ta	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

Note: Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operation Condition

(V_{SS} = 0.0 V)

Parameter	Symbol	Requirements		Unit	Remarks
		Min.	Max.		
Supply voltage	V_{CC}	2.2*1	6.0	V	Usual operation guarantee range
		1.5	6.0	V	RAM-data-holding guarantee range at stop mode
Supply voltage for LCD	V0 to V3	V_{SS}	V_{CC}	V	V0 to V3 pins for MB89150 The voltage range supplied to LCD and its optimum value depend on the LCD
Input voltage (H level)	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	P00 to P07, P10 to P17, P20 to P27
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	$\overline{RST}$, MOD0, MOD1, EC,SI, SCK, INT10 to INT13, INT20 to INT27
Input voltage (L level)	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	P00 to P07, P10 to P17, P20 to P27
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	$\overline{RST}$, MOD0, MOD1, EC,SI, SCK, INT10 to INT13, INT20 to INT27
Applied voltage at open-drain output pin	V_D	V_{SS} – 0.3	V_{SS} + 6.0*2	V	Applicable to P20 to P27, P31 to P32, P40 to P47, P50 to P57 without pull-up resistor
Operation temperature	Ta	–40	+85	°C	

*1: The minimum operating power supply voltage varies with the set values of frequency and instruction execution time (instruction cycle time) used.

*2: P31 and P32 are applicable for the MB89150 and P40 to P47 and P50 to P57 are applicable when port output is selected.

(Ta = –40° to 85 °C, V_{SS} = 0.0 V)

Parameter	Instruction cycle time*3	Minimum operating power supply voltage (V)				Remarks
		MB8915X	MB8915XA	MB89P155/A	MB89PV150	
Supply voltage	>0.95 µs	2.7	2.7	2.7	2.7	fch = 4.2 MHz, N = 4
	>1.33 µs	2.2	2.2			fch = 3 MHz, N = 4
	≥2.00 µs	2.2*4				fch = 2 MHz, N = 4
	≥4.00 µs	2.2*4				fch = 1 MHz, N = 4

*3: Instruction cycle time = N/fch (fch: frequency of main clock, N: gear set value = 4, 8, 16, 64)

*4: If the minimum operating power supply voltage is below 2.2 V, the guaranteed value should be treated individually.

3. DC Characteristics

(Ta = –40° to 85 °C, V_{CC} = 5.0 V, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Requirements			Unit	Remarks
				Min.	Typ.	Max.		
Output voltage (H level)	V_{OH1}	P00 to P07, P10 to P17	I_{OH} = –2.0 mA	2.4	—	—	V	
	V_{OH2}	P30	I_{OH} = –6.0 mA	4.0	—	—	V	
Output voltage (L level)	V_{OL1}	P00 to P07, P10 to P17, P20, P22 to P25, P30, P31 to P32, P40 to P47, P50 to P57	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL3}	P21, P26, P27	I_{OL} = 8.0 mA	—	—	0.4	V	
Input leak current (Hi-z output leak current)	I_{LI1}	MOD0, MOD1, P30, P00 to P07, P10 to P17	0.45 V < V_I < V_{CC}	—	—	±5	µA	When pull-up available is not specified
Open-drain output leak current (off state)	I_{LO1}	P20 to P26, P30 to P32, P40 to P47, P50 to P57	0.45 V < V_I < V_{CC}	—	—	±1	µA	When pull-up available is not specified
Pull-up resistance value	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57, $\overline{RST}$	V_I = 0.0V	25	50	100	kΩ	When pull-up available is specified
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 5.0 V	—	—	2.5	kΩ	
Segment output impedance	R_{VSEG}	SEG0 to 35	V1 to V3 = 5.0 V	—	—	15	kΩ	
LCD divided resistance	R_{LCD}	V_{CC} to V0		300	500	750	kΩ	Only MB89150
LCD leak current	I_{LCDL}	V0 to V3, COM0 to COM3, SEG0 to SEG35		—	—	±1	µA	
Output voltage for boosting LCD	V_{OV3}	V3	I_{IN} = 0µA	TBD	4.5	TBD	V	Only MB89150A
	V_{OV2}	V2		TBD	3.0	TBD	V	
	V_{OV1}	V1		TBD	1.5	TBD	V	
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	10	—	pF	

Note: For pins for selection of segments (SEG20 to SEG35) and ports (P40 to P47, P50 to P57), see the limits values of ports when port output is selected and those for segments when segment output is selected. P31 and P32 are applicable only for the MB89150 (for the MB89150A, external capacitor connection pins are applicable).

(Ta = –40° to 85 °C, V_{SS} = 0.0 V)

Parameter	Symbol	Condition	Requirements						Unit	Remarks
			MB8915X			MB8915XA				
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Power supply voltage*1	Icc	fc_H = 3 MHz, Vcc = 5 V t_{INST} = 4/fc_H	—	5	10	—	5	10	mA	Main RUN mode t_{INST} = 1.3 µs
	Icc_2	fc_H = 3 MHz, Vcc = 3 V t_{INST} = 64/fc_H	—	TBD	TBD	—	TBD	TBD	mA	Main RUN mode t_{INST} = 21 µs
	Icc_S	fc_H = 3 MHz, Vcc = 5 V t_{INST} = 4/fc_H	—	2.5	5	—	2.5	5	mA	Main sleep mode t_{INST} = 1.3 µs
	Icc_{S2}	fc_H = 3 MHz, Vcc = 3 V t_{INST} = 64/fc_H	—	TBD	TBD	—	TBD	TBD	mA	Main sleep mode t_{INST} = 21 µs
	Icc_{SB}	fc_L = 32 kHz, Vcc = 3 V t_{INST} = 2/fc_L	—	50	100	—	TBD	TBD	µA	Sub RUN mode t_{INST} = 64 µs
	Icc_{SBS}	fc_L = 32 kHz, Vcc = 3 V	—	25	50	—	TBD	TBD	µA	Subsleep mode
	Icc_T	fc_L = 32 kHz, Vcc = 3 V	—	10	15	—	TBD	TBD	µA	Watch mode
	Icc_H	Ta = 25°C, Vcc = 5 V	—	0.1	1	—	—	—	µA	Stop mode

*1: Specified under conditions where external clock and output pin kept open. t_{INST} is the set value to the instruction execution time (instruction cycle time).

(Ta = –40° to 85 °C, V_{SS} = 0.0 V)

Parameter	Symbol	Condition	Requirements						Unit	Remarks
			MB8915X			MB8915XA				
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Power supply voltage*2	Icc	fc_H = 3 MHz, Vcc = 5 V t_{INST} = 4/fc_H	—	TBD	TBD	—	TBD	TBD	mA	Main RUN mode t_{INST} = 1.3 µs
	Icc_2	fc_H = 3 MHz, Vcc = 3 V t_{INST} = 64/fc_H	—	TBD	TBD	—	TBD	TBD	mA	Main RUN mode t_{INST} = 21 µs
	Icc_{SB}	fc_L = 32 kHz, Vcc = 3 V t_{INST} = 2/fc_L	—	TBD	TBD	—	TBD	TBD	µA	Sub RUN mode t_{INST} = 64 µs
	Icc_H	Ta = 25°C, Vcc = 5 V	—	0.1	10	—	—	—	µA	Stop mode

*2: Defined under the condition of external clock and output pins opened. t_{INST} is the set value of instruction execution time (instruction cycle time). See the limit values of the MB8915X/15XA for the other specifications of the power supply voltage.

4. AC Standard

• Clock timing

(Ta = –40° to 85°C, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Requirements			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	fc_H	X0, X1	1	—	4.2	MHz	Main clock
	fc_L	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1	238	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	Subclock
Input clock duty ratio*1	duty	X0	30	—	70	%	Applied when using external clock
	$duty_1$	X0A					
Input clock pulse rise/fall time	t_{CR} t_{CF}	X0, X0A	—	—	10	ns	

*1: duty = P_{WH}/t_{HCYL}
$duty_1 = P_{WHL}/t_{HCYL}$

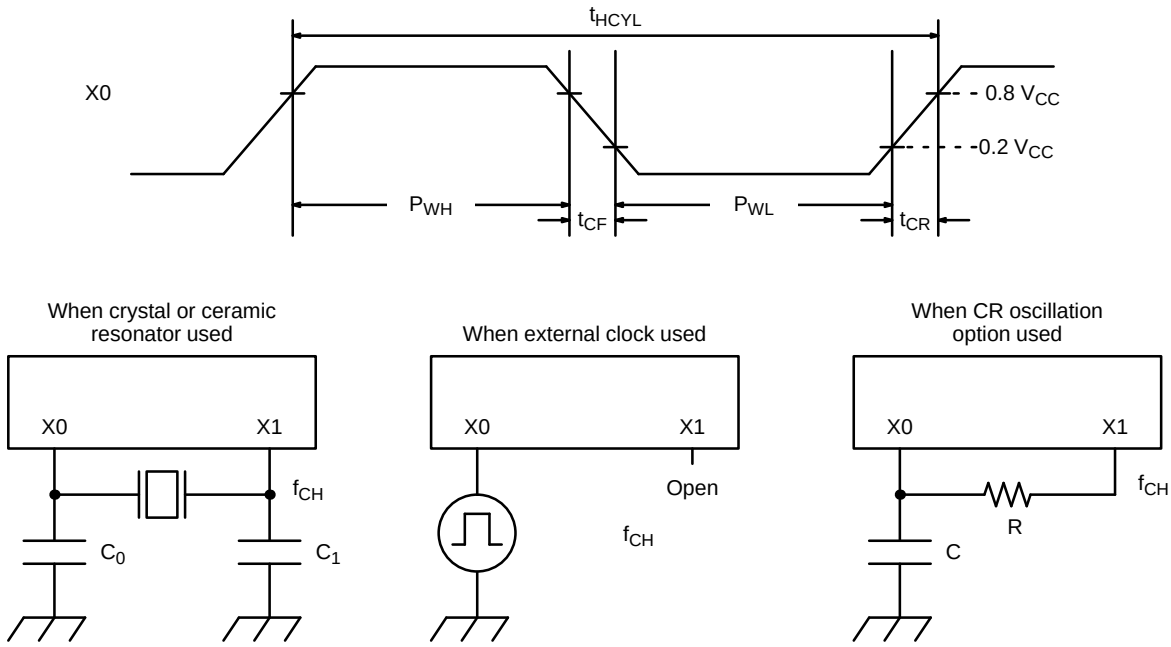
• Instruction cycle time

(Ta = –40° to 85°C, V_{SS} = 0.0 V)

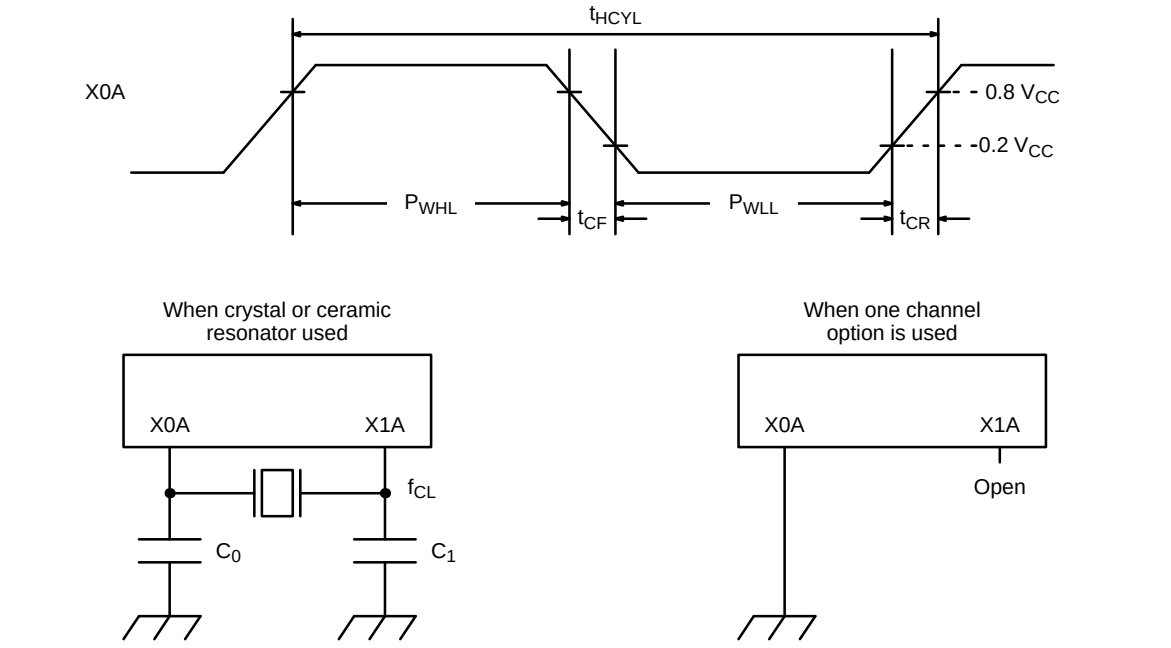
Parameter	Symbol	Pin	Requirements			Unit	Remarks
			Min.	Typ.	Max.		
Minimum instruction execution time (Instruction cycle time)	t_{INST}	*1	0.95	—	64	µs	At main clock operation
		*2	—	61.036	—	µs	At subclock operation

*1: t_{INST} in the main clock mode varies with the setting of the instruction execution time (gear) over the range of $4/fc_H$ to $64/fc_H$.
*2: t_{INST} in the subclock mode is $2/fc_L$.

– Main clock timing and application condition



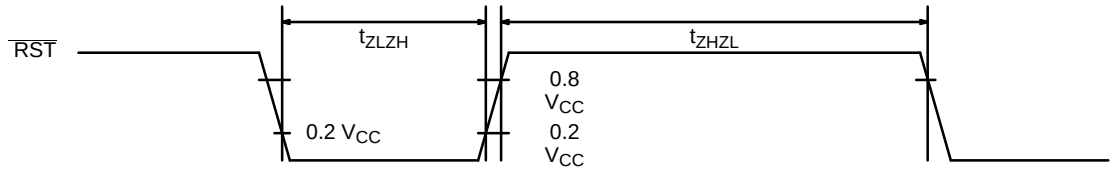
– Subclock timing and application condition



• Reset timing

(Ta = –40° to 85°C, V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V)

Parameter	Symbol	Condition	Requirements		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ LOW pulse width	t_{ZLZH}		8 t_{HCYL}	—	ns	
$\overline{RST}$ HIGH pulse width	t_{ZHZL}		4 t_{HCYL}	—	ns	



• Power-on reset

(Ta = –40° to 85°C, AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Condition	Requirements		Unit	Remarks
			Min.	Max.		
Power rise time	t_R		—	50	ms	Only when Power-on reset provided
Power off time	t_{OFF}		1	—	ms	At repetitive operation

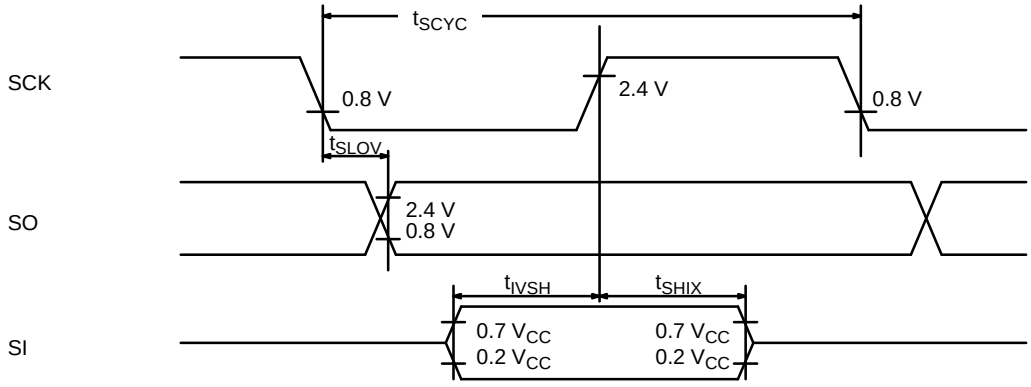
Note: If Power-on Reset Provided is selected, an abrupt change in the power supply voltage could cause a power-on reset. When changing the power supply voltage during operation, voltage fluctuations should be two or less times for smooth start-up.

• Serial I/O timing

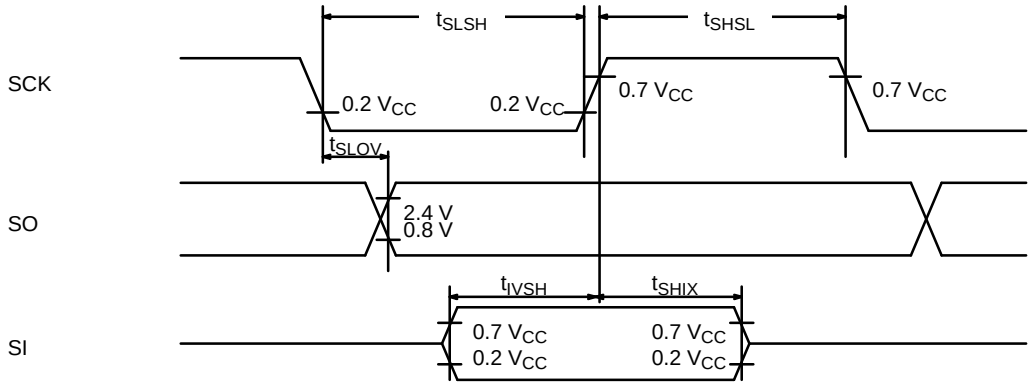
(Ta = –40° to 85°C, V_{CC} = 5 V ±10%, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Requirements		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation	2 t_{INST}	—	ns	
SCK ↓ ⇒ SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Effective SI ⇒ SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{INST}	—	ns	
SCK ↑ ⇒ effective SI hold time	t_{SHIX}	SCK, SI		0.5 t_{INST}	—	ns	
Serial clock pulse width at HIGH level	t_{SHSL}	SCK	External clock operation	t_{INST}	—	ns	
Serial clock pulse width at LOW level	t_{SLSH}	SCK		t_{INST}	—	ns	
SCK ↓ ⇒ SO time	t_{SLOV}	SCK, SO		0	200	ns	
Effective SI ⇒ SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{INST}	—	ns	
SCK ↑ ⇒ effective SI hold time	t_{SHIX}	SCK, SI		0.5 t_{INST}	—	ns	

– Serial I/O Timing (Internal Clock Mode)



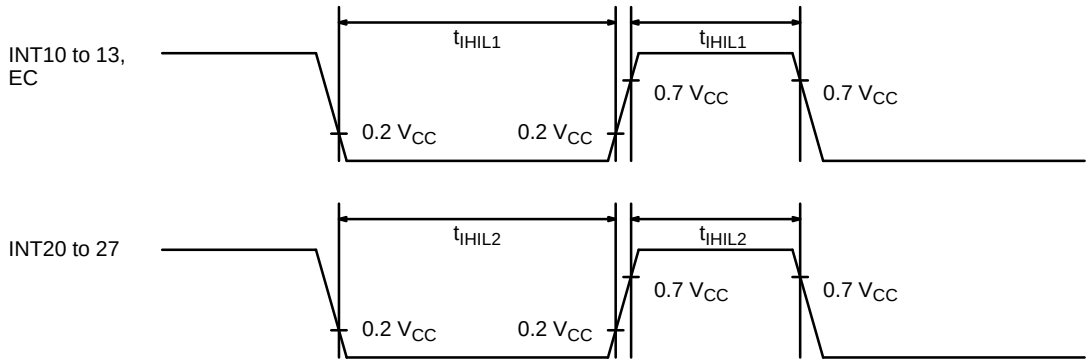
– Serial I/O Timing (External Clock Mode)



• Source input timing

(Ta = –40° to 85°C, V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Requirements		Unit	Remarks
			Min.	Max.		
Source input H Pulse width 1	t_{ILIH1}	INT10 to INT13, EC	t_{INST}	—	µs	
Source input L Pulse width 1	t_{IHIL1}	INT10 to INT13, EC	t_{INST}	—	µs	
Source input H Pulse width 2	t_{ILIH2}	INT20 to INT27	$2t_{INST}$	—	µs	
Source input L Pulse width 2	t_{IHIL2}	INT20 to INT27	$2t_{INST}$	—	µs	



L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir:0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir:1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir:2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW	CLRB dir:3	BBC dir:3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#dB		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir:4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV A,dir	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir:5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	MOV @IX+d,A	XOR A,@IX+d	AND A,@IX+d	OR A,@IX+d	MOV @IX+d,#d8	CMP @IX+d,#d8	CLRB dir:6	BBC dir:6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:7	BBC dir:7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir:0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir:1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir:2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir:3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir:4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir:5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir:6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir:7,rel	INC R7	DEC R7	CALLV #7	BLT rel