

F²MC-8L FAMILY MICROCONTROLLERS

MB89180 SERIES HARDWARE MANUAL

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MICROCONTROLLERS

MB89180 SERIES
HARDWARE MANUAL

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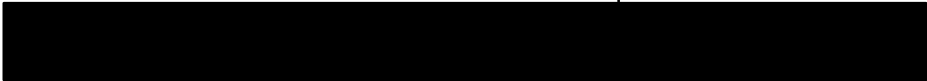
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1. GENERAL

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The MB89180 series microcontrollers contain various resources such as an LCD controller/driver, timers, serial interfaces, a remote-control carrier frequency generator, and external interrupts, including the compact instruction set.

1.1 FEATURES

- CPU core to common to F²MC-8L CPU
- Double-clock pulse control
- Maximum memory space: 64 Kbyte
- Minimum instruction execution time: 0.95 μ s at 4.2 MHz
- I/O ports: Max. 43
- 21-bit time-base counter
- 8/16-bit timer/counter: 1 channel
- 8-bit serial I/O: 1 channel
- External interrupt (Wake-up): 4 pins (Edge selection enabled) + 8 pins (Level interrupt)
- Buzzer output
- 15-bit watch prescaler
- LCD controller/driver with 32 segment outputs \times 4 common outputs (max. 128 pixels)
- Built-in remote-control carrier frequency generator
- Internal power-on reset (option)
- Low-power consumption modes (stop mode, sleep mode and watch mode)
- Package: QFP-64
- CMOS technology

1.2 PRODUCT SERIES

Table 1-1 lists the types and functions of the MB89180 series of microcontrollers.

Table 1-1 Types and Functions of MB89180 Series of Microcontrollers

Model Name	MB89181	MB89182	MB89183	MB89P185	MB89PV180
Classification	Mass-produced product (mask ROM product)			Temporary product	Piggyback/evaluation product (for development)
ROM capacity	4 K × 8 bits	6 K × 8 bits	8 K × 8 bits	16 K × 8 bits (Internal PROM, writable by general-purpose writer)	32 K × 8 bits (External ROM)
RAM capacity	128 × 8 bits	256 × 8 bits		512 × 8 bits	
CPU functions	Number of basic instructions		136		
	Instruction bit length		8 bits		
	Instruction length		1 to 3 bytes		
	Data bit length		1, 8, 16 bits		
	Minimum instruction execution time		0.95 μs/4.2 MHz		
	Interrupt processing time		9 μs/4.2 MHz		
Port	I/O port (N-ch open drain)		8 (6 also used as resource pins)		
	Output port (N-ch open drain)		18 (16 also used as segment pins*1, 2 also used as common pins*2)		
	I/O port (CMOS)		16 (8 also used as interrupt pins, 8 also used as segment pins*1)		
	Output port (CMOS)		1 (also used as remote-control pin)		
	Total		43 (max.)		
Timer counter	2 channels for 8-bit timer counter or 1 channel for 16-bit event counter				
Serial I/O	8-bit length 1 channel Selectable from least significant bit (LSB) first or most significant bit (MSB) first				
LCD controller and driver	Common output		4 (COM2 and COM3 used as output ports)		
	Segment output		32 (Max. 128 pixels)*1		
	Biased power pin		3		
	RAM capacity for LCD display		32 × 4 bits		
	Built-in dividing resistor for driving LCD (selectable from external resistor)				
Number of external interrupts	4 (selectable from rising edge, falling edge, or both edges)*1, used as segment pins 8 (interrupt for level only)				
Buzzer output	1 (7-type frequencies are programmable)				
Remote-control carrier frequency	1 (pulse width and cycle are programmable)				
Standby mode	Sleep, Stop and Watch mode				
Process	CMOS				
Package	QFP-64			MQFP-64	
Operating voltage	2.2 V to 6.0 V*3		2.7 V to 6.0 V		2.7 V to 6.0 V
EMROM used	MBM27C256A-25 (LCC package)				

*1 Selected by the mask option.

*2 Pseudo N-ch open-drain output.

*3 Operation under 2.2 volt will be provided individually.

1.3 BLOCK DIAGRAM

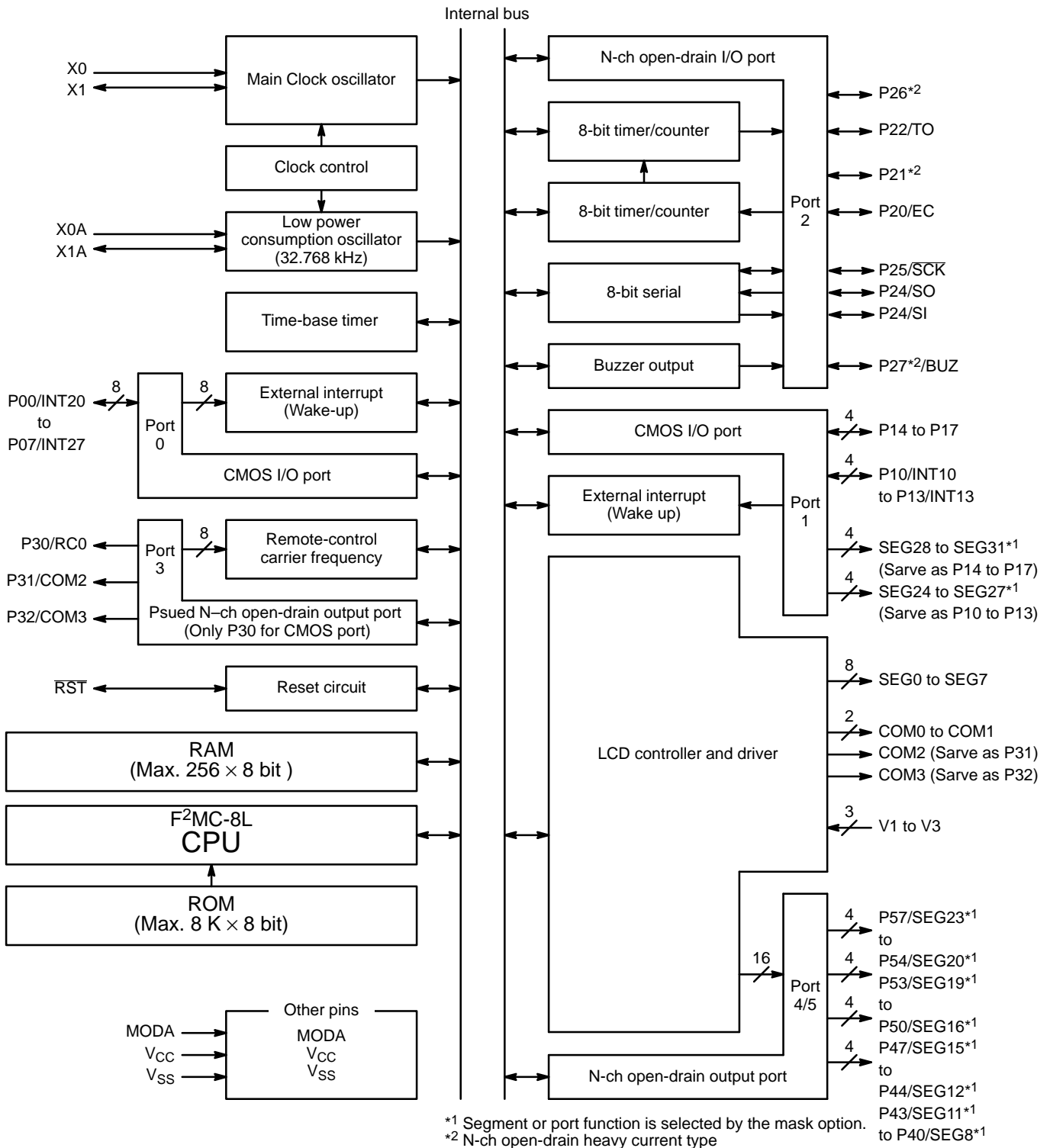
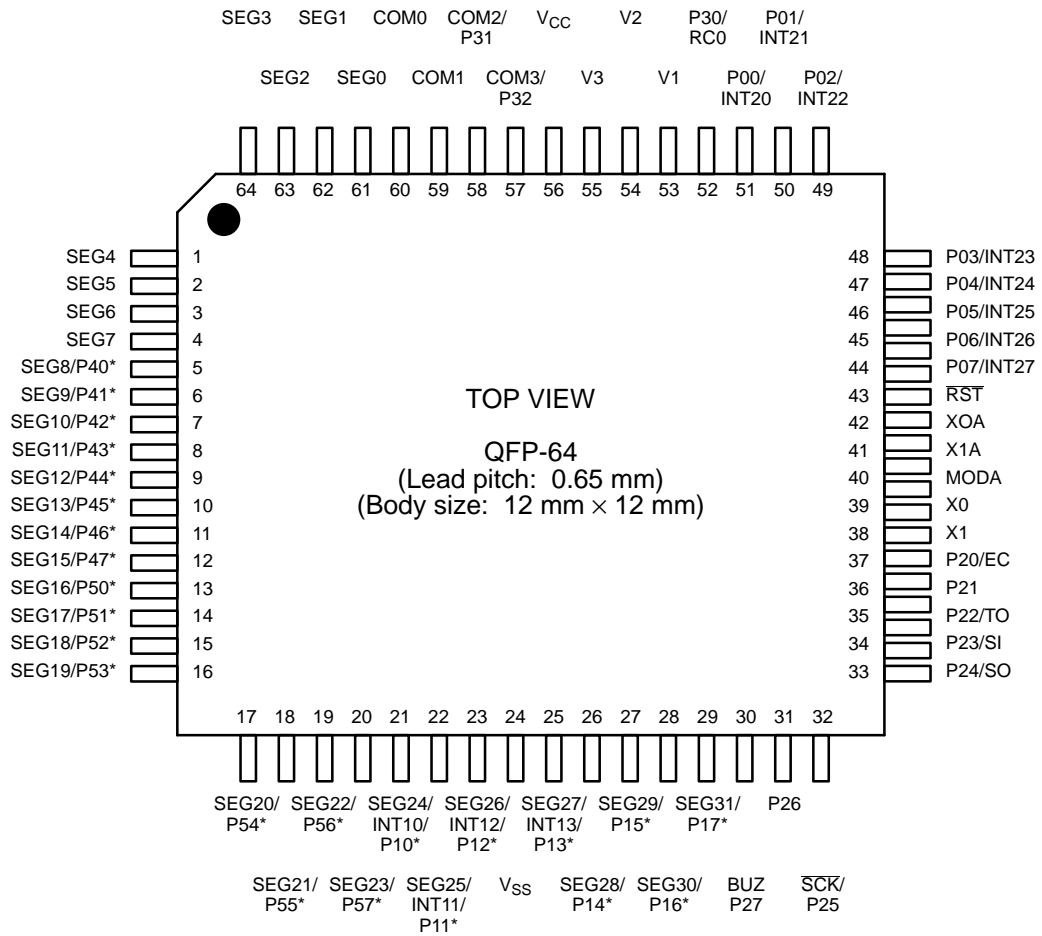


Fig. 1.1 Block Diagram

1.4 PIN ASSIGNMENT

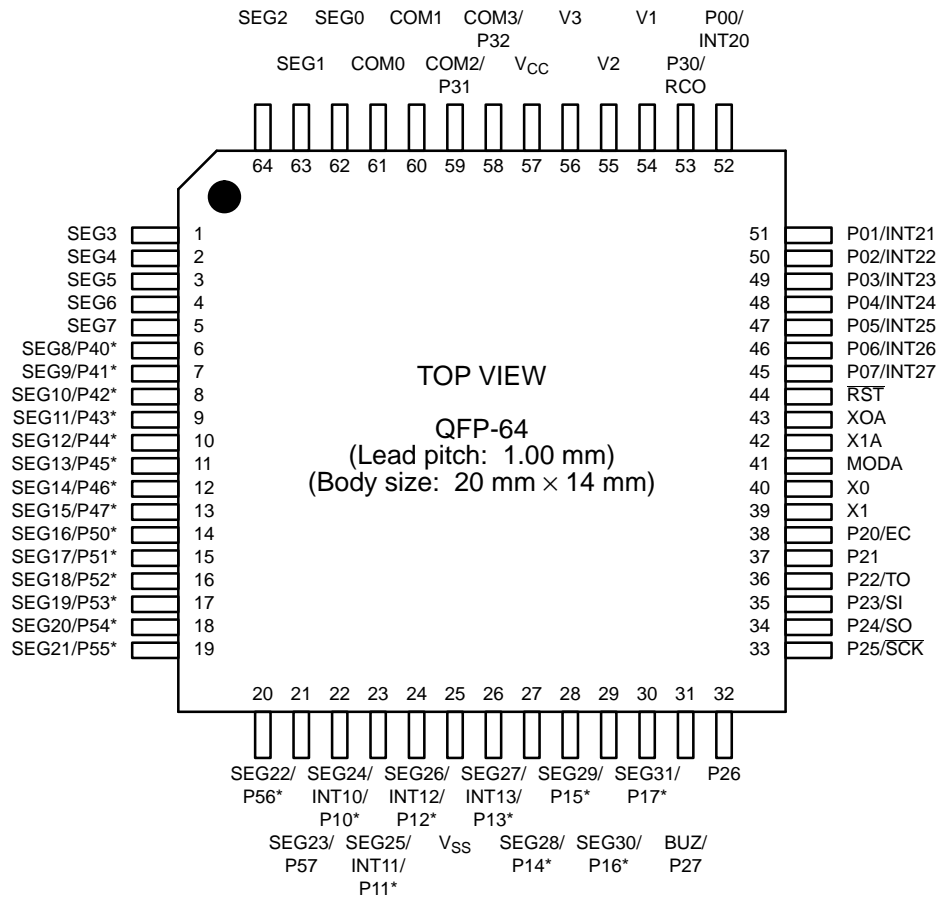
- Model with this pin assignment: MB8918X/P185



* Selected by the mask option at four pins

Fig. 1.2 Pin Assignment (FPT-64P-M09)

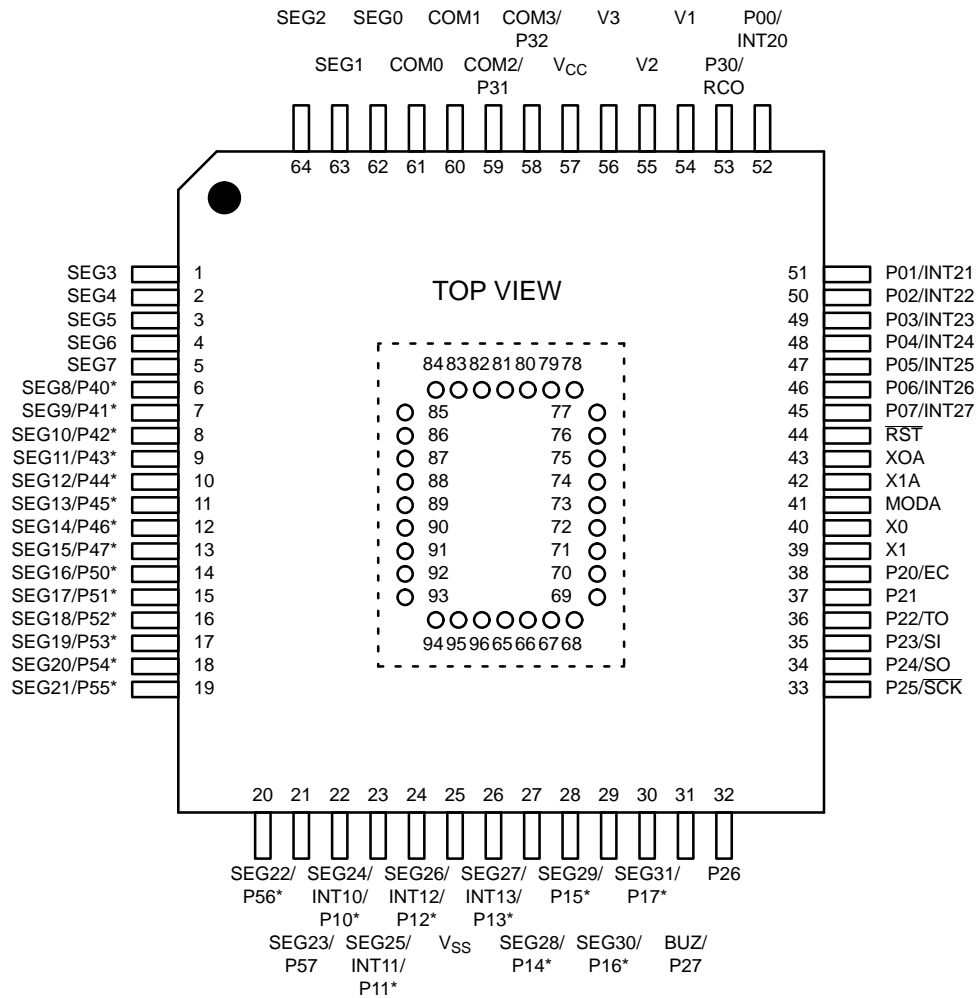
- Model with this pin assignment: MB89181/182/183/P185



* Selected by the mask option at four pins

Fig. 1.3 Pin Assignment (FPT-64P-M06)

- Model with this pin assignment: MB89PV180



* Selected by the mask option at four pins

Fig. 1.4 Pin Assignment (MQP-64C-P01)

1.5 PIN FUNCTION DESCRIPTION

Table 1-2 and Table 1-3 lists the pin function and Figure 1.3 shows the input/output circuit configurations.

Table 1-2 Pin Function Description

Pin No.		Pin Name	Circuit type	Function
QFP 0.65	QFP 1.00			
39	40	X0	A	Crystal oscillator pins for main clock CR oscillation available (only for mask product)
38	39	X1		
40	41	MODA	B	Operation-mode select pins These pins are connected directly to V _{SS} .
43	44	$\overline{\text{RST}}$	C	Reset I/O pin This pin consists of an N-ch open-drain output with a pull-up resistor and hysteresis input. A Low level is output from this pin. The internal circuit is initialized at input of a Low level.
51 to 44	52 to 45	P00/INT20 to P07/INT27	D	General-purpose I/O ports These ports also serve as external interrupt 2 input (wake-up input) pins. Input is hysteresis type.
21 to 25	22 to 26	P10/INT10/SEG24 to P13/INT13/SEG27	D/J	General-purpose I/O ports These ports also serve as pins for input of external interrupt 1. Input of external interrupt 1 is hysteresis type. These ports also serve as LCDC segment output pins. They should be switched by the mask option.
26 to 29	27 to 30	P14/SEG28 to P17/SEG31	E/J	General-purpose I/O port These ports also serve as LCDC segment output pins. They should be switched by the mask option.
37	38	P20/EC	G	N-ch open-drain type general-purpose I/O port This port also serves as an external clock input pin for the timer. The resource is hysteresis input.
36	37	P21	H	N-ch open-drain type general-purpose I/O port
35	36	P22/TO	H	N-ch open-drain type general-purpose I/O port This port also serves as a timer output pin.
34	35	P23/SI	G	N-ch open-drain type general-purpose I/O port This port also serves as a serial I/O data input pin. The resource is hysteresis input.
33	34	P24/SO	H	N-ch open-drain type general-purpose I/O port This port also serves as a serial I/O data output pin.
32	33	P25/ $\overline{\text{SCK}}$	G	N-ch open-drain type general-purpose I/O port This port also serves as a serial I/O clock output pin. The resource is hysteresis input.
31	32	P26	H	N-ch open-drain type general-purpose I/O port
30	31	P27/BUZ	H	N-ch open-drain type general-purpose I/O port This port also serves as a buzzer output pin.

Table 1-2 Pin Function Description (Continued)

Pin No.		Pin Name	Circuit type	Function
QFP 0.65	QFP 1.00			
52	53	P30/RCO	F	General-purpose output-only port This port also serves as a remote-control carrier frequency output pin.
20 to 13	21 to 14	P57/SEG23 to P50/SEG16	I/J	N-ch open-drain type general-purpose output ports These ports also serve as LCDC segment output pins. They should be switched by the mask option.
12 to 5	13 to 6	P47/SEG15 to P40/SEG8	I/J	N-ch open-drain type general-purpose output ports These ports also serve as LCDC segment output pins. They should be switched by the mask option.
4 to 61	5 to 62	SEG7 to SEG0	J	LCDC segment output-only pins
57 58	58 59	COM3/P32 COM2/P31	K	Pseudo N-ch open-drain type general-purpose output ports These ports also serve as LCDC common output-only pins.
59 60	60 61	COM1 COM0	J	LCDC common output-only pins
55 54 53	56 55 54	V3 V2 V1	—	Power pins for driving LCD
42	43	X0A	A'	Low-speed clock pulse oscillation pin (32.768 KHz)
41	42	X1A		
56	57	V _{CC}	—	Power pin
24	25	V _{SS}	—	Power (GND) pin

Table 1-3 Pins for External ROM

Pin No.	Pin Name	Circuit type	Function
QFP 1.00			
66	V _{PP}	Output	High-level output pin
67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	Output	Address-output pins
77 78 79	01 02 03	Input	Data-input pins
80	V _{SS}	Output	Power (GND) pin
82 83 84 85 86	04 05 06 07 08	Input	Data-input pins
87	\overline{CE}	Output	Chip-enable pin for ROM A High level is output in the standby mode.
88	A10	Output	Address-output pin
89	\overline{OE}	Output	Output-enable pin for ROM A Low level is always output.
91 92 93	A11 A9 A8	Output	Address-output pins
94	A13	Output	Address-output pin
95	A14	Output	Address-output pin
96	V _{CC}	Output	Power pin for EPROM
65 76 81 92	NC	—	Internal-connection pins. These pins must always be kept open.

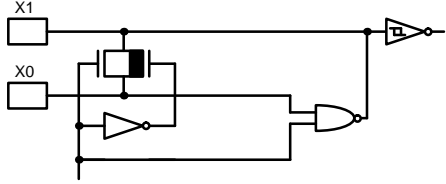
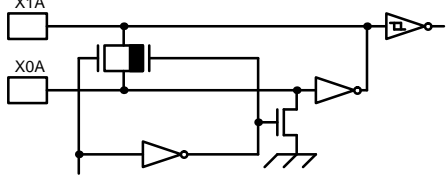
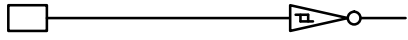
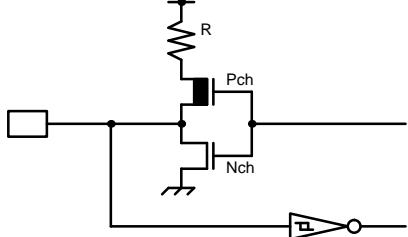
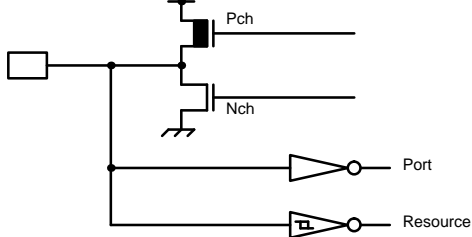
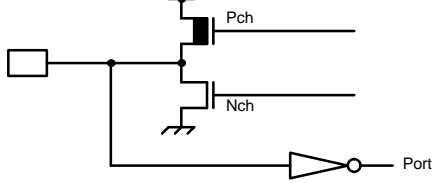
Classification	Circuit	Remarks
A	 <p>Standby control signal</p>	<p>Used for high speed pulse</p> <ul style="list-style-type: none"> • Feedback resistor: About 2 MΩ • CR oscillation can be selected (only for mask product)
A'	 <p>Standby control signal</p>	<p>Used for low speed pulse</p>
B		<ul style="list-style-type: none"> • Hysteresis input
C		<ul style="list-style-type: none"> • Output pull-up resistor (P-ch): About 50 kΩ (5 V) • Hysteresis input
D		<ul style="list-style-type: none"> • CMOS input/output • The resource is hysteresis input • The pull-up resistor is available (not available for MB89PV180)
E		<ul style="list-style-type: none"> • CMOS input/output • The pull-up resistor is available (not available for MB89PV180)

Fig. 1.5 Input/Output Circuit Configurations

Classification	Circuit	Remarks
F		<ul style="list-style-type: none"> • CMOS output • P-ch is driven with heavy current
G		<ul style="list-style-type: none"> • N-ch open-drain input/output • CMOS input • The resource is hysteresis input. • The pull-up resistor is available (not available for MB89P185 and MB89PV180)
H		<ul style="list-style-type: none"> • N-ch open-drain input/output • CMOS input • P21, P26, and P27 are heavy-current drive type pins. • The pull-up resistor is available (not available for MB89P185 and MB89PV180)
I		<ul style="list-style-type: none"> • N-ch open-drain output • The pull-up resistor is available (not available for MB89P185 and MB89PV180)
J		<ul style="list-style-type: none"> • LCDC segment output
K		<ul style="list-style-type: none"> • N-ch open-drain output • Common output and programmable • The pull-up resistor is not available

Fig. 1.5 Input/Output Circuit Configurations (Continued)

1.6 HANDLING DEVICES

(1) Preventing latch-up

Latch-up may occur if a voltage higher than V_{CC} or lower than V_{SS} is applied to the input or output pins, or if voltage exceeding the rated value is applied between V_{CC} and V_{SS} .

When latch-up occurs, the supply current increases rapidly, sometimes resulting in overheating and destruction. Therefore, no voltage exceeding the maximum ratings should be used.

(2) Handling unused input pins

Leaving unused input pins open may cause a malfunction. Therefore, these pins should be set to pull-up or pull-down.

(3) Setting Non-Connection (NC) pin

Always set NC (Non-Connection) open.

(4) Variations in supply voltage

Although the specified V_{CC} supply voltage operating range is assured, a sudden change in the supply voltage within the specified range may cause a malfunction. Therefore, the voltage supply to the IC should be kept as constant as possible. The V_{CC} ripple (P-P value) at the supply frequency (50 - 60 Hz) should be less than 10% of the typical V_{CC} value, or the coefficient of excessive variation should be less than 0.1 V/ms instantaneous change when the power supply is switched.

(5) Precautions for external clocks

It takes some time for oscillation to stabilize after changing the mode to power-on reset (option selection) and stop. Consequently, an external clock must be input.



2. HARDWARE CONFIGURATION

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2.14	WATCHDOG TIMER RESET	2-68

This chapter describes each block of the CPU hardware.

CPU

2.1 CPU

● This section describes the memory space and register composing CPU hardware.

■ Memory Space

The MB89180 series of microcontrollers have a memory area of 64K bytes. All I/O, data, and program areas are located in this space. The I/O area is near the lowest address and the data area is immediately above it. The data area may be divided into register, stack, and direct-address areas according to the applications. The program area is located near the highest address and the tables of interrupt and reset vectors and vector-call instructions are at the highest address. Figure 2.1 shows the structure of the memory space for the MB89180 series of microcontrollers.

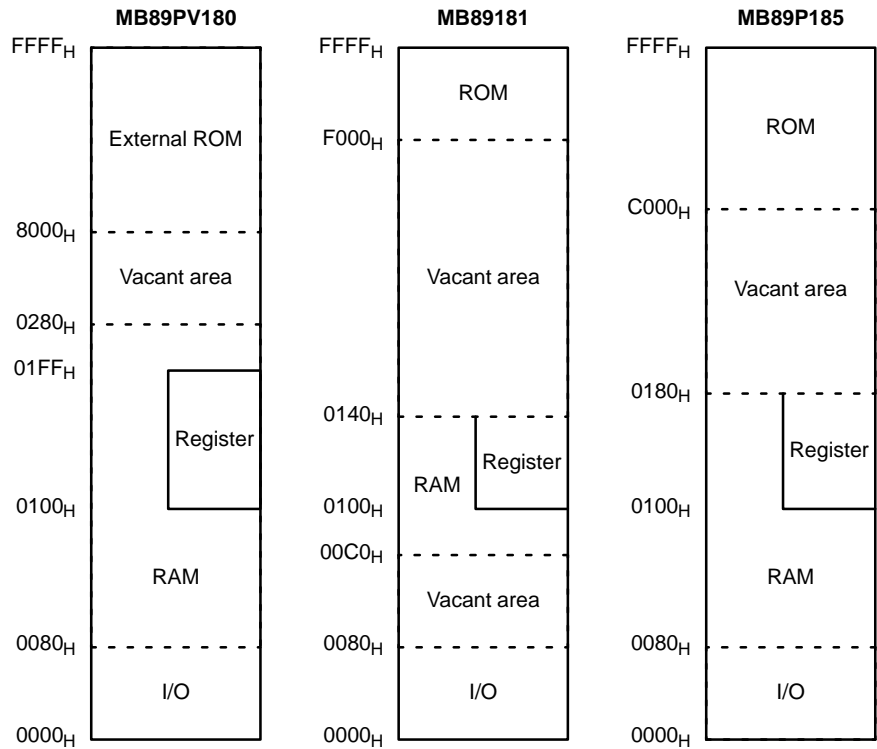


Fig. 2.1 Memory Space of MB89180 Series of Microcontrollers

CPU

- I/O area

This area is where various resources such as control and data registers are located. The memory map for the I/O area is given in APPENDIX A.

- RAM area

This area is where the static RAM is located. Addresses from 0100_H to 01FF_H are also used as the general-purpose register area.

- ROM area

This area is where the internal ROM is located. Addresses from FFC0_H to FFFF_H are also used for the table of reset and vector-call instructions. Table 2-1 shows the correspondence between each interrupt number or reset and the table addresses to be referenced for the MB89180 series of microcontrollers.

Table 2-1 Table of Reset and Interrupt Vectors

	Table address	
	Upper data	Lower data
CALLV #0	FFC0 _H	FFC1 _H
CALLV #1	FFC2 _H	FFC3 _H
CALLV #2	FFC4 _H	FFC5 _H
CALLV #3	FFC6 _H	FFC7 _H
CALLV #4	FFC8 _H	FFC9 _H
CALLV #5	FFCA _H	FFCB _H
CALLV #6	FFCC _H	FFCD _H
CALLV #7	FFCE _H	FFCF _H

	Table address	
	Upper data	Lower data
Interrupt #11	FFE4 _H	FFE5 _H
Interrupt #10	FFE6 _H	FFE7 _H
Interrupt #9	FFE8 _H	FFE9 _H
Interrupt #8	FFEA _H	FFEB _H
Interrupt #7	FFEC _H	FFED _H
Interrupt #6	FFEE _H	FFEF _H
Interrupt #5	FFF0 _H	FFF1 _H
Interrupt #4	FFF2 _H	FFF3 _H
Interrupt #3	FFF4 _H	FFF5 _H
Interrupt #2	FFF6 _H	FFF7 _H
Interrupt #1	FFF8 _H	FFF9 _H
Interrupt #0	FFFA _H	FFFB _H
Reset mode	——	FFFD _H
Reset vector	FFFE _H	FFFF _H

Note: FFFC_H is already reserved.

CPU

■ Arrangement of 16-bit Data in Memory

When the MB89180 series of microcontrollers handle 16-bit data, the data written at the lower address is treated as the upper data and that written at the next address is treated as the lower data as shown in Figure 2.2.

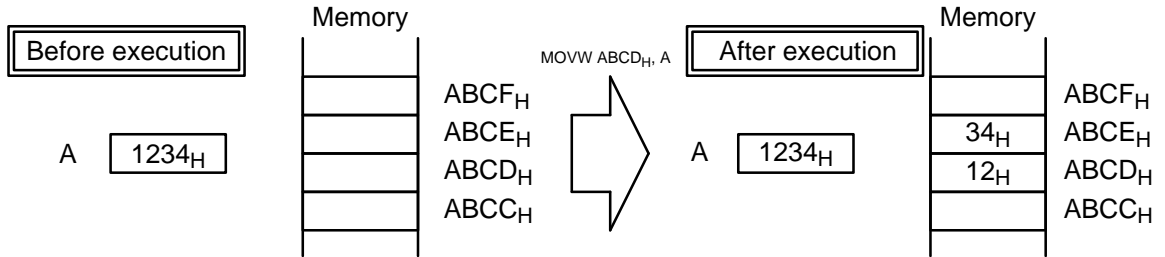
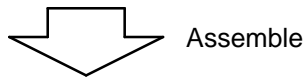


Fig. 2.2 Arrangement of 16-bit Data in Memory

This is the same as when 16-bits are specified by the operand during execution of an instruction. Bits closer to the OP code are treated as the upper byte and those next to it are treated as the lower byte. This is also the same when the memory address or 16-bit immediate data is specified by the operand.

[Example]

```
MOV A, 5678H ; Extended address
MOV A, #1234H ; 16-bit immediate data
```



```

:
XXXXH XX XX
XXXXH 60 56 78 ; Extended address
XXXXH E4 12 34 ; 16-bit immediate data
XXXXH XX
:

```

Fig. 2.3 Arrangement of 16-bit Data during Execution of Instruction

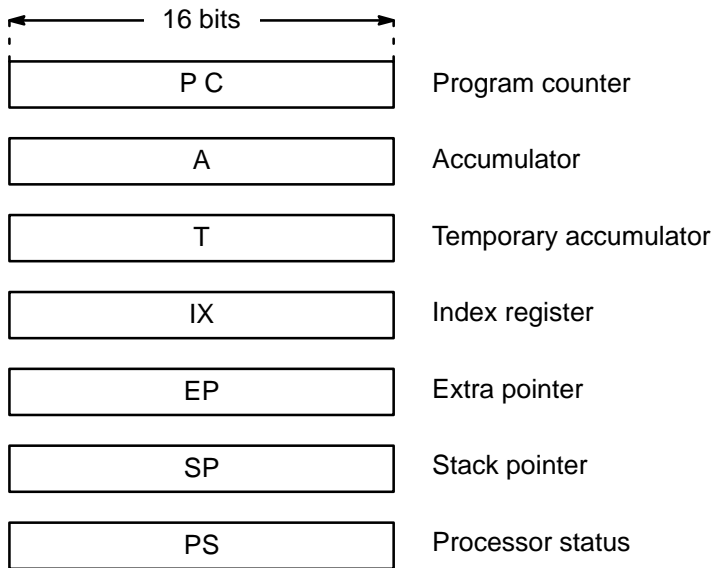
Data saved in the stack by an interrupt is also treated in the same manner.

CPU

■ Internal Registers in CPU

The MB89180 series of microcontrollers have dedicated registers in the CPU and general-purpose registers in memory.

- Program counter (PC) 16-bit long register indicating location where instructions stored
- Accumulator (A) 16-bit long register where results of operations stored temporarily; the lower byte is used to execute 8-bit data processing instructions.
- Temporary accumulator (T) 16-bit long register; the operations are performed between this register and the accumulator. The lower one byte is used to execute 8-bit data processing instructions
- Stack pointer (SP) 16-bit long register indicating stack area
- Processor status (PS) 16-bit long register where register pointers and condition codes stored
- Index register (IX) 16-bit long register for index modification
- Extra pointer (EP) 16-bit long register for memory addressing



The 16 bits of the processor status (PS) can be divided into 8 upper bits for a register bank pointer (RP) and 8 lower bits for a condition code register (CCR). (See Figure 2.4.)

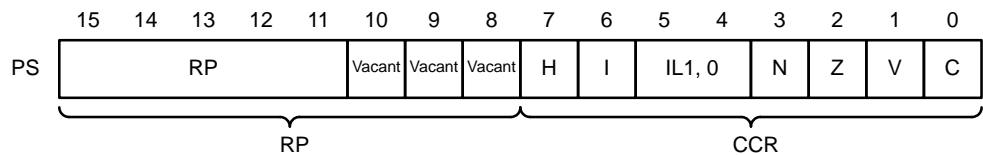


Fig. 2.4 Structure of Processor Status

CPU

The RP indicates the address of the current register bank and the contents of the RP; the real addresses are translated as shown in Figure 2.5.

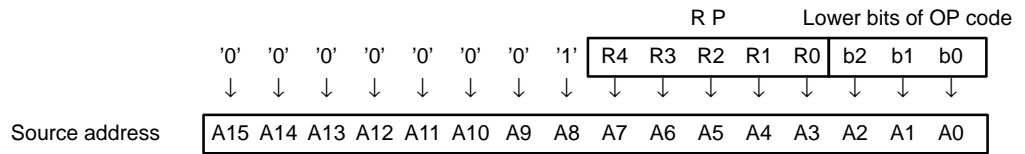


Fig. 2.5 Rule for Translating Real Addresses at General-purpose Register Area

The CCR has bits indicating the results of operations and transfer data contents, and bits controlling the CPU operation when an interrupt occurs.

- H-flag H-flag is set when a carry or a borrow out of bit 3 into bit 4 is generated as a result of operations; it is cleared in other cases. This flag is used for decimal-correction instructions.
- I-flag An interrupt is enabled when this flag is 1 and is disabled when it is 0. The I-flag is 0 at reset.
- IL1 and IL0 These bits indicate the level of the currently-enabled interrupt. The CPU executes interrupt processing only when an interrupt with a value smaller than the value indicated by this bit is requested.

IL1	IL0	Interrupt level	High and low
0	0	1	<div style="display: flex; align-items: center; justify-content: center;"> High ↑ ↓ Low = No interrupt </div>
0	1		
1	0	2	
1	1	3	

- N-flag The N-flag is set when the most significant bit is 1 as a result of operations; it is cleared when the MSB is 0.
- Z-flag Z-flag is set when the bit is 0 as a result of operations; it is cleared in other cases.
- V-flag V-flag is set when a two's complement overflow occurs as a result of operations; it is reset when an overflow does not occur.
- C-flag C-flag is set when a carry or a borrow out of bit 7 is generated as a result of operations; it is cleared in other cases. When the shift instruction is executed, the value of the C-flag is shifted out.

CPU

- General-purpose registers
General-purpose registers are 8-bit long registers for storing data.

The 8-bit long general-purpose registers are in the register banks in memory. One bank has eight registers and up to 8 banks are available for the MB89181 series of microcontrollers, respectively. The register bank pointer (RP) indicates the currently-used bank.

Note: The number of register banks used depends on the RAM capacity.

$$\text{Address} = 0100_{\text{H}} + 8 * (\text{RP})$$

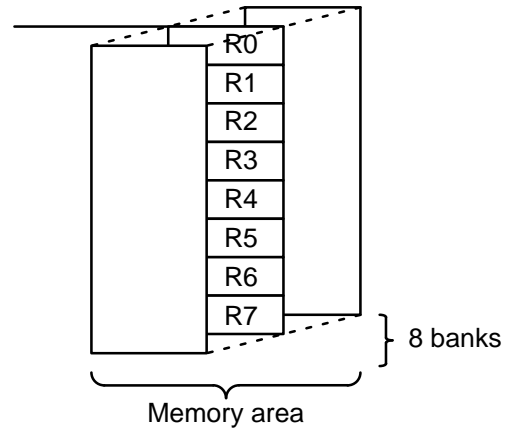


Fig. 2.6 Register Bank Configuration

CPU

■ Operation Modes

The MB89180 series of microcontrollers only has the single-chip mode. The memory map is as follows:

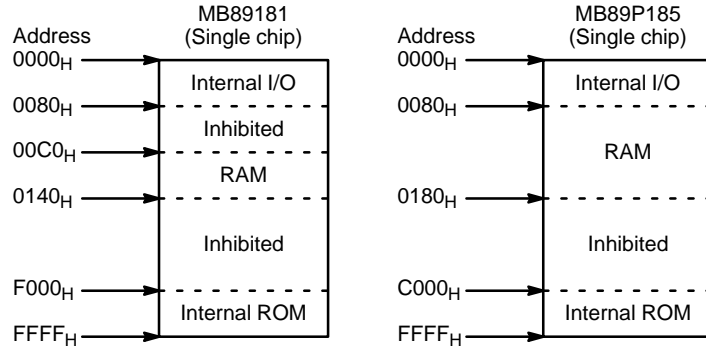


Fig. 2.7 Memory Map in Various Modes

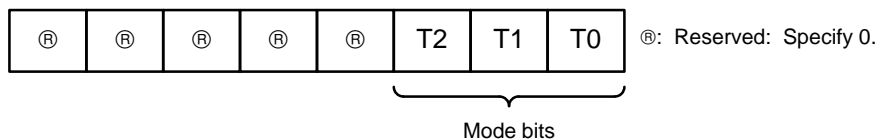
The mode that the device enters depends on the states of the device-mode pins and the contents of the mode data fetched during the reset sequence.

The relationship between the states and operations of the device-mode pins is shown below. (Only 00 can be set for MB89180.)

MODA	Description
0	Reset vectors are read from the internal ROM. The external access does not function.
1	

Write mode for products containing EPROM.

The following functions are selected according to the mode-data setting conditions.



T2	T1	T0	Operation
0	0	0	Select single-chip mode.
Other than above			Reserved. Do not set.

Note: Do not select the single-chip mode with the externally-fetched mode data

MAIN/SUBCLOCK CONTROL BLOCK

2.2 MAIN/SUB CLOCK CONTROL BLOCK

● This block controls the standby operation, oscillation stabilization time, software reset, and clock switching.

■ **Block Diagram**

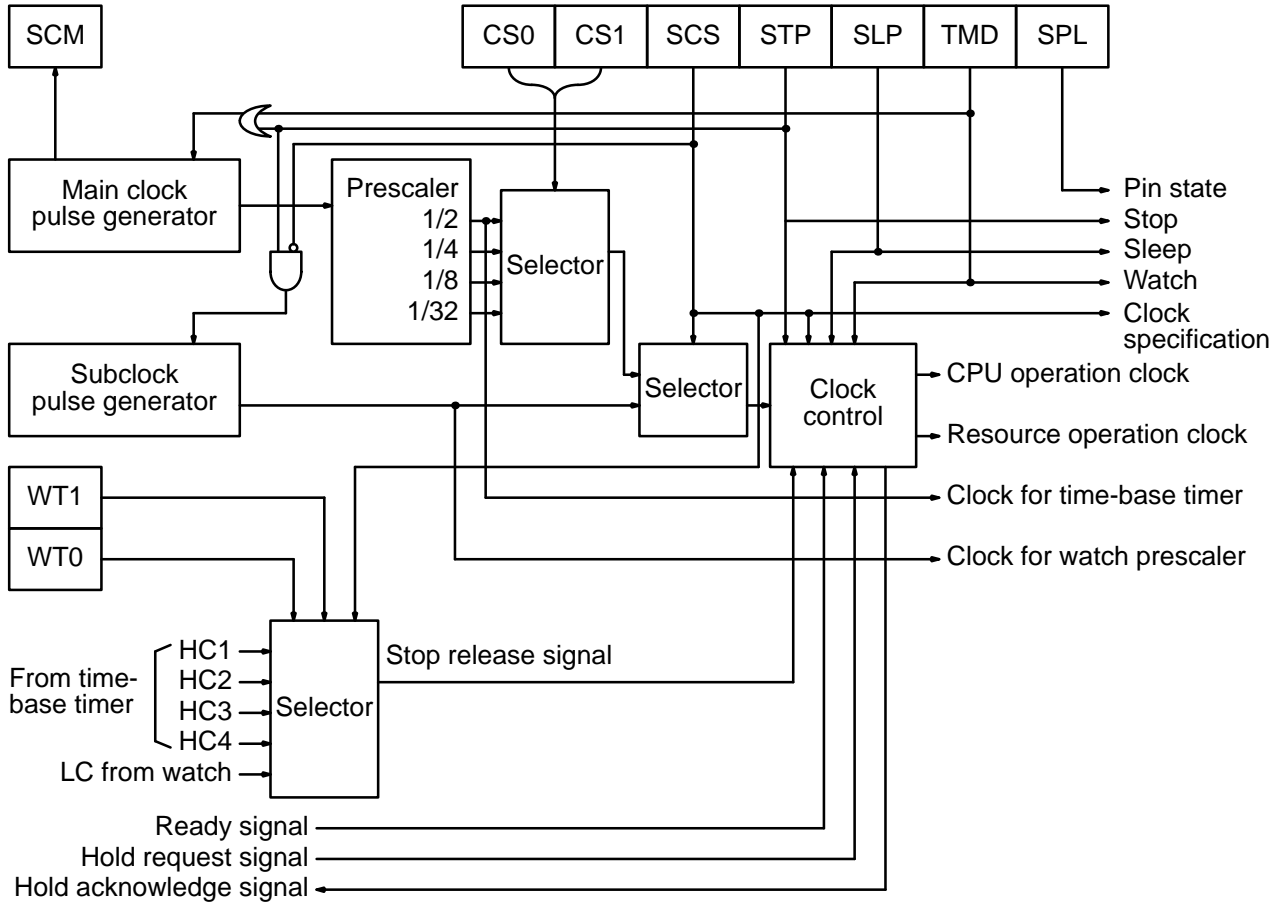


Fig. 2.8 Machine Clock Control Block Diagram

■ **Register List**

Main/sub clock control block consists of standby control register (STBC) and system clock control register (SYCC).

	8 bit	
Address: 0007 _H	SYCC	R/W System clock control register
Address: 0008 _H	STBC	R/W Standby control register

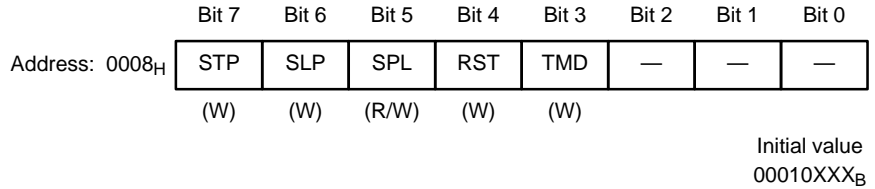
**MAIN/SUBCLOCK
CONTROL BLOCK**

Address: SYCC
0007_H
Address: STBC
0008_H

■ Description of Registers

The detail of each register is described below.

(1) Standby-control register (STBC)



[Bit 7] STP: Stop bit

This bit is used to specify switching CPU to the stop mode.

0	No operation
1	Stop mode

This bit is cleared at reset or stop cancellation.

0 is always read when this bit is read.

[Bit 6] SLP: Sleep bit

This bit is used to specify switching the CPU and resources to the sleep mode.

0	No operation
1	Sleep mode

This bit is cleared at reset, sleep or stop cancellation.

0 is always read when this bit is read.

[Bit 5] SPL: Pin state specifying bit

This bit is used to specify the external pin state in the stop mode.

0	Holds state and level immediately before stop mode
1	High impedance

This bit is cleared at resetting.

[Bit 4] RST: Software reset bit

This bit is used to specify the software reset.

0	Generates 4-cycle reset signal
1	No operation

1 is always read when this bit is read.

If a software reset is performed during operation in a submode, an oscillation stabilization period is required to switch to the main mode. Therefore, a reset signal is output during the oscillation stabilization period.

MAIN/SUBCLOCK CONTROL BLOCK

[Bit 3] TMD: Watch bit

This bit is used to specify switching to the watch mode.

0	No operation
1	Watch mode

Writing at this bit is possible only in the submode (SCS = 0). 0 is always read when this bit is read. This bit is cleared at an interrupt request or reset.

This STBC register is also used to set low power consumption mode.

Address:

SYCC

0007_H

Address:

STBC

0008_H

(2) System clock control register (SYCC)

This register controls the clock for operating the CPU and resources.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0007 _H	SCM	—	—	WT1	WT0	SCS	CS1	CS0
	(R)			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
								Initial value X--MM100 _B

[Bit 7] SCM: System clock monitor bit

This bit is used to check whether the current system clock is the main clock or subclock.

0	Subclock (Main clock is stopping or oscillation of main clock stabilizing)
1	Main clock

[Bits 4 and Bit 3] WT1 and WT0: Oscillation stabilization time select bits

These bit are used to select the oscillation stabilization wait time of the main clock.

WT1	WT0	Oscillation stabilization time	Value at f _{CH} = 3 MHz
1	1	Approximate 2 ¹⁸ /f _{CH}	Approximate 87.4 ms
1	0	Approximate 2 ¹⁶ /f _{CH}	Approximate 21.8 ms
0	1	Approximate 2 ¹² /f _{CH}	Approximate 1.4 ms
0	0	Approximate 2 ⁴ /f _{CH}	Approximate 0 ms

f_{CH}: Oscillation frequency of main clock

If the main mode is specified by the system clock select bit (SCS), the mode switches to main mode after the selected wait time has elapsed.

The initial value of this bit is determined by the mask option. Do not rewrite this bit during the oscillation stabilization period nor rewrite it concurrently with switching from low speed to high speed.

MAIN/SUBCLOCK CONTROL BLOCK
--

The oscillation stabilization time of the main clock is generated by dividing down the frequency of the main clock. Since the oscillation frequency is unstable immediately after oscillation starts, use the above table.

[Bit 2] SCS: System clock select bit

This bit is used to select the system clock mode.

0	Selects subclock (32.768 kHz) mode
1	Selects main clock mode

[Bits 1 and 0] CS1 and CS0: System clock select bits

If the main mode is specified by the system clock select bit (SCS), the system clock is as given in the table below.

CS1	CS0	Instruction cycle	Instruction execution time at $f_{CH} = 3 \text{ MHz}$
0	0	$64/f_{CH}$	21.3 μs
0	1	$16/f_{CH}$	5.33 μs
1	0	$8/f_{CH}$	2.67 μs
1	1	$4/f_{CH}$	1.33 μs

f_{CH} : frequency of main clock

MAIN/SUBCLOCK CONTROL BLOCK

■ Description of Operation

Main/sub clock block has normal and low-power consumption mode. The low-power consumption mode are described below.

(1) Low-power consumption mode

This chip has three operation modes. The sleep mode, and stop mode in the table below reduce the power consumption. In the main mode, four system clocks can be selected according to the system condition to minimize power consumption.

Table 2-2 Operating State of Low-power Consumption Modes

Clock mode of CPU	(CS1, CS0)	State mode	Clock pulse		Each operating clock pulse (3 MHz main clock)				Wake-up source in each mode
			Main	Sub	CPU	Time-base timer	Each resource	Clock	
Main mode	(1, 1)	RUN	Oscillates	Oscillates	1.5 MHz	1.5 MHz	1.5 MHz	32.768 kHz	Various interrupt requests
		SLEEP							External interrupt
		STOP	Stops		Stops	Stops	Stops		
	(1, 0)	RUN	Oscillates	Oscillates	750 kHz	1.5 MHz	750 kHz	32.768 kHz	Various interrupt requests
		SLEEP							External interrupt
		STOP	Stops		Stops	Stops	Stops		
	(0, 1)	RUN	Oscillates	Oscillates	375 kHz	1.5 MHz	375 kHz	32.768 kHz	Various interrupt requests
		SLEEP							External interrupt
		STOP	Stops		Stops	Stops	Stops		
	(0, 0)	RUN	Oscillates	Oscillates	98.4 kHz	1.5 MHz	98.4 kHz	32.768 kHz	Various interrupt requests
		SLEEP							External interrupt
		STOP	Stops		Stops	Stops	Stops		
Submode	—	RUN		Oscillates	32.768 kHz		32.768 kHz	32.768 kHz	Various interrupt requests
		SLEEP	Stops			Stops			External interrupt
		STOP		Stops	Stops	Stops	Stops		
Watch mode			Stops	Oscillates	Stops	Stops	32.768 kHz	Watch external interrupt	

- The submode stops oscillation of the main clock.
- The SLEEP mode stops only the operating clock pulse of the CPU; other operations are continued.
- The WATCH mode stops the functions of all chips other than the special resources.
- The STOP state stops the oscillation. Data can be held with the lowest power consumption in this mode.

**MAIN/SUBCLOCK
CONTROL BLOCK**

(a) WATCH mode

- Switching to WATCH mode
 - Writing 1 at the TMD bit of the STBC register switches the mode to WATCH mode. Writing is invalid if 1 is set at the SCS bit (bit 2) of the SYCC register.
 - The WATCH mode stops all chip functions except the watch prescaler, external interrupt, and wake-up functions. Therefore, data can be held with the lowest power consumption.
 - The input/output pins and output pins during the WATCH mode can be controlled by the SPL bit of the STBC register so that they are held in the state immediately before entering the WATCH mode or so that they enter the high-impedance state.
 - If an interrupt is requested when 1 is written at the TMD bit, instruction execution continues without switching to the WATCH mode.
 - In the WATCH mode, the values of registers and RAM immediately before entering the WATCH mode are held.
- Canceling WATCH mode
 - The WATCH mode is canceled by inputting the reset signal and requesting an interrupt.
 - When the reset signal is input during the WATCH mode, the CPU is switched to the reset state and the WATCH mode is canceled.
 - When an interrupt higher than level 11 is requested from a resource during the WATCH mode, the WATCH mode is canceled.
 - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the WATCH mode.
 - If the WATCH mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Therefore, the reset sequence is not executed unless the oscillation stabilization time is elapsed. The oscillation stabilization time will be that of the main clock selected by the WT1 and WT0 bits. However, when Power-on Reset is not specified by the mask option, the CPU is not switched to the oscillation stabilization wait state, even if the WATCH mode is canceled by inputting the reset signal.

(b) SLEEP state

- Switching to Sleep State
 - Writing 1 at the SLP bit (bit 6) of the STBC register switches the mode to SLEEP state.
 - The SLEEP state is the mode to stop clock pulse operating the CPU; only the CPU stops and the resources continue to operate.
 - If an interrupt is requested when 1 is written at the SLP bit (bit 6), instruction execution continues without switching to the SLEEP state.
 - In the SLEEP state, the values of registers and RAM immediately before entering the SLEEP state are held.

MAIN/SUBCLOCK CONTROL BLOCK
--

- Canceling SLEEP state
 - The SLEEP state is canceled by inputting the reset signal and requesting an interrupt.
 - When the reset signal is input during the SLEEP state, the CPU is switched to the reset state and the SLEEP state is canceled.
 - When an interrupt level higher than 11 is requested from a resource during the SLEEP state, the SLEEP state is canceled.
 - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the SLEEP state.

(c) STOP state

- Switching to STOP state
 - Writing 1 at the STP bit (bit 7) of the STBC register switches the mode to STOP state.
 - The STOP state varies when the main clock is operating and when the subclock is operating.
 - When the main clock is operating: The main clock stops but the subclock does not stop. All chip functions except the watch function stop. However, no watch interrupt can be accepted.
 - When subclock is operating: Both the main clock and subclock stop. All chip functions stop.
 - The input/output pins and output pins during the STOP state can be controlled by the SPL bit (bit 5) of the STBC register so that they are held in the state immediately before entering the STOP state, or so that they enter in the high-impedance state.
 - If an interrupt is requested when 1 is written at the STP bit (bit 7), instruction execution continues without switching to the STOP state.
 - In the STOP state, the values of registers and RAM immediately before entering the STOP state are held.
- Canceling STOP state
 - The STOP mode is canceled either by inputting the reset signal or by requesting an interrupt.
 - When the reset signal is input during the STOP state, the CPU is switched to the reset state and the STOP state is canceled.
 - When an interrupt higher than level 11 is requested from the external interrupt circuit during the STOP state, the STOP state is canceled.
 - When the I flag and IL bit are enabled like an ordinary interrupt after canceling, the CPU executes the interrupt processing. When they are disabled, the CPU executes the interrupt processing from the instruction next to the one before entering the STOP state.
 - Four oscillation stabilization times of the main clock can be selected by the WT1 and WT0 bits. The oscillation stabilization time of the subclock is fixed (at $2^{15}/f_{CL}$ — f_{CL} : frequency of subclock).

MAIN/SUBCLOCK CONTROL BLOCK
--

- If the STOP state is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Therefore, the reset sequence is not executed unless the oscillation stabilization time is elapsed. The oscillation stabilization time corresponds to the oscillation stabilization time of the main clock selected by the WT1 and WT0 bits. However, when Power-on Reset is not specified by the mask option, the CPU is not switched to the oscillation stabilization wait state even if the STOP state is canceled by inputting the reset signal.

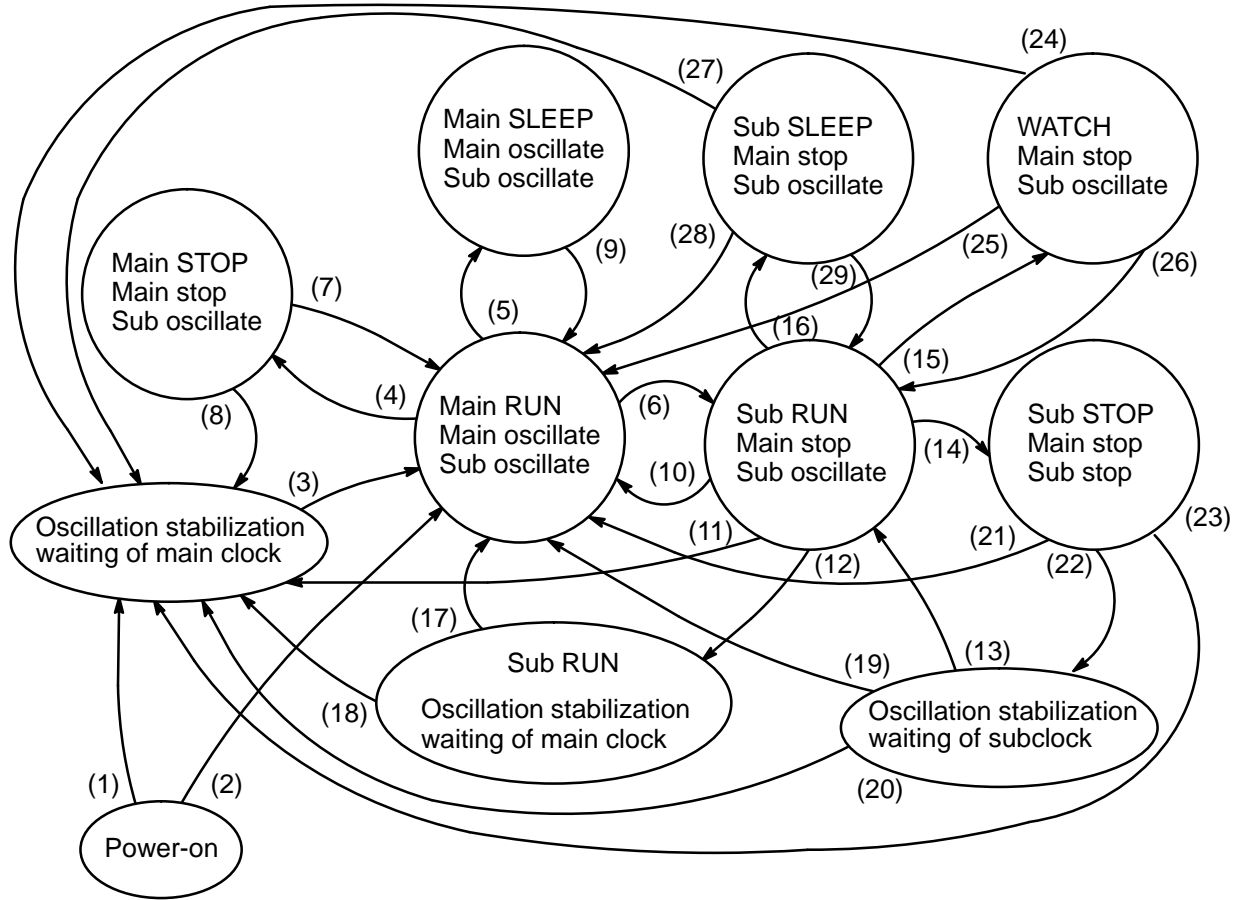
(2) Setting low power consumption mode

STBC Register			Mode
STP (Bit 7)	SLP (Bit 6)	TMD (Bit 3)	
0	0	0	Normal
0	0	1	WATCH
0	1	0	SLEEP
1	0	0	STOP
1	×	×	Disable

Note: When the mode is switched from the subclock mode to the main clock mode, do not set the stop, sleep, and watch states. If the SCS bit of the SYCC register is rewritten from 0 to 1, set the above states after the SCM bit of the SYCC register has been set to 1.

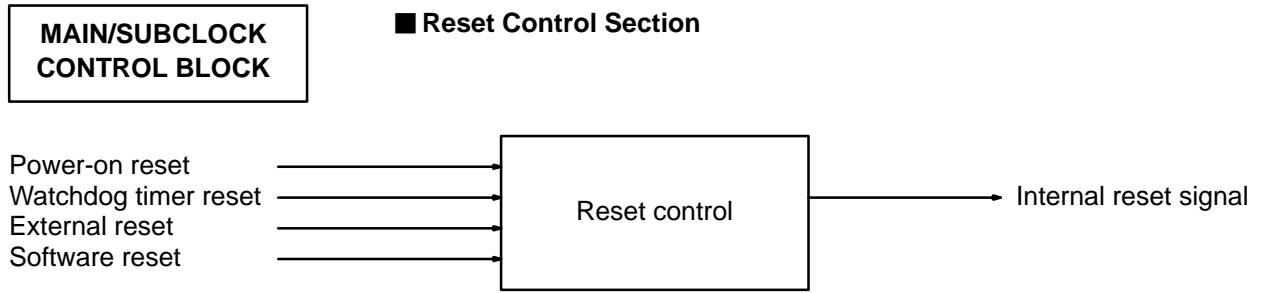
MAIN/SUBCLOCK CONTROL BLOCK

(3) State transition diagram at low power consumption mode



- (1) When power-on reset option is selected
- (2) When power-on reset option is not selected
- (3) After oscillation stabilized
- (4) Set STP bit to 1.
- (5) Set SLP bit to 1.
- (6) Set SCS bit to 0.
- (7) External reset when power-on reset option not selected
- (8) External reset or interrupt when power-on reset option selected
- (9) External reset or interrupt
- (10) External reset when power-on reset option not selected
- (11) External reset or other reset when power-on reset option selected
- (12) Set SCS bit to 1.
- (13) After oscillation stabilized
- (14) Set STP bit to 1.
- (15) Set TMD bit to 1.
- (16) Set SLP bit to 1.
- (17) External reset after oscillation stabilized or when power-on reset option not selected
- (18) External reset or other reset when power-on reset option selected

- (19) External reset after oscillation is stabilized or when power-on reset option not selected
- (20) External reset when power-on reset option selected
- (21) External reset when power-on reset option not selected
- (22) Interrupt
- (23) External reset when power-on reset option selected
- (24) External reset when power-on reset option selected
- (25) External reset when power-on reset option not selected
- (26) Interrupt
- (27) External reset when power-on reset option selected
- (28) External reset when power-on reset option not selected
- (29) Interrupt



- Reset

There are four types of resets as shown in Table 2-3.

Table 2-3 Sources of Reset

Reset name	Description
Power-on reset	Turns power on
Watchdog reset	Overflows watchdog timer
External-pin reset	Sets external-reset pin to Low
Software reset	Writes 0 at RST (bit 4) of STBC

When the power-on reset and reset during the stop state are used, the oscillation stabilization time is needed after the oscillator operates. The time-base timer or watch prescaler controls this stabilization time. Consequently, the operation does not start immediately even after canceling the reset.

However, if Power-on Reset Disabled is selected by the mask option, no oscillation stabilization time is required in any state after external pins have been released from the reset.

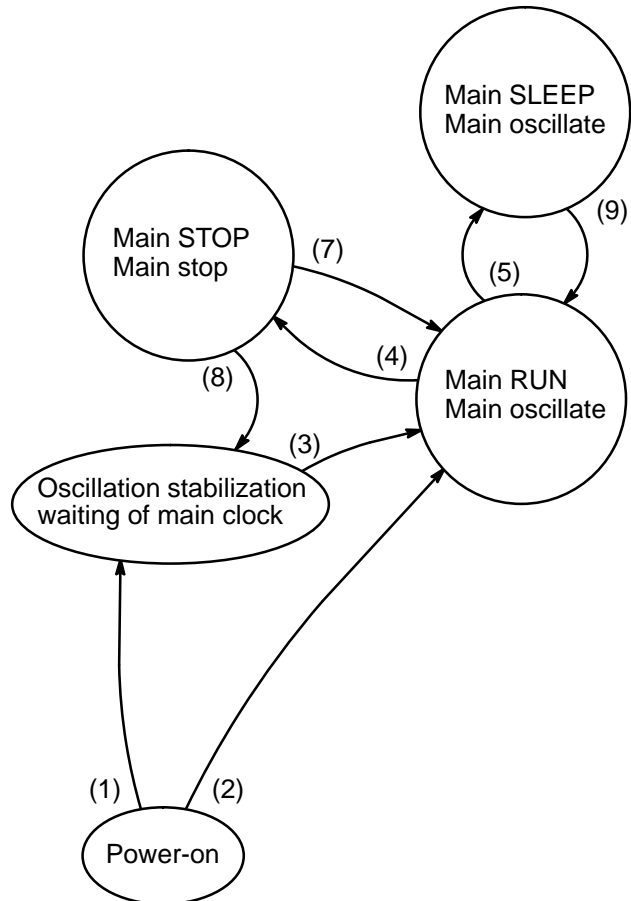
Note: If Power-on Reset Disabled is selected, the RST pin must be kept Low until the oscillation stabilization time selected by the option has elapsed after power on.

**MAIN/SUBCLOCK
CONTROL BLOCK**

■ **Single Clock**

The single clock can be selected by the mask option. In the single clock operation, the functions are the same as those of the double clock module except that the subclock mode cannot be set. Therefore, the input pin X0A of the subclock should be connected to GND. The X1A pin must be kept open.

- State transition diagram



- (1) When power-on reset option selected
- (2) When power-on reset option not selected
- (3) After oscillation stabilized
- (4) Set STP bit to 1.
- (5) Set SLP bit to 1.
- (6) External reset
- (7) External reset when power-on reset option not selected
- (8) External reset or interrupt when power-on reset option selected
- (9) External reset or interrupt

INTERRUPT CONTROLLER

2.3 INTERRUPT CONTROLLER

● The interrupt controller for the F²MC-8L family is located between the F²MC-8L CPU and each resource. This controller receives interrupt requests from the resources, assigns priority to them, and transfers the priority to the CPU; it also decides the priority of same-level interrupts.

■ **Block Diagram**

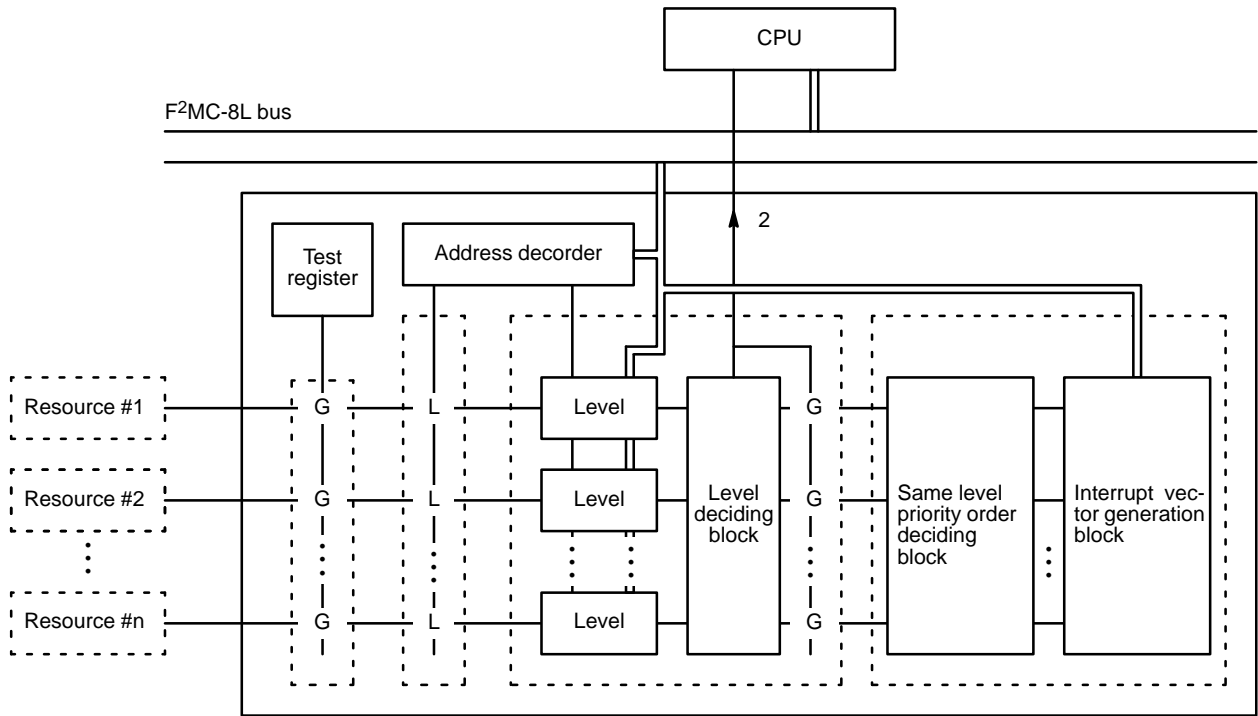


Fig. 2.9 Interrupt Controller Block Diagram

■ **Register List**

Interrupt controller consists of interrupt-level registers (ILR1, 2, and 3) and interrupt-test register (ITR).

	← 8 bit →	
Address: 007C _H	ILR1	W Interrupt level register #1
Address: 007D _H	ILR2	W Interrupt level register #2
Address: 007E _H	ILR3	W Interrupt level register #3
Address: 007F _H	ITR	— Interrupt test register

INTERRUPT CONTROLLER

- Address: 007C_H ILR1
- Address: 007D_H ILR2
- Address: 007E_H ILR3
- Address: 007F_H ITR

■ Description of Registers

The detail of each register is described below.

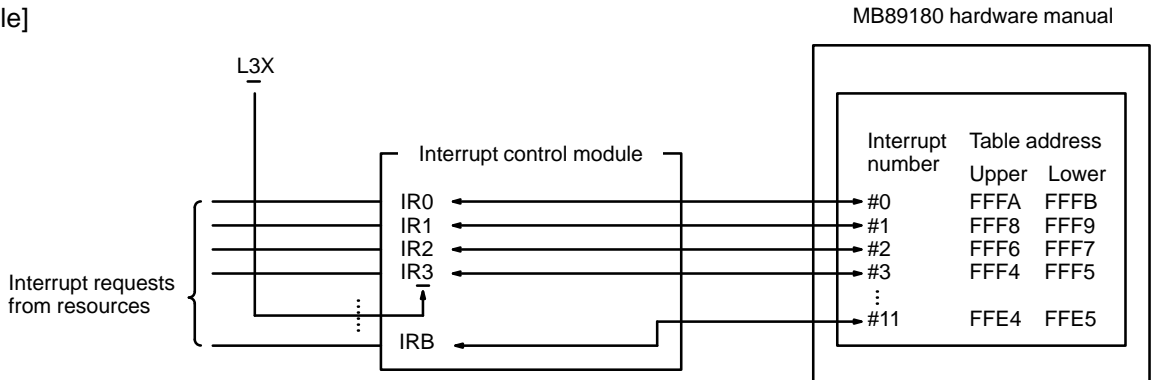
(1) Interrupt level register (ILRX: Interrupt Level Register X)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 007C _H	L31	L30	L21	L20	L11	L10	L01	L00
Address: 007D _H	L71	L70	L61	L60	L51	L50	L41	L40
Address: 007E _H	LB1	LB0	LA1	LA0	L91	L90	L81	L80
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

Initial value
11111111_B

The ILRX sets the interrupt level of each resource. The digits in the center of each bit correspond to the interrupt numbers.

[Example]



When an interrupt is requested from a resource, the interrupt controller transfers the interrupt level based on the value set at the 2-bits of the ILRX corresponding to the interrupt to the CPU. The relationship between the 2 bits of the ILRX and the required interrupt levels is as follows:

Lx1	Lx0	Required interrupt level
0	×	1
1	0	2
1	1	3 (None)

- Address: 007C_H ILR1
- Address: 007D_H ILR2
- Address: 007E_H ILR3
- Address: 007F_H ITR

(2) Interrupt test register (ITR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 007F _H	—	—	—	—	—	—	EV	EN
							(—)	(—)

Initial value
-----00_B

The ITR is used for testing. Do not access it.

INTERRUPT CONTROLLER

■ Description of Operation

The functions of interrupt controllers are described below.

(1) Interrupt functions

The MB89180 series of microcontrollers have 12 inputs for interrupt requests from each resource. The interrupt level is set by 2-bit registers corresponding to each input. When an interrupt is requested from a resource, the interrupt controller receives it and transfers the contents of the corresponding level register to the CPU. The interrupt to the device is processed as follows:

- (a) An interrupt source is generated inside each resource.
- (b) If an interrupt is enabled, an interrupt request is output from each resource to the interrupt controller by referring to the interrupt-enable bit inside each resource.
- (c) After receiving this interrupt request, the interrupt controller determines the priority of simultaneously-requested interrupts and then transfers the interrupt level for the applicable interrupt to the CPU.
- (d) The CPU compares the interrupt level requested from the interrupt controller with the IL bit in the processor status register.
- (e) As a result of the comparison, if the priority of the interrupt level is higher than that of the current interrupt processing level, the contents of the I-flag in the same processor status register are checked.
- (f) As a result of the check in step (e), if the I-flag is enabled for an interrupt, the contents of the IL bit are set to the required level.
- (g) When an interrupt source is cleared by software in the user's interrupt processing routine, the CPU terminates the interrupt processing.

Figure 2.8 outlines the interrupt operation for the MB89180 series of microcontrollers.

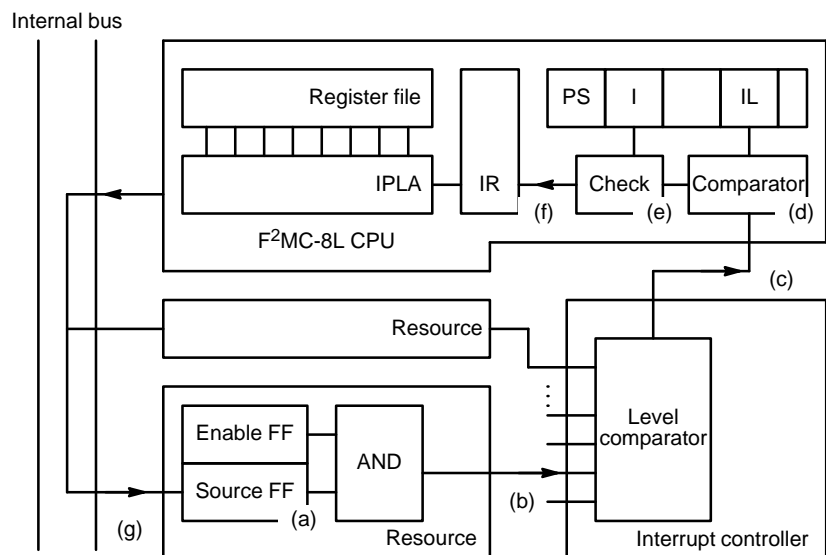


Fig. 2.10 Interrupt-processing Flowchart

I/O PORTS

2.4 I/O PORTS

- The MB89180 series of microcontrollers have six parallel ports (43 pins). P00 to P07, P10 to P17, and P20 to P27 serve as 8-bit I/O ports; P40 to P47 and P50 to P57 serve as 8-bit output-only ports; P30 to P32 serves as a 3-bit output-only port.
- Each ports are also used as the I/O pin for the resource.

■ List of port functions

Table 2-4 List of Port Functions

Pin name	Input type	Output type	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P00 to P07	CMOS	CMOS push-pull	Parallel port 00 to 07	P07	P06	P05	P04	P03	P02	P01	P00
	Hysteresis		Resource	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20
P10 to P17	CMOS	CMOS push-pull	Parallel port 10 to 17	P17	P16	P15	P14	P13	P12	P11	P10
	Hysteresis		Resource 1					INT13	INT12	INT11	INT10
			Resource 2	SEG31	SEG30	SEG29	SEG28	SEG27	SEG26	SEG25	SEG24
P20 to P27	CMOS	N-ch open drain	Parallel port 20 to 27	P27	P26	P25	P24	P23	P22	P21	P20
	Hysteresis		Resource	BUZ		SCK	SO	SI	TO		EC
P30 to 32	—	CMOS push-pull	Parallel port 30 to 32						P32	P31	P30
			Resource					COM3	COM2	RCO	
P40 to 47	—	N-ch open drain	Parallel port 40 to 47	P47	P46	P45	P44	P43	P42	P41	P40
			Resource	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8
P50 to 57	—	N-ch open drain	Parallel port 50 to 57	P57	P56	P55	P54	P53	P52	P51	P50
			Resource	SEG23	SEG22	SEG21	SEG20	SEG19	SEG18	SEG17	SEG16

Notes:

1. P10 to P17, P40 to 47 and P50 to 57 serve as output ports only when they are selected by the mask option for use as ports.
2. INT10 to INT13 of P10 to P13 serves as resource inputs when they are selected by the mask option for use as resource inputs.

I/O PORTS

Register list

I/O port consists of the following registers.

Address	Register Name	Access	Description	Initial value
Address: 0000 _H	PDR0	R/W	Port 00 to 07 data register	Initial value = XXXXXXXX _B
Address: 0001 _H	DDR0	W	Port 00 to 07 data direction register	Initial value = 00000000 _B
Address: 0002 _H	PDR1	R/W	Port 10 to 17 data register	Initial value = XXXXXXXX _B
Address: 0003 _H	DDR1	W	Port 10 to 17 data direction register	Initial value = 00000000 _B
Address: 0004 _H	PDR2	R/W	Port 20 to 27 data register	Initial value = XXXXXXXX _B
Address: 0005 _H	DDR2	W	Port 20 to 27 data direction register	Initial value = 00000000 _B
Address: 000C _H	PDR3	R/W	Port 30 to 37 data register	Initial value = XXXXX111 _B
Address: 000E _H	PDR4	R/W	Port 40 to 47 data register	Initial value = 11111111 _B
Address: 000F _H	PDR5	R/W	Port 50 to 57 data register	Initial value = 11111111 _B

Description of functions

The function of each port is described below.

- (1) P00 to P07: CMOS-type I/O ports
 P10 to P17: CMOS-type I/O ports
 (also used as segment output pins)

- Switching input and output
 These ports have a data-direction register (DDR) and port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input.
- Operation for output port (DDR = 1)
 The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.
- Operation for input port (DDR = 0)
 When settings the input, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

I/O PORTS

- Segment output operation
When selected as segment pins by the mask option, P10 to P17 output segments. In this case, these pins cannot be used as ports and interrupt pins. When they are used as segment pins, the pull-up option cannot be selected as well.
- State when reset
The DDR is initialized to 0 by resetting and the output impedance goes High at all bits. The PDR is not initialized by resetting. Therefore, set the value of the PDR before setting the DDR to output.
- State in watch and stop modes
With the SPL bit of the standby-control register set to 1, in the watch or stop mode, the output impedance goes High irrespective of the value of the DDR.

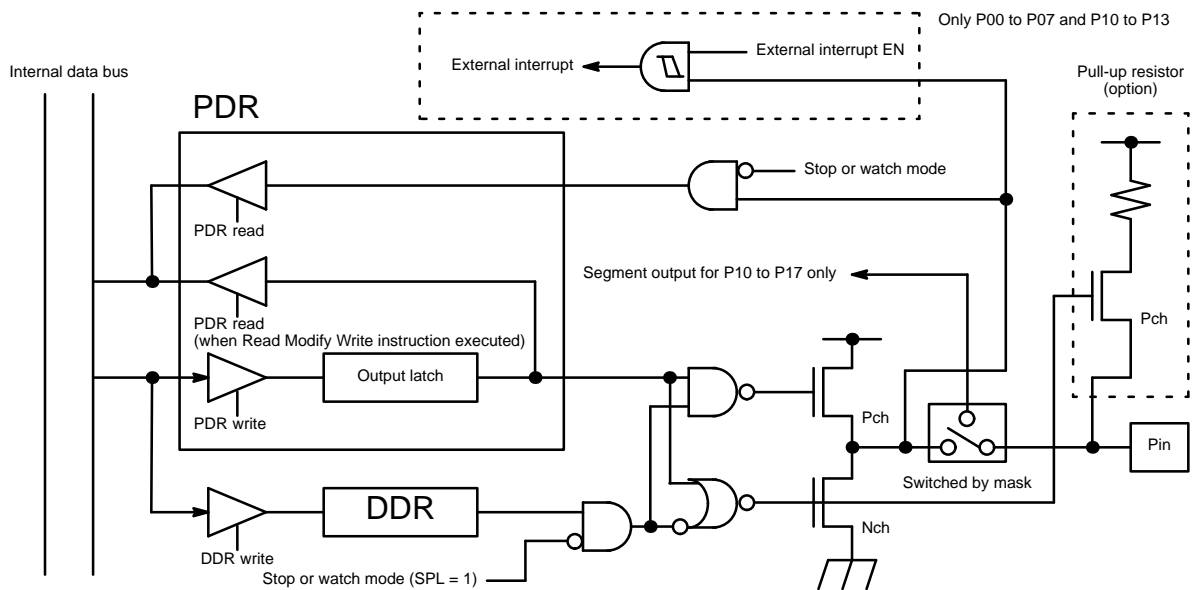


Fig. 2.11 Ports 00 to 07 and 10 to 17

(2) P20 to P27: N-ch open-drain type I/O port
(also used as resource input and output)

- Switching input and output
This port has a data-direction register (DDR) and a port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input.
- Operation for output port (DDR = 1)
The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

I/O PORTS

- Resource output operation (DDR=1)
When using as the resource output, setting is performed by the resource output enable bit. (See the description of each resource.) Even when the output from each resource is enabled, the read value of the port is valid except when the Read Modify Write instruction is read, so the pin state can be checked.
- Operation for input port (DDR = 0)
When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read. Since the PRD is not initialized by reset, set the value before setting DDR to output.
- State when reset
When reset, the DDR is initialized to 0 and the output impedance goes High at all bits. When reset, the PDR is not initialized. Therefore, set the value of the PDR before setting the DDR to output.
- State in watch and stop modes
With the SPL bit of the standby-control register set to 1, in the watch or stop mode, the output impedance goes High irrespective of the value of the DDR.

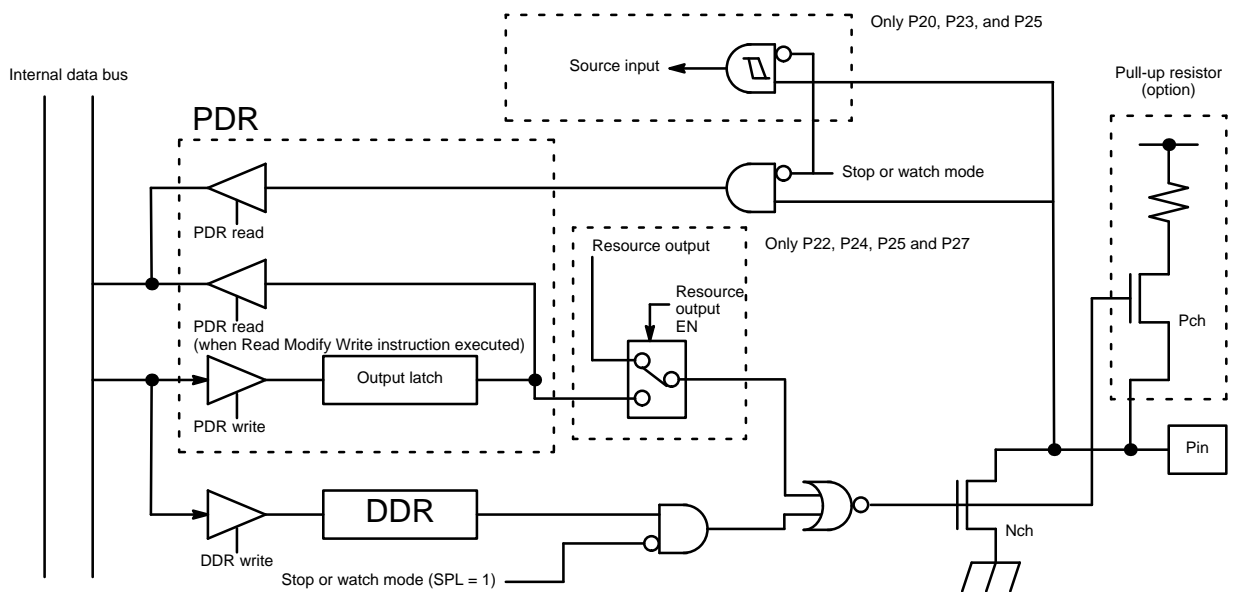


Fig. 2.12 Ports 20 to 27

I/O PORTS

(3) P30/RCO: COMS-type output-only ports
(also used as resource output)

- Operation for output port
The value written at the PDR is output to the pin. When the PDR is read at this port, the data of the output latch can always be read instead of the pin state.
- Operation for resource output
When using as the resource output, setting is performed by the resource output enable bit. (See the description of each resource.) Even if the output from each resource is enabled, the read value of the port is effective except when the Read Modify Write instruction is read, so the pin state can be checked.
- State when reset
At reset, the PDR is initialized to 1 and the output transistors of all bits are turned off.
- State in stop mode
With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR.

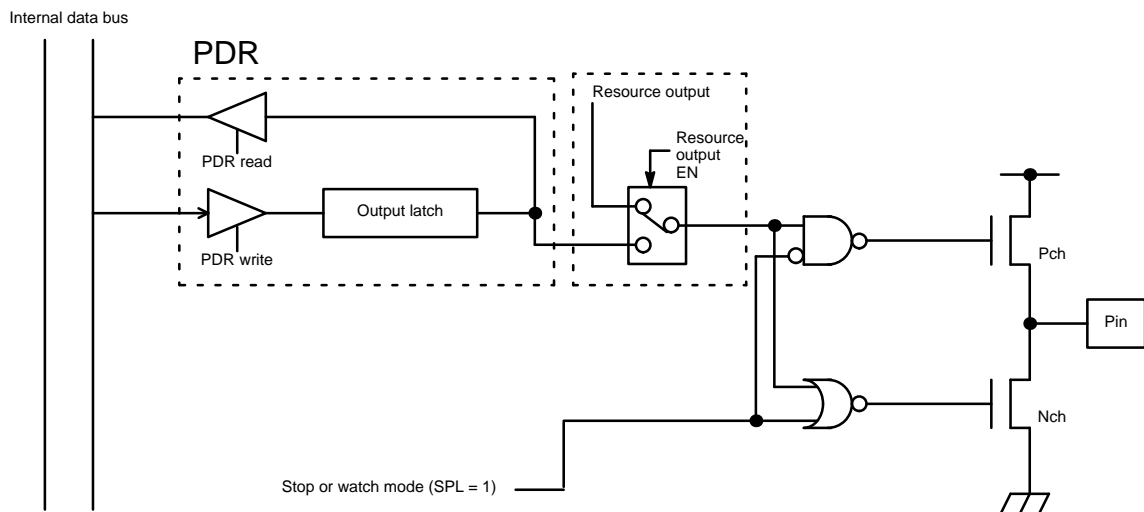


Fig. 2.13 Port 30

(4) P40 to P47: N-ch open-drain type output-only ports
(also used as segment output)
P50 to P57: N-ch open-drain type output-only ports
(also used as segment output)

- Operation for output port
The value written at the PDR is output to the pin. When the PDR is read in this port, usually, the contents of the output latch is read instead of the value of the pin.

I/O PORTS

- **Segment output**
When selected by the mask option for use as segment pins, P40 to P47 and P50 to P57 serve as segment outputs, In this case, they cannot be used as output ports. When selected for use as segment pins, they cannot be selected for the pull-up option.
- **State when reset**
The PDR is initialized to 1 at reset, so the output register is turned off at all bits.
- **State in stop mode**
When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

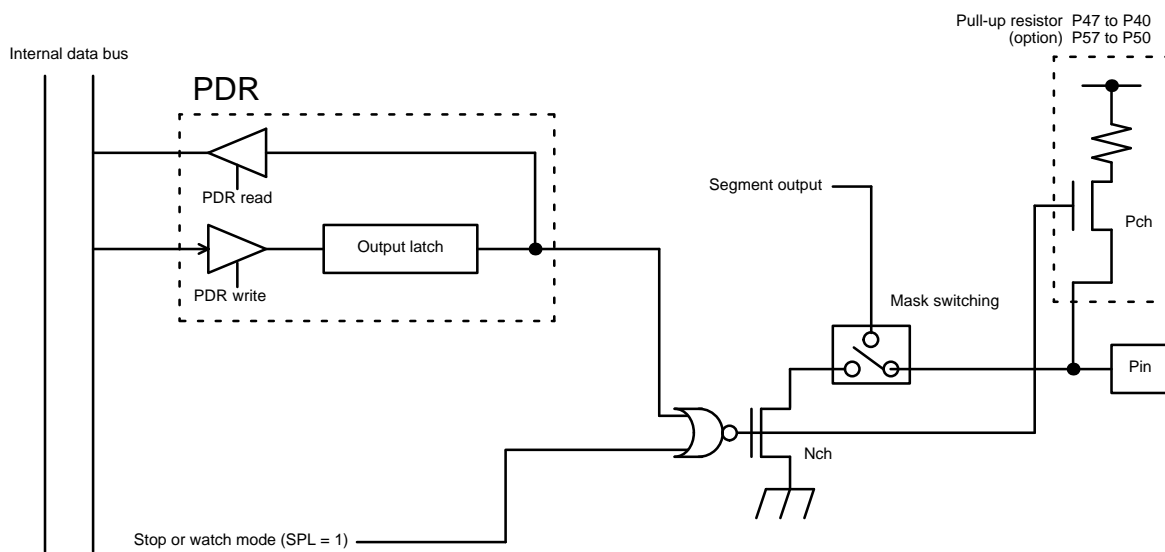


Fig. 2.14 Ports 40 to 47 and 50 to 57

(5) P31 /P32: N-ch open-drain type output-only ports (also used as common output)

- **Operation for output port**
The value written at the PDR is output to the pin. When the PDR is read in this port, usually, the contents of the output latch is read instead of the value of the pin.
- **Switching port and common output**
When not used as a common output, P31 and P32 can be used as ports. They are switched as follows:
 - When using P31 as a port, select a duty other than 1/4 by setting the display mode selection bit of the LCDC control register (072H).
 - When using P32 as a port, select a duty other than 1/3 and 1/4 by setting the display mode selection bit of the LCDC control register (072H).

I/O PORTS

- Common output operation
When using P31 and P32 as common outputs, set the value of each PRD to 1.
- State when reset
The PDR is initialized to 1 at reset, so the output register is turned off at all bits.
- State in stop mode
When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

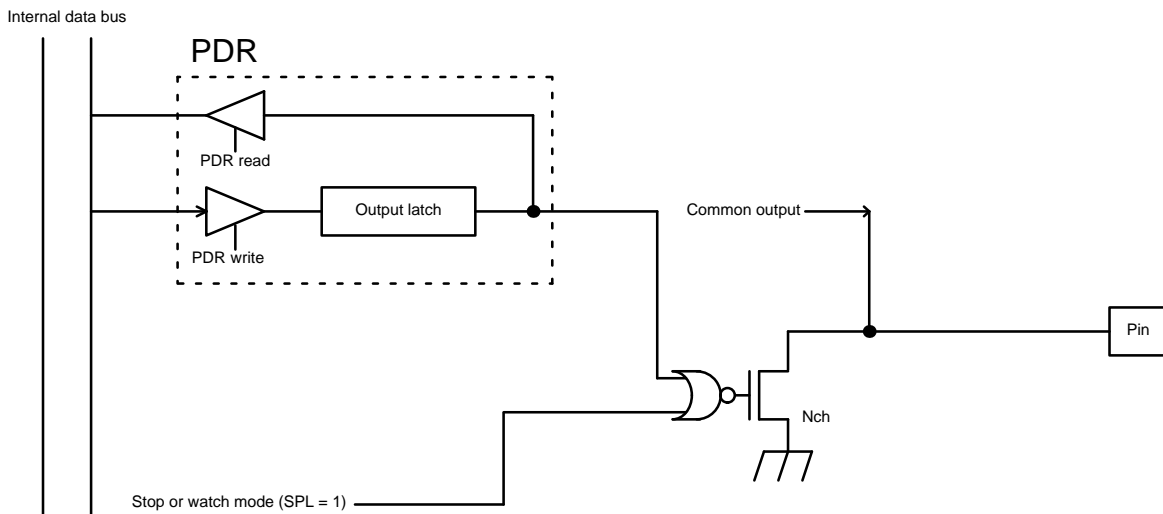


Fig. 2.15 Ports 31 and 32

**8/16-BIT TIMER
(TIMER 1 AND TIMER 2)**

2.5 8/16-BIT TIMER (Timer 1 and Timer 2)

- Three internal clock pulses and one external clock pulse can be selected.
- Operation in 8-bit 2-ch mode or 16-bit 1-ch mode can be selected.
- A square-wave output function is included.

■ Block Diagram

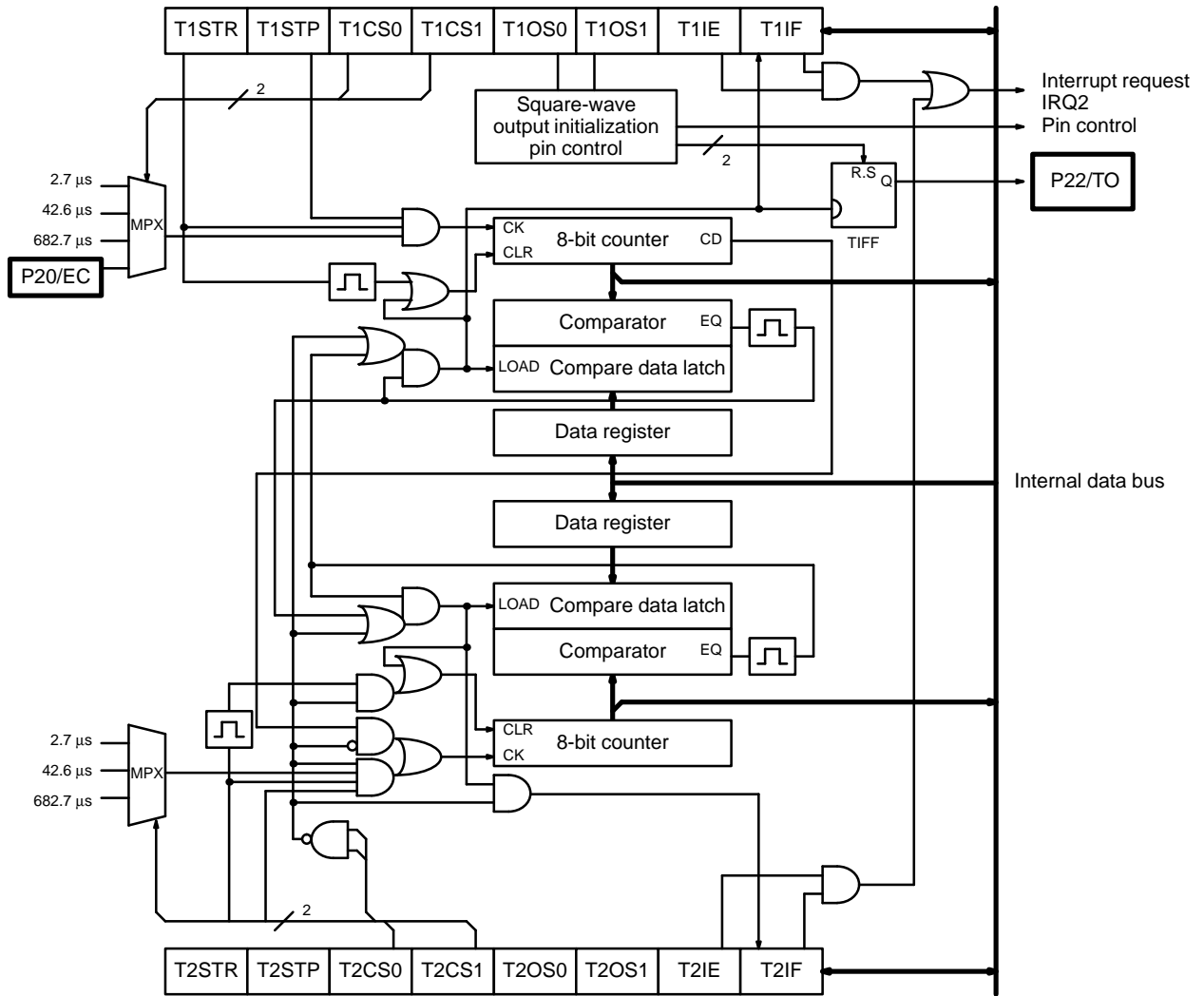
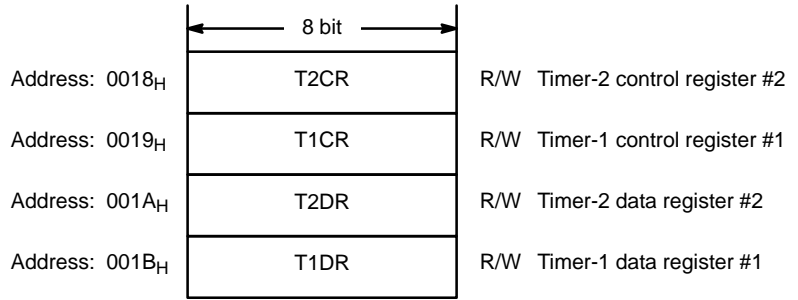


Fig. 2.16 8/16-bit Timer Block Diagram

n Register List



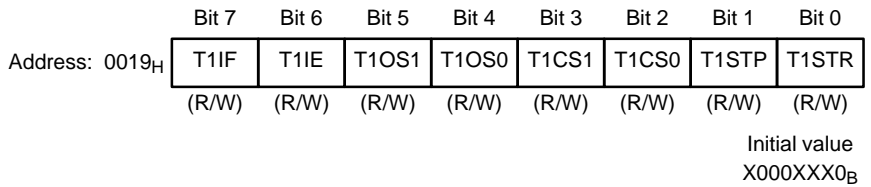
**8/16-BIT TIMER
(TIMER 1 AND TIMER 2)**

- Address: 0019_H T1CR
- Address: 0018_H T2CR
- Address: 001B_H T1DR
- Address: 001A_H T2DR

■ Description of Register Details

The detail of each register is described below.

(1) Timer 1 control register (T1CR)



[Bit 7] T1IF: Interrupt request flag
(When write)

0	Interrupt request flag clearing
1	No operation

(When read)

0	No interrupt request
1	Interval interrupt request

1 is always read when the Read Modify Write instruction is executed.

[Bit 6] T1IE: Interrupt enable bit

0	Interrupt disabled
1	Interrupt enabled

[Bit 5 and 4] T1OS1 and T1OS0: Square-wave output control bit

These bits are used to control the square-wave output when the timer stops
(See page 2-36 for the setting.)

T1OS1	T1OS0	
0	0	Makes output port [P22(TO)] general-purpose port
0	1	Holds data setting square-wave output to Low level
1	0	Holds data setting square-wave output to High level
1	1	Sets square-wave output to held value

When the T1STR bit is 0, the square-wave output is set to the set value.

[Bit 3 and 2] T1CS1 and T1CS0: Clock source select bit

T1CS1	T1CS0	Clock cycle time (When 1/2 of 3 MHz is selected)	
0	0	Internal clock	2 instruction cycle
0	1		32 instruction cycle
1	0		512 instruction cycle
1	1	External colck	—

**8/16-BIT TIMER
(TIMER 1 AND TIMER 2)**

[Bit 1] T1STP: Timer stop bit

0	Counting continued without clearing counter
1	Counting suspended

[Bit 0] T1STR: Timer start bit

0	Terminates operation
1	Clears counter and starts operation

Note: When using the timer 1 in the 8-bit 1-ch mode, set its bit-3 and bit-2 of the timer-2 control register to a value other than 11. Use of the timer without setting this register causes a malfunction.

Address: 0019_H T1CR

Address: 0018_H T2CR

Address: 001B_H T1DR

Address: 001A_H T2DR

(2) Timer 2 control register (T2CR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0018 _H	T2IF	T2IE	T2OS1	T2OS0	T2CS1	T2CS0	T2STP	T2STR
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value
X000XXX0_B

[Bit 7] T2IF: Interrupt request flag
(When write)

0	Interrupt request flag clearing
1	No operation

(When read)

0	No interrupt request
1	Interval interrupt request

1 is always read when the Read Modify Write instruction is executed.

[Bit 6] T2IE: Interrupt enable bit

0	Interrupt disabled
1	Interrupt enabled

[Bit 5 and 4] T2OS1 and T2OS0: Vacant bit

These are vacant bits, Always write 00.

[Bit 3 and 2] T2CS1 and T2CS0: Clock source select bit

These bits are used to select timer clock source.

T2CS1	T2CS0	Clock cycle time (When 1/2 of 3 MHz is selected)		
0	0	Internal clock	2 instruction cycle	2.7 μ s
0	1		32 instruction cycle	42.6 μ s
1	0		512 instruction cycle	682.7 μ s
1	1	16-bit mode	—	—

**8/16-BIT TIMER
(TIMER 1 AND TIMER 2)**

[Bit 1] T2STP: Timer stop bit

0	Operation continued without clearing counter
1	Count operation suspended

[Bit 0] T2STR: Timer start bit

0	Operation stopped
1	Operation started after clearing counter

Address: 0019_H T1CR

Address: 0018_H T2CR

Address: 001B_H T1DR

Address: 001A_H T2DR

(3) Timer 1 and 2 data registers (T1DR and T2DR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 001B _H								
Address: 001A _H								
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
	Initial value XXXXXXXX _B							

Write data is the set interval times and read data is the counted times.

**8/16-BIT TIMER
(TIMER 1 AND TIMER 2)**

■ **Description of Operation**

(1) 8-bit internal clock mode

In the 8-bit internal clock mode, three internal clock inputs can be selected by setting the clock source select bits (T1CS1 and T1CS0, T2CS1 and T2CS0) of the timer control registers (T1CR and T2CR). The timer data registers (T1DR and T2DR) serve as interval time setting registers.

To start the timer, set the interval time as the timer data registers, write 1 at the timer start bits (T1STR and T2STR) of the timer control registers to clear the counter to 00_H, and load the values of the timer data registers into the compare latch. Then, counting starts.

When the values of the counter agree with those of the timer data registers, the interval interrupt request flags (T1IF and T2IF) are set to 1. At this time, the counter is cleared to 00_H, the values of the timer data registers are re-loaded into the compare latch, and counting is continued. If the interrupt enable bits (T1IE and T2IE) are set to 1, an interrupt request is output to the CPU. Assuming the set value of the timer data register is n and the selected clock is ϕ , the interval time (T) can be calculated as follows.

$$T = \phi \times (n + 1) [\mu\text{s}]$$

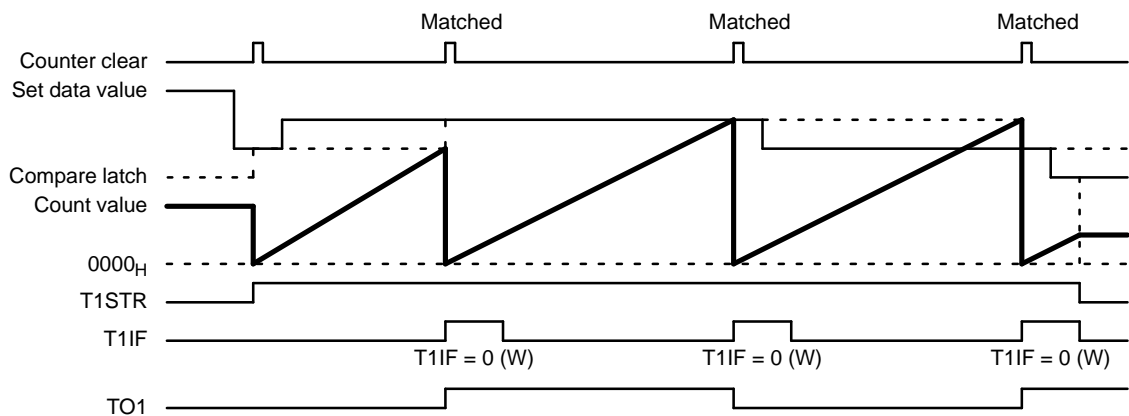


Fig. 2.17 Description Diagram for Internal Clock Mode Operation

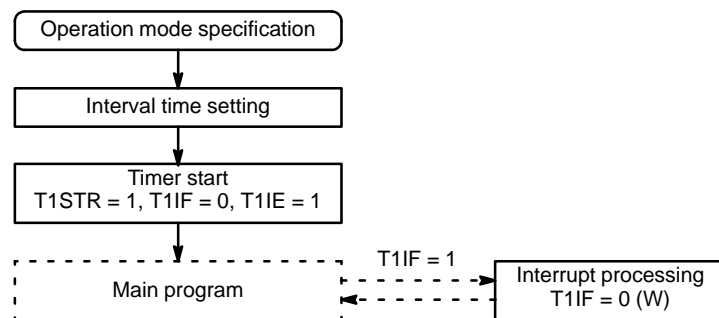


Fig. 2.18 Flow Diagram for Timer Setting

**8/16-BIT TIMER
(TIMER 1 AND TIMER 2)**

(2) Initializing square-wave output

The square-wave output can be set to any value only when the timer stops (T1STR = 0).

To set, proceed as follows:

- (a) Write the set values (01 and 10) at the initialize bits (T1OS1 and T1OS0) of the square wave output. The values are held in the level latch shown in the figure below and not output to the pin.
(Note that the previous square wave state is output to the pin.)
- (b) Write 11 at the same bits. This initializes the square wave output to the set value. If the T1STR bit is set to 0, the square wave output of the pin is set to the set value in step (a) during this write cycle. The pin state of the square wave output in step (a) and (b) is shown below.
- (c) Start the timer when the T1STR bit is 1.

These initialize bits can be set by the bit manipulation instruction.

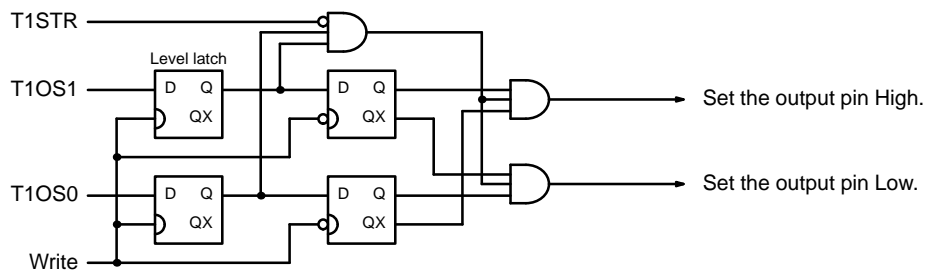
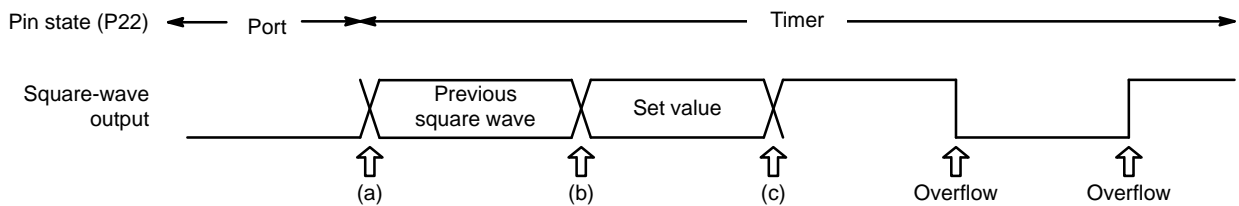


Fig. 2.19 Initialization of Equivalent Circuit



(3) 8-bit external clock mode

In the 8-bit external clock mode, the external clock input can be selected by setting the clock source select bits (T1CS1 and T1CS0) of the timer 1 control register (T1CR). The external clock input pin of the timer corresponds to P20 (EC).

To start the timer, write 1 at the timer start bit (T1STR) of the T1CR to clear the counter.

**8/16-BIT TIMER
(TIMER 1 AND TIMER 2)**

When the value of the counter agrees with that of the timer data register, the interval interrupt request flag bit (T1IF) is set to 1. At this time, if an interrupt is enabled (T1IE = 1), an interrupt request is output to the CPU.

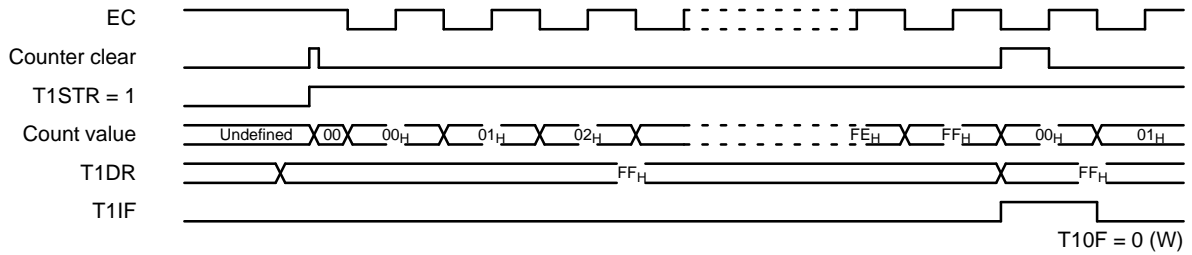


Fig. 2.20 External Cock Mode Operation Description Diagram

(4) Precautions for use of timer stop bit

If the timer is stopped by the timer start bit after being suspended by the timer stop bit, the input clock pulse to the timer may increment the count value by 1 as shown in Figure 2.19 (the count value is not incremented when the input clock pulse is High but incremented when it is Low). Therefore, if the timer is suspended by the timer stop bit, read the counter and then write 0 at the timer start bit.

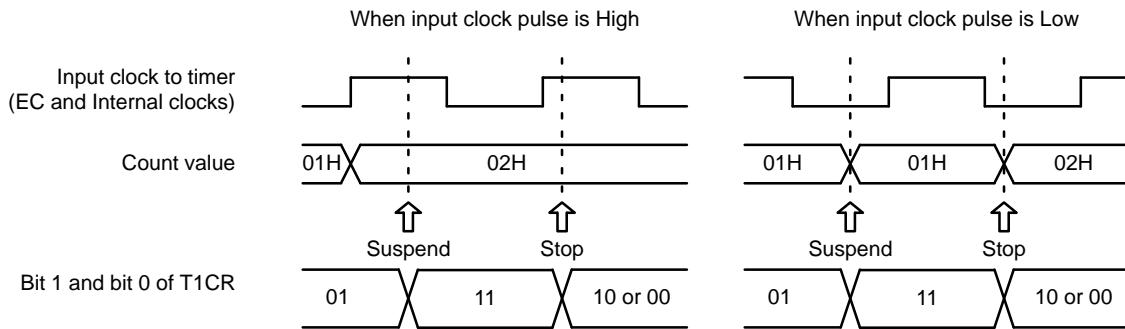


Fig. 2.21 Operation Diagram when Timer Stop Bit is Used

- Address: 0019_H T1CR
- Address: 0018_H T2CR
- Address: 001B_H T1DR
- Address: 001A_H T2DR

(5) 16-bit mode

In the 16-bit mode, each bit of the timer control registers is as shown below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0019 _H	T1IF	T1IE	T1OS1	T1OS0	T1CS1	T1CS0	T1STP	T1STR
Address: 0018 _H	T2IF	T2IE	T2OS1	T2OS0	T2CS1	T2CS0	T2STP	T2STR
	No operation		Set to 00		Set to 11		No operation	

In the 16-bit mode, write 11 at the T2CS1 and T2CS0 bits of the T2CR and set 00 at the T2OS1 and T2OS0 bits.

**8/16-BIT TIMER
(TIMER 1 AND TIMER 2)**

When in the 16-bit mode, the timer is controlled by the T1CR. The timer data registers T2DR and T1DR use the upper and lower bytes, respectively.

The clock source is selected by the T1CS1 and T1CS0 bits of the T1CR. To start the timer, write 1 at the T1STR bit of the T1CR to clear the counter.

If the value of the counter agrees with that of the timer data register, the T1IF bit is set to 1. At this time, an interrupt request is output to the CPU if the T1IE bit is 1.

Note: To read the value of the counter in the 16-bit mode, always read the value twice to check that it is valid and use the data.

See the 8-bit operation diagram for 16-bit mode operation.

(6) Starting and suspending timer

Timer 2 is the same as Timer 1. Therefore, the explanation only describes Timer 1.

(a) Clearing counter to start counting

When the T1STR bit is 0, write 01 at the T1STP and T1STR bits, respectively. The timer is cleared at the edge where the T1STR bit is set from 0 to 1 to start counting.

(b) Suspending timer to start counting without clearing counter

To suspend counting, set the T1STP and T1STR bits to 11. To start counting from the suspended state without clearing the counter, set the T1STP and T1STR bits from 11 to 01.

The state of the timer according to the setting conditions of T1STP and T1STR bits and the operation of the timer when started from the suspended state (when T1STP and T1STR bits = 01) are as follows.

T1STP	T1STR	Timer state setting	Operation of timer when started from timer state setting (bits 1 and 0 = 01)
0	0	Counting is stopped	Counter is cleared to start counting.
0	1	Counting is started	Counting is continued
1	0	Counting is stopped	Counter is cleared to start counting.
1	1	Counting is suspended	Counting is continued without clearing counter.

8-BIT SERIAL I/O

2.6 8-BIT SERIAL I/O

- 8-bit serial data transfer is possible by the clock synchronous method.
- LSB first or MSB first can be selected for data transfer.
- Four shift-clock modes (three internal and one external) can be selected.

■ **Block Diagram**

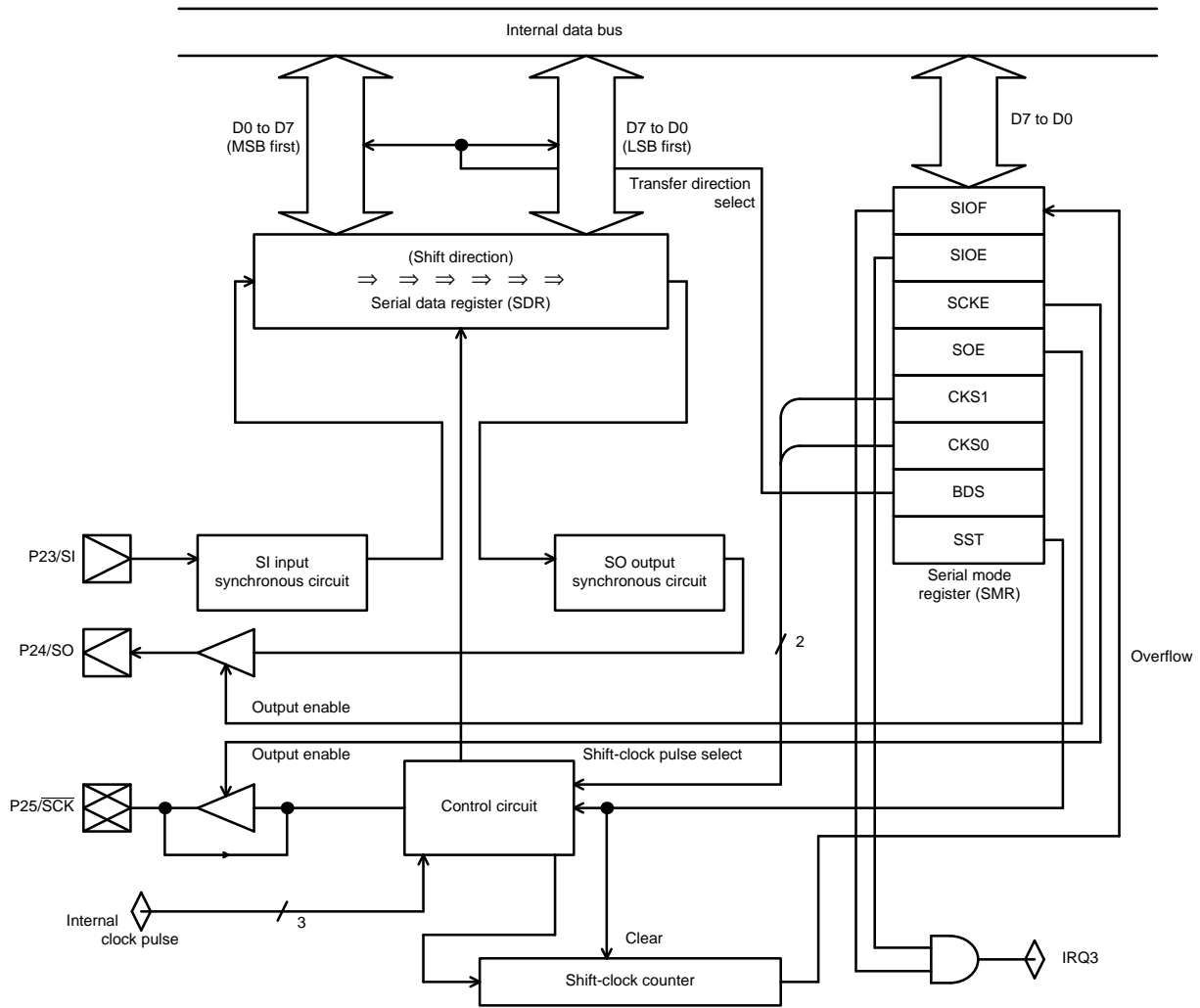


Fig. 2.22 8-bit Serial I/O Block Diagram

■ **Register list**

The 8-bit serial I/O consists of serial mode register (SMR) and serial data register (SDR).

Address: 001C _H	← 8 bit →	R/W Serial mode register
Address: 001D _H	SMR	
	SDR	R/W Serial data register

8-BIT SERIAL I/O

Address: 001C_H **SMR**

Address: 001D_H **SDR**

■ **Description of Registers**

The detail of each register is described below.

(1) Serial mode register (SMR)

The SMR is used to control serial I/O.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 001C _H	SIOF	SIOE	SCKE	SOE	CKS1	CKS0	BDS	SST
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
	Initial value 0000000 _B							

[Bit 7] SIOF: Serial I/O interrupt-request flag

This bit is used to indicate the serial I/O transfer state.

The meaning of each bit when reading is as follows:

0	Serial data transfer not terminated
1	Serial data transfer terminated

Note that 1 is always read when the Read Modify Write instruction is read. If this bit is set when an interrupt is enabled (SIOE = 1), an interrupt request is output to the CPU.

The meaning of each bit when writing is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

The end-of-transfer decision may be made by either the SST bit (bit 0) of the SMR or by this bit.

[Bit 6] SIOE: Serial I/O interrupt-enable bit

This bit is used to enable a serial I/O interrupt request.

0	Serial I/O interrupt-output disable
1	Serial I/O interrupt-output enable

[Bit 5] SCKE: Shift-clock output enable bit

This bit is used to control the shift-clock I/O pins.

0	General-purpose port pin (P30) or SCK input pin
1	SCK (shift clock) output pin

When using the P25/ $\overline{\text{SCK}}$ pin as an external clock, always set the DDR to input (bit 5 of DDR2 = 0).

8-BIT SERIAL I/O

[Bit 4] SOE: Serial-data output enable bit
 This bit is used to control the output pin for serial I/O.

0	General-purpose port pin (P24)
1	SO (serial data) output pin

When using P23/SI pin as external clock, always set the DDR to input (bit 3 of DDR2 = 0).

[Bits 3 and 2] CKS1 and CKS0: Shift-clock select bits
 These bits are used to select the serial shift-clock modes.

CKS1	CKS0	Mode	Clock cycle time	SCK
0	0	Internal shift-clock mode	(instruction cycle) × 2	Output
0	1	Internal shift-clock mode	(instruction cycle) × 8	Output
1	0	Internal shift-clock mode	(instruction cycle) × 32	Output
1	1	External shift-clock mode	SCK	Input

[Bit 1] BDS: Transfer direction select bit
 At serial data transfer, this bit is used to select whether data transfer is performed from the least significant bit first (LSB first) or from the most significant bit first (MSB first).

0	LSB first
1	MSB first

Note that when this bit is rewritten after writing data to the SDR, the data become invalid.

[Bit 0] SST: Serial I/O transfer-start bit
 This bit is used to start serial I/O transfer. The bit is automatically cleared to 0 when transfer is terminated.

0	Serial I/O transfer stop
1	Serial I/O transfer start

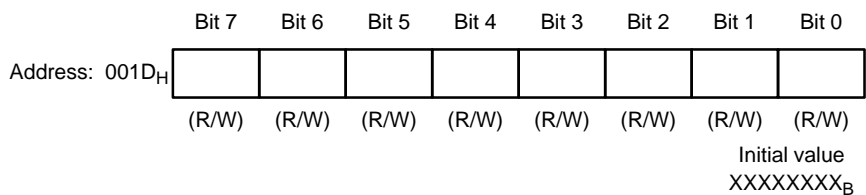
Before starting transfer, ensure that transfer is stopped (SST = 0).

Address: 001C_H SMR

Address: 001D_H SDR

(2) Serial-data register (SDR)

This 8-bit register is used to hold serial I/O transfer data. Do not write data to this register during the serial I/O operation.



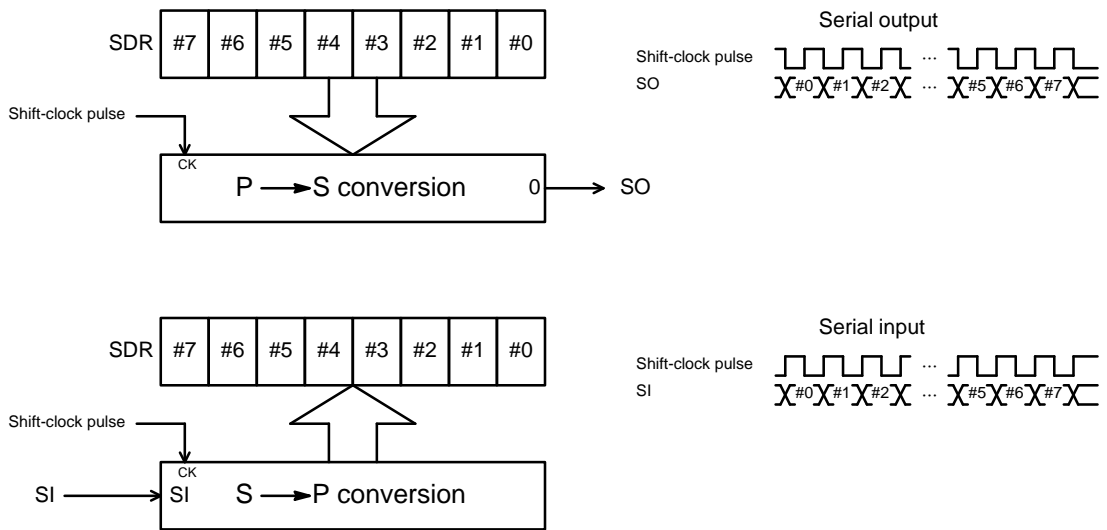
8-BIT SERIAL I/O

■ Description of Operation

The operation of 8-bit serial I/O is described below.

(1) Outline

This module consists of the serial-mode register (SMR) and serial-data register (SDR). At serial output, data in the SDR is output in bit serial to the serial output pin (SO) in synchronization with the falling edge of a serial shift-clock pulse generated from the internal or external clock. At serial input, data is input in bit serial from the serial input pin (SI) to the SDR at the rising edge of a serial shift-clock pulse.



(2) Operation modes

The serial I/O has three internal shift-clock modes and one external shift-clock mode, which are specified by the SMR. Mode switching or clock selection should be made with serial I/O stopped (SST bit (bit 0) of SMR = 0).

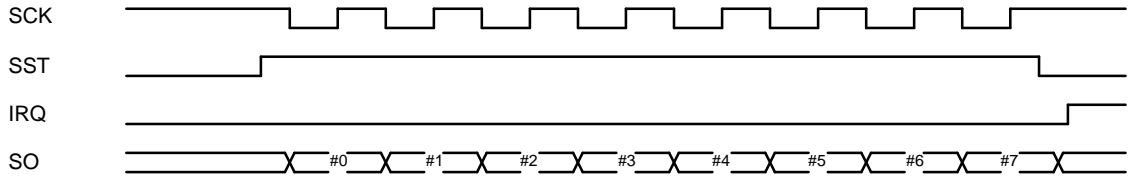
- Internal shift-clock mode
Operation is performed by the internal clock. A shift-clock pulse with a duty of 50% is output from the SCK pin as a synchronous timing output. Data is transferred bit-by-bit at every clock pulse.
- External shift-clock mode
Data is transferred bit-by-bit at every clock pulse in synchronization with the external shift-clock pulse input from the SCK pin. The transfer speed can be from DC to 1/2 oscillation (two instruction cycles). When one instruction cycle is 2.0 μs (at 2 MHz main clock frequency), the transfer speed can be up to 0.25 MHz.

Do not write data to the SMR and SDR during the serial I/O operation in either mode.

8-BIT SERIAL I/O

(3) Interrupt functions

This module can output an interrupt request to the CPU. To output an interrupt request, set the SIOE (bit 6) of the SMR to 1 to enable an interrupt and then set the interrupt flag SIOF (bit 7) of the SMR after 8-bit data transfer is terminated.

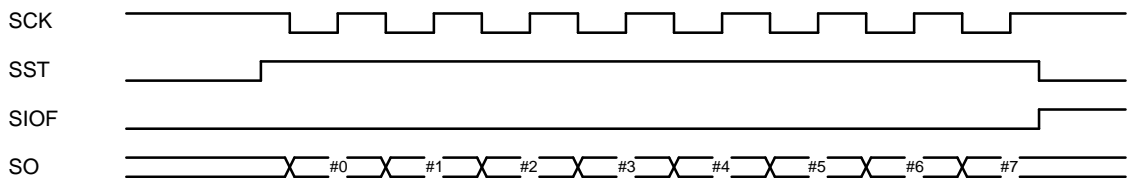


(4) Shift start/stop timing

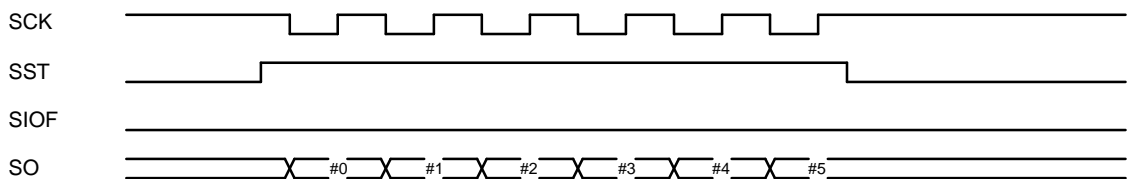
Data transfer starts when 1 is written at the SST (bit 0) bit of the SMR, and stops when 0 is written. When data transfer is terminated, the SST bit is automatically cleared to 0, which stops the operation.

- Internal shift-clock mode (LSB first)

[When transfer terminated]

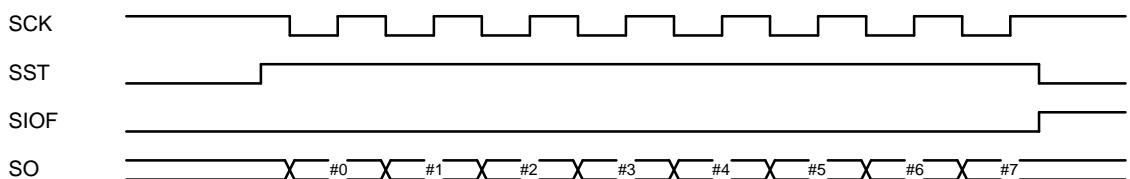


[When transfer suspended]

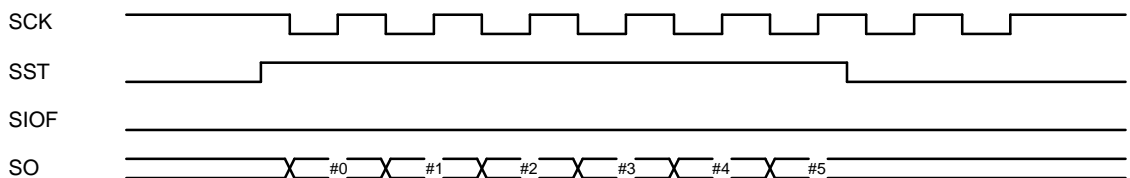


- External shift-clock mode (LSB first)

[When transfer terminated]



[When transfer suspended]



Note: When data is written at the SDR, the output data changes at the falling edge of the external-clock pulse.

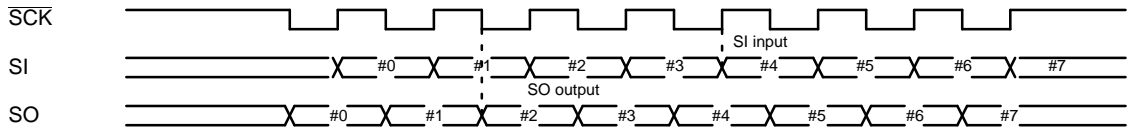
Fig. 2.23 Shift Start/Stop Timing

8-BIT SERIAL I/O

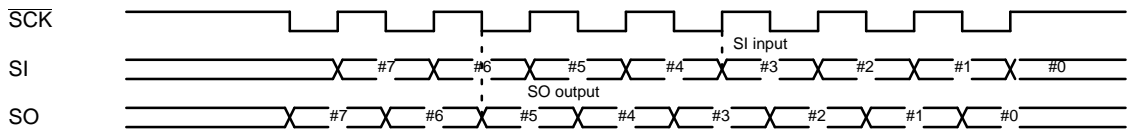
(5) Input/output shift timing

Data is output from the serial output pin (SO) at the falling edge of the shift-clock pulse, and is input from the serial input pin (SI) to the SDR at the rising edge of the shift-clock pulse.

• LSB first (BDS = 0)



• MSB first (BDS = 1)



DI7 to DI0 indicate input data, and DO7 to DO0 indicate output data.

Fig. 2.24 Input/Output Shift Timing

**EXTERNAL INTERRUPT 1
(WAKE UP 1)**

2.7 EXTERNAL INTERRUPT 1 (Wake Up 1)

The external interrupt 1 is controlled by the external interrupt control and external interrupt flag registers.

- Four external interrupt inputs
- An interrupt request is output at the falling edge of the input signal.
- Inverting an input signal outputs an interrupt request at the rising edge.
- Usable as wake-up input

■ **Block Diagram**

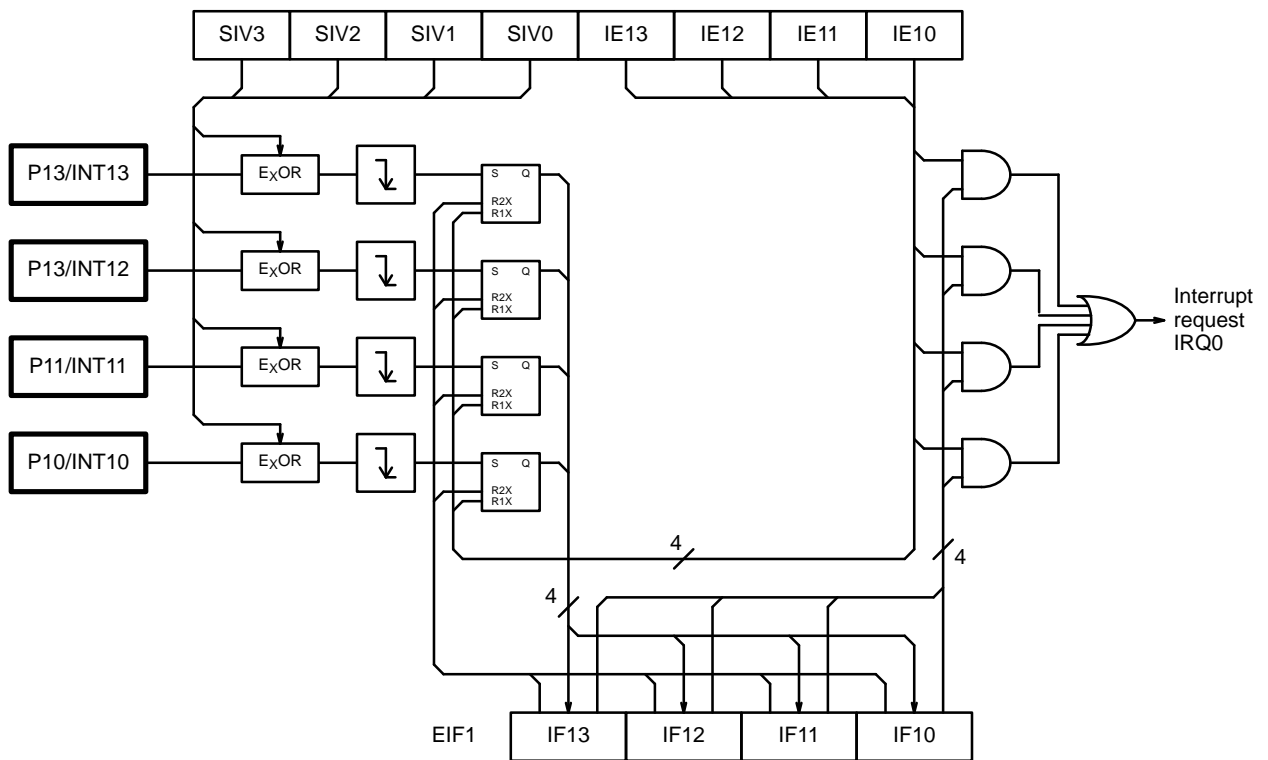


Fig. 2.25 External Interrupt 1 Block Diagram

■ **Register List**

Address: 0030 _H	<div style="border: 1px solid black; width: 100px; height: 15px; margin: 0 auto;"></div> 8 bit	R/W External interrupt 1 control register
Address: 0031 _H	<div style="border: 1px solid black; width: 100px; height: 15px; margin: 0 auto;"></div> EIF1	R/W External interrupt 1 flag register

**EXTERNAL INTERRUPT 1
(WAKE UP 1)**

Address: 0030_H **T1CR**

Address: 0031_H **T2CR**

■ Description of Register Details

The detail of each register is described below.

(1) External-interrupt 1 control register (EIE1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIV3	SIV2	SIV1	SIV0	IE13	IE12	IE11	IE10
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value
00000000_B

[Bit 7 to Bit 4] SIV3 to SIV0: Interrupt invert bit
These bits are used to invert external interrupts EI13 to EI10.

0	External interrupt signal not inverted
1	External interrupt signal inverted

[Bit 3 to Bit0] IE13 to IE10: Interrupt enable bit
These bits are used to enable external interrupts EI13 to EI10.

0	External interrupt disabled (edge detect flag initialized)
1	External interrupt enabled

Note: The interrupt flag may be turned on immediately after an interrupt is enabled or an interrupt input is inverted.

Address: 0030_H **T1CR**

Address: 0031_H **T2CR**

(2) External interrupt 1 flag register (EIF1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	—	—	—	IF13	IF12	IF11	IF10
—	—	—	—	(R/W)	(R/W)	(R/W)	(R/W)

Initial value
----0000_B

[Bit 3 to Bit 0] IF13 to IF10: Falling edge detect flag
Detect the falling edges of EI13 to EI10.

(When write)

0	Falling edge detect flag cleared
1	No operation

(When read)

0	Falling edge not detected
1	Falling edge detected

If the interrupt enable bits (IE13 to IE10) of the external interrupt 1 control register (EIE1) are 1, an interrupt request is output to the CPU when the corresponding falling edge detect flag bits (IF13 to IF10) are set to 1.

**EXTERNAL INTERRUPT 2
(WAKE UP 2)**

2.8 EXTERNAL INTERRUPT 2 (Wake up 2)

External interrupt 2 is controlled by the external interrupt control and external interrupt flag registers.

- Eight external interrupt input pins
- An interrupt request is output by Low-level input signals.
- Also usable as wake-up input

■ Block Diagram

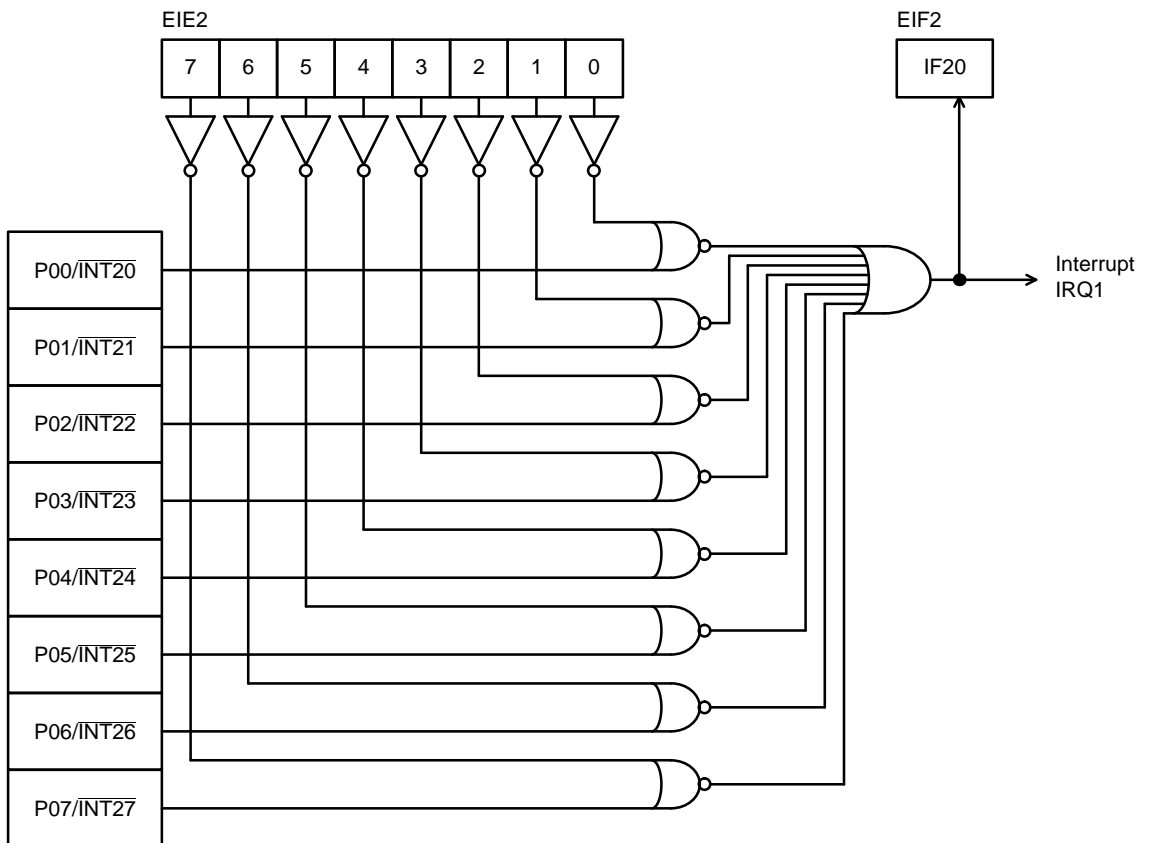


Fig. 2.26 External Interrupt 2 Block Diagram

■ Register list

This external interrupt 2 consists of external interrupt 2 control register (EIE2) and external interrupt 2 flag register (EIF2).

	← 8 bit →	
Address: 0032 _H	EIE2	R/W External-interrupt control register 2
Address: 0033 _H	EIF2	R/W External-interrupt flag register 2

**EXTERNAL INTERRUPT 2
(WAKE UP 2)**

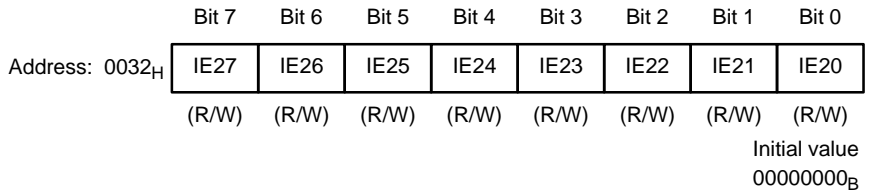
Address: 0032_H EIE2

Address: 0033_H EIF2

■ Description of Registers

The detail of each register is described below.

(1) External interrupt 2 control register (EIE2)



[Bit 7 to Bit 0] IE27 to IE20: Interrupt enable bit

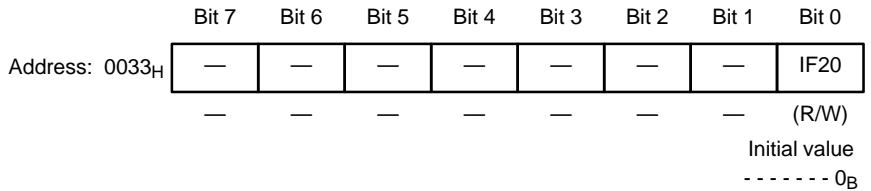
These bits are used to enable external interrupt of INT27 to INT20.

0	External interrupt 2 disabled
1	External interrupt 2 enabled

Address: 0032_H EIE2

Address: 0033_H EIF2

(2) External interrupt 2 flag register (EIF2)



[Bit 0] IF20: Low level detect flag.

This bit is used to detect Low level of INT27 to INT20.

(When write)

0	Clears flag for detecting Low level
1	No operation

(When read)

0	No Low level input
1	Low level input detected

If any of the interrupt enable bits (IE27 to IE20) of the external interrupt 2 control register (EIE2) is 1, the Low level detect flag bit (IF20) is set to 1 and an interrupt request is output to the CPU when a Low level is input to the port corresponding to this bit.

Note: Unlike other resources, even if the external interrupt 2 control register is disabled for an interrupt, it keeps generating interrupts until the interrupt source is cleared. Therefore, always clear the interrupt source after disabling an interrupt.

**BUZZER OUTPUT
CIRCUIT**

2.9 BUZZER OUTPUT CIRCUIT

- The buzzer output sound for checking key input can be output from port 27.
- Seven frequencies can be output by setting the registers.

■ **Block Diagram**

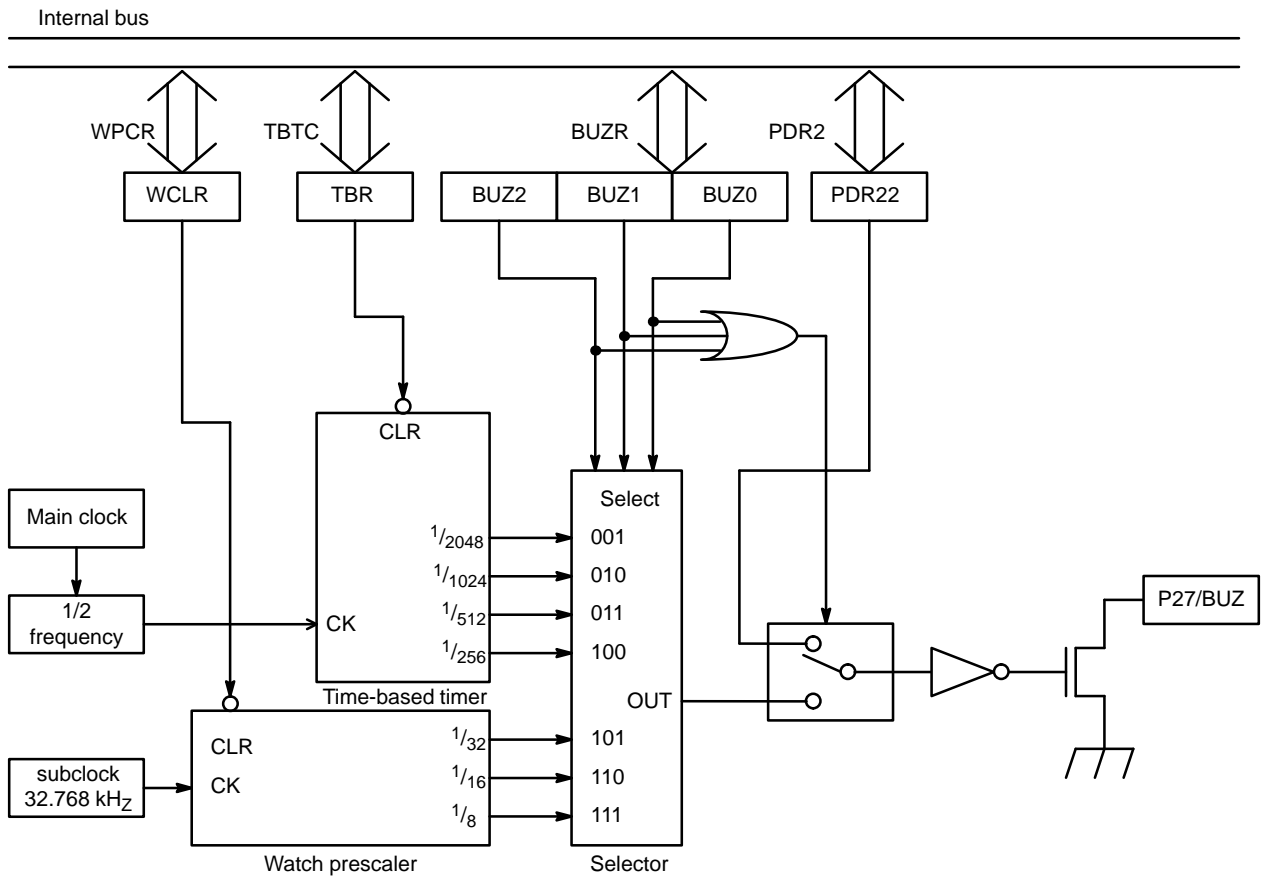
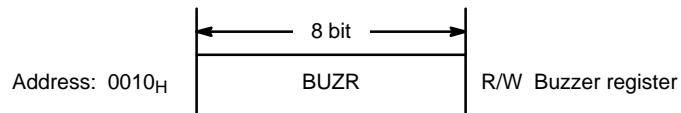


Fig. 2.27 Buzzer output circuit Block Diagram

■ **Registers**

The buzzer output block has buzzer register (BUZR).



**BUZZER OUTPUT
CIRCUIT**

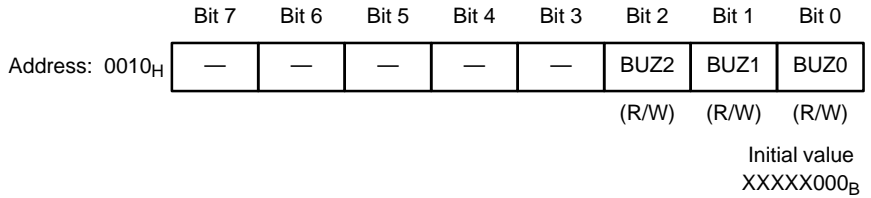
Address: 0010_H BUZR

■ Description of Registers

The detail of buzzer register is described below.

(1) Buzzer register (BUZR)

This 3-bit register enables buzzer output and selects the frequency.



[Bits 2 to Bit0] BUZ2 to BUZ0: Buzzer-select bits

These bits are used to enable buzzer output and select the frequency. The buzzer output function is disabled by 000 and the port operates normally. In other cases, the frequencies listed in the table below are selected.

Table 2-5 Buzzer Output Frequencies
(at $f_{CH} = 3 \text{ MHz}$ and $f_{CL} = 32.768 \text{ kHz}$)

BUZ2	BUZ1	BUZ0	Buzzer output frequency
0	0	0	General-purpose port operation
0	0	1	732 Hz
0	1	0	1456 Hz
0	1	1	2930 Hz
1	0	0	5859 Hz
1	0	1	1024 Hz
1	1	0	2048 Hz
1	1	1	4096 Hz

f_{CH} : Main clock frequency
 f_{CL} : Subclock frequency

■ Description of Operation

This circuit outputs a signal for use as a check sound. The buzzer register is used to enable buzzer output and select the frequency. When values other than 000 are set at the BUZR register, the square wave of the set frequency is output at the port.

■ Precautions for Buzzer Output Circuit

Part of the time-base timer or watch prescaler is used as the buzzer output. Therefore, setting conditions of the time-base timer or watch prescaler affects the circuit.

**LCD CONTROLLER/
DRIVER**

2.10 LCD CONTROLLER/DRIVER

The LCD controller/driver consists of the display controller that generates segment and common signals according to the display data and memory data, and the segment and common drivers that can drive the LCD panel directly.

- Direct LCD driving
- Built-in dividing resistor for driving LCD (option)
- Four common outputs (COM0 to COM3) and 32 segment outputs (SEG0 to SEG31)
- 16-byte display data memory
- 1/2, 1/3, or 1/4 selected as duty.
- Main clock (32.768 kHz) and subclock (32.768 kHz) can be selected as drive clock source.
- SEG8 to SEG31 can be used as general-purpose ports (option).

■ **Block Diagram**

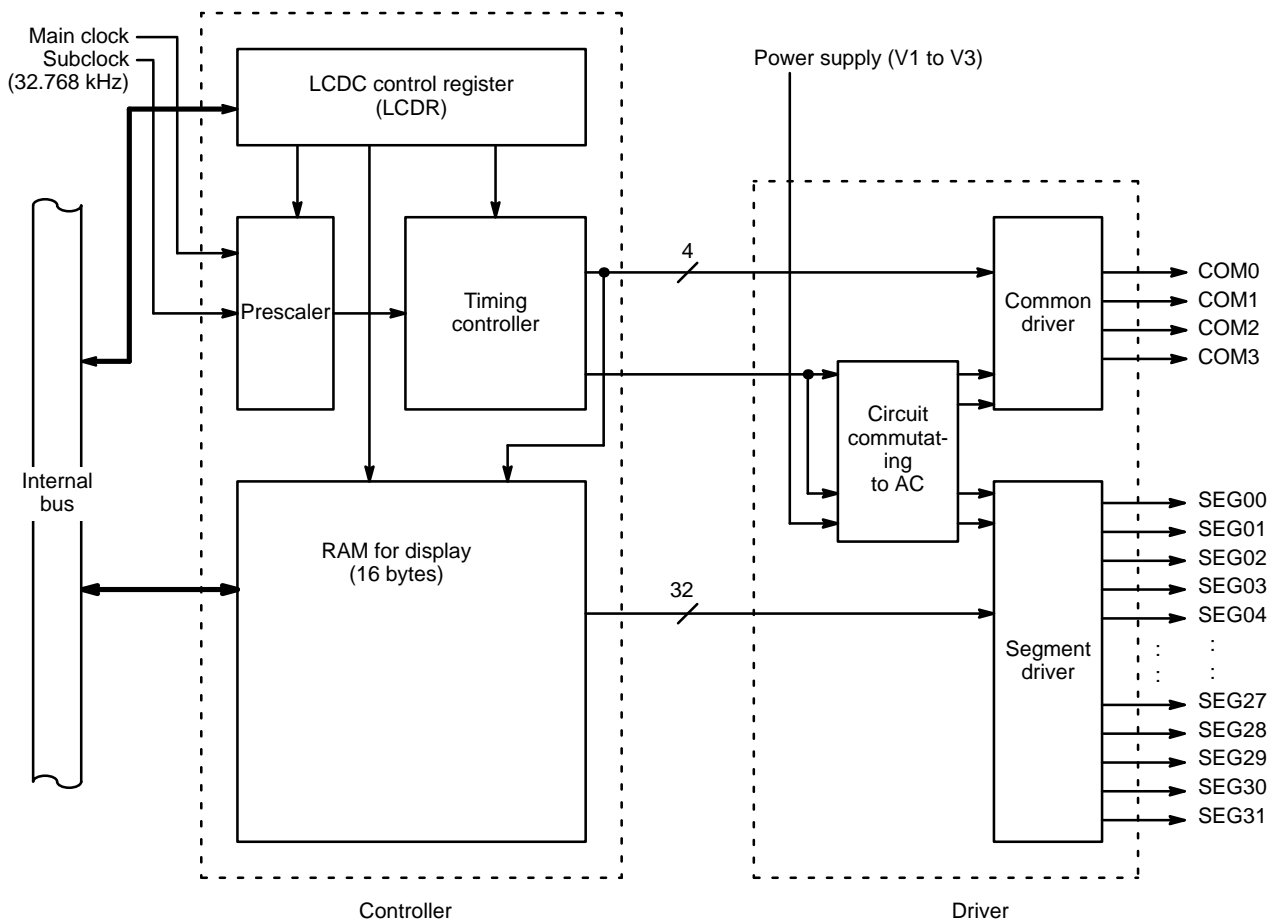
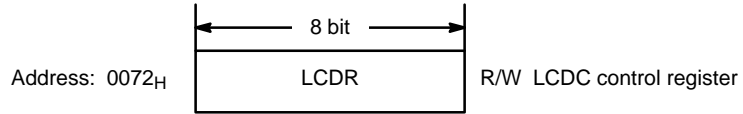


Fig. 2.28 LCD Controller/Driver Block Diagram

**LCD CONTROLLER/
DRIVER**

■ **Registers**

The LCD controller/driver has the LCDC control register (LCDR).



■ **Description of Registers**

The detail of LCDC control register is described below.

Address: 0072_H LCDR

(1) LCDC control register (LCDR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0072 _H	CSS	LCEN	VSEL	BK	MS1	MS0	FP1	FP0
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)

Initial value
00010000_B

[Bit 7] CSS: Clock source select bit

This bit is used to select a frame cycle generation clock.

0	Main clock
1	Subclock

[Bit 6] LCEN: Operation enable bit

This bit is used to enable LCD controller/driver operation at watch mode

0	Terminates the operation at watch mode
1	Executes operation at watch mode

[Bit 5] VSEL: Drive power control bit

This bit is used to control LCD drive power.

0	Connection of internal resistor for divided voltage enters off state
1	Connection of internal resistor for divided voltage enters on state

[Bit 4] BK: Display or display blanking select bit

This bit is used to select display or display blanking. The segment output in display blanking is a non-conforming waveform.

0	Display
1	Display blanking

**LCD CONTROLLER/
DRIVER**

[Bit 3 and Bit 2] MS1 and MS0: Display mode select bit

These bits are used to select display mode. The mode is set according to the following table.

MS1	MS0	Display mode	Number of time divisions: N
0	0	LCD operation stop	—
0	1	1/2 duty output mode	2
1	0	1/3 duty output mode	3
1	1	1/4 duty output mode	4

[Bit 1 and Bit 0] FP1 and FP0: Clock cycle select bit

These bits are used to select the LCD clock cycle. The frame frequency is shown below. Calculate the optimum frame frequency and set the register according to the LCD module.

FP1	FP0	Frame frequency (at $f_{CH} = 3 \text{ MHz}$ and $f_{CL} = 32.768 \text{ kHz}$)			
		CSS = 0		CSS = 1	
0	0	$f_{CH}/(2^{12} \times N)$	183 Hz (N = 4)	$f_{CL}/(2^5 \times N)$	256 Hz (N = 4)
0	1	$f_{CH}/(2^{13} \times N)$	92 Hz (N = 4)	$f_{CL}/(2^6 \times N)$	128 Hz (N = 4)
1	0	$f_{CH}/(2^{14} \times N)$	46 Hz (N = 4)	$f_{CL}/(2^7 \times N)$	64 Hz (N = 4)
1	1	$f_{CH}/(2^{15} \times N)$	23 Hz (N = 4)	$f_{CL}/(2^8 \times N)$	32 Hz (N = 4)

N: Number of time divisions

f_{CH} : Main clock frequency

f_{CL} : Subclock frequency

**LCD CONTROLLER/
DRIVER**

RAM for Display

The LCD controller/driver contains the 16 × 8-bit RAM for generating a segment output signal. The data of this RAM is automatically read in synchronization with the common signal select timing and the waveform corresponding to this data is output from the segment output pin.

32 segment signals correspond to 16 locations of the display RAM. Each location bit is in synchronization with the common signal select timing: bits 0 and 4 with COM0, bits 1 and 5 with COM1, bits 2 and 6 with COM2, and bits 3 and 7 with COM3. If the value of each bit is 1, the signal is converted to LCD voltage and if it is 0, the signal is converted to non-LCD and is not output. However, at reset, COM0 to COM3 and SEG0 to SEG32 go Low to provide no LCD display.

The waveform is output from the segment pins in synchronization with the common signal select timing, irrespective of the CPU operation. Therefore, reading and writing from and to the display RAM are possible in any timing.

When using SEG9 to SEG31 as general-purpose output ports, the 12 upper bytes are usually used as RAM. When reset, the impedance of these ports goes High.

Address	b3	b2	b1	b0	SEG00	
060 _H	b7	b6	b5	b4	SEG01	
061 _H	b3	b2	b1	b0	SEG02	
	b7	b6	b5	b4	SEG03	
062 _H	b3	b2	b1	b0	SEG04	
	b7	b6	b5	b4	SEG05	
063 _H	b3	b2	b1	b0	SEG06	
	b7	b6	b5	b4	SEG07	
064 _H	b3	b2	b1	b0	SEG08	} Multiplexed with ports 40 to 47
	b7	b6	b5	b4	SEG09	
065 _H	b3	b2	b1	b0	SEG10	
	b7	b6	b5	b4	SEG11	
066 _H	b3	b2	b1	b0	SEG12	} Multiplexed with ports 50 to 57
	b7	b6	b5	b4	SEG13	
067 _H	b3	b2	b1	b0	SEG14	
	b7	b6	b5	b4	SEG15	
068 _H	b3	b2	b1	b0	SEG16	} Multiplexed with ports 10 to 17
	b7	b6	b5	b4	SEG17	
069 _H	b3	b2	b1	b0	SEG18	
	b7	b6	b5	b4	SEG19	
06A _H	b3	b2	b1	b0	SEG20	
	b7	b6	b5	b4	SEG21	
06B _H	b3	b2	b1	b0	SEG22	
	b7	b6	b5	b4	SEG23	
06C _H	b3	b2	b1	b0	SEG24	
	b7	b6	b5	b4	SEG25	
06D _H	b3	b2	b1	b0	SEG26	
	b7	b6	b5	b4	SEG27	
06E _H	b3	b2	b1	b0	SEG28	
	b7	b6	b5	b4	SEG29	
06F _H	b3	b2	b1	b0	SEG30	
	b7	b6	b5	b4	SEG31	
	COM3	COM2	COM1	COM0		

**LCD CONTROLLER/
DRIVER**

■ **Operation**

First, write the data to be displayed by display RAM. Then, set the value corresponding to the LCD panel to be used to LCR (LCD control register). The LCD drive waveform is output according to the data in the display RAM, when the clock pulse is supplied. A high-speed clock or low-speed clock can be selected as clock source. The clock source can be switched during the LCD display. However, the display tends to flicker by switching. Therefore, it is best to stop the display by blanking, etc. before switching the clock.

The display drive output has a 2-frame AC waveform. The combination of bias and duty shown below may be possible. Examples of waveforms are shown in the following pages.

	1/2 duty	1/3 duty	1/4 duty
1/2 bias	⊙	×	×
1/3 bias	×	⊙	⊙

⊙ Recommended mode
 ×: Application disabled

The COM2 and COM3 output waveforms are non-conforming waveforms in the 1/2 duty mode. The COM3 output waveform is also a non-conforming waveform at 1/3 duty.

When LCD operation is terminated, both common and segment output waveforms at L level. However, when SEG08 to SEG 31 are specified as general-purpose port by the mask option, segment data are not output.

LCD CONTROLLER/
DRIVER

■ LCD drive output waveform

(1) Waveform at 1/2 bias and 1/2 duty

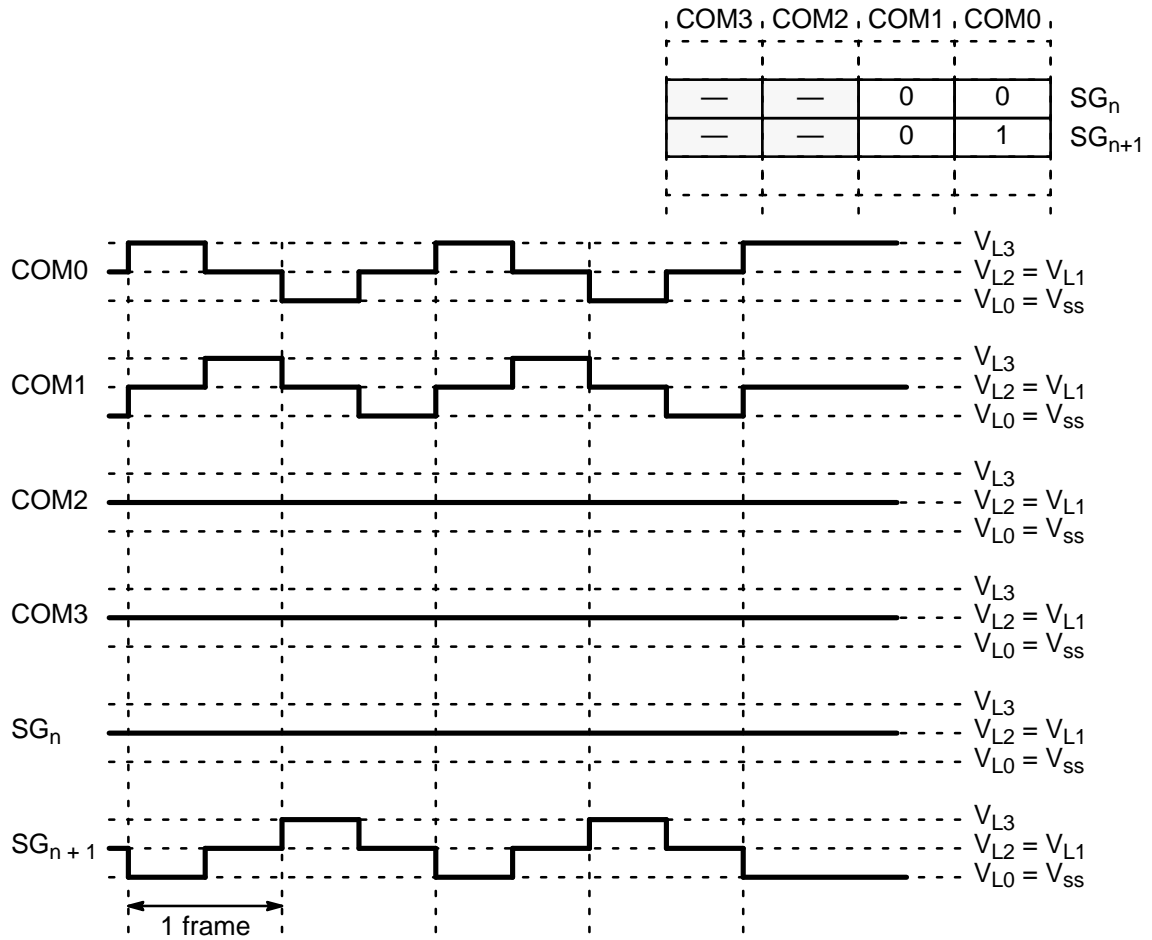


Fig. 2.29 Example of Waveform at Pin Corresponding to the RAM Data for Display

LCD CONTROLLER/
DRIVER

(2) Waveform at 1/3 bias and 1/3 duty

	COM3	COM2	COM1	COM0	
—	1	0	0	0	SG_n
—	1	0	0	1	SG_{n+1}

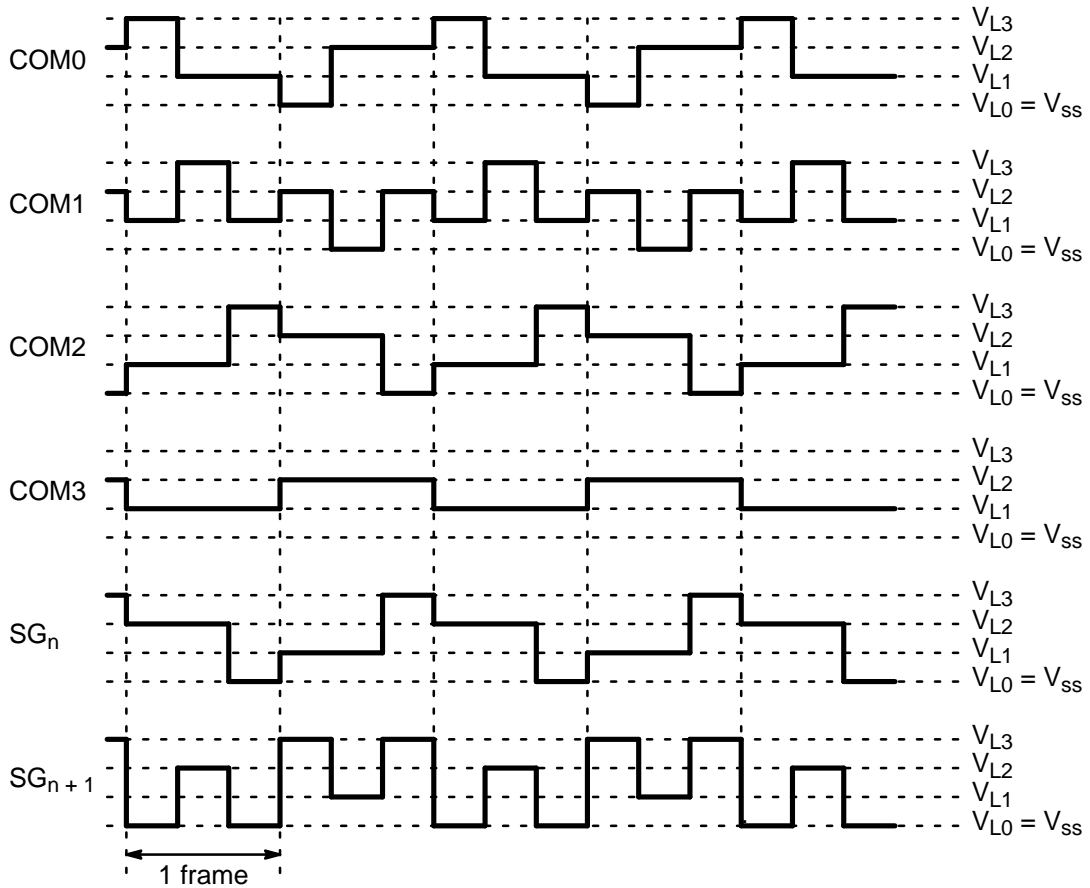


Fig. 2.30 Example of Waveform at Pin Corresponding to the RAM Data for Display

LCD CONTROLLER/
DRIVER

(3) Waveform at 1/3 bias and 1/4 duty

	COM3	COM2	COM1	COM0	
	0	1	0	0	SG_n
	0	1	0	1	SG_{n+1}

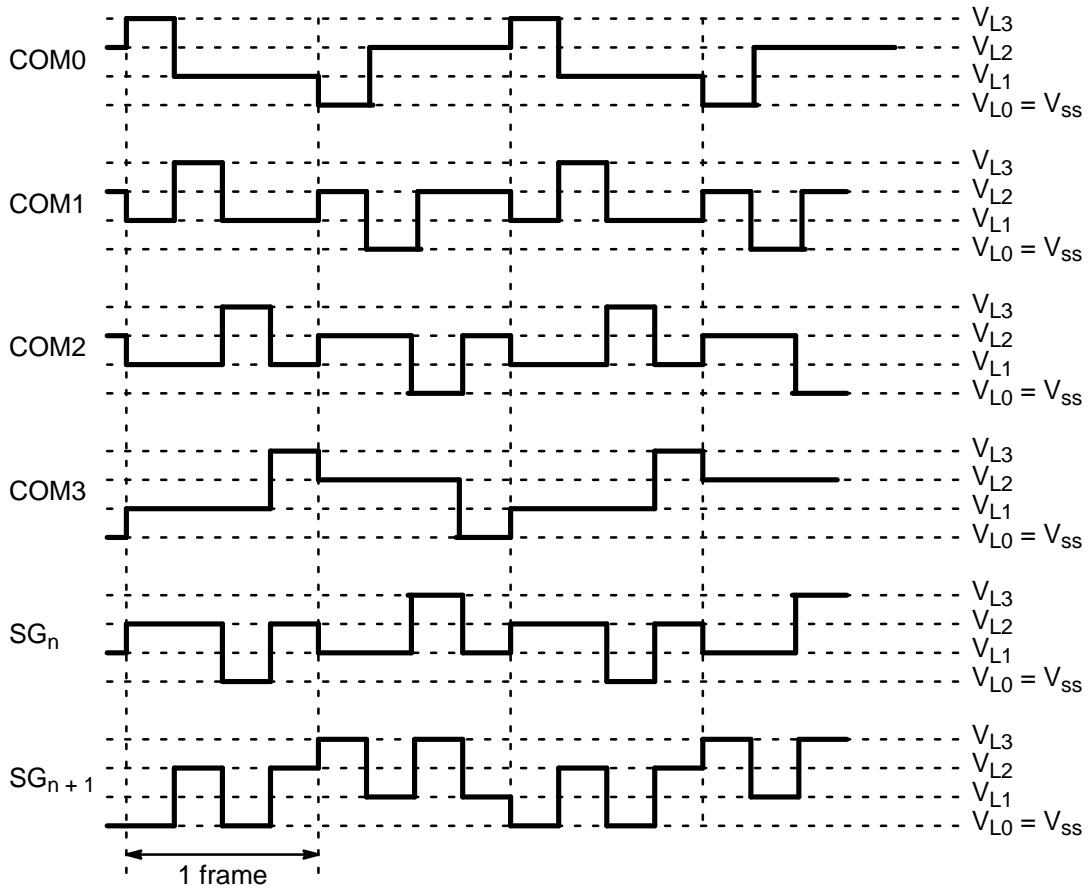


Fig. 2.31 Example of Waveform at Pin Corresponding to the RAM Data for Display

**LCD CONTROLLER/
DRIVER**

■ **Voltage setting at power pins (V_3 , V_2 and V_1) for driving LCD**

Set the voltages at the LCD power pins (V_3 , V_2 and V_1) as shown below.

	V_3	V_2	V_1
1/2 bias	V_{LCD}	$1/2 V_{LCD}$	$1/2 V_{LCD}$
1/3 bias	V_{LCD}	$2/3 V_{LCD}$	$1/3 V_{LCD}$

V_{LCD} : LCD operating voltage

A connection example for supply power to drive the LCD is shown in Figure 2.29.

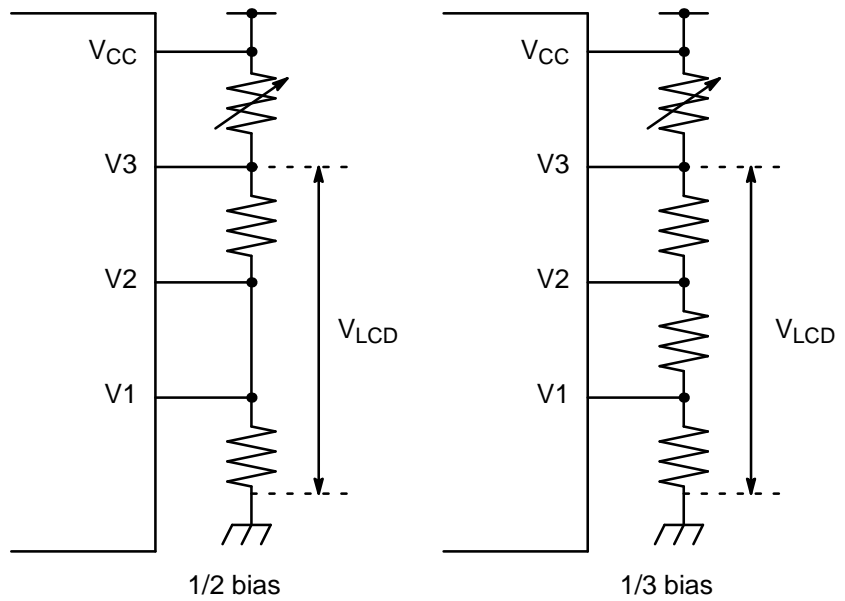


Fig. 2.32 Connection Examples for Supply Power for Driving LCD

Notes:

1. To set a 1/2 duty when using the external dividing resistor (ladder circuit), short-circuit the pins V_2 and V_1 .
2. To switch the LCD off at standby, use the built-in dividing resistor to cut the current to the LCD.

• **Built-in voltage dividing resistor**

The built-in voltage dividing resistors are connected as shown in Figure 2.30.

Writing 1 at the VSEL bit connects the built-in voltage dividing resistors. Therefore, write 1 at the VSEL bit to connect the resistors and set 0 to disconnect the resistors.

The built-in voltage dividing circuit is connected to the V_{SS} through the transistor within chip. Therefore, the current flowing into the resistor can be cut when the LCDC stops.

**LCD CONTROLLER/
DRIVER**

In the figure, the LCDC enable bit becomes inactive in the LCD stop and WATCH modes (LCEN = 0).

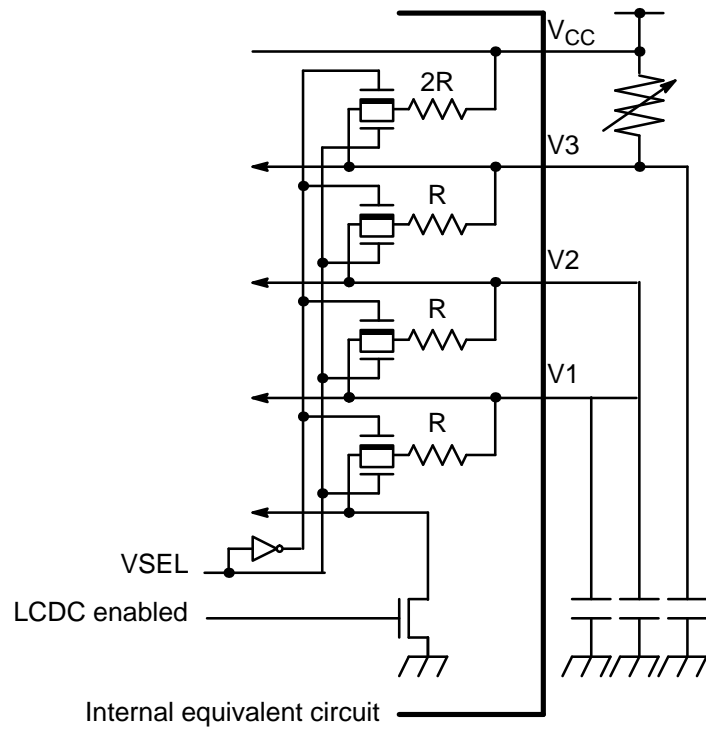


Fig. 2.33 Built-in Voltage Dividing resistors

**REMOTE-CONTROL
CARRIER FREQUENCY
GENERATOR**

2.11 REMOTE-CONTROL CARRIER FREQUENCY GENERATOR

- This generator is a remote-control circuit for generating remote-control carrier frequencies.
- The 6-bit binary counter is built in.
- Four internal clock pulses can be selected to set a duty (H width) and cycle.

■ **Block Diagram**

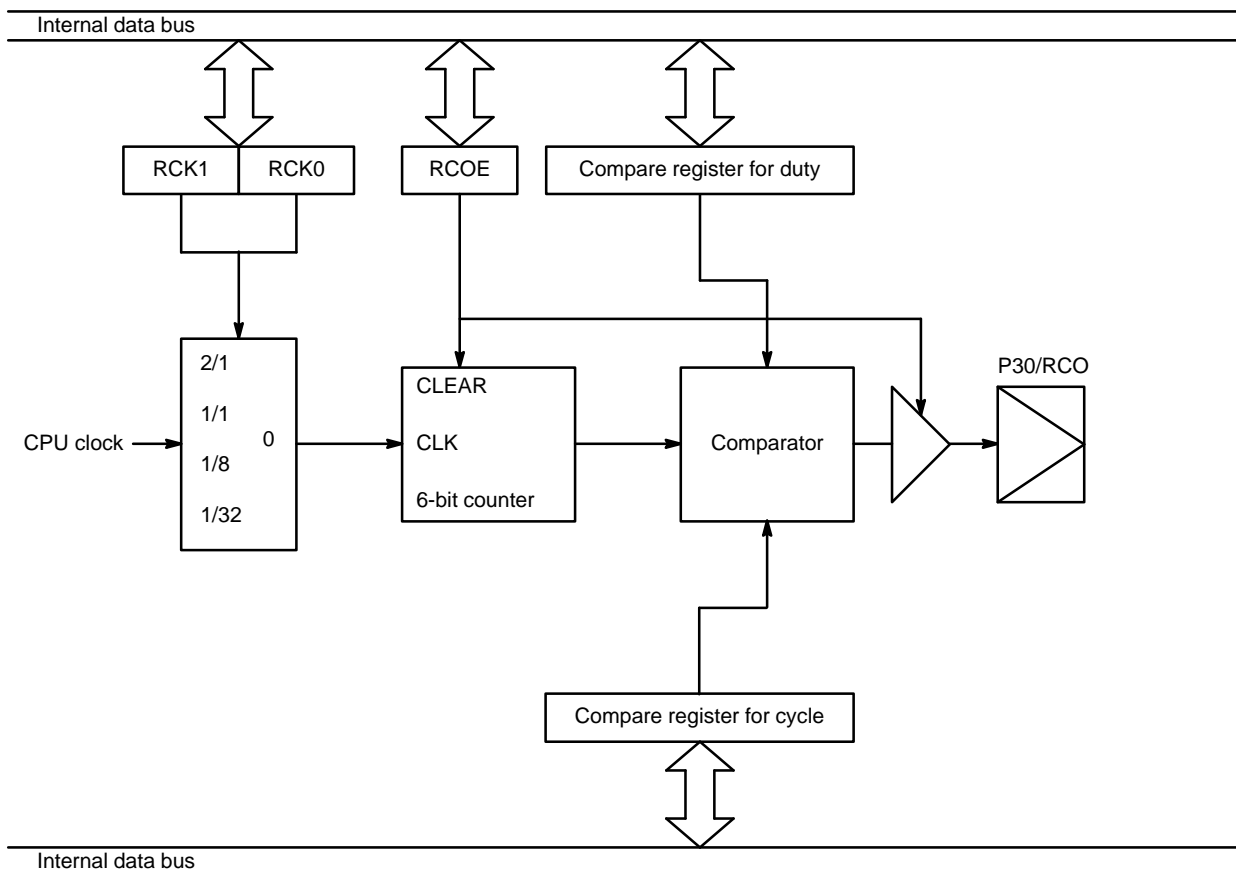


Fig. 2.34 Remote-control Carrier Frequency Generator Block Diagram

■ **Registers**

Address: 0014 _H	← 8 bit →	R/W Remote control register 1
Address: 0015 _H	RCR 2	R/W Remote control register 2

**REMOTE-CONTROL
CARRIER FREQUENCY
GENERATOR**

Address: 0014_H RCR1

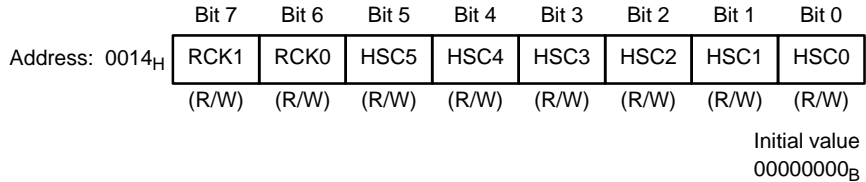
Address: 0015_H RCR2

■ **Description of Registers**

The detail of each register is described below.

(1) Remote-control register 1 (RCR1)

This register is used to select the reference clock and set the duty of remote-control carrier frequency.



[Bits 7 and Bit 6] RCK1 and RCK0: Clock source for remote-control carrier frequency select bit

These bits are used to select the clock source for the remote-control carrier frequency.

RCK1	RCK0	Reference clock	Reference clock at $f_{CH} = 3 \text{ MHz}$
0	0	(Instruction cycle time) × 1/2	0.67 μs
0	1	(Instruction cycle time) × 1	1.33 μs
1	0	(Instruction cycle time) × 8	10.33 μs
1	1	(Instruction cycle time) × 32	42.56 μs

Instruction cycle: Selectable from 1/4 to 1/64 oscillations of main clock by setting system clock control register (SYCC).

f_{CH} : Oscillation frequency of main clock

[Bit 5 to Bit 0] HSC5 to HSC0: Bits for setting duty of remote-control carrier frequency

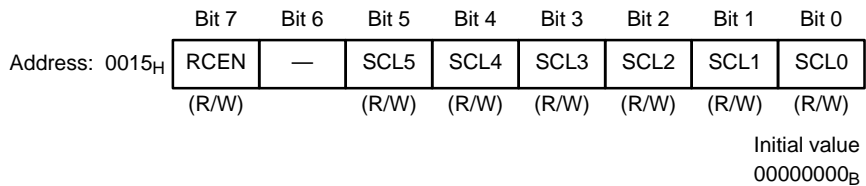
These bits are used for the 6-bit compare register to set the duty of the remote-control carrier frequency. To set the duty of the remote-control carrier frequency, set the value calculated from the clock source in binary at these bits. For example, to set a duty of 26 μs, select clock source = instruction × 1 and set 010100 (1/20 oscillation) at these 6 bits.

Address: 0014_H RCR1

Address: 0015_H RCR2

(2) Remote-control register 2 (RCR2)

This register is used to enable the output and set the cycle of remote-control carrier frequency.



**REMOTE-CONTROL
CARRIER FREQUENCY
GENERATOR**

[Bit 7] RCEN: Bit for enabling output of remote-control carrier frequency
This bit is used to enable the output of remote-control carrier frequency to the P30/RCO pin. Setting this bit to 0 enables clearing of the 6-bit counter.

[Bits 5 to Bit 0] SCL5 to SCL0: Bits for setting cycle of remote-control carrier frequency

These bits are used for the 6-bit compare register to set the cycle of the remote-control carrier frequency.

To set the cycle of the remote-control carrier frequency, set the value calculated from the clock source in binary at these bits. For example, to set a cycle of 66.5 μs, select reference clock = instruction × 1 and set 110010 (1/50 oscillation) at these 6 bits. This enables selection of a cycle of 66.5 μs.

■ Description of Operation

Remote-control registers 1 and 2 (RCR1 and RCR2) control a 6-bit counter to output the remote-control carrier frequency to the P30/RCO pin.

A usage example is given below.

- Example

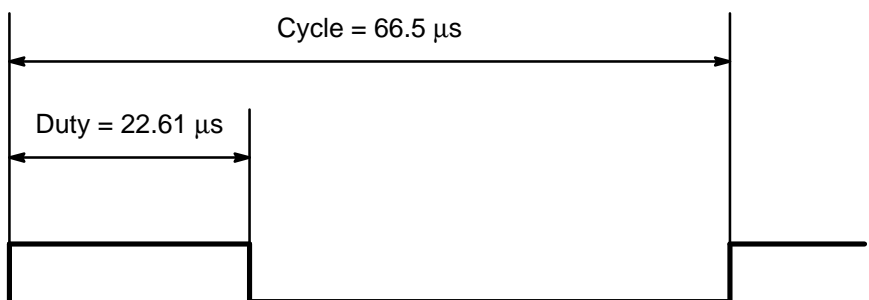
Cycle: 15 kHz

Duty: 1/3

Reference clock: instruction cycle × 1

RCR1 set value: 01 010001
 └──┬──┘ Duty set value (1/17 oscillation)
 └──┬──┘ Reference clock set value

RCR2 set value: 1X 110010
 └──┬──┘ Cycle set value (1/50 oscillation)
 └──┬──┘ Output enable



Note: To set the duty and cycle, the cycle set value must always be greater than the set duty value.

**WATCH
PRESCALER**

2.12 WATCH PRESCALER

- This prescaler has a 15-bit binary counter
- Four interval times and three clock pulses can be selected.
- This function cannot be used when the single clock module is selected by the mask option.

■ **Block Diagram**

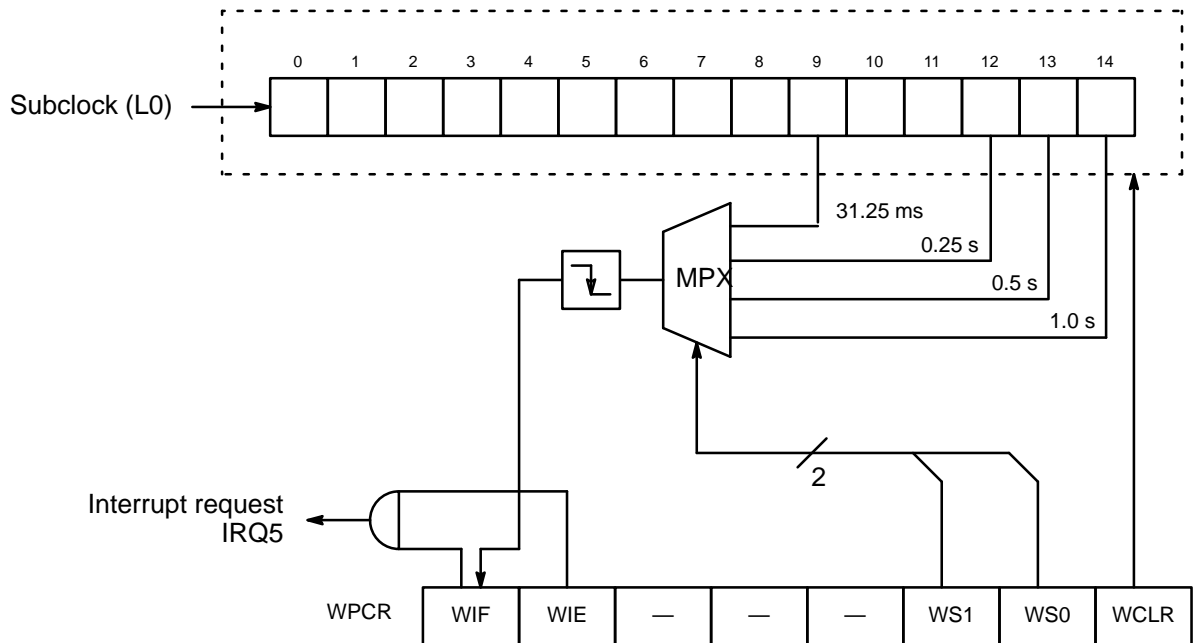
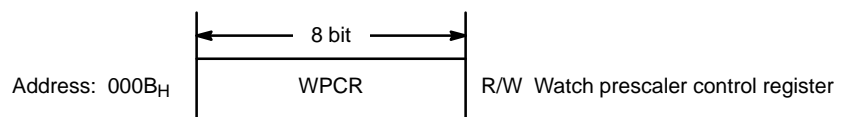


Fig. 2.35 Watch Prescaler Block Diagram

■ **Register list**



**WATCH
PRESCALER**

Address: 000B_H **WPCR**

■ **Description of Registers**

The detail of watch prescaler is described below.

(1) Watch prescaler control register (WPCR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 000B _H	WIF	WIE	—	—	—	WS1	WS0	WCLR
	(R/W)	(R/W)				(R/W)	(R/W)	(R/W)
								Initial value 00XXX000 _B

[Bit 7] WIF: Watch interrupt flag
When writing, this bit is used to clear the watch interrupt flag.

0	Clears watch interrupt flag
1	No operation

When reading, this bit indicates that the watch interrupt has occurred.

0	Watch interrupt not occurred
1	Watch interrupt occurred

1 is read when the Read Modify Write instruction is read. If the WIF bit is set to 1 when the WIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 6] WIE: Watch interrupt enable bit
This bit is used to enable an interrupt by the watch.

0	Interrupt by watch disabled
1	Interrupt by watch enabled

[Bit 2 and 1] WS1, WS0: Interrupt interval time specification bit by watch
These bits are used to specify the interrupt cycles.

WS1	WS0	Interrupt cycle	Value at $f_{CL} = 32.768 \text{ kHz}$
0	0	$2^{10}/f_{CL}$	31.25 ms
0	1	$2^{13}/f_{CL}$	0.25 s
1	0	$2^{14}/f_{CL}$	0.50 s
1	1	$2^{15}/f_{CL}$	1.00 s

f_{CL} : Subclock oscillation frequency

[Bit 0] WCLR: Bit clearing watch prescaler
This bit is used to clear the watch prescaler.

0	Watch prescaler cleared
1	No operation

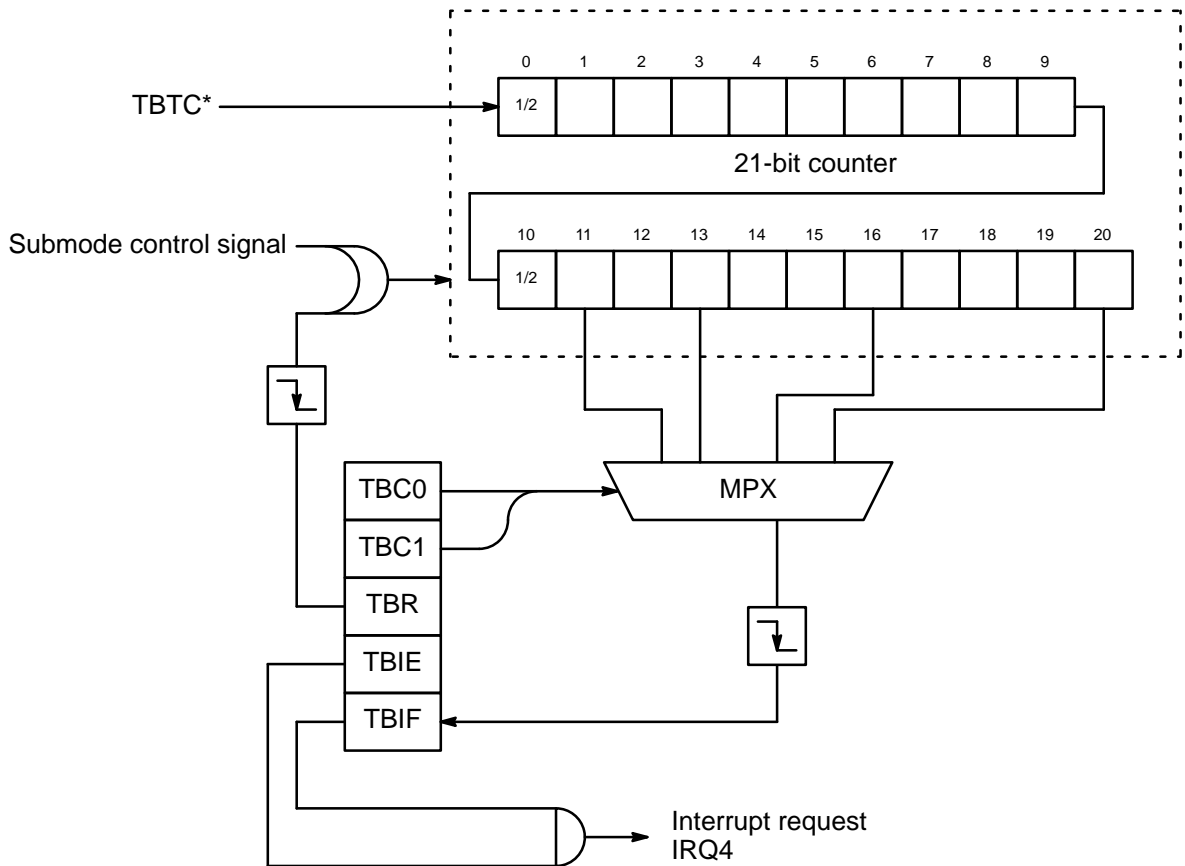
1 is always read when this bit is read.

TIME-BASE TIMER

2.13 TIME-BASE TIMER

- This timer has a 21-bit binary counter and uses a clock pulse with 1/2 oscillation of the main clock.
- Four interval times can be selected.
- This function cannot be used when the main clock is stopped.

■ Block Diagram

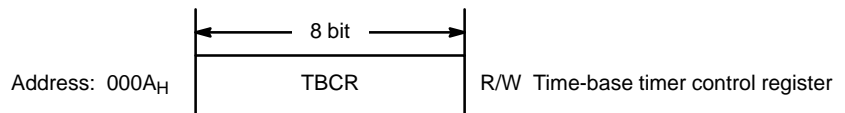


* TBTC is a clock pulse with 1/2 oscillation of the original oscillation.

Fig. 2.36 Time-base Timer Block Diagram

■ Register list

The time-base timer has time-base timer control register (TBCR).



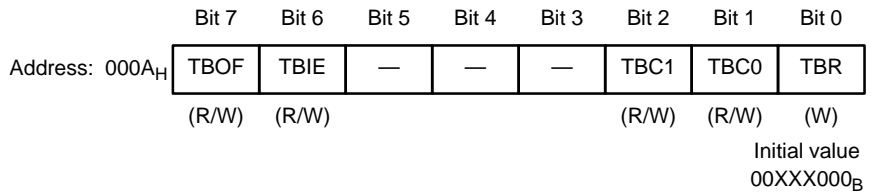
TIME-BASE TIMER

Address: 000A_H TBCR

■ Description of Registers

The detail of time-base timer control register (TBCR) is described below.

(1) Time-base timer control register (TBCR)



[Bit 7] TBOF: Interval timer overflow bit

When writing, this bit is used to clear the interval timer overflow flag.

0	Interval timer overflow flag cleared
1	No operation

When reading, this bit indicates that an interval timer overflow has occurred.

0	Interval timer overflow not occurred
1	Interval timer overflow occurred

1 is read when the Read Modify Write instruction is read. If the TBIF bit is set to 1 when the TBIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 6] TBIE: Interval-timer interrupt enable bit

This bit is used to enable an interrupt by the interval timer.

0	Interval interrupt disabled
1	Interval interrupt enabled

[Bit 2 and 1] TBC1, TBC2: Interval time specification bit

These bits are used to specify interval timer cycle.

TBC1	TBC0	Interval time	Value at $f_{CH} = 3 \text{ MHz}$
0	0	$2^{13}/f_{CH}$	2.73 ms
0	1	$2^{15}/f_{CH}$	10.92 ms
1	0	$2^{18}/f_{CH}$	87.38 ms
1	1	$2^{22}/f_{CH}$	1398.10 ms

f_{CH} : main clock frequency

[Bit 0] TBR: Time-base timer clear bit

This bit is used to clear time-base timer.

0	Time-base timer cleared
1	No operation

1 is always read when this bit is read.

WATCHDOG TIMER RESET

2.14 WATCHDOG TIMER RESET

- Either of a signal output from the time-base timer for counting with the main clock or a signal output from the watch prescaler for counting with the subclock can be selected as a clock.

■ Block Diagram

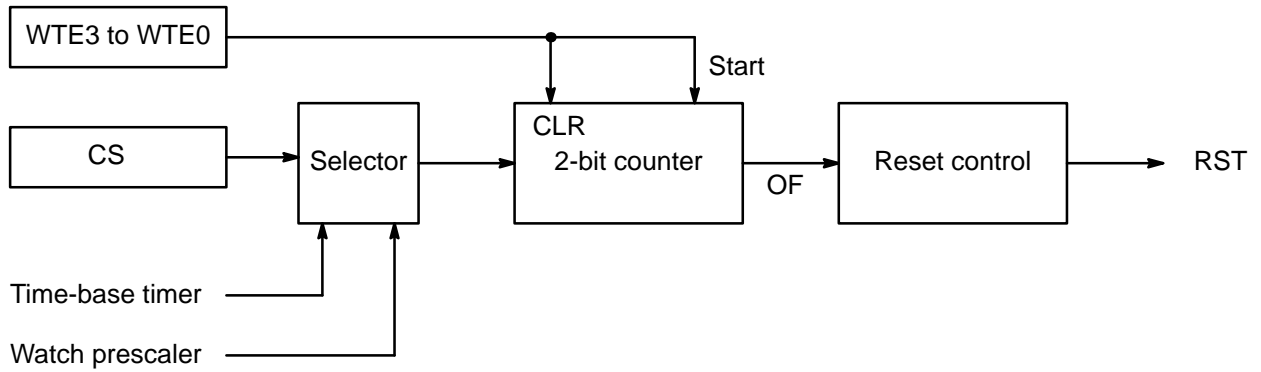
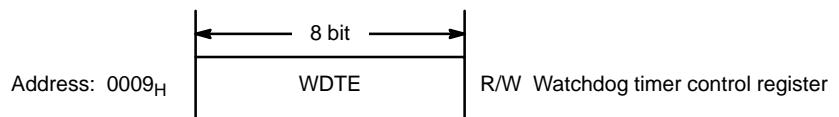


Fig. 2.37 Watchdog Timer Reset Block Diagram

■ Registers

The watchdog timer reset has watchdog timer control register (WDTE).



■ Description of Register

The detail of the watchdog timer control register (WDTE) is described below.

Address: 0009_H **WDTE**

(1) Watchdog timer control register (WDTE)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0009 _H	CS	—	—	—	WTE3	WTE2	WTE1	WTE0
	(R/W)				(W)	(W)	(W)	(W)
								Initial value 0XXXXXX _B

[Bit 7] CS: Clock source switching bit

This bit is used to select a count clock from either the watch prescaler or time-base timer.

0	Time-base timer cycle = $2^{22} / f_{CH}$
1	Watch prescaler cycle = $2^{14} / f_{CL}$

f_{CH} : Main clock frequency
 f_{CL} : Subclock frequency

**WATCHDOG TIMER
RESET**

Set this bit as soon as the watchdog timer is started. Do not change the bit after the timer is started. When using the submode, always select the watch prescaler.

[Bit 3 to Bit 0] WTE3 to WTE0: Watchdog timer control bit
These bits are used to control the watchdog timer.

First write only after reset

0101	Watchdog timer started
Other than the above	No operation

Second and later write

0101	Watchdog timer counter cleared
Other than the above	No operation

The watchdog timer can be stopped only by reset. 1111 is read when these bit are read.

■ Description of operation

The watchdog timer enables detection of a program malfunction.

(1) Starting watchdog timer

The watchdog timer starts when 0101 is written at the watchdog timer control bits.

(2) Clearing watchdog timer

When 0101 is written at the watchdog timer control bits after start, the watchdog timer is cleared. The counter of the watchdog timer is cleared when changing to the standby mode (STOP, SLEEP, WATCH).

(3) Watchdog timer reset

If the watchdog timer is not cleared within the time given in the table below, a watchdog timer reset occurs to reset the chip internally.

	Clock source	
	Time-base timer	Watch prescaler
Minimum time	Approx. 1398.1 ms	Approx. 512 ms
Maximum time	Approx. 2796.2 ms	Approx. 1024 ms

High-speed: 3.58 MHz clock
Low-speed: 32.768 kHz clock

(4) Stopping watchdog timer

Once started, the watchdog timer will not stop until a reset occurs.



3. OPERATION

3.1	CLOCK PULSE GENERATOR	3-3
3.2	RESET	3-4
3.3	INTERRUPT	3-6
3.4	LOW-POWER CONSUMPTION MODES	3-8
3.5	PIN STATES FOR SLEEP, STOP, WATCH AND RESET	3-9

The operation of MB89180 is described below.

3.1 CLOCK PULSE GENERATOR

The MB89180 series of microcontrollers incorporate the system clock pulse generator. The crystal oscillator is connected to the X0 and X1 pins to generate clock pulses. Clock pulses can also be supplied internally by inputting externally-generated clock pulses to the X0 pin. The X1 pin should be kept open.

The X0A and X1A pins are used for the subclock and generates clock pulses by connecting the crystal oscillator to them.

When the single clock module is selected by the option, the X0A pin should be connected to GND and the X1A pin should be kept open.

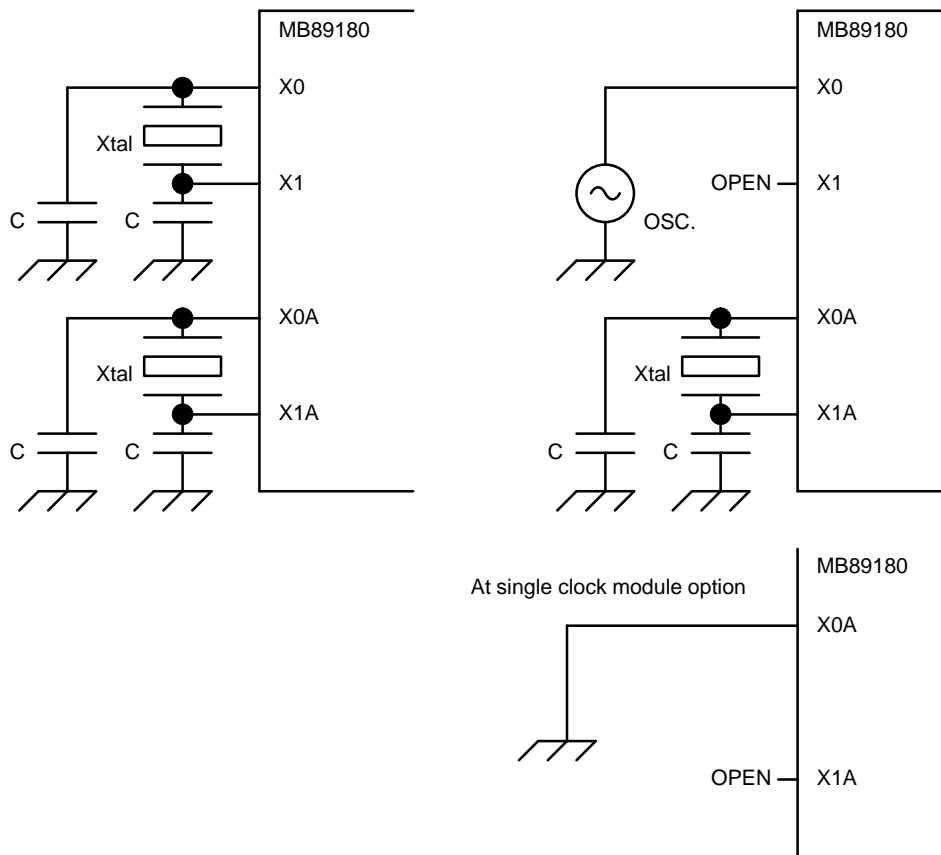


Fig. 3.1 Clock Pulse Generator

3.2 RESET

The detail of reset operation and reset sources are described below.

3.2.1 Reset Operation

When reset conditions occur, the MB89180 series of microcontrollers suspend the currently-executing instruction to enter the reset state. The contents written at the RAM do not change before and after reset. However, if a reset occurs during writing of 16-bit long data, data is written to the upper bytes and may not be written to lower bytes. If a reset occurs around write timing, the contents of the addresses being written are not assured.

When the reset conditions are cleared, the MB89180 series of microcontrollers are released from the reset state and start operation after fetching the mode data from address $FFFD_H$, the upper bytes of the reset vectors from address $FFFE_H$, and the lower bytes from address $FFFF_H$, in that order. Figure 3.2 shows the flow-chart for the reset operation.

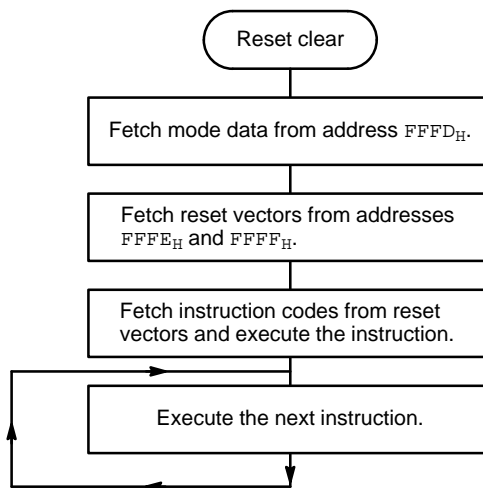
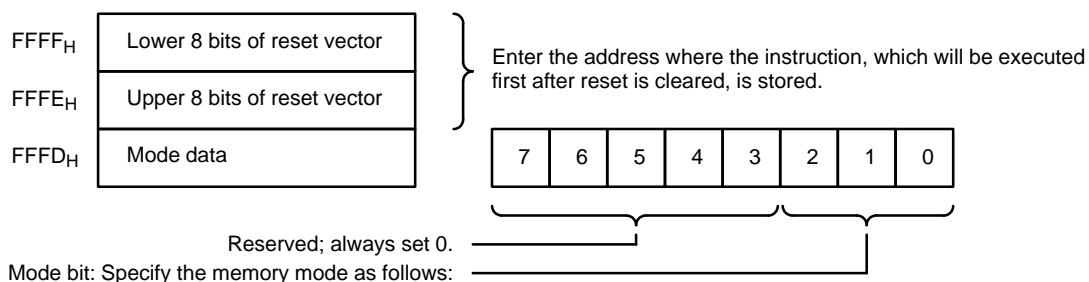


Fig. 3.2 Outline of Reset Operation

Figure 3.3 indicates the structure of data to be stored in addresses $FFFD_H$, $FFFE_H$, and $FFFF_H$.



T2	T1	T0	Operation
0	0	0	External-access disable (single chip)
Other than above			Reserved; do not set.

Fig. 3.3 Reset Vector Structure

3.2.2 Reset Sources

The MB89180 series of microcontrollers have the following reset sources.

- | | |
|-------------------------------|--|
| (1) External pin | A Low level is input to the $\overline{\text{RST}}$ pin. |
| (2) Specification by software | 0 is written at the RST bit of the standby-control register. |
| (3) Power-on | The power is turned on when the power-on reset option is selected. |
| (4) Watchdog function | The watchdog function is enabled by the watchdog-control register and reaccess to this register is not obtained within the specified time. |

When the stop mode is cleared by reset or power-on reset (option selected), operation is started after elapse of the oscillation stabilization time.

For details, see pages 2-16 and 2-17.

3.3 INTERRUPT

If the interrupt controller and CPU are ready to accept interrupts when an interrupt request is output from the internal resources or by an external-interrupt input, the CPU temporarily suspends the currently-executing instruction and executes the interrupt-processing program. Figure 3.4 shows the interrupt-processing flowchart.

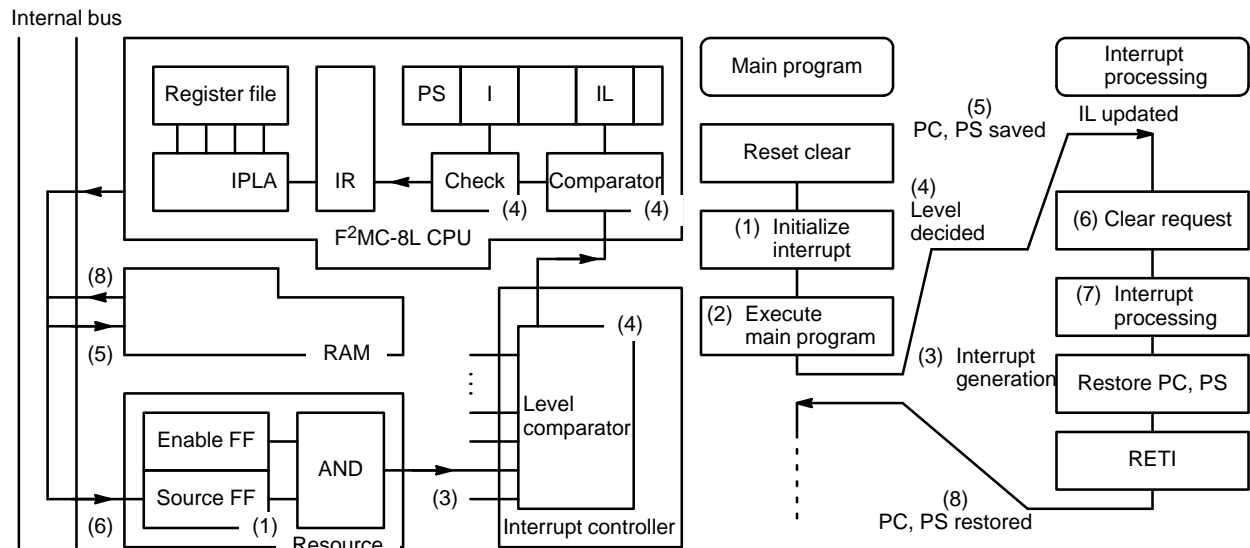


Fig. 3.4 Interrupt-processing Flowchart

All interrupts are disabled after a reset is cleared. Therefore, initialize interrupts in the main program (1). Each resource generating interrupts and the interrupt-level-setting registers (ILR1 to ILR3) in the interrupt controller corresponding to these interrupts are to be initialized. The levels of all interrupts can be set by the interrupt-level-setting registers (ILR1 to ILR3) in the interrupt controller. The interrupt level can be set from 1 to 3, where 1 indicates the highest level, and 2 the second highest level. Level 3 indicates that no interrupt occurs. The interrupt request of this level cannot be accepted. After initializing the registers, the main program executes various controls (2). Interrupts are generated from the resources (3). The highest-priority interrupt requests are identified from those occurring at the same time by the interrupt controller and are transferred to the CPU. The CPU then checks the current interrupt level and the status of the I-flag (4), and starts the interrupt processing.

The CPU performs the interrupt processing to save the contents of the current PC and PS in the stack (5) and fetches the entry addresses of the interrupt program from the interrupt vectors. After updating the IL value in the PS to the required one, the CPU starts executing the interrupt-processing routine.

Clear the interrupt sources (6) and process the interrupts in the user's interrupt-processing routine. Finally, restore the PC and PS values saved by the RETI instruction in the stack (8) to return to the interrupted instruction.

Note: Unlike the F²MC-8 family, A and T are not saved in the stack at the interrupt time.

Table 3-1 lists the relationships between each interrupt source and interrupt vector.

Table 3-1 Interrupt Sources and Interrupt Vectors

Interrupt source	Upper vector address	Lower vector address
IRQ0 (External interrupt 1)	FFFA _H	FFFB _H
IRQ1 (External interrupt 2)	FFF8 _H	FFF9 _H
IRQ2 (16-bit timer counter)	FFF6 _H	FFF7 _H
IRQ3 (8-bit serial I/O)	FFF4 _H	FFF5 _H
IRQ4 (Interval timer)	FFF2 _H	FFF3 _H
IRQ5 (Watch))	FFF0 _H	FFF1 _H

3.4 LOW-POWER CONSUMPTION MODES

The MB89180 series of microcontrollers have three standby modes: sleep, stop, and watch to reduce the power consumption. Writing to the standby control register (STBC) switches to these three standby modes. See 2.2 for setting and releasing each mode.

The MB89180 series of microcontrollers have a double clock module, and the low-power consumption modes vary with the main clock and subclock modes. Whether or not an oscillation stabilization period is required at release from each low-power consumption mode depends on the mask option of the power-on reset (See pages 2-16 and 2-17).

If the single clock module is specified with the mask option, the MB89180 series of microcontrollers can be used as single clocks. If the microcontrollers are used as single clocks without specifying the single clock module with the mask option, once the subclock mode is entered, it cannot be released. Therefore, when using these controllers as a single clock, specify the single clock module with the mask option.

Table 3-2 Low-power Consumption Mode at Each Clock Mode

Function		Note	Main mode			Sub mode			
			RUN	SLEEP	STOP	RUN	SLEEP	STOP	Watch
Main clock		—	Operate	Operate	Stop	Stop	Stop	Stop	Stop
Subclock		—	Operate	Operate	Operate	Operate	Operate	Stop	Operate
CPU	Instruction	—	Operate	Stop	Stop	Operate	Stop	Stop	Stop
	ROM	—	Operate	Hold	Hold	Operate	Hold	Hold	Hold
	RAM	—							
Re-source	I/O	A	Operate	Hold	Hold	Operate	Hold	Hold	Hold
	Watch prescaler	B	Operate	Operate	Operate*1	Operate	Operate	Stop	Operate
	Time-base timer	B	Operate	Operate	Stop	Stop	Stop	Stop	Stop
	16-bit timer	A	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	8-bit SIO	A	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	Remote-control carrier	A	Operate	Operate	Stop	Operate	Operate	Stop	Stop
	LCDC	A	Operate	Operate	Stop	Operate	Operate	Stop	Operate*2
	External interrupt	A	Operate	Operate	Operate	Operate	Operate	Operate	Operate
	Buzzer output	B	Operate	Operate	Operate*2	Operate*2	Operate*2	Stop	Operate*2
	Watchdog timer	B	Operate	Stop	Stop	Operate*2	Stop	Stop	Stop

Notes:

A: Clock mode (main mode or submode) and gear function affect the operation speed or others of resources.

B: Clock mode (main mode or submode) and gear function do not affect the operation speed or others of resources.

*1 Watch prescaler can operate counting but watch interrupt cannot be operated.

*2 When clock source is used as watch prescaler.

3.5 PIN STATES FOR SLEEP, STOP, WATCH AND RESET

The state of each pin of the MB89180 series of microcontrollers at sleep, stop and reset is as follows:

- (1) Sleep The pin state immediately before the sleep state is held.
- (2) Stop The pin state immediately before the stop state is held when the stop mode is started and bit 5 of the standby-control register (STBC) is set to 0; the impedance of the output and input/output pins goes High when the bit is set to 1.
- (3) Reset When the MOD pin is 00, the impedance of all I/O and resource pins (excluding pins for pull-up option) goes High.

For details, see Table 3-3.

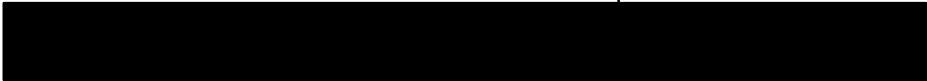
Table 3-3 Pin State of MB89180

Pin name	Normal	Sleep	Stop (Sub) SPL = 0	Stop (Sub) SPL = 1	Reset
P07/INT27 to P00/INT20	Port input/output	Previous state	Previous state	High impedance Resource input	High impedance
P17 to P14*1	Port input/output	Previous state	Previous state	High impedance	High impedance
P13/INT13 to P10/INT10*1	Port input/output	Previous state	Previous state	High impedance Resource input	High impedance
X0, X0A	Input for oscillation	Input for oscillation	High impedance	High impedance	Input for oscillation
X1, X1A	Output for oscillation	Output for oscillation	H output	H output	Output for oscillation
MODA	Mode input	Mode input	Mode input	Mode input	Mode input
RST*2	Reset input	Reset input	Reset input	Reset input	Reset input*2
P27/BUZ	Port output	Previous state	Previous state	High impedance	High impedance
P26	Port output	Previous state	Previous state	High impedance	High impedance
P25/SCK	Port output	Previous state	Previous state	High impedance	High impedance
P24/SO	Port output	Previous state	Previous state	High impedance	High impedance
P23/SI	Port output	Previous state	Previous state	High impedance	High impedance
P22/TO	Port output	Previous state	Previous state	High impedance	High impedance
P21	Port output	Previous state	Previous state	High impedance	High impedance
P20/EC	Port output	Previous state	Previous state	High impedance	High impedance
P32/COM3*3	Port output	Previous state	Previous state	High impedance	High impedance
P31/COM2*3	Port output	Previous state	Previous state	High impedance	High impedance
P30/RCO	Port output	Previous state	Previous state	High impedance	H output
P47 to P40*1	Port output	Previous state	Previous state	High impedance	High impedance
P57 to P50*1	Port output	Previous state	Previous state	High impedance	High impedance
COM0 to COM1	Common output	Previous state	Previous state	Previous state	L output
SEG31 to SEG0	Segment output	Previous state	Previous state	Previous state	L output

*1 If segment output is selected, these pins serve as SEG35 to SEG0.

*2 The reset pin is used as output pin according to the option setting.

*3 When common output is selected, the previous state is held at stop (SPL = 1).



4. INSTRUCTIONS

4.1 TRANSFER INSTRUCTIONS	4-3
4.2 OPERATION INSTRUCTIONS	4-4
4.3 BRANCH INSTRUCTIONS	4-5
4.4 OTHER INSTRUCTIONS	4-5
4.5 F ² MC-8LC FAMILY INSTRUCTION MAP	4-6

4.1 TRANSFER INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	MOV dir,A	3	2	(dir) ← (A)	-	-	-	- - - -	45
2	MOV @IX+off,A	4	2	((IX)+off) ← (A)	-	-	-	- - - -	46
3	MOV ext,A	4	3	(ext) ← (A)	-	-	-	- - - -	61
4	MOV @EP,A	3	1	((EP)) ← (A)	-	-	-	- - - -	47
5	MOV Ri,A	3	1	(Ri) ← (A)	-	-	-	- - - -	48 to 4F
6	MOV A,#d8	2	2	(A) ← d8	AL	-	-	+ + - -	04
7	MOV A,dir	3	2	(A) ← dir	AL	-	-	+ + - -	05
8	MOV A,@IX+off	4	2	(A) ← ((IX)+off)	AL	-	-	+ + - -	06
9	MOV A,ext	4	3	(A) ← (ext)	AL	-	-	+ + - -	60
10	MOV A,@A	3	1	(A) ← ((A))	AL	-	-	+ + - -	92
11	MOV A,@EP	3	1	(A) ← ((EP))	AL	-	-	+ + - -	07
12	MOV A,Ri	3	1	(A) ← (Ri)	AL	-	-	+ + - -	08 to 0F
13	MOV dir,#d8	4	3	(dir) ← d8	-	-	-	- - - -	85
14	MOV @IX+off,#d8	5	3	((IX)+off) ← d8	-	-	-	- - - -	86
15	MOV @EP,#d8	4	2	((EP)) ← d8	-	-	-	- - - -	87
16	MOV Ri,#d8	4	2	(Ri) ← d8	-	-	-	- - - -	88 to 8F
17	MOVW dir,A	4	2	(dir) ← (AH), (dir+1) ← (AL)	-	-	-	- - - -	D5
18	MOVW @IX+off,A	5	2	((IX)+off) ← (AH), ((IX)+off+1) ← (AL)	-	-	-	- - - -	D6
19	MOVW ext,A	5	3	(ext) ← (AH), (ext+1) ← (AL)	-	-	-	- - - -	D4
20	MOVW @EP,A	4	1	((EP)) ← (AH), ((EP)+1) ← (AL)	-	-	-	- - - -	D7
21	MOVW EP,A	2	1	(EP) ← (A)	-	-	-	- - - -	E3
22	MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + - -	E4
23	MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir+1)	AL	AH	dH	+ + - -	C5
24	MOVW A,@IX+off	5	2	(AH) ← ((IX)+off), (AL) ← ((IX)+off+1)	AL	AH	dH	+ + - -	C6
25	MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext+1)	AL	AH	dH	+ + - -	C4
26	MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)+1)	AL	AH	dH	+ + - -	93
27	MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP)+1)	AL	AH	dH	+ + - -	C7
28	MOVW A,EP	2	1	(A) ← (EP)	-	-	dH	- - - -	F3
29	MOVW EP,#d16	3	3	(EP) ← d16	-	-	-	- - - -	E7
30	MOVW IX,A	2	1	(IX) ← (A)	-	-	-	- - - -	E2
31	MOVW A,IX	2	1	(A) ← (IX)	-	-	dH	- - - -	F2
32	MOVW SP,A	2	1	(SP) ← (A)	-	-	-	- - - -	E1
33	MOVW A,SP	2	1	(A) ← (SP)	-	-	dH	- - - -	F1
34	MOV @A,T	3	1	((A)) ← (T)	-	-	-	- - - -	82
35	MOVW @A,T	4	1	((A)) ← (TH), ((A)+1) ← (TL)	-	-	-	- - - -	83
36	MOVW IX,#d16	3	3	(IX) ← d16	-	-	-	- - - -	E6
37	MOVW A,PS	2	1	(A) ← (PS)	-	-	dH	- - - -	70
38	MOVW PS,A	2	1	(PS) ← (A)	-	-	-	+ + + +	71
39	MOVW SP,#d16	3	3	(SP) ← d16	-	-	-	- - - -	E5
40	SWAP	2	1	(AH) ↔ (AL)	-	-	AL	- - - -	10
41	SETB dir:n	4	2	(dir):n ← 1	-	-	-	- - - -	A8 to AF
42	CLRB dir:n	4	2	(dir):n ← 0	-	-	-	- - - -	A0 to A7
43	XCH A,T	2	1	(AL) ↔ (TL)	AL	-	-	- - - -	42
44	XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	- - - -	43
45	XCHW A,EP	3	1	(A) ↔ (EP)	-	-	dH	- - - -	F7
46	XCHW A,IX	3	1	(A) ↔ (IX)	-	-	dH	- - - -	F6
47	XCHW A,SP	3	1	(A) ↔ (SP)	-	-	dH	- - - -	F5
48	MOVW A,PC	2	1	(A) ← (PC)	-	-	dH	- - - -	F0

Notes

1. In byte transfer to A, T ← A is only for low bytes.
2. Operands for two or more operand instructions should be stored in the order designated in MNEMONIC (Opposite order to F²MC-8 family).

4.2 OPERATION INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	ADDC A,Ri	3	1	(A) ← (A)+(Ri)+C	-	-	-	+++ +	28 to 2F
2	ADDC A,#d8	2	2	(A) ← (A)+d8+C	-	-	-	+++ +	24
3	ADDC A,dir	3	2	(A) ← (A)+(dir)+C	-	-	-	+++ +	25
4	ADDC A,@IX+off	4	2	(A) ← (A)+((IX)+off)+C	-	-	-	+++ +	26
5	ADDC A,@EP	3	1	(A) ← (A)+((EP))+C	-	-	-	+++ +	27
6	ADDCW A	3	1	(A) ← (A)+(T)+C	-	-	dH	+++ +	23
7	ADDC A	2	1	(AL)←(AL)+(TL)+C	-	-	-	+++ +	22
8	SUBC A,Ri	3	1	(A) ← (A)-(Ri)-C	-	-	-	+++ +	38 to 3F
9	SUBC A,#d8	2	2	(A) ← (A)-d8-C	-	-	-	+++ +	34
10	SUBC A,dir	3	2	(A) ← (A)-(dir)-C	-	-	-	+++ +	35
11	SUBC A,@IX+off	4	2	(A) ← (A)-((IX)+off)-C	-	-	-	+++ +	36
12	SUBC A,@EP	3	1	(A) ← (A)-((EP))+C	-	-	-	+++ +	37
13	SUBCW A	3	1	(A) ← (T)-(A)-C	-	-	dH	+++ +	33
14	SUBC A	2	1	(AL)←(TL)-(AL)-C	-	-	-	+++ +	32
15	INC Ri	4	1	(Ri)←(Ri)+1	-	-	-	+++ -	C8 to CF
16	INCW EP	3	1	(EP)←(EP)+1	-	-	-	--- -	C3
17	INCW IX	3	1	(IX)←(IX)+1	-	-	-	--- -	C2
18	INCW A	3	1	(A) ← (A)+1	-	-	dH	+++ -	C0
19	DEC Ri	4	1	(Ri)←(Ri)-1	-	-	-	+++ -	D8 to DF
20	DECW EP	3	1	(EP)←(EP)-1	-	-	-	--- -	D3
21	DECW IX	3	1	(IX)←(IX)-1	-	-	-	--- -	D2
22	DECW A	3	1	(A) ← (A)-1	-	-	dH	+++ -	D0
23	MULU A	19	1	(A) ← (AL)*(TL)	-	-	dH	--- -	01
24	DIVU A	21	1	(A) ← (T)/(AL), MOD→(T)	dL	00	00	--- -	11
25	ANDW A	3	1	(A) ← (A) ∩ (T)	-	-	dH	++R -	63
26	ORW A	3	1	(A) ← (A) ∪ (T)	-	-	dH	++R -	73
27	XORW A	3	1	(A) ← (A) ⊕ (T)	-	-	dH	++R -	53
28	CMP A	2	1	(TL)-(AL)	-	-	-	+++ +	12
29	CMPW A	3	1	(T)-(A)	-	-	-	+++ +	13
30	RORC A	2	1		-	-	-	++- +	03
31	ROLC A	2	1		-	-	-	++- +	02
32	CMP A,#d8	2	2	(A)-d8	-	-	-	+++ +	14
33	CMP A,dir	3	2	(A)-dir	-	-	-	+++ +	15
34	CMP A,@EP	3	1	(A)-((EP))	-	-	-	+++ +	17
35	CMP A,@IX+off	4	2	(A)-((IX)+off)	-	-	-	+++ +	16
36	CMP A,Ri	3	1	(A)-(Ri)	-	-	-	+++ +	18 to 1F
37	DAA	2	1	decimal adjust for addition	-	-	-	+++ +	84
38	DAS	2	1	decimal adjust for subtraction	-	-	-	+++ +	94
39	XOR A	2	1	(A) ← (AL) ⊕ (TL)	-	-	-	++R -	52
40	XOR A,#d8	2	2	(A) ← (AL) ⊕ d8	-	-	-	++R -	54
41	XOR A,dir	3	2	(A) ← (AL) ⊕ (dir)	-	-	-	++R -	55
42	XOR A,@EP	3	1	(A) ← (AL) ⊕ ((EP))	-	-	-	++R -	57
43	XOR A,@IX+off	4	2	(A) ← (AL) ⊕ ((IX)+off)	-	-	-	++R -	56
44	XOR A,Ri	3	1	(A) ← (AL) ⊕ (Ri)	-	-	-	++R -	58 to 5F
45	AND A	2	1	(A) ← (AL) ∩ (TL)	-	-	-	++R -	62
46	AND A,#d8	2	2	(A) ← (AL) ∩ d8	-	-	-	++R -	64
47	AND A,dir	3	2	(A) ← (AL) ∩ (dir)	-	-	-	++R -	65
48	AND A,@EP	3	1	(A) ← (AL) ∩ ((EP))	-	-	-	++R -	67
49	AND A,@IX+off	4	2	(A) ← (AL) ∩ ((IX)+off)	-	-	-	++R -	66
50	AND A,Ri	3	1	(A) ← (AL) ∩ (Ri)	-	-	-	++R -	68 to 6F
51	OR A	2	1	(A) ← (AL) ∪ (TL)	-	-	-	++R -	72
52	OR A,#d8	2	2	(A) ← (AL) ∪ d8	-	-	-	++R -	74
53	OR A,dir	3	2	(A) ← (AL) ∪ (dir)	-	-	-	++R -	75
54	OR A,@EP	3	1	(A) ← (AL) ∪ ((EP))	-	-	-	++R -	77
55	OR A,@IX+off	4	2	(A) ← (AL) ∪ ((IX)+off)	-	-	-	++R -	76
56	OR A,Ri	3	1	(A) ← (AL) ∪ (Ri)	-	-	-	++R -	78 to 7F
57	CMP dir,#d8	5	3	(dir) - d8	-	-	-	+++ +	95
58	CMP @EP,#d8	4	2	((EP)) - d8	-	-	-	+++ +	97
59	CMP @IX+off,#d8	5	3	((IX)+off) - d8	-	-	-	+++ +	96
60	CMP Ri,#d8	4	2	(Ri) - d8	-	-	-	+++ +	98 to 9F
61	INCW SP	3	1	(SP)←(SP) + 1	-	-	-	--- -	C1
62	DECW SP	3	1	(SP)←(SP) - 1	-	-	-	--- -	D1

4.3 BRANCH INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	BZ/BEQ rel	3	2	if Z=1 then PC ← PC+rel	-	-	-	- - - -	FD
2	BNZ/BNE rel	3	2	if Z=0 then PC ← PC+rel	-	-	-	- - - -	FC
3	BC/BLO rel	3	2	if C=1 then PC ← PC+rel	-	-	-	- - - -	F9
4	BNC/BHS rel	3	2	if C=0 then PC ← PC+rel	-	-	-	- - - -	F8
5	BN rel	3	2	if N=1 then PC ← PC+rel	-	-	-	- - - -	FB
6	BP rel	3	2	if N=0 then PC ← PC+rel	-	-	-	- - - -	FA
7	BLT rel	3	2	if V⊕N=1 then PC ← PC+rel	-	-	-	- - - -	FF
8	BGE rel	3	2	if V⊕N=0 then PC ← PC+rel	-	-	-	- - - -	FE
9	BBC dir:b,rel	5	3	if (dir:b)=0 then PC ← PC+rel	-	-	-	- + - -	B0 to B7
10	BBS dir:b,rel	5	3	if (dir:b)=1 then PC ← PC+rel	-	-	-	- + - -	B8 to BF
11	JMP @A	2	1	(PC) ← (A)	-	-	-	- - - -	E0
12	JMP ext	3	3	(PC) ← ext	-	-	-	- - - -	21
13	CALLV #vct	6	1	vector call	-	-	-	- - - -	E8 to EF
14	CALL ext	6	3	subroutine call	-	-	-	- - - -	31
15	XCHW A,PC	3	1	(PC) ← (A), (A) ← (PC)+1	-	-	dH	- - - -	F4
16	RET	4	1	return from subroutine	-	-	-	- - - -	20
17	RETI	6	1	return from interrupt	-	-	-	restore	30

4.4 OTHER INSTRUCTIONS

NO	MNEMONIC	~	#	OPERATION	TL	TH	AH	N Z V C	OP CODE
1	PUSHW A	4	1	SP ← SP-2 (SP) ← A	-	-	-	- - - -	40
2	POPW A	4	1	A ← (SP) SP ← SP + 2	-	-	dH	- - - -	50
3	PUSHW IX	4	1	SP ← SP-2 (SP) ← IX	-	-	-	- - - -	41
4	POPW IX	4	1	IX ← (SP) SP ← SP + 2	-	-	-	- - - -	51
5	NOP	1	1	NO OPERATION	-	-	-	- - - -	00
6	CLRC	1	1	C ← 0	-	-	-	- - - R	81
7	SETC	1	1	C ← 1	-	-	-	- - - S	91
8	CLRI	1	1	I ← 0	-	-	-	- - - -	80
9	SETI	1	1	I ← 1	-	-	-	- - - -	90

4.5 F²MC-8LC FAMILY INSTRUCTION MAP

L H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RETI	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir :0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr:16	CALL addr:16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir :1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir :2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir:3	BBC dir :3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#dB		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir :4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir :5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:6	BBC dir :6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:7	BBC dir :7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir :0,rel	INCW R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir :1,rel	INCW R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir :2,rel	INCW R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir :3,rel	INCW R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir :4,rel	INCW R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir :5,rel	INCW R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir :6,rel	INCW R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir :7,rel	INCW R7	DEC R7	CALLV #7	BLT rel



5. MASK OPTIONS

Table 5-1 Mask Options

NO	Type	MB8918X	MB89P185	MB89PV180
	Specification method	Select when ordering mask	Set by EPROM writer	Cannot be set
1	Pull-up resistor P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57 selected	Can be selected for each pin. (However, P10 to P17, P40 to P47 and P50 to P57 are specified only when segment output is not selected)	P00 to P07 and P10 to P17 can be selected for each pin (However, P10 to P17 are specified only when segment output is not selected. Only P40 to P27, P50 to P57 and P20 to P27 do not have pull-up resistor)	Pull-up resistor not provided
2	Power-on reset { Power-on reset available Power-on reset not available	Can be selected	Can be set	Power-on reset available
3	Oscillation stabilization time • Initial value of oscillation stabilization time of main clock can be set by selecting the values of WTM1 and WTM0 shown in the light columns	Can be selected WTM1 WTM0 0 0 : 2 ² /f 0 1 : 2 ¹² /f 1 0 : 2 ¹⁶ /f 1 1 : 2 ¹⁸ /f	Can be set WTM1 WTM0 0 0 : 2 ² /f 0 1 : 2 ¹² /f 1 0 : 2 ¹⁶ /f 1 1 : 2 ¹⁸ /f	Oscillation stabilization: 2 ¹⁶ /f
4	Types of main clock oscillation { Crystal or ceramic oscillator CR	Can be selected	Can be set	Reset output available
5	Reset pin output { Double clock mode Single clock mode	Can be selected	Can be set	Double clock mode
6	Clock mode selection { Double clock mode Single clock mode	Can be selected	Can be set	Double clock mode
7	Segment output switching selection 32: Port unselected 28: P17 to P14 selected 24: P17 to P10 selected 20: P17 to 10, P57 to P54 selected 16: P17 to P10, P57 to P50 selected 12: P17 to P10, P57 to 50, P47 to 44 selected 8: P17 to P10, P57 to P50, P47 to P40 selected	Selectable Select by number of segments		-101: 32 -102: 28 -103: 24 -104: 20 -105: 16 -106: 12 -107: 8

Table 5-2 Configuration of Product Series

Version			Selected content
Product series	Temporary product	Piggyback/evaluation	Number of segments
MB8918X	MB89P185-101	MB89PV180-101	32
	MB89P185-102	MB89PV180-102	28
	MB89P185-103	MB89PV180-103	24
	MB89P185-104	MB89PV180-104	20
	MB89P185-105	MB89PV180-105	16
	MB89P185-106	MB89PV180-106	12
	MB89P185-107	MB89PV180-107	8



APPENDIX

APPENDIX A I/O MAP

Addresses 00_H to 17_H

Address	Read/Write	Register	Description of register
00 _H	(R/W)	PDR0	Port 00 to 07 data register
01 _H	(W)	DDR0	Port 00 to 07 data direction register
02 _H	(R/W)	PDR1	Port 10 to 17 data register
03 _H	(W)	DDR1	Port 10 to 17 data direction register
04 _H	(R/W)	PDR2	Port 20 to 27 data register
05 _H	(W)	DDR2	Port 20 to 27 data direction register
06 _H	—	—	—
07 _H	(R/W)	SYCC	System clock control register
08 _H	(R/W)	STBC	Standby control register
09 _H	(R/W)	WDTC	Watchdog timer control register
0A _H	(R/W)	TBTC	Time-base timer control register
0B _H	(R/W)	WPCR	Watch prescaler control register
0C _H	(R/W)	PDR3	Port 30 to 37 data register
0D _H	—	—	—
0E _H	(R/W)	PDR4	Port 40 to 44 data register
0F _H	(R/W)	PDR5	Port 50 to 51 data register
10 _H	(R/W)	BZCR	Buzzer register
11 _H	—	—	—
12 _H	—	—	—
13 _H	—	—	—
14 _H	(R/W)	RCR1	Remote-control register 1
15 _H	(R/W)	RCR2	Remote-control register 2
16 _H	—	—	—
17 _H	—	—	—

Address 18_H to 7F_H

Address	Read/Write	Register	Description of register
18 _H	(R/W)	T2CR	Timer 2 control register
19 _H	(R/W)	T1CR	Timer 1 control register
1A _H	(R/W)	T2DR	Timer 2 data register
1B _H	(R/W)	T1DR	Timer 1 data register
1C _H	(R/W)	SMR1	Serial mode register
1D _H	(R/W)	SDR1	Serial data register
1E _H to 2F _H	—	—	—
30 _H	(R/W)	EIE1	External interrupt 1 control register 1
31 _H	(R/W)	EIF1	External interrupt 1 flag register 1
32 _H	(R/W)	EIE2	External interrupt 2 control register 2
33 _H	(R/W)	EIF2	External interrupt 2 flag register 2
34 _H to 5F _H	—	—	—
60 _H to 6F _H	(R/W)	VRAM	RAM displaying data
72 _H	(R/W)	LCR1	LCDC control register 1
73 _H to 7B _H	—	—	—
7C _H	(W)	ILR1	Interrupt level setting register 1
7D _H	(W)	ILR2	Interrupt level setting register 2
7E _H	(W)	ILR3	Interrupt level setting register 3
7F _H	Access disable	ITR	Interrupt test register

APPENDIX B EPROM SETTING FOR MB89P155

MB89P185 is provided with the function corresponding to MBM27C256A by EPROM setting. The setting can be performed by writing program data with general-purpose EPROM writer through adaptor for exclusive use. (The electro-signature mode cannot be used.)

- Setting

(1) Set the EPROM writer to MBM27C256A.

(2) Load the program data from address 4000_H to address $7FFF_H$ of EPROM writer.

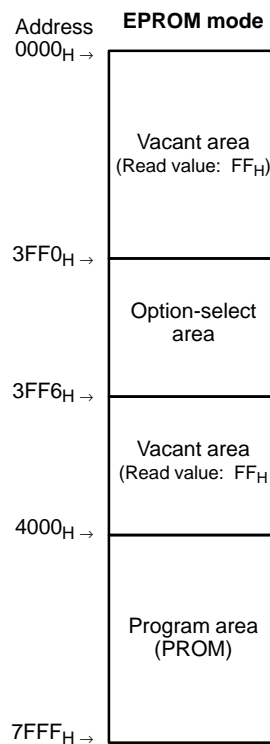
(The data is loaded from address 8000_H to address $0FFFF_H$ in the operation mode, and from address 4000_H to address $7FFF_H$ in the EPROM mode.)

Load the option information from address $3FF0_H$ to address $3FF6_H$ of the EPROM writer.

(For the correspondence between the addresses and options, see the Bit Map on the next page.)

(3) Write the data with the EPROM writer.

The memory space in the EPROM mode is as follows:



• Bit Map for PROM Option

	7	6	5	4	3	2	1	0
3FF0 _H	Empty Readable	Empty Readable	Oscillation stabilization time		Empty Readable	Reset pin output	Clock mode selection	Power-on reset
			WTM1	WTM2				
			See Mask option List					
3FF1 _H	P07 Pull-up register 1:Unavailable 0:Available	P06 Pull-up register 1:Unavailable 0:Available	P05 Pull-up register 1:Unavailable 0:Available	P04 Pull-up register 1:Unavailable 0:Available	P03 Pull-up register 1:Unavailable 0:Available	P02 Pull-up register 1:Unavailable 0:Available	P01 Pull-up register 1:Unavailable 0:Available	P00 Pull-up register 1:Unavailable 0:Available
	3FF2 _H	P17 Pull-up register 1:Unavailable 0:Available	P16 Pull-up register 1:Unavailable 0:Available	P15 Pull-up register 1:Unavailable 0:Available	P14 Pull-up register 1:Unavailable 0:Available	P13 Pull-up register 1:Unavailable 0:Available	P12 Pull-up register 1:Unavailable 0:Available	P11 Pull-up register 1:Unavailable 0:Available
3FF3 _H	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable
3FF4 _H	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable
3FF5 _H	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable	Empty Readable
3FF6 _H	Empty Not readable	Empty Not readable	Empty Not readable	Empty Not readable	Empty Not readable	Empty Not readable	Empty Not readable	Empty Not readable

Notes:

1. The initial value of each bit is 1.
2. Do not set 0 at empty bits.
The read value of each empty bit is 1 unless 0 is set.
3. The address 3FF6_H cannot be read. Do not access it.

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