FUJITSU SEMICONDUCTOR
MICROCONTROLLER MANUAL

CM25–10118–1E

F²MC-8L FAMILY MICROCONTROLLERS

MB89610 SERIES

HARDWARE MANUAL

FUJITSU

F^{2}MC-8L FAMILY
MICROCONTROLLERS

MB89610 SERIES
HARDWARE MANUAL

Edition 1.0 January 1995

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■ PREFACE

The MB89610 series of microcontrollers are application-specific integrated circuits. They are general-purpose and high-speed products in the F^{2}MC-8L Family series of 8-bit single-chip microcontrollers operating at low voltages.

This manual covers the functions and operations of the MB89610 series of microcontrollers. Refer to the *F^{2}MC-8L Family Software Manual* for instructions.

Table of Contents

Figures

Tables

1. INTRODUCTION

The MB89610 series of single-chip microcontrollers use the F^{2}MC-8L CPU core for high-speed processing even at low voltages.

They contain resources such as timers, serial interfaces, and an external-interrupt input; they can be used widely in civil and industrial equipment, including portable equipment.

1.1 FEATURES

- Various package options
  - Four types of QFP package (0.5-mm, 0.65-mm, and 1-mm pitch)
  - SDIP package

- High-speed processing even at low voltages
  Minimum instruction execution time: 0.4 µs at 3.5 V, 0.8 µs at 2.7 V

- F^{2}MC-8L CPU core
  Instruction system most suited to controller
  - Multiplication and division instructions
  - 16-bit arithmetic operation
  - Instruction test and branch instruction
  - Bit manipulation instruction, etc.

- Four types of timers
  - 8-bit PWM timer (usable as both reload timer and PWM timer)
  - 8-bit pulse-width count timer (applicable to remote control)
  - 16-bit timer/counter
  - 20-bit time-based timer

- Two serial interfaces
  The transfer direction can be selected to communicate with various equipment.

- External-interrupt input
  - Four channels
  - Four channels can be used independently to cancel the low-power consumption modes.
  - An edge-detection function is provided.

- Low-power consumption modes
  - Stop mode (Oscillation stops to minimize the current consumption.)
  - Sleep mode (The CPU stops to reduce current consumption to about 30% of normal.)

- Bus interface
  Supports hold and ready functions

1.2 PRODUCT SERIES

Table 1-1 lists the types and functions of the MB89610 series of microcontrollers.

Table 1-1 Types and Functions of MB89610 Series of Microcontrollers

Model Name	MB89613	MB89615	MB89P625/W625*1	MB89PV620*1
Classification	Mass-produced product (Mask ROM product)		One-time programmable products/EPROMs	Piggy back/Evaluation and development
ROM capacity	8K × 8 bits (Internal ROM)	16K × 8 bits (Internal ROM)	16K × 8 bits (Internal PROM, writable by general-purpose writers)	32K × 8 bits (External ROM)
RAM capacity	256 × 8 bits	512 × 8 bits	512 × 8 bits	1K × 8 bits
CPU function	Number of basic instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum instruction execution time: 0.4 µs at 10 MHz Interrupt processing time: 3.6 µs at 10 MHz			
Port	Input port: 5 (4 used as resources) Output port (N-ch open drain): 8 I/O port (N-ch open drain): 8 (4 used as resources) Output port (CMOS): 8 (8 used as bus-control pins) I/O port (CMOS): 24 (24 used as both bus pins and resources) Total: 53			
PWM timer	8-bit reload timer operation (toggle output possible, count clock cycle: 0.4 µs to 3.3 ms) 8-bit resolution PWM operation (conversion cycle: 10 µs to 839 ms)			
Pulse-width count timer	8-bit timer operation (overflow output possible, count clock cycle: 0.4 µs to 12.8 µs) 8-bit reload timer operation (toggle output possible, operating clock cycle: 0.4 µs to 12.8 µs) 8-bit pulse-width measurement (continuous measurement possible: High and Low widths, and from ↑ to ↑ and from ↓ to ↓)			
Timer/counter	16-bit timer operation (count clock cycle: 0.4 µs) 16-bit event counter operation (selectable from rising edge, falling edge, or both edges)			
Serial I/O 1 Serial I/O 2	8-bit length Selectable from least significant bit (LSB) first or most significant bit (MSB) first Transfer clock (external, 0.8 µs, 3.2 µs, 12.8 µs)			
External-interrupt input	Four independent channels (edge selection, interrupt vector, interrupt source flag) Selectable from rising or falling edge Used for clearing stop or sleep mode (The edge can be detected even in the stop mode.)			
Standby mode	Sleep mode and stop mode			
Process	CMOS			
Operating voltage*2	2.2 V to 6.0 V		2.7 V to 6.0 V	2.7 V to 6.0 V
EPROM used				MBM27C256A-20

*1: One-time programmable products, EPROM products, and piggy-back/evaluation chip are common with the MB89620 series.

*2: Varies according to conditions such as frequency (see Electrical Characteristics). The operating voltage of the MB89PV620 differs depending on connected ICE or EPROM.

1.3 BLOCK DIAGRAM

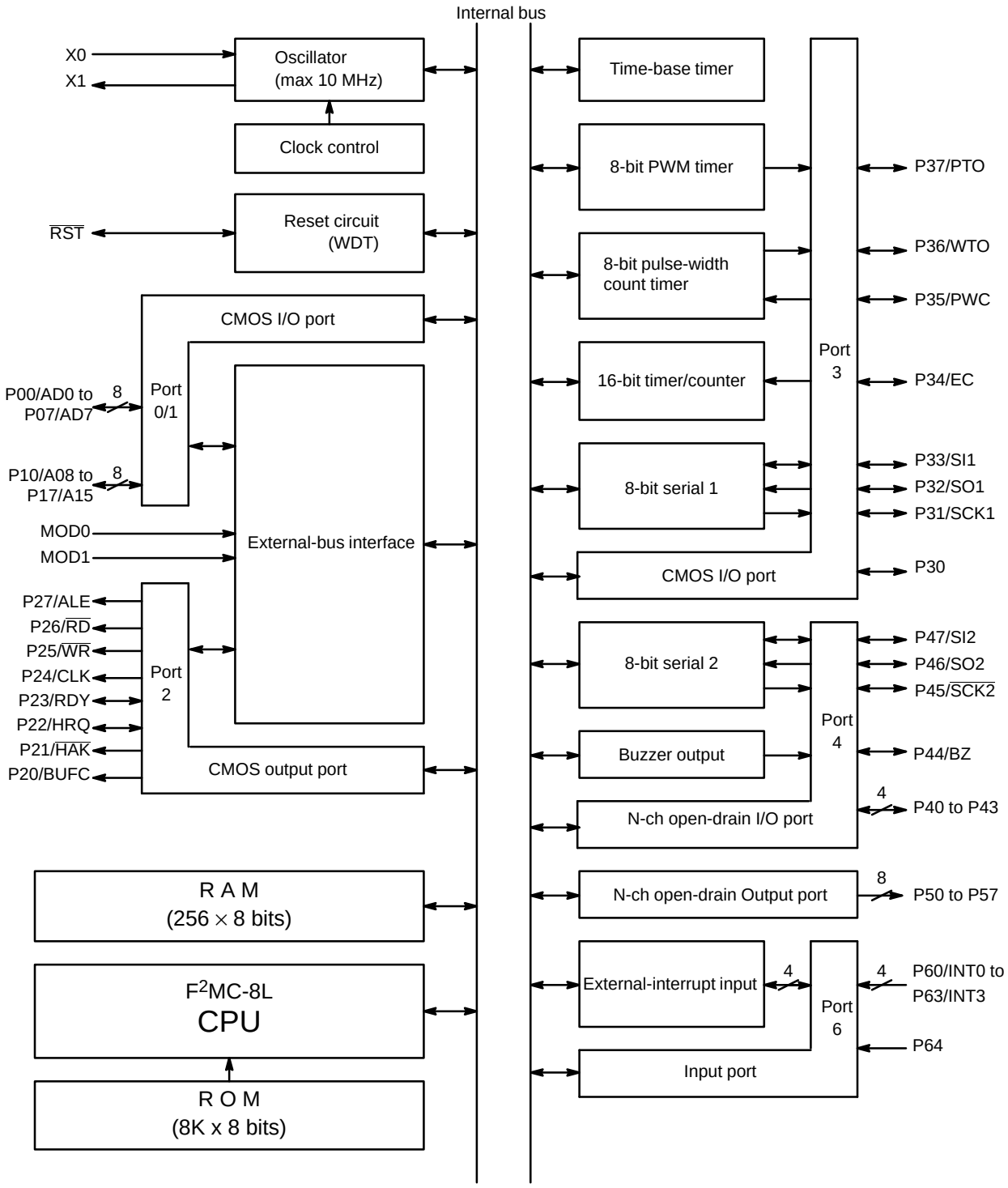


Fig. 1.1 Block Diagram

1.4 PIN ASSIGNMENT

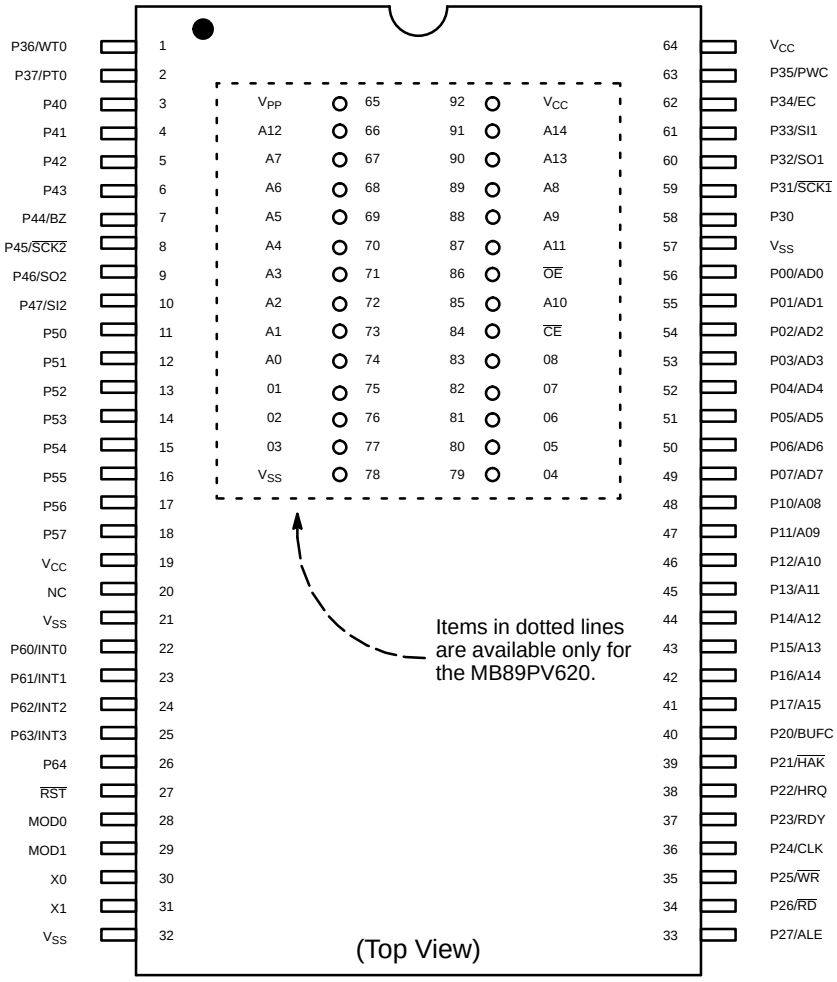


Fig. 1.2 Pin Assignment (DIP-64P-M01 and MDP-64C-P02)

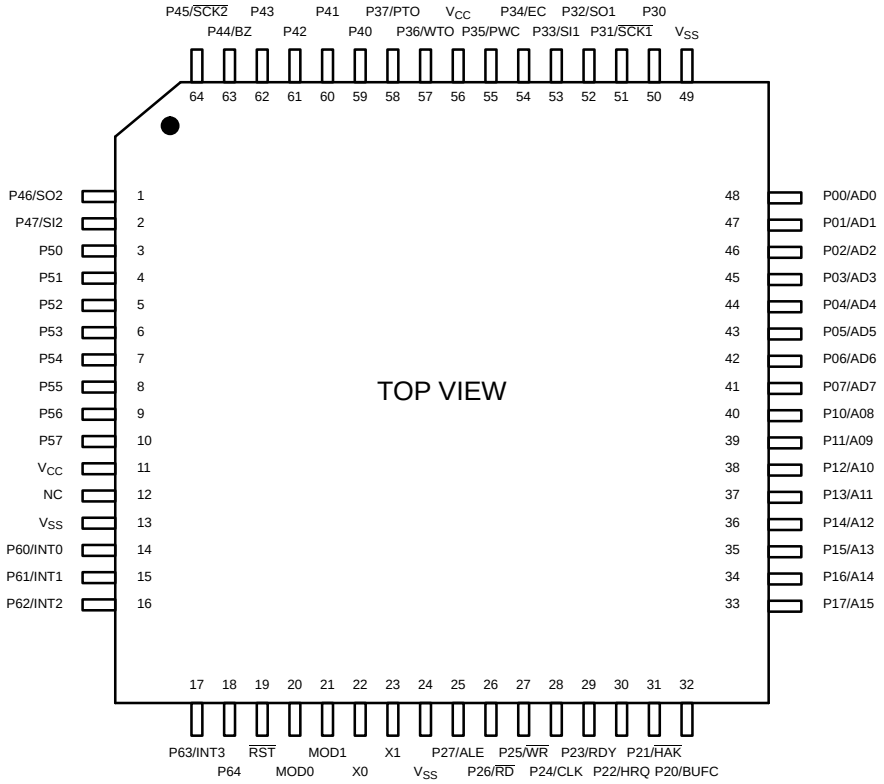
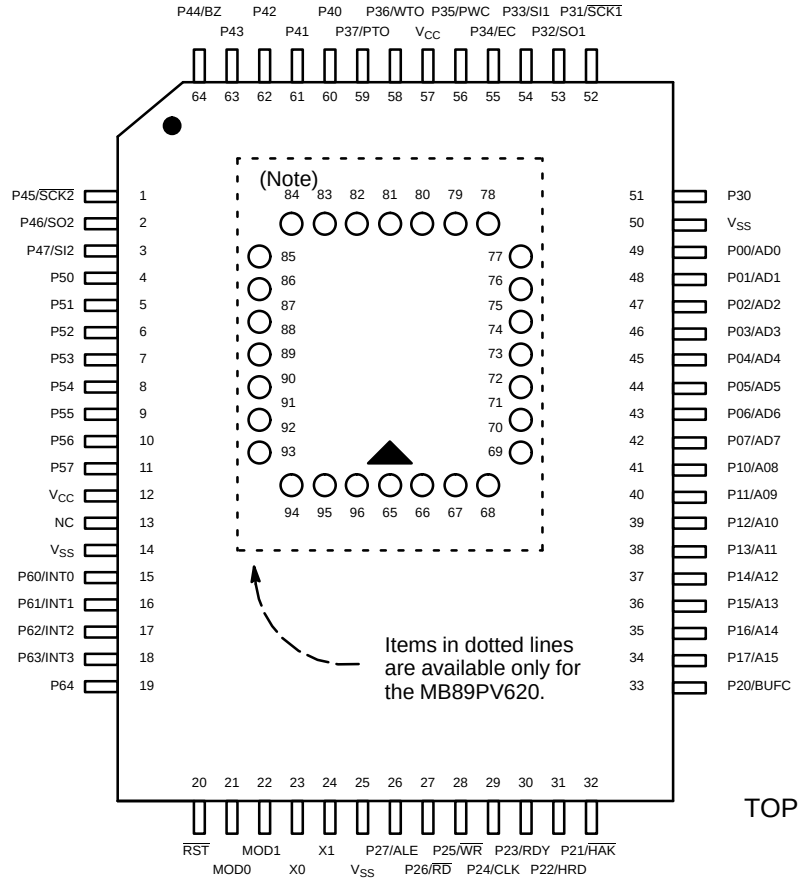


Fig. 1.3 Pin Assignment (FPT-64P-M03 and FPT-64P-M09)



Note: Pin assignment on top of package (only for piggyback/evaluation type)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
65	NC	73	A2	81	N.C.	89	$\overline{0E}$
66	V_{PP}	74	A1	82	04	90	NC
67	A12	75	A0	83	05	91	A11
68	A7	76	N.C.	84	06	92	A9
69	A6	77	01	85	07	93	A8
70	A5	78	02	86	08	94	A13
71	A4	79	03	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

Note: NC (No connection): Always open because internal connection is made

Fig. 1.4 Pin Assignment (FPT-64P-M06 and MQP-64C-P01)

1.5 PIN DESCRIPTION

Table 1-2 lists the pin functions and Figure 1.5 shows the input/output circuits.

Table 1-2 Pin Description

Pin No.			Pin Name	Circuit type	Function
DIP-64P-M01	FPT-64P-M06	FPT-64P-M03/M09			
30	23	22	X0	A	**Crystal oscillator pins**
31	24	23	X1		
28	21	20	MOD0	B	**Operation-mode select pins** These pins are connected directly to V_{CC} or V_{SS}.
29	22	21	MOD1		
27	20	19	$\overline{RST}$	C	**Reset I/O pin** This pin consists of an N-ch open-drain output with a pull-up resistor and hysteresis input. A Low level is output from this pin. The internal circuit is initialized at input of a Low level.
56 to 49	49 to 42	48 to 41	P00/AD0 to P07/AD7	D	**General-purpose I/O ports** When the external bus is used, these ports also serve as multiplex pins for output of lower addresses or input and output of data.
48 to 41	41 to 34	40 to 33	P10/A08 to P17/A15	D	**General-purpose I/O ports** When the external bus is used, these ports also serve as pins for output of upper addresses.
40	33	32	P20/BUFC	F	**General-purpose output-only port** When the external bus is used, this port also serves as a buffer-control output pin by setting BCTR.
39	32	31	P21/$\overline{HAK}$	F	**General-purpose output-only port** When the external bus is used, this port also serves as a hold-acknowledge pin by setting BCTR.
38	31	30	P22/HRQ	D	**General-purpose output-only port** When the external bus is used, this port also serves as a hold-request input pin by setting BCTR.
37	30	29	P23/RDY	D	**General-purpose output-only port** When the external bus is used, this port also serves as a ready-input
36	29	28	P24/CLK	F	**General-purpose output-only port** When the external bus is used, this port also serves as a clock-output pin.
35	28	27	P25/$\overline{WR}$	F	**General-purpose output-only port** When the external bus is used, this port also serves as a write-signal output pin.
34	27	26	P26/$\overline{RD}$	F	**General-purpose output-only port** When the external bus is used, this port also serves as a read-signal output pin.
33	26	25	P27/ALE	F	**General-purpose output-only port** When the external bus is used, this port also serves as an address-latch signal- output pin.
58	51	50	P30	E	**General-purpose I/O port** Input is hysteresis type.
59	52	51	P31/$\overline{SCK1}$	E	**General-purpose I/O port** This port also serves as a clock I/O pin for serial I/O 1. Input is hysteresis type.

Table 1-2 Pin Description (*Continued*)

Pin No.			Pin Name	Circuit type	Function
DIP-64P-M01	FPT-64P-M06	FPT-64P-M03/M09			
60	53	52	P32/SO1	E	**General-purpose I/O port** This port also serves as a data-output pin for serial I/O 1. Input is hysteresis type.
61	54	53	P33/SI1	E	**General-purpose I/O port** This port also serves as a data-input pin for serial I/O 1. Input is hysteresis type.
62	55	54	P34/EC	E	**General-purpose I/O port** This port also serves as an external-clock input pin for the 16-bit timer/counter. Input is hysteresis type.
63	56	55	P35/PWC	E	**General-purpose I/O port** This port also serves as a measured-pulse input pin for the 8-bit pulse-width counter. Input is hysteresis type.
1	58	57	P36/WTO	E	**General-purpose I/O port** This port also serves as a toggle output pin for the 8-bit pulse-width counter. Input is hysteresis type.
2	59	58	P37/PTO	E	**General-purpose I/O port** This port also serves as a toggle output pin for the 8–bit PWM timer. Input is hysteresis type.
3 to 6	60 to 63	59 to 62	P40 to P43	G	**N-ch open-drain I/O ports** Input is hysteresis type.
7	64	63	P44/BZ	G	**N-ch open-drain I/O port** This port also serves as the buzzer output pin. Input is hysteresis type.
8	1	64	P45/$\overline{SCK2}$	G	**N-ch open-drain I/O port** This port also serves as a clock I/O pin for serial I/O 2. Input is hysteresis type.
9	2	1	P46/SO2	G	**N-ch open-drain I/O port** This port also serves as a data-output pin for serial I/O 2. Input is hysteresis type.
10	3	2	P47/SI2	G	**N-ch open-drain I/O port** This port also serves as a data-output pin for serial I/O 2. Input is hysteresis type.
11 to 18	4 to 11	3 to 10	P50 to P57	H	**N-ch open-drain output-only ports**
22 to 25	15 to 18	14 to 17	P60INT0 to P63/INT3	I	**General-purpose input-only ports** These ports also serve as external-interrupt input pins. Input is hysteresis type.
26	19	18	P64	I	**General-purpose input-only ports.** Input is hysteresis type.
19 64	12 57	11 56	V_{CC}	—	**Power pin**
21 32 57	14 25 50	13 24 49	V_{SS}	—	**Power (GND) pins**
20	13	12	N.C.	—	It should be used at the same potential at V_{SS}.

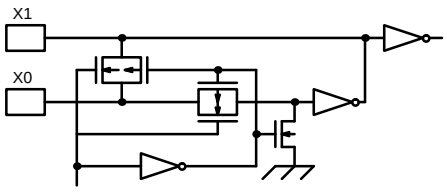
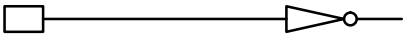
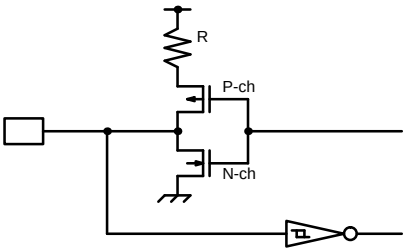
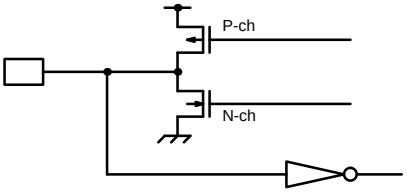
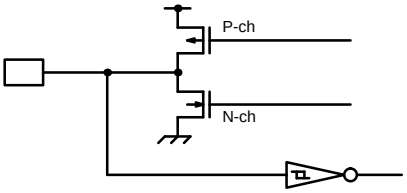
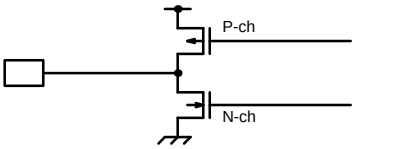
Classification	Circuit	Remarks
A	 Standby control signal	• Feedback resistor: About 2 MΩ
B		• CMOS input
C		• Output pull-up resistor (P-ch): About 50 kΩ (5 V) • Hysteresis input
D		• CMOS output • CMOS input • The pull-up resistor is optional. (P22 and P23 are excluded.)
E		• CMOS output • Hysteresis input • The pull-up resistor is optional.
F		• CMOS output

Fig. 1.5 I/O Circuits

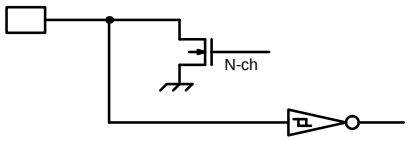
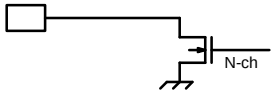
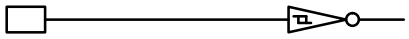
Classification	Circuit	Remarks
G		• N-ch open-drain output • Hysteresis input
H		• N-ch open-drain output
I		• Hysteresis input • The pull-up resistor is optional.

Fig. 1.5 I/O Circuits (*Continued*)

1.6 HANDLING DEVICES

(1) Preventing latch-up

Latch-up may occur if a voltage higher than Vcc or lower than Vss is applied to the input or output pins other than port 4, or if voltage exceeding the rated value is applied between Vcc and Vss.
When latch-up occurs, the supply current increases rapidly, sometimes resulting in overheating and destruction.
Therefore, no voltage exceeding the maximum ratings should be used.

(2) Handling unused input pins

Leaving unused input pins open may cause a malfunction.
Therefore, these pins should be set to pull-up or pull-down.

(3) Variations in supply voltage

Although the specified Vcc supply voltage operating range is assured, a sudden change in the supply voltage within the specified range may cause a malfunction. Therefore, the voltage supply to the IC should be kept as constant as possible. The V_{CC} ripple (P-P value) at the supply frequency (50 - 60 Hz) should be less than 10% of the typical Vcc value, or the coefficient of excessive variation should be 0.1 V/ms max. instantaneous change when the power supply is switched.

(4) Precautions for external clocks

It takes some time for oscillation to stabilize after changing the mode to power-on reset (option selection) and stop.
Consequently, an external clock must be input.

2. PINS AND PACKAGE

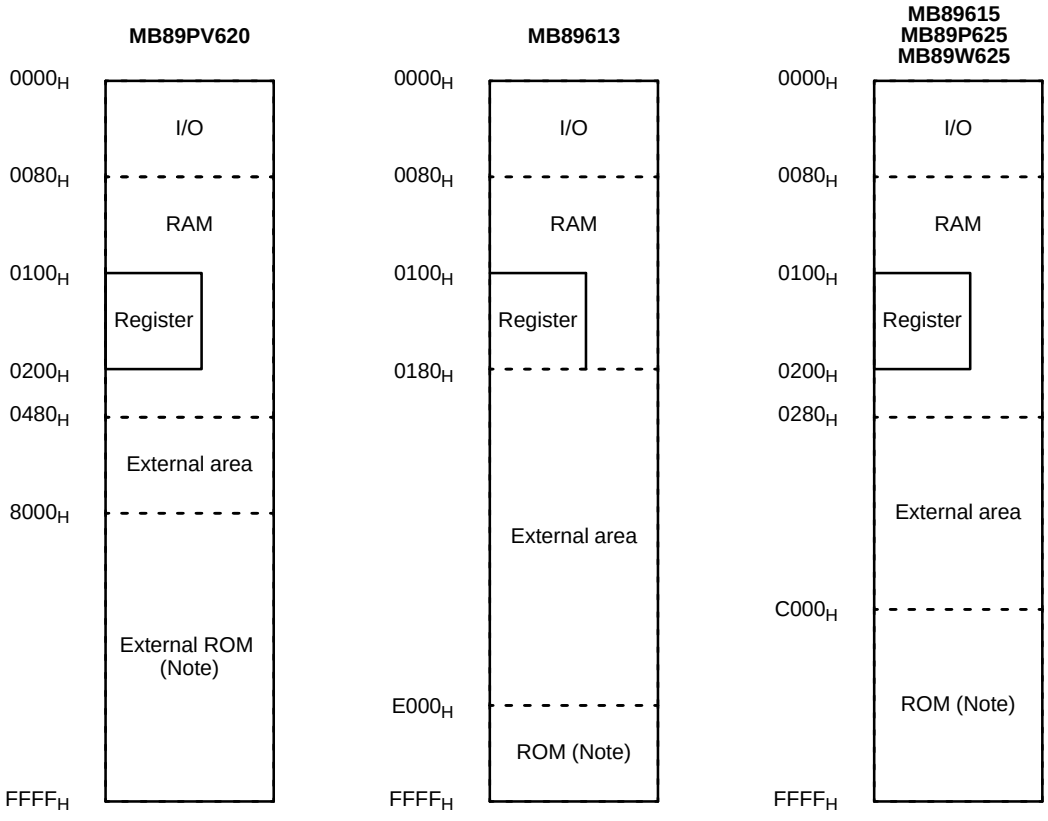
CPU

2.1 CPU

- This section describes the CPU hardware composition. The CPU has the following six functions.
  - Memory Space
  - Arrangement of 16-bit Data in Memory
  - Registers
  - Operation Modes and External Bus Operation
  - Clock Control Block
  - Interrupt Controller

■ Memory Space

The MB89610 series of microcontrollers have a memory area of 64 Kbytes. All I/O, data, and program areas are located in this space. The I/O area is near the lowest address and the data area is immediately above it. The data area may be divided into register, stack, and direct-address areas according to the applications. The program area is located near the highest address and the tables of interrupt and reset vectors and vector-call instructions are at the highest address. Figure 2.1 shows the structure of the memory space for the MB89610 series of microcontrollers.



Note: These areas serve as external areas according to the mode.

Fig. 2.1 Memory Space of MB89610 Series of Microcontrollers

CPU

(1) I/O area

This area is where various resources such as control and data registers are located. The memory map for the I/O area is given in Appendix 1.

(2) RAM area

This area is where the static RAM is located. Addresses from **0100_H** to **$017F_H$** are also used as the general-purpose register area.

(3) External area

When data is read and written from and to this area with the external-bus function specified, the external device is accessed via ports 0, 1, and 2. Examples of expanding the external memory and peripheral resources by using the external- bus pins are described in 3.4 Memory Access Modes.

(4) ROM area

This area is where the internal ROM is located. Addresses from **$FFC0_H$** to **$FFFF_H$** are also used for the tables of interrupt and reset vectors and vector-call instructions. Table 2-1 shows the correspondence between each interrupt number or reset and the table addresses to be referenced for the MB89610 series of microcontrollers.

Table 2-1 Table of Reset and Interrupt Vectors

	Table address	
	Upper data	Lower data
CALLV #0	$FFC0_H$	$FFC1_H$
CALLV #1	$FFC2_H$	$FFC3_H$
CALLV #2	$FFC4_H$	$FFC5_H$
CALLV #3	$FFC6_H$	$FFC7_H$
CALLV #4	$FFC8_H$	$FFC9_H$
CALLV #5	$FFCA_H$	$FFCB_H$
CALLV #6	$FFCC_H$	$FFCD_H$
CALLV #7	$FFCE_H$	$FFCF_H$

	Table address	
	Upper data	Lower data
Interrupt #11	$FFE4_H$	$FFE5_H$
Interrupt #10	$FFE6_H$	$FFE7_H$
Interrupt #9	$FFE8_H$	$FFE9_H$
Interrupt #8	$FFEA_H$	$FFEB_H$
Interrupt #7	$FFEC_H$	$FFED_H$
Interrupt #6	$FFEE_H$	$FFEF_H$
Interrupt #5	$FFF0_H$	$FFF1_H$
Interrupt #4	$FFF2_H$	$FFF3_H$
Interrupt #3	$FFF4_H$	$FFF5_H$
Interrupt #2	$FFF6_H$	$FFF7_H$
Interrupt #1	$FFF8_H$	$FFF9_H$
Interrupt #0	$FFFA_H$	$FFFB_H$
Reset mode	———	$FFFD_H$
Reset vector	$FFFE_H$	$FFFF_H$

Note: $FFFC_H$ is already reserved.

CPU

■ Arrangement of 16-bit Data in Memory Space

When the MB89610 series of microcontrollers handle 16-bit data, the data written at the lower address is treated as the upper data and that written at the next address is treated as the lower data as shown in Figure 2.2.

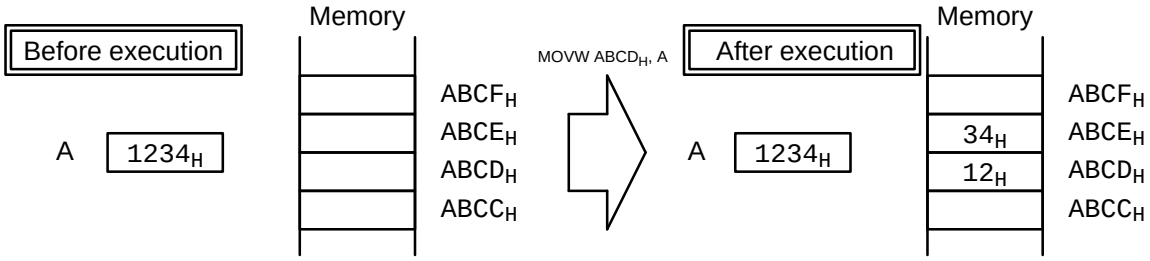


Fig. 2.2 Arrangement of 16 bit Data in Memory Space

This is the same as when 16 bits are specified by the operand during execution of an instruction. Bits closer to the OP code are treated as the upper byte and those next to it are treated as the lower byte. This is also the same when the memory address or 16-bit immediate data is specified by the operand.

[Example]

```
MOV A, 5678H      ; Extended address
MOV A, #1234H     ; 16-bit immediate data
```

Assemble

```
        ⋮
XXXXH XX XX
XXXXH 60 56 78 ; Extended address
XXXXH E4 12 34 ; 16-bit immediate data
XXXXH XX
        ⋮
```

Fig. 2.3 Arrangement of 16 bit Data during Execution of Instruction

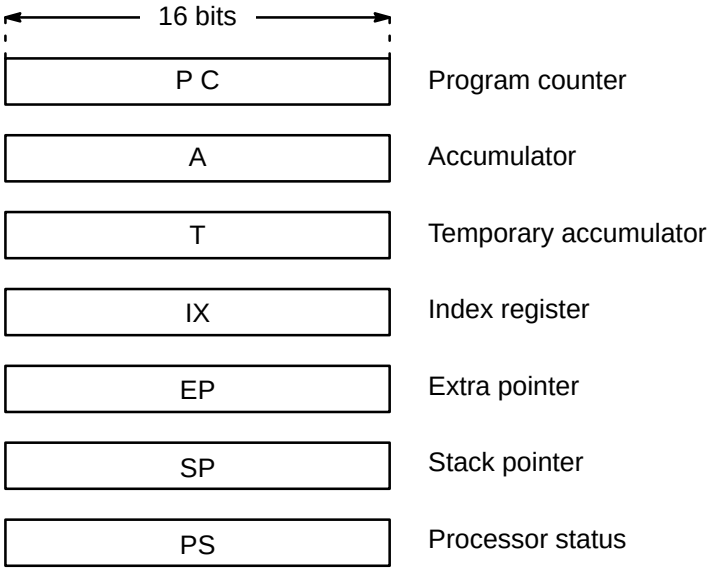
Data saved in the stack by an interrupt is also treated in the same manner.

CPU

■ Internal Registers in CPU

The MB89610 series of microcontrollers have dedicated registers in the CPU and general-purpose registers in memory.

- Program counter (PC) — 16-bit long register indicating location where instructions stored
- Accumulator (A) — 16-bit long register where results of operations stored temporarily. The lower byte is used to execute 8-bit data processing instructions.
- Temporary accumulator (T) — 16-bit long register where the operations are performed between this register and the accumulator. The lower one byte is used to execute 8-bit data processing instructions
- Stack pointer (SP) — 16-bit long register indicating stack area
- Processor status (PS) — 16-bit long register where register pointers and condition codes are stored
- Index register (IX) — 16-bit long register for index modification
- Extra pointer (EP) — 16-bit long register for memory addressing



The 16 bits of the processor status (PS) can be divided into 8 upper bits for a register bank pointer (RP) and 8 lower bits for a condition code register (CCR). (See Figure 2.4.)

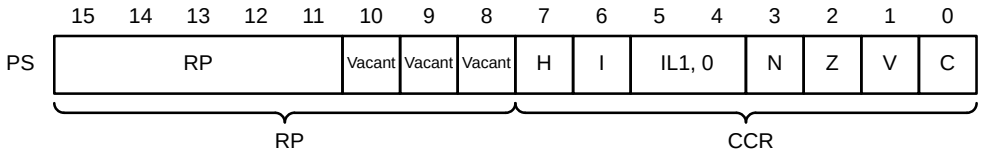


Fig. 2.4 Structure of Processor Status

CPU

The RP indicates the address of the current register bank. The rule for translating for the data the contents of the RP and the real addresses are as shown in Figure 2.5.

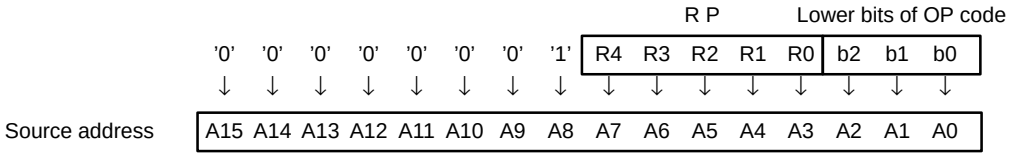


Fig. 2.5 Rule for Translating Real Addresses at General-purpose Register Area

The CCR has bits indicating the results of operations and transfer data contents, and bits controlling the CPU operation when an interrupt occurs.

– H-flag H-flag is set when a carry or a borrow out of bit 3 into bit 4 is generated as a result of operations; it is cleared in other cases. This flag is used for decimal-correction instructions.

– I-flag An interrupt is enabled when this flag is 1 and is disabled when it is 0. The I-flag is 0 at reset.

– IL1 and IL0 These bits indicate the level of the currently-enabled interrupt. The CPU executes interrupt processing only when an interrupt with a value smaller than the value indicated by this bit is requested.

IL1	IL0	Interrupt level	High and low
0	0	1	High ↕ Low = No interrupt
0	1		
1	0	2	
1	1	3	

– N-flag The N-flag is set when the most significant bit is 1 as a result of operations; it is cleared when the MSB is 0.

– Z-flag Z-flag is set when the bit is 0 as a result of operations; it is cleared in other cases.

– V-flag V-flag is set when a two's complement overflow occurs as a result of operations; it is reset when an overflow does not occur.

– C-flag C-flag is set when a carry or a borrow out of bit 7 is generated as a result of operations; it is cleared in other cases. When the shift instruction is executed, the value of the C-flag is shifted out.

CPU

• General-purpose registers

General-purpose registers are 8-bit long registers for storing data.

The 8-bit long general-purpose registers are in the register banks in memory. One bank has eight registers and up to 32 banks are available for the MB89610 series of microcontrollers. In the MB89613 microcontroller, when the external RAM is allocated to **0180_H** to **$01FF_H$** by the external circuit, 16 remaining banks can be extended externally. The register bank pointer (RP) indicates the currently-used bank.

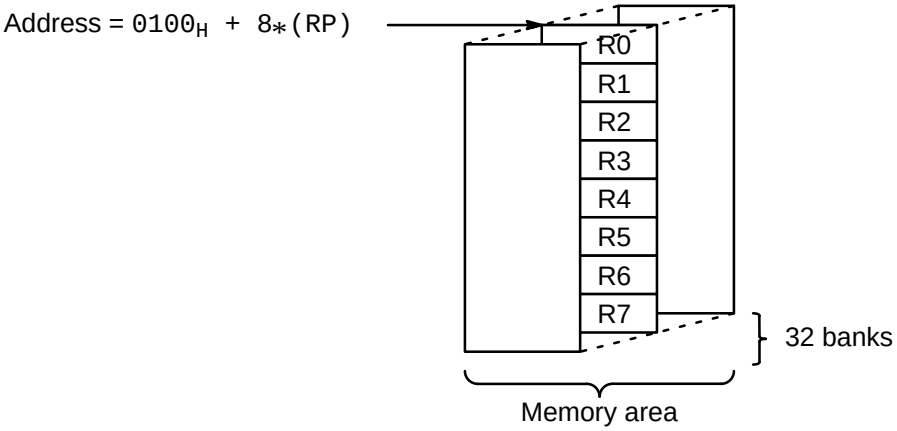


Fig. 2.6 Register Bank Configuration

CPU

■ Operation Modes

The MB89610 series of microcontrollers have the following three operation modes.

(1)Single-chip mode
(2) External-ROM mode
(3)External-access internal-ROM mode

The memory map for each mode is as follows:

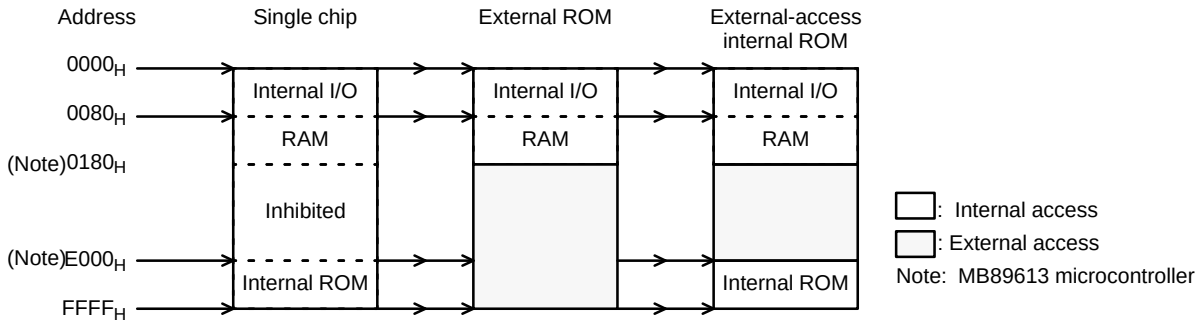
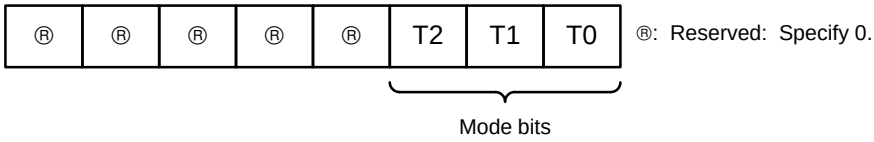


Fig. 2.7 Memory Maps in Various Modes

The mode that the device enters depends on the states of the device-mode pins and the contents of the mode data fetched during the reset sequence. The relationship between the states and operations of the device-mode pins is shown below.

MOD1	MOD0	Description
0	0	Reset vectors are read from the internal ROM. The external access does not function.
0	1	Reset vectors are read from the external ROM. The external access functions.
1	0	Reserved for future expansion and testing.
1	1	Write mode for products containing EPROM.

The following functions are selected according to the mode-data setting conditions.



T2	T1	T0	Operation
0	0	0	Select single-chip mode.
0	0	1	External access allowed.
Other than above			Reserved. Do not set.

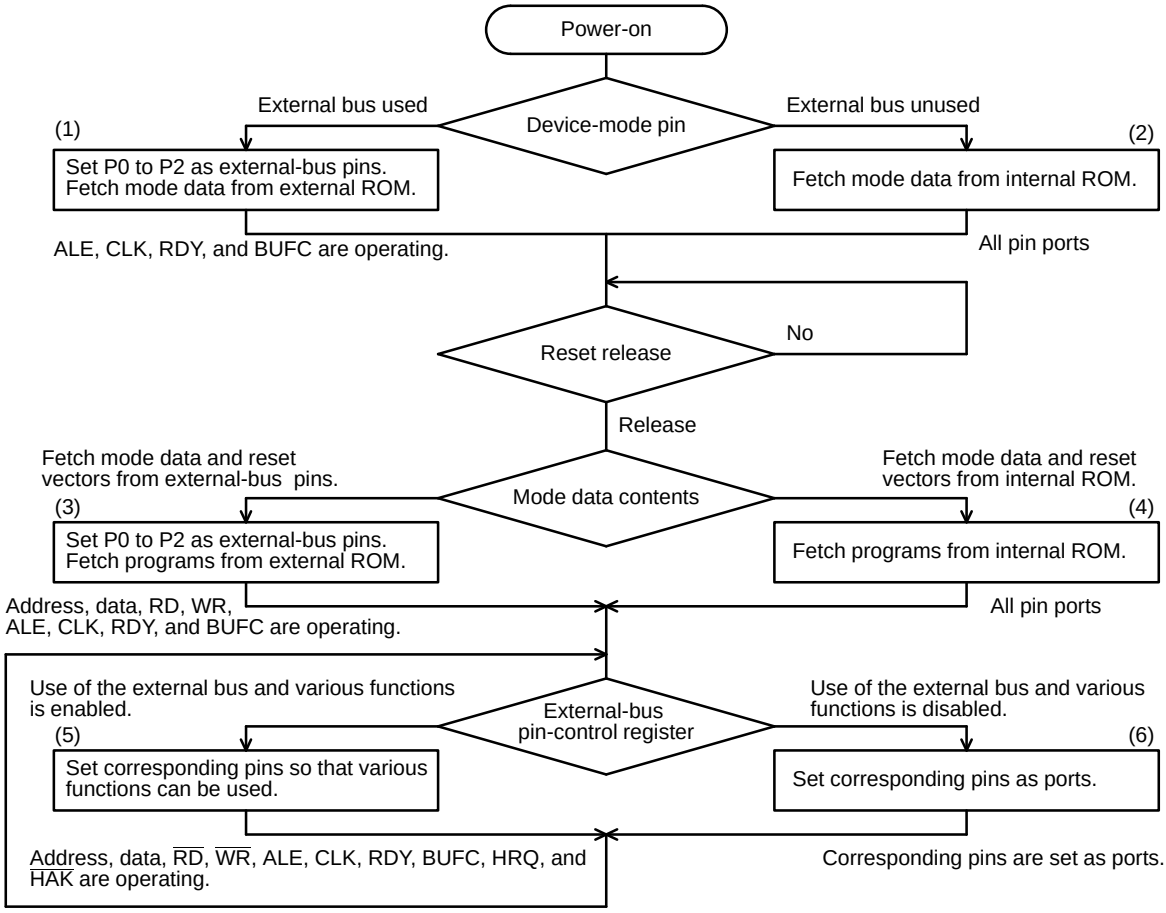
Note: Do not select the single-chip mode with the externally-fetched mode data.

CPU

As shown in the flowchart below, each mode is set according to the status of the device-mode pins and the contents of the mode data fetched during the reset sequence.

Setting procedure	Mode selected	Mode pin	Mode data
(2)→(4)→(6)	Single-chip mode	00	XXXXX000
(1)→(3)→ *(5)or(6)	External-ROM mode	01	XXXXX001
(2)→(3)→ *(5)or(6)	External-access internal-ROM mode	00	XXXXX001

* Depends on whether ready or hold function used



When the external-bus function is used, the following pins become active at default.

A08 to A15, AD0 to AD7, $\overline{RD}$, $\overline{WR}$, ALE, CLK, RDY, BUFC

The external-bus pin-control register (BCTR) is used to switch the function of the pin controlling the external bus for port 2 in the external-bus mode. When either of the bits is set to 0, the pin corresponding to the bit serves as the port. In the single-chip mode, the contents of both bits are ignored and all 8 bits of port 2 serve as parallel ports. Access to this register is not allowed in modes other than the external-bus mode. The structure of the BCTR is as follows:

CPU

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0005_H	—	—	—	—	—	—	HLD	BUF
							(W)	(W)
				Initial value $XXXXX01_B$				

[Bit 1] HLD: Hold-enable bit.

Bit 1 is used to enable the holding operation.

0	In external-bus mode, P21 and P22 serve as ports.
1	In external-bus mode, P21 used for $\overline{HAK}$ output and P22 used for HRQ input.

[Bit 0] BUF: BUFC-operation enable bit.

Bit 0 is used to enable the operation of the BUFC pin.

0	In external-bus mode, P20 serves as port.
1	In external-bus mode, P20 used for BUFC output.

The states of the bus pins in each mode are follows:

Pin name	Single chip	External Access
P00 to P07	P00 to P07	AD7 to AD0
P17	P17	A15
P16	P16	A14
P15	P15	A13
P14	P14	A12
P13	P13	A11
P12	P12	A10
P11	P11	A09
P10	P10	A08
P27	P27	ALE
P26	P26	$\overline{RD}$
P25	P25	$\overline{WR}$
P24	P24	CLK
P23	P23	RDY
P22	P22	HRQ
P21	P21	$\overline{HAK}$
P20	P20	BUFC

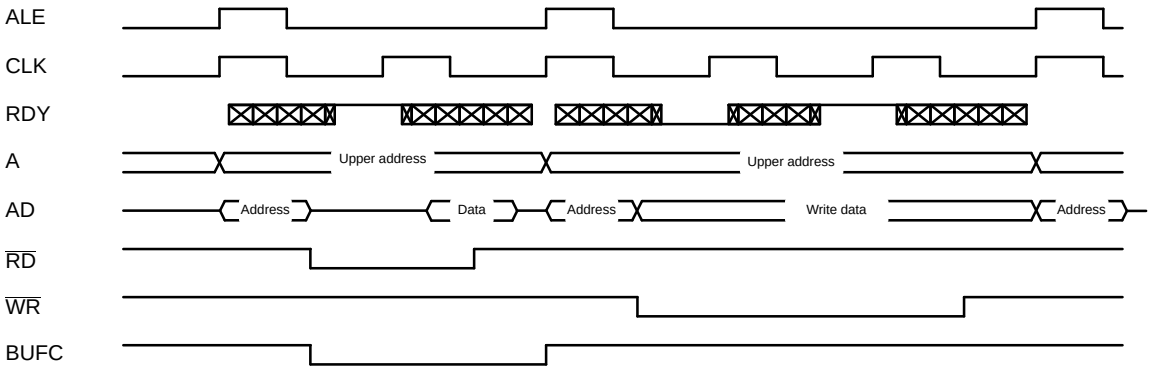
Meaning of each signal

AD0 to AD7	:	Address/data multiplex bus
A08 to A15	:	Address bus
ALE	:	Address-latch enable
$\overline{RD}$	:	Read strobe (Active at L)
$\overline{WR}$	:	Write strobe (Active at L)
CLK	:	Clock output
RDY	:	Bus-ready input (Wait at L)
HRQ	:	Hold request
$\overline{HAK}$	:	Hold-acknowledge output (Active at L)
BUFC	:	Buffer control

Note: RD, WR, and BUFC are not output when the address indicates the internal area.

The timing concept for external access is shown below. Refer to the data sheet for details about the ERECTRICAL CHARACTERISTICS.

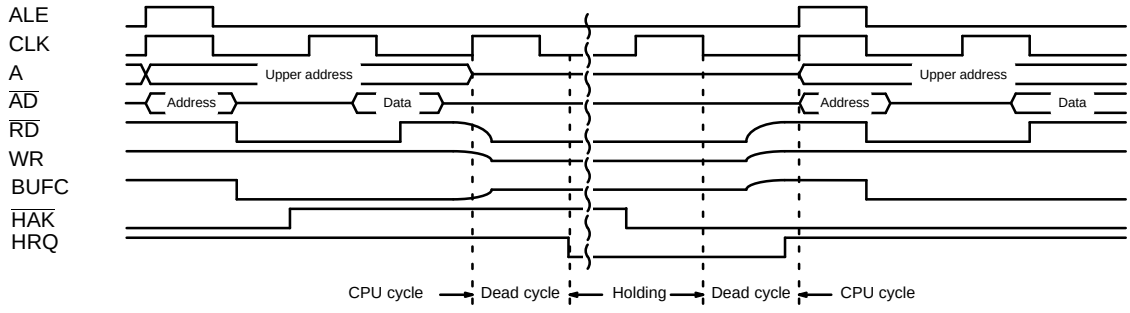
CPU



Note: The read cycle of the RDY signal is prolonged in the same manner as the write cycle.

The RDY signal is used for the ready function. When a Low level is input, the bus cycle is prolonged in CLK cycles. Fetching is carried out near the rising edge of the CLK signal. To prolong the bus cycle, set the RDY signal to Low before the rising edge of the CLK signal.

The HRQ and $\overline{HAK}$ signals are used for the hold function. To obtain the external bus, set the HRQ signal to High. After that, the CPU recognizes the bus request between instructions to stop operation and sets the $\overline{HAK}$ signal to Low after waiting one half cycle. It signals the outside that the bus is open in this way. When another device terminates use of the bus, set the HRQ signal to Low to notify the CPU. When the CPU detects the Low level of the HRQ signal, it sets the $\overline{HAK}$ signal to High and starts using the external bus after waiting one half cycle. The hold function timing concept is as follows:



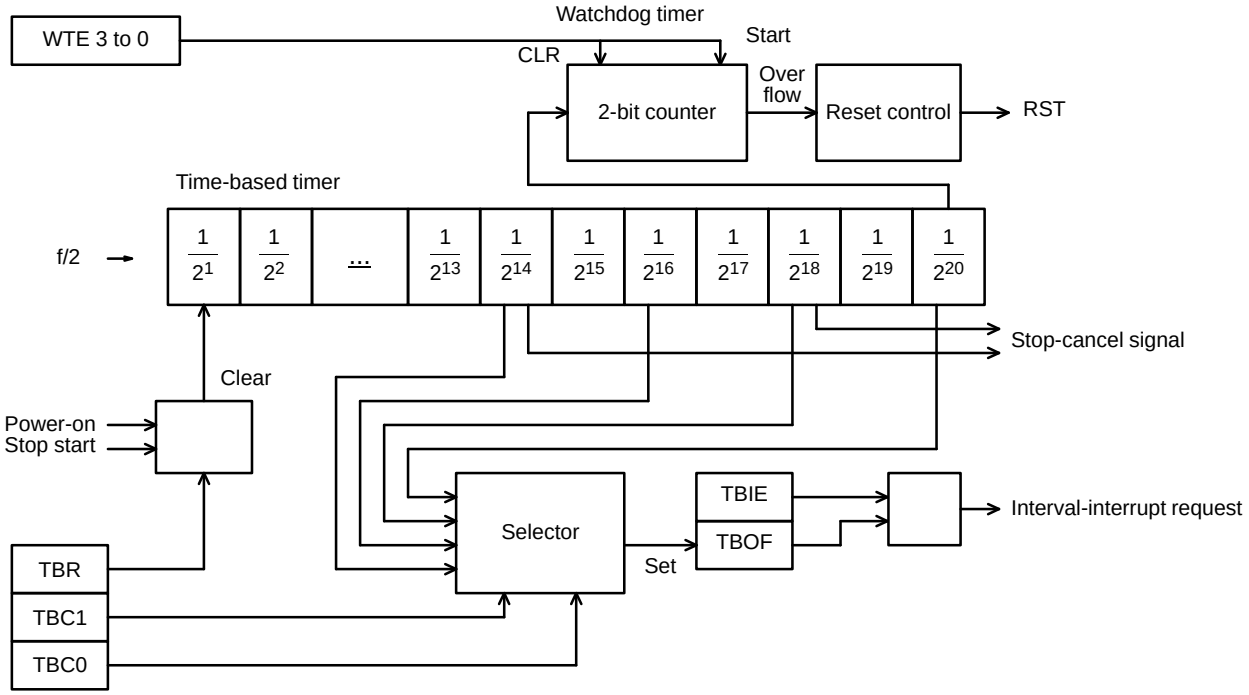
CLOCK CONTROL BLOCK

2.2 CLOCK CONTROL BLOCK

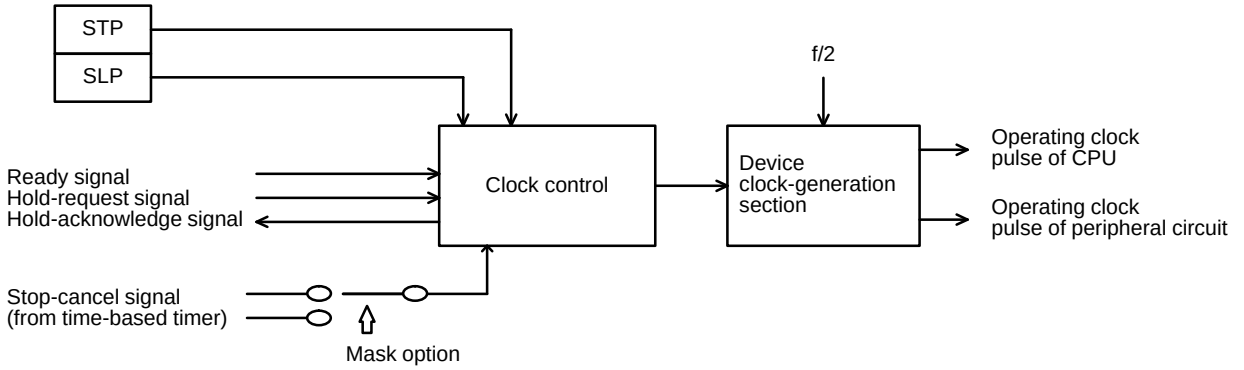
● This block controls the standby operation, software reset, time-based timer, and watchdog timer.

■ Clock Control Block Diagram

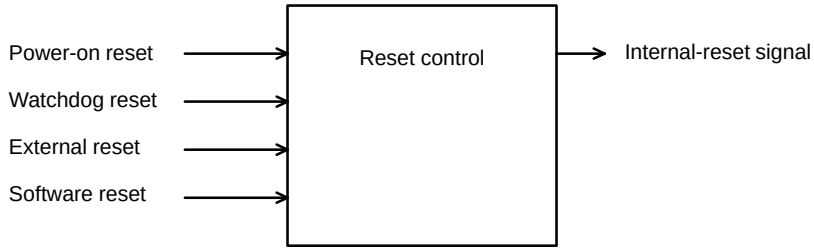
(a) Time-based timer and watchdog timer



(b) Device clock control section



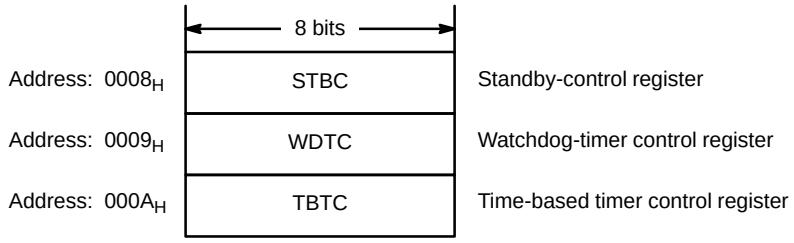
(c) Reset-control section



CLOCK CONTROL BLOCK

■ Register List

Main/sub clock control block consists of standby control register (STBC) and system clock control register (SYCC).

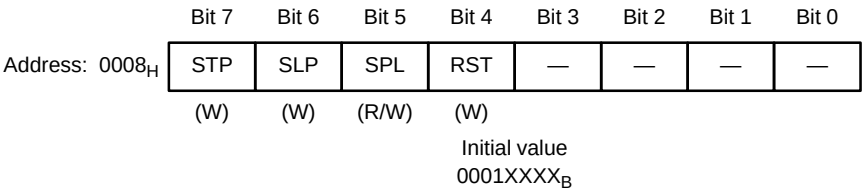


n Description of Registers

The detail of each register is described below.

Address: STBC
0008H
Address: WDTC
0009H
Address: 000AH TBTC

(1) Standby-conrol register (STBC)



[Bit 7] STP: Stop bit
Bit 7 is used to specify switching to the stop mode.

0	No operation
1	Stop mode

This bit is cleared at reset or stop cancellation.
0 is read whenever this bit is read.

[Bit 6] SLP: Sleep bit
Bit 6 is used to specify switching to the sleep mode.

0	No operation
1	Sleep mode

This bit is cleared at reset or sleep and stop cancellation.
The stop mode is selected when 1 is written simultaneously to the STP and SLP bits. 0 is read whenever this bit is read.

[Bit 5] SPL: Pin state specifying bit

Bit 5 is used to specify the state of the external pin in the stop mode.

0	Holds state and level immediately before stop mode
1	High impedance

This bit is cleared at reset.

CLOCK CONTROL BLOCK

[Bit 4] RST: Software reset bit
Bit 4 is used to specify the software reset.

0	Generates 4-cycle reset signal
1	No operation

1 is read when this bit is read.

Address: STBC
0008_H
Address: WDTC
0009_H
Address: $000A_H$ TBTC

(2) Watchdog-timer control register (WDTC)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0009_H	—	—	—	—	WTE3	WTE2	WTE1	WTE0
					(W)	(W)	(W)	(W)
					Initial value			
					$XXXXXXXX_B$			

The WDTC register controls the watchdog timer.

[Bits 3 to 0] WTE3 to WTE0: Watchdog timer control bits
These bits are used to control the watchdog timer.

1) First write after reset

0101	Start watchdog timer
Other than above	No operation

2) Second write after reset

0101	Clear watchdog-timer counter
Other than above	No operation

The watchdog timer can be stopped only by reset.
1111 is read when these bits are read.

Address: STBC
0008_H
Address: WDTC
0009_H
Address: $000A_H$ TBTC

(3) Time-based timer control register (TBTC)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $000A_H$	—	—	—	TBIE	TBOF	TBR	TBC1	TBC0
				(R/W)	(R/W)	(W)	(R/W)	(R/W)
				Initial value				
				$XXX00000_B$				

The TBTC register controls the time-based timer and interval timer.

CLOCK CONTROL BLOCK

[Bit 4] TBIE: Interval-interrupt enable bit

Bit 4 is used to enable an interrupt by the interval timer.

0	Interval-interrupt disabled
1	Interval-interrupt enabled

This bit is cleared at reset.

[Bit 3] TBOF: Interval-timer overflow bit

(1) This bit is used to clear the interval-timer overflow flag when writing.

0	Clear interval-timer overflow flag.
1	No operation

(2) This bit indicates that the interval timer overflows at reading.

0	Interval timer does not overflow
1	Interval timer overflows

1 is read when the Read Modify Write instructions are read. If the TBOF bit is set to 1 when the TBIE bit is 1, an interrupt request is output.
This bit is cleared at reset.

[Bit 2] TBR: Time-based timer initialize bit

Bit 2 is used to clear the time-based timer counter.

0	Time-based timer counter cleared
1	No operation

1 is read when this bit is read.

[Bits 1 and 0] TBC1 and TBC0: Interval-time setting bits

These bits are used to set the cycle of the interval timer.

TBC1	TBC0	Interval time at 10 MHz oscillation
0	0	3.3 ms
0	1	13.1 ms
1	0	52.4 ms
1	1	209.7 ms

These bits are cleared at reset.

CLOCK CONTROL BLOCK

■ Description of Operation

(1) Low-power consumption mode

There are two low-power consumption modes: sleep and stop. Table 2-2 lists the state in each operation mode.

Table 2-2 Operating State in Low-Power Consumption Modes

Operation mode	Switching conditions	Oscillation	Clock	CPU	Peripheral circuit	Pin	Canceling
Sleep	SLP=1	Operates	Operates	Stops	Operates	Operates	Reset/interrupt
Stop (SPL = 0)	STP=1	Stops	Stops	Stops	Stops	Stops	Reset/interrupt
Stop (SPL = 1)	STP=1	Stops	Stops	Stops	Stops	Hi-Z	Reset/interrupt

- The sleep mode stops only the operating clock pulse of the CPU; other operations are continued.
- The stop mode stops oscillation. Therefore, data can be held with the lowest power consumption.

(a) Sleep mode

- Switching to sleep mode
  - Writing 1 at the SLP bit (bit 6) of the STBC switches the mode to sleep.
  - The sleep mode stops the operating clock pulses of the CPU; only the CPU stops and the peripheral circuits continue to operate.
  - If an interrupt is requested when 1 is written at the SLP bit (bit 6), execution of the instruction continues without switching to the sleep mode.
  - The contents of registers and RAM are held in the sleep mode.
- Canceling sleep mode
  - The sleep mode is canceled by inputting the reset signal and requesting an interrupt.
  - When the reset signal is input during the sleep mode, the CPU is switched to the reset state and the sleep mode is canceled.
  - When an interrupt higher than level 11 is requested from the peripheral circuit during the sleep mode, the sleep mode is canceled.
  - When the I-flag and IL bits are set to accept an interrupt after canceling, the CPU executes the interrupt processing. When they are set to ignore, the CPU executes the interrupt processing from the next instruction.

(b) Stop mode

- Switching to stop mode
  - Writing 1 at the STP bit (bit 7) of the STBC switches the mode to stop.
  - The stop mode stops oscillation and all chip functions stop. Therefore, data can be held with the lowest power consumption.

CLOCK CONTROL BLOCK

- During the stop mode, whether the I/O and output pins are set to the previous or high-impedance state can be controlled by the SPL bit (bit 5) of the STBC.
- If an interrupt is requested when 1 is written at the STP bit (bit 7), execution of the instruction continues without switching to the stop mode.
- The contents of registers and RAM are held in the stop mode.

• Canceling stop mode

- The stop mode is canceled by inputting the reset signal and requesting an interrupt.
- When a reset signal is input during the sleep mode, the CPU is switched to the reset state, but the stop mode is canceled.
- When an interrupt higher than level 11 is requested from the external-interrupt circuit during the stop mode, the stop mode is canceled.
- After the oscillation stabilization time since the stop mode was canceled has elapsed, when the I-flag and IL bits are set to accept an interrupt, the CPU executes the interrupt processing. When they are set to ignore, the CPU executes the interrupt processing from the next instruction.
- The oscillation stabilization time can be selected from the two types in Table 3 by the mask option.
- With Power-on Reset Available selected, when the stop mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization wait state. Thus, the reset sequence is executed after the oscillation stabilization time has elapsed.

Table 2-3 Selection of Oscillation Stabilization Time

Number of counts for minimum instruction time	Time at 10 MHz oscillation	Remarks
About 2^{16}counts	About 26.2 ms	For crystal oscillator
About 2^{12}counts	About 1.64 ms	For ceramic oscillator

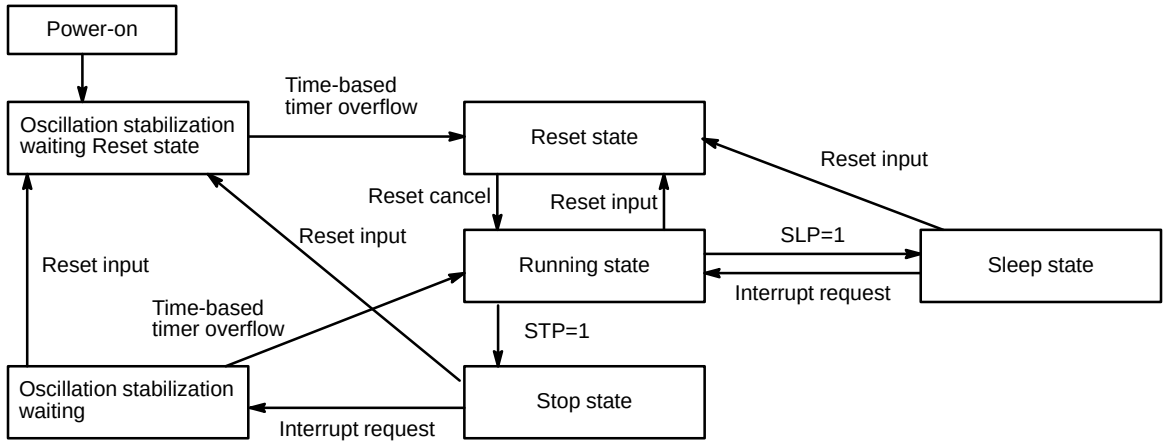


Fig. 2.8 State Transition Diagram at Low-power Consumption(with power–on reset)

CLOCK CONTROL BLOCK

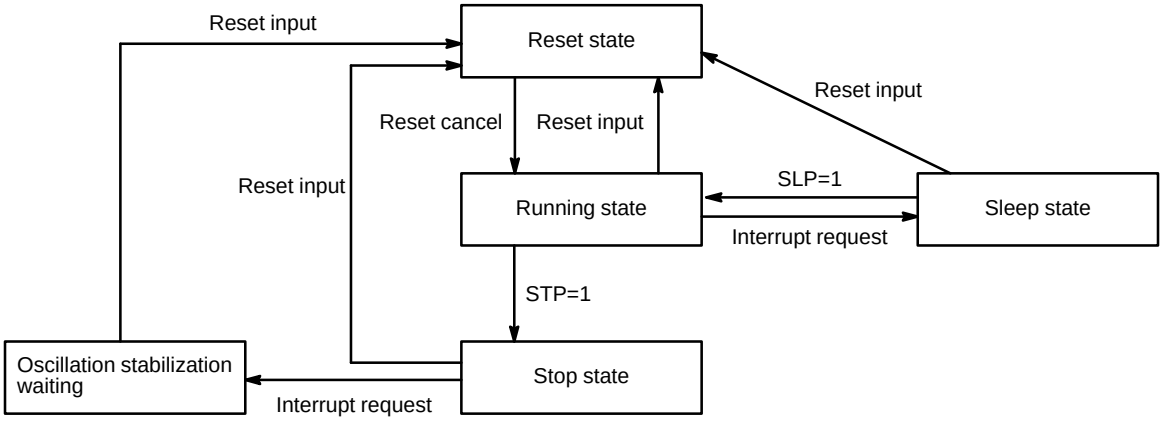


Fig. 2.9 State Transition Diagram in Low-power Consumption Modes(without power–on reset)

(2) Watchdog timer

Program runaway is detected by the watchdog timer.

(a) Starting watchdog timer

- Write 0101 first at the WTE3 to WTE0 bits (bits 3 - 0) of the WDTC after reset.

(b) Operation watchdog timer

- Write the second or later 0101 at the WTE3 to WTE0 bits (bits 3 - 0) to clear the watchdog-timer counter.
- If the watchdog-timer counter is not cleared within the time specified in Table 4, a reset occurs in the watchdog timer after about two instruction cycles to initialize the chip.
- The watchdog-timer counter is cleared by switching to the standby and hold states.
- The clock source for the watchdog timer is supplied from the time-based timer. Therefore, the watchdog timer is cleared as soon as the time-based timer is cleared.
- Once started, the watchdog timer cannot be stopped until a reset occurs.

Table 2-4 Watchdog Timer Interval Time (at 10 MHz Oscillation)

Minimum time	Maximum time
About 209.7 ms	About 419.4 ms

CLOCK CONTROL BLOCK

(3) Time-based timer

The time-based timer consists of 20 counters which use a 1/2 oscillation as a clock source. This timer has functions for the watchdog timer, the timer for waiting for stable oscillation, and the interval timer for causing an interrupt in a fixed cycle.

(a) Control of time-based timer

- The time-based timer counter is cleared by writing 0 at the TBR bit (bit 2) of the TBTC, or by switching to the stop mode.
- In other cases, the counter is incremented for as long as the clock pulse oscillates.

(b) Functions of interval timer

- The TBOF bit (bit 3) is set at every interval time specified by the TBC1 and TBC0 bits (bits 1 and 0) of the TBTC.
- This interval time is based on the time when the time-based timer counter is finally cleared.
- The TBOF bit (bit 3) is cleared by switching to the stop mode since the time-based timer is used as the counter for waiting for oscillation stabilization in returning.
- If 1 is already set at the TBIE bit (bit 4) when the TBOF bit (bit 3) is set, an interval interrupt occurs.
- The interrupt source is cleared by writing 0 at the TBOF bit (bit 3).

(4) Reset

There are four types of resets as shown in Table 2-5.

Table 2-5 Sources of Reset

Reset name	Description
External-pin reset	Sets external-reset pin to Low
Software reset	Writes 0 at RST (bit 4) of STBC
Watchdog reset	Overflows watchdog timer
Power-on reset	Turns power on

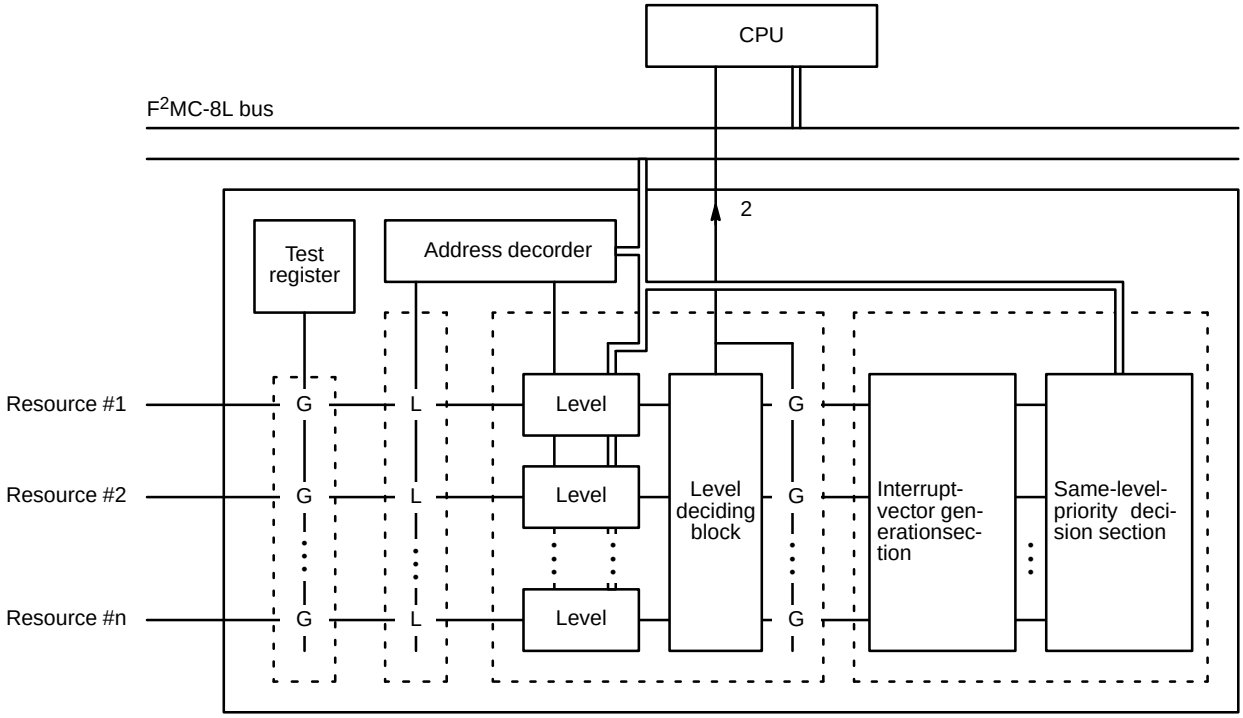
When the power-on reset and reset during the stop mode are used, the oscillation stabilization time is needed after the oscillator operates. The time-based timer controls this stabilization time. Consequently, the operation does not start immediately even after canceling the reset.

INTERRUPT CONTROLLER

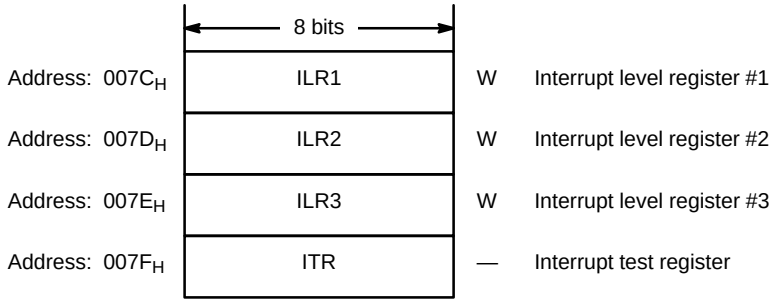
2.3 INTERRUPT CONTROLLER

The interrupt controller for the F^{2}MC-8L is located between the CPU and each resource. This controller receives interrupt requests from the resources, assigns priority to them, and transfers the priority to the CPU; it also decides the priority of same-level interrupts.

■ Block Diagram



■ Register List



INTERRUPT CONTROLLER

Address: $007C_H$ ILR1

Address: $007D_H$ ILR2

Address: $007E_H$ ILR3

Address: $007F_H$ ITR

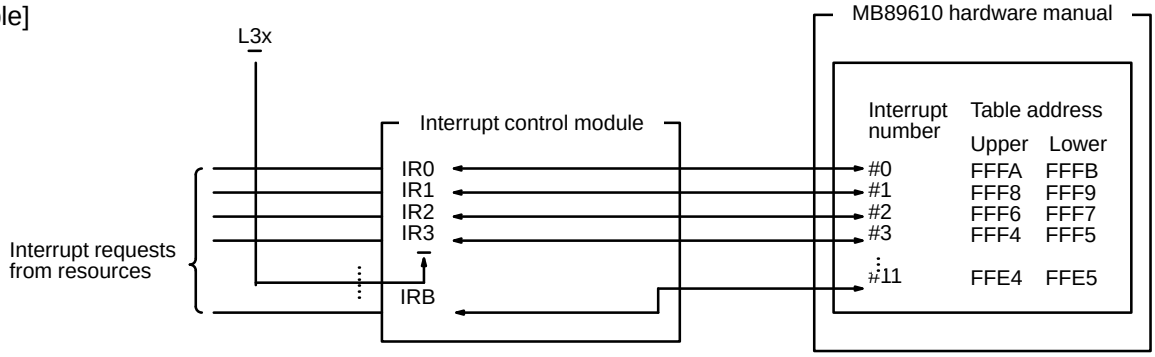
■ Description of Registers

(1) Interrupt level register (ILRx: Interrupt Level Register x)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $007C_H$	L31	L30	L21	L20	L11	L10	L01	L00
Address: $007D_H$	L71	L70	L61	L60	L51	L50	L41	L40
Address: $007E_H$	LB1	LB0	LA1	LA0	L91	L90	L81	L80
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)
Initial value	11111111_B							

The ILRx sets the interrupt level of each resource. The figure at the center of each bit corresponds to the interrupt number.

[Example]



[Bit 7 and 6][Bit 5 and 4][Bit 3 and 2][Bit 1 and 0]Lx1, Lx0: Interrupt level setting bit

When an interrupt is requested from a resource, the interrupt controller transfers the interrupt level based on the value set at the 2 bits of the ILRx corresponding to the interrupt to the CPU. The relationship between the 2 bits of the ILRx and the required interrupt levels is as follows:

Lx1	Lx0	Required interrupt level
0	X	1
1	0	2
1	1	3 (None)

Address: $007C_H$ ILR1

Address: $007D_H$ ILR2

Address: $007E_H$ ILR3

Address: $007F_H$ ITR

(2) Interrupt test register (ITR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $007F_H$	—	—	—	—	—	—	※	※
Initial value	—							

The ITR is used for testing. Access to this register is prohibited.

INTERRUPT CONTROLLER

■ Description of Operation

(1) Interrupt functions

The MB89610 series of microcontrollers have 12 inputs for interrupt requests from each resource. The interrupt level is set by 2-bit registers corresponding to each input. When an interrupt is requested from a resource, the interrupt controller receives it and transfers the contents of the corresponding register to the CPU. The interrupt to the device is processed as follows:

(a) An interrupt source is generated inside each resource.
(b) If an interrupt is enabled, an interrupt request is output from each resource to the interrupt controller by referring to the interrupt-enable bit inside each resource.
(c) After receiving this interrupt request, the interrupt controller determines the priority of simultaneously-requested interrupts and then transfers the interrupt level for the applicable interrupt to the CPU.
(d) The CPU compares the interrupt level requested from the interrupt controller with the IL bit in the processor status register.
(e) As a result of the comparison, if the priority of the interrupt level is higher than that of the current interrupt processing level, the contents of the I-flag in the same processor status register are checked.
(f) As a result of the check in step (5), if the I-flag is enabled for an interrupt, the contents of the IL bit are set to the required level. As soon as the currently-executing instruction is terminated, the CPU performs the interrupt processing and transfers control to the interrupt-processing routine.
(g) When an interrupt source is cleared by software in the user's interrupt processing routine, the CPU terminates the interrupt processing.

Fig. 2.10 outlines the interrupt operation for the MB89610 series of microcontrollers.

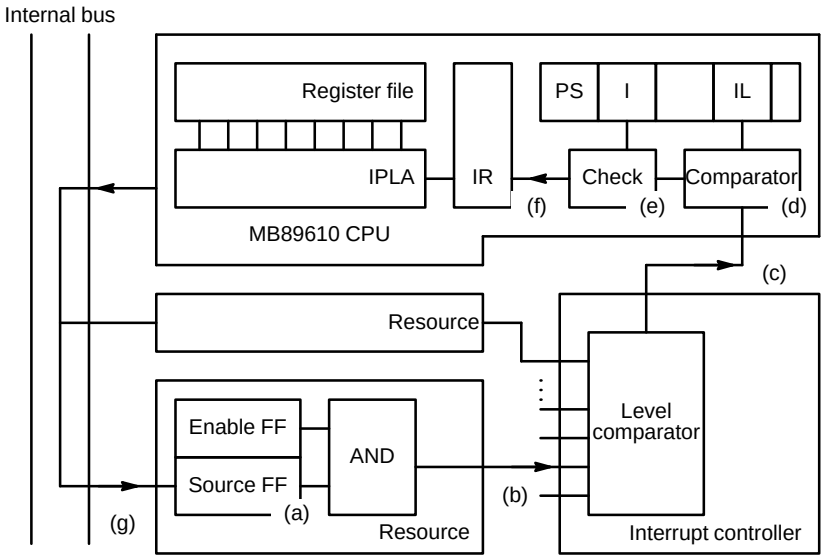


Fig. 2.10 Interrupt-processing Flowchart

I/O PORTS

2.4 I/O PORTS

- The MB89610 series of microcontrollers have seven parallel ports (53 ports). Ports 0, 1, 3, and 4 serve as 8-bit I/O ports; ports 2 and 5 serve as 8-bit output-only ports and port 6 serves as a 5-bit input-only port.
- Each port is also used as a resource (ports 3 and 4) and as external-bus pins (ports 0 to 2) (if P40 to P43 and P64 are used only for ports).

■ List of port functions

Table 2-6 List of Port Functions

Pin name	Input type	Output type	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P00 to P07	CMOS	CMOS push-pull	Parallel port 0	P07	P06	P05	P04	P03	P02	P01	P00
			External-address mode	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
P10 to P17	CMOS	CMOS push-pull	Parallel port 1	P17	P16	P15	P14	P13	P12	P11	P10
			External-address mode	A15	A14	A13	A12	A11	A10	A09	A08
P20 to P27	—	CMOS push-pull	Parallel port 2	P27	P26	P25	P24	P23	P22	P21	P20
			External-address mode	ALE	$\overline{RD}$	$\overline{WR}$	CLK	RDY	HRQ	$\overline{HAK}$	BUFC
P30 to P37	CMOS (Hysteresis)	CMOS push-pull	Parallel port 3	P37	P36	P35	P34	P33	P32	P31	P30
			Resource	PTO	WTO	PWC	EC	SI1	SO1	$\overline{SCK1}$	—
P40 to P47	CMOS (Hysteresis)	N-ch open drain	Parallel port 4	P47	P46	P45	P44	P43	P42	P41	P40
			Resource	SI2	S02	$\overline{SCK2}$	BZ	—	—	—	—
P50 to P57	—	N-ch open drain	Parallel port 5	P57	P56	P55	P54	P53	P52	P51	P50
P60 to P64	CMOS (Hysteresis)	—	Parallel port 6	—	—	—	P64	P63	P62	P61	P60
			Resource	—	—	—	—	INT3	INT2	INT1	INT0

I/O PORTS

■ Register list

I/O port consists of the following registers.

	8 bits			
Address: 0000_H	PDR0	R/W*1	Port-0 data register	Initial value = $XXXXXXXX_B$
Address: 0001_H	DDR0	W*1	Port-0 data direction register	Initial value = 00000000_B
Address: 0002_H	PDR1	R/W*1	Port-1 data register	Initial value = $XXXXXXXX_B$
Address: 0003_H	DDR1	W*1	Port-1 data direction register	Initial value = 00000000_B
Address: 0004_H	PDR2	R/W	Port-2 data register	Initial value = 00000000_B
Address: 0005_H	BCTR	W*2	External-bus pin-control register	Initial value = $XXXXXX01_B$
Address: $000C_H$	PDR3	R/W	Port-3 data register	Initial value = $XXXXXXXX_B$
Address: $000D_H$	DDR3	W	Port-3 data direction register	Initial value = 00000000_B
Address: $000E_H$	PDR4	R/W	Port-4 data register	Initial value = 11111111_B
Address: 0010_H	PDR5	R/W	Port-5 data register	Initial value = 11111111_B
Address: 0011_H	PDR6	R	Port-6 data register	Initial value = $XXXXXXXX_B$

*1: Data can be read and written only in the single-chip mode.
*2: Data can be written only when the external bus is extended.

■ Description of functions

The function of each port is described below.

(1) P00 to P07: CMOS-type I/O ports
(used as external-address/data bus)
P10 to P17: CMOS-type I/O ports
(used as external-address bus)

- Operation when external bus extended
  See the description of the bus functions.
- Switching input and output
  These ports have a data-direction register (DDR) and port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input. Note that the DDR is ineffective when the external bus is used.

I/O PORTS

- Operation for output port (DDR = 1)
  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

- Operation for input port (DDR = 0)
  When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

- State when reset
  In the single-chip mode (MOD0 = Low, MOD1 = Low), the DDR is initialized to 0 by resetting and the output impedance goes High at all bits. The PDR is not initialized by resetting. Therefore, set the value of the PDR before setting the DDR to output.

- State in stop mode
  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR.

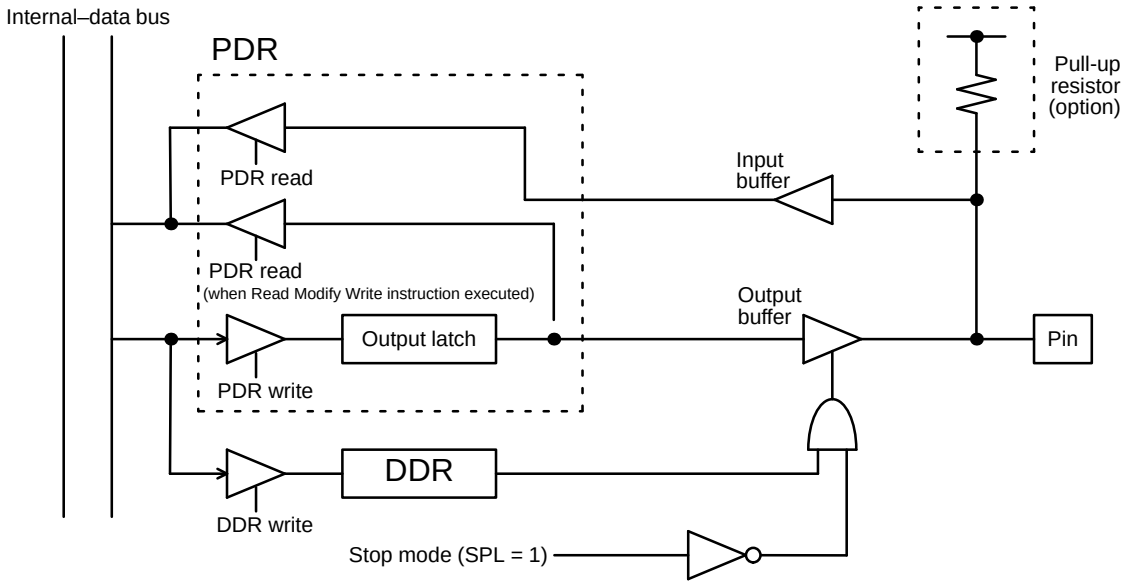


Fig. 2.11 Ports 0 and 1 (in Single-chip Mode)

(2) P20 to P27: CMOS-type output-only ports
(used as external-bus control pin)

- Operation when external bus extended
  See the description of the bus functions.

I/O PORTS

- Operation for output port
  In the single-chip mode, the value written at the PDR is output to the pin. When the PDR is read, the contents of the output latch are always read, so the bit- processing instruction is used even if the output level changes due to the load.

- State when reset
  In the single-chip mode, the pin impedance goes High at reset. As soon as a vector is fetched, output of the port is enabled and the port starts operation as the output port. Since the PDR is initialized to 0 by resetting, the Low level is output to the pin.

- State in stop mode
  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

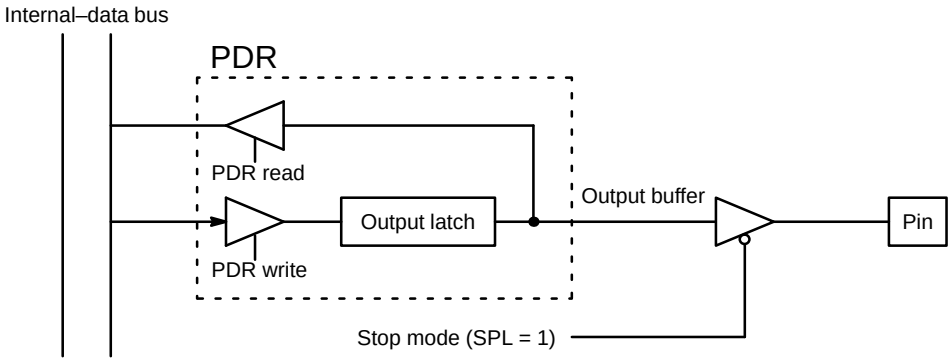


Fig. 2.12 Port 2 (in Single-chip Mode)

(3) P30 to P37: CMOS type I/O ports
(used as resource input and output)

- Switching input and output
  This port has a data-direction register (DDR) and a port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input. When the resource-output enable bit is enabled, the pin is set to output irrespective of the DDR setting conditions.

- Operation for output port (DDR = 1)
  The value written at the PDR is output to the pin when the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.

- Operation for input port (DDR = 0)
  When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.

I/O PORTS

- Operation for resource output
  When using as the resource output, setting is performed by the resource output- enable bit (See the description of each resource). If the output of each resource is enabled with the DDR set to 0, the port is set to output. Since the reading of the parallel port is effective even if the output of each resource is enabled, the output value of each resource can be read.
- Operation for resource input
  Input to the resource is irrelevant to the setting conditions of the DDR and resource. The value of the pin is always input to the port serving as the resource input. When using an external signal at the resource, set the DDR to input.
- State when reset
  When reset, the DDR and resource output-enable bit are initialized to 0 and the output impedance goes High at all bits. When reset, the PDR is undefined. Therefore, set the value of the PDR before setting the DDR to output.
- State in stop mode
  With the SPL bit of the standby-control register set to 1, in the stop mode, the output impedance goes High irrespective of the value of the DDR.

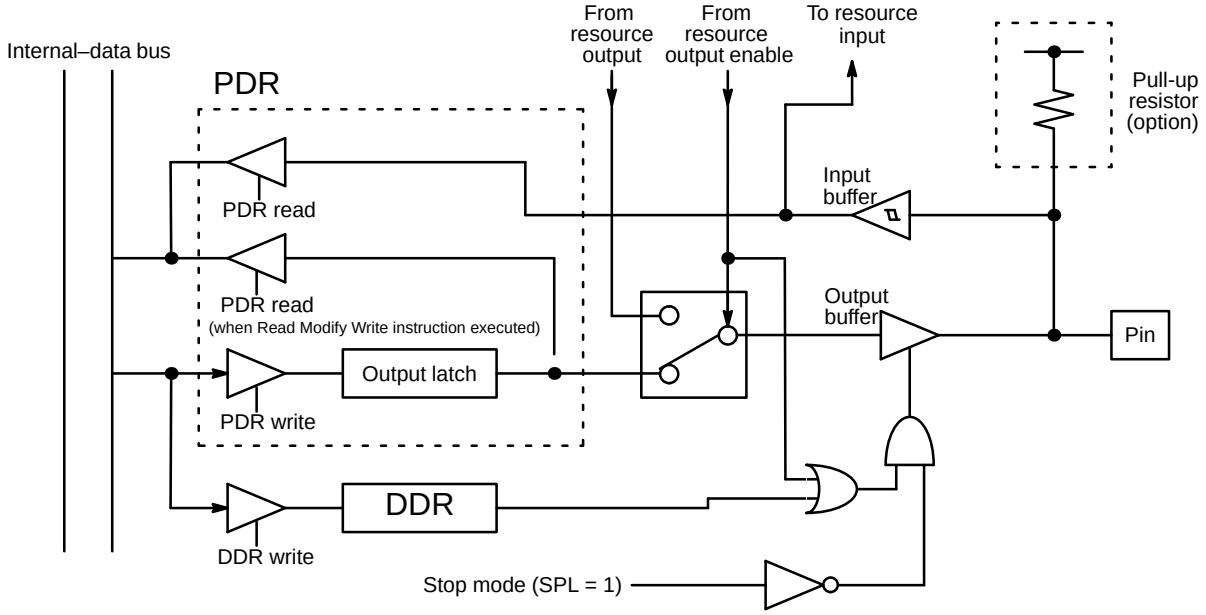


Fig. 2.13 Port 3

(4) P40 to P47: N-ch open-drain-type I/O ports
(used as resource input/output)

- Switching input and output
  These ports have no register for specifying input or output. When using as an input port, set 1 at the PDR.

I/O PORTS

- Operation for output port
  The value written at the PDR is output to the pin. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other.
- Operation for input port
  When using as the input port, set 1 at the PDR to turn off the output transistor. When the PDR is read under this condition, the value of the pin can always be read.
- Operation for resource output
  When using as a resource output, setting is performed by the resource output- enable bit (see description of each resource). Even if output of each resource is enabled, the port can be read other than when the Read Modify Write instruction is read. Therefore, the state of the pin can be checked.
- Operation for resource input
  Input to the resource is not related to the setting conditions of the PDR and the resource. The value of the pin is always input to the port serving as the resource input. When using an external signal at the resource, set 1 at the PDR.
- State when reset
  The PDR is initialized to 1 at reset, so the output register is turned off at all bits.
- State in stop mode
  When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

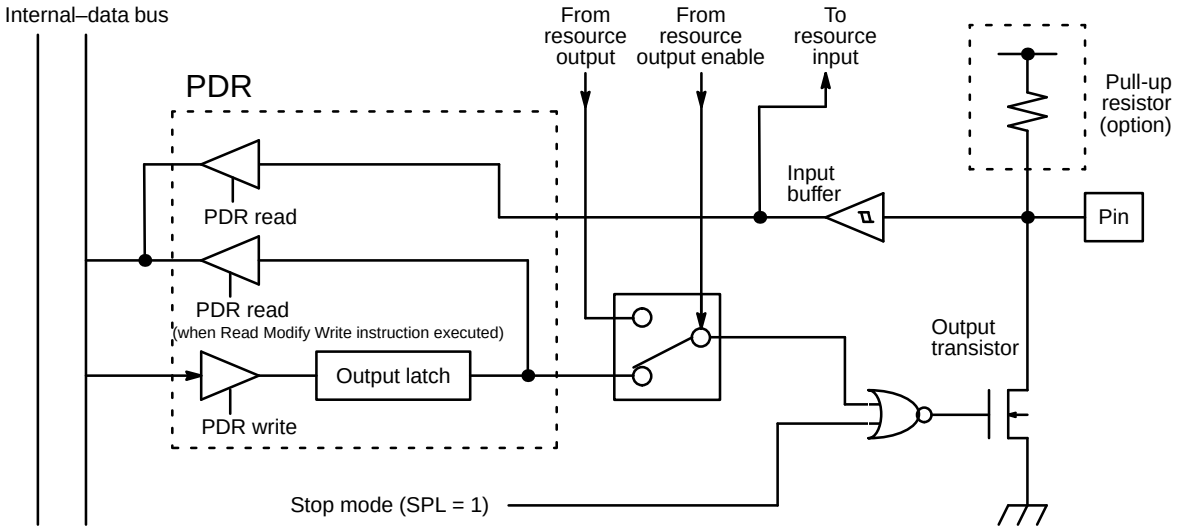


Fig. 2.14 Port 4

(5) P50 to P57 N-ch open-drain-type output ports

- Operation for output port
  The value written at the PDR is output to the pin. When the PDR is read, the contents of the output latch are always read. Therefore, the state of the pin cannot be read.
- State when reset
  When reset, the PDR is initialized to 1. Therefore, the output transistor is turned off at all bits.
- State in stop mode
  When the SPL bit of the standby-control register is set to 1, in the stop mode, the output impedance goes High irrespective of the value of the PDR.

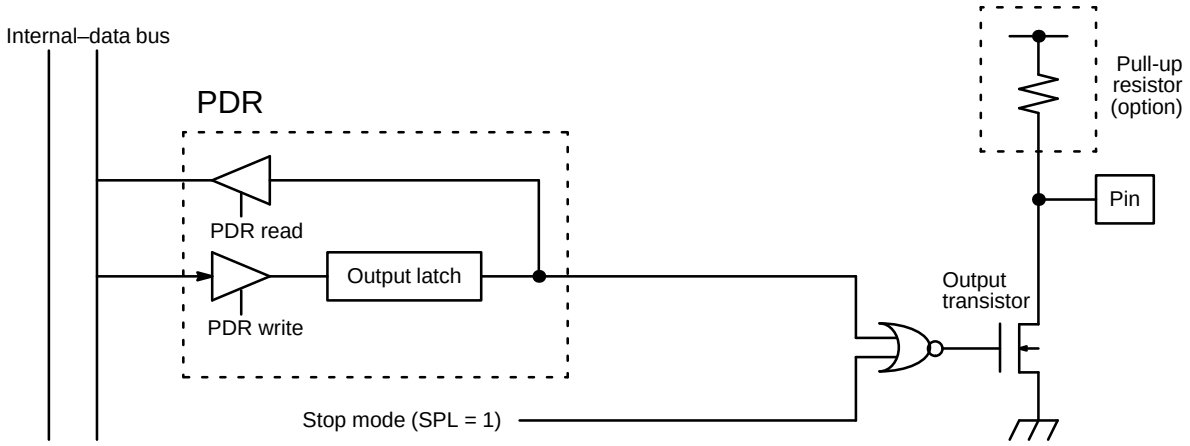


Fig. 2.15 Port 5

(6) P60 to P67 Input-only ports (used as external-interrupt input)

- Operation for external-interrupt input
  See the description of the external interrupts.
- Operation for input port
  The PDR can only be read and the value of the pin is always read. When using as an external-interrupt input, the value of the pin can also be read.

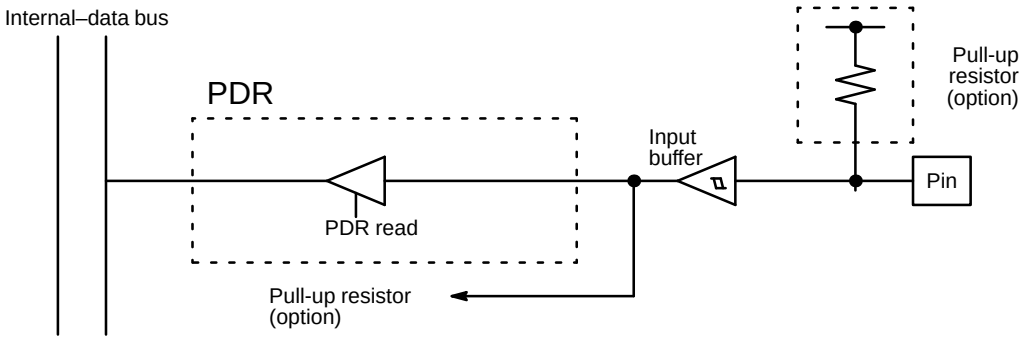


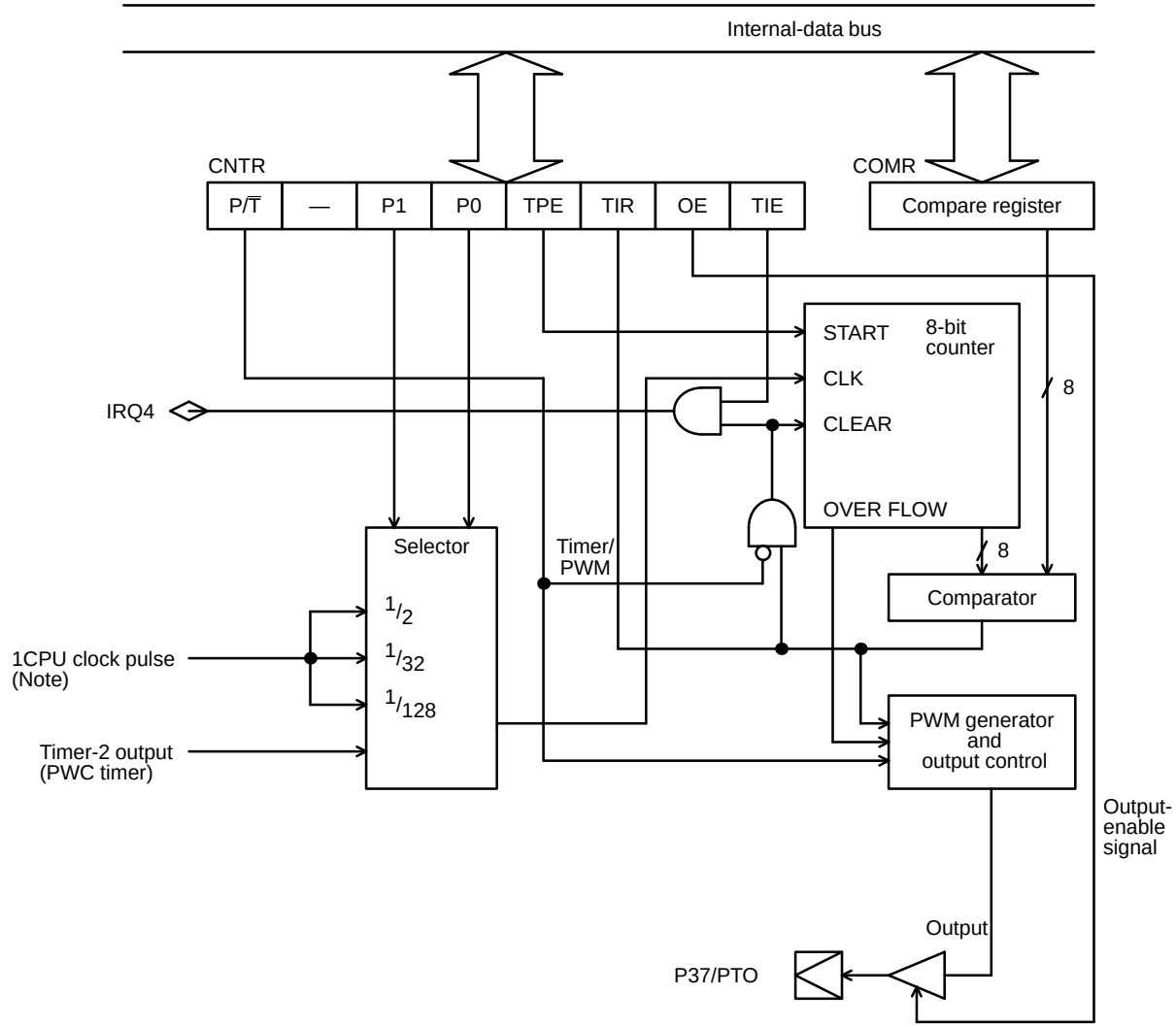
Fig. 2.16 Port 6

8-BIT PWM TIMER (TIMER 1)

2.5 8-BIT PWM TIMER (TIMER 1)

- This timer can be used as an 8-bit timer or PWM-control circuit with 8-bit resolution.
- Four clock pulses can be selected.

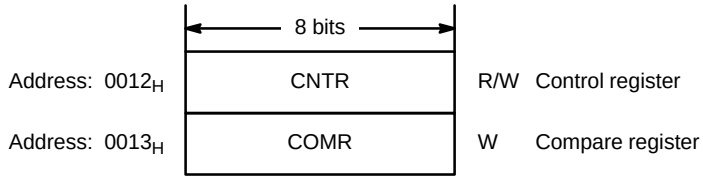
■ Block Diagram



Note: The CPU clock pulse is the pulse with 1/2 oscillation. Free running is performed after canceling the reset.

Fig. 2.17 8-bit PWM Timer Block Diagram

■ Register List



8-BIT PWM TIMER (TIMER 1)

Address: 0012_H CNTR

Address: 0013_H COMR

■ Description of Register Details

(1) Control register (CNTR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0012_H	P/TX	—	P1	P0	TPE	TIR	OE	TIE
	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
				Initial value $0X000000_B$				

[Bit 7] $P/\overline{T}$: Timer/PWM operation-mode switching bit

The operation is performed as the timer when Bit 7 is set to 0, and as the PWM- control circuit when Bit 7 is set to 1.

0	Timer
1	PWM-control circuit

The timer/PWM operation mode should be switched when the counter stops operation (TPE = 0), the interrupt is enabled (TIE = 0), and the interrupt request flag is cleared (TIR = 0).

[Bits 5 and 4] P1 and P0: Clock-pulse select bits

Clock pulses from the prescaler or WT 0 output of timer 2 (pulse-width counter timer) can be selected by P1 and P0.

P1	P0	Clock cycle
0	0	Internal clock pulse 1 instruction cycle
0	1	Internal clock pulse 1/16 instruction cycle
1	0	Internal clock pulse 1/64 instruction cycle
1	1	Timer 2 cycle

Note that these bits must not be rewritten when the counter is in operation (TPE = 1).

[Bit 3] TPE: Counter-operation enable bit

When Bit 3 is set to 1, the timer or PWM-control circuit starts operation.

0	Counter operation stop
1	Counter operation start

[Bit 2] TIR: Interrupt-request flag bit

When an interrupt source occurs, Bit 2 goes to 1. To clear the generated interrupt source, write 0 at this bit. The meaning of each bit to be read is as follows:

0	Values of counter and COMR do not agree
1	Values of counter and COMR agree

8-BIT PWM TIMER (TIMER 1)

Note that 1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

Note: In the PWM operation mode, neither the read nor write values of this bit have any meaning.

[Bit 1] OE: Output-signal control bit

When Bit 1 is 1, the port serves as the timer/PWM output. In the timer operation mode, usually, a signal which is reversed each time the values of the counter and compare register agree, is output. In the PWM operation mode, a PWM signal is output.

0	General-purpose port (P37)
1	Counter/PWM output pin (PTO)

If this bit is 1, the port functions as the timer/PWM output pin even after the DDR of P37 is set to input (bit 7 of DDR3 = 0).

[Bit 0] TIE: Interrupt-enable bit (timer mode)

If Bit 0 is set to 1, an interrupt occurs when the values of the counter and compare register agree.

0	Counter interrupt-output disabled
1	Counter interrupt-output enabled

However, in the PWM operation mode, an interrupt occurs irrespective of the value of this bit.

Address: 0012_H CNTR

Address: 0013_H COMR

(2) Compare register (COMR)

This register is used to set the value to be compared with the value of the counter in the timer-operation mode. The counter is cleared in the timer-operation mode and when the values of the counter and this register agree. In the PWM operation mode, the High pulse width can be specified by the value of this register.

Address: 0013_H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)
			Initial value $XXXXXXXX_B$				

8-BIT PWM TIMER (TIMER 1)

■ Description of Operation

(1) Timer operation

Setting the P/$\overline{T}$ bit (bit 7) of the CNTR to 0 gives the timer-operation mode. When the TPE bit (bit 3) of the CNTR is set to 1, the counter starts incrementing from **00_H**. When the value of the counter agrees with that of the COMR, the counter is cleared on the next count clock pulse and incrementing restarts. Therefore, the TIR bit (bit 2) is set and the output pin is reversed (when the TPE bit (bit 3) is 0, the output pin is fixed at Low level) in cycles of the count clock pulses when **00_H** is written at the COMR, or in cycles 256 times longer than those of the count clock pulses when **FF_H** is written.

If the value of the COMR is rewritten in the timer-operation mode, it becomes effective from the next cycle (when the value of the counter is **00_H**, the value of the COMR is transferred to the comparator latch).

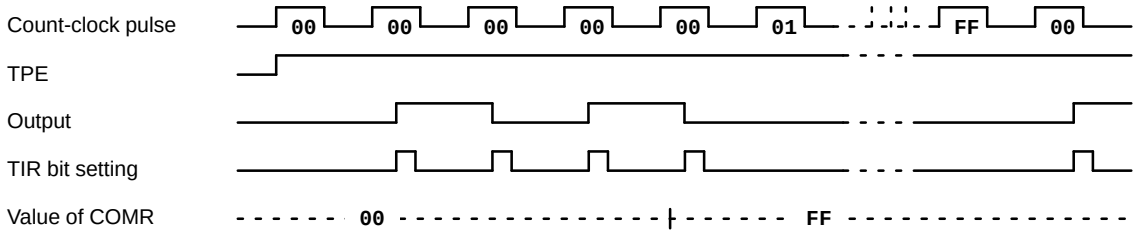


Fig. 2.18 Timer Operation

If the TIE bit (bit 0) of the CNTR is set to 1, an interrupt occurs when the values of the counter and COMR agree. During interrupt processing, the TIR bit (bit 2) is used as the interrupt flag. The TIR bit (bit 2) is set irrespective of the value of the TIE bit (bit 0). However, if the values of the counter and COMR agree, the TIR bit (bit 2) is set to 1 even after an interrupt is disabled.

Writing 0 at the TIR bit (bit 2) permits clearing of the interrupt source or the TIR bit (bit 2). When the Read Modify Write instruction is read, the TIR bit (bit 2) is set so that 1 can always be read to prevent erroneous clearing.
The count clock pulse can be selected from three clock pulses from the prescaler and from pulses from the internal timer by the clock-pulse select bits P0 and P1 of the CNTR.

(2) PWM operation

Setting the P/$\overline{T}$ bit (bit 7) of the CNTR to 1 gives the PWM operation mode. The COMR specifies the duty of the output pulse. Pulses can be output with 1/256 resolution and a duty of 0% to 99.6% .
When 0 (**00_H**) is written at the COMR, the duty of the PWM output pulse is 0%; when 128 (**80_H**) is written, the duty is 50%, and when 255 (**FF_H**) is written, it is 99.6%.
The value of COMR is transferred to the comparator latch when the value of the counter is **00_H**. If the value of the COMR is rewritten in the PWM operation mode, it becomes effective from the next cycle.

8-BIT PWM TIMER (TIMER 1)

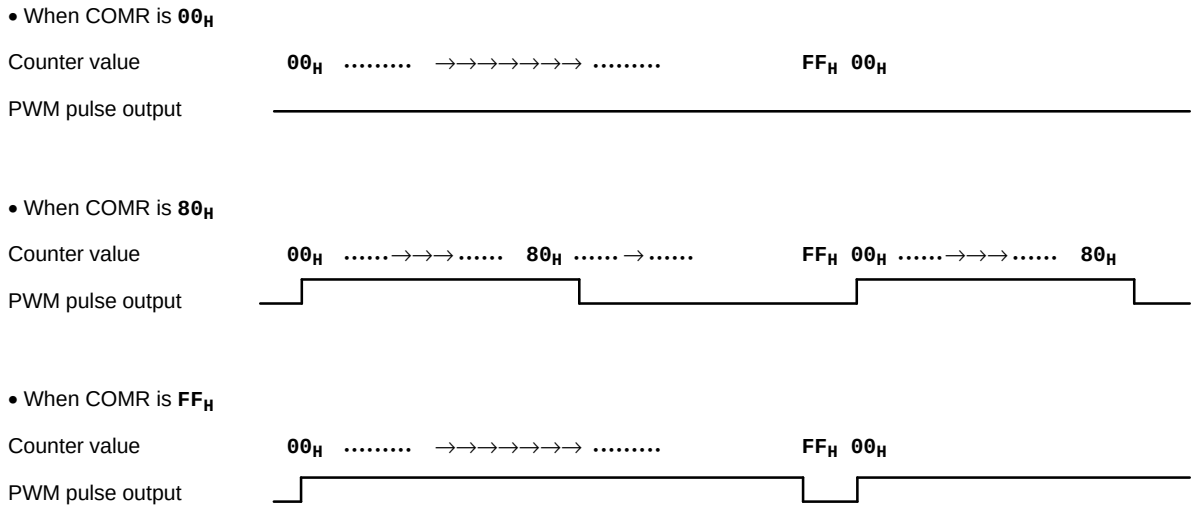


Fig. 2.19 PWM Pulse Output

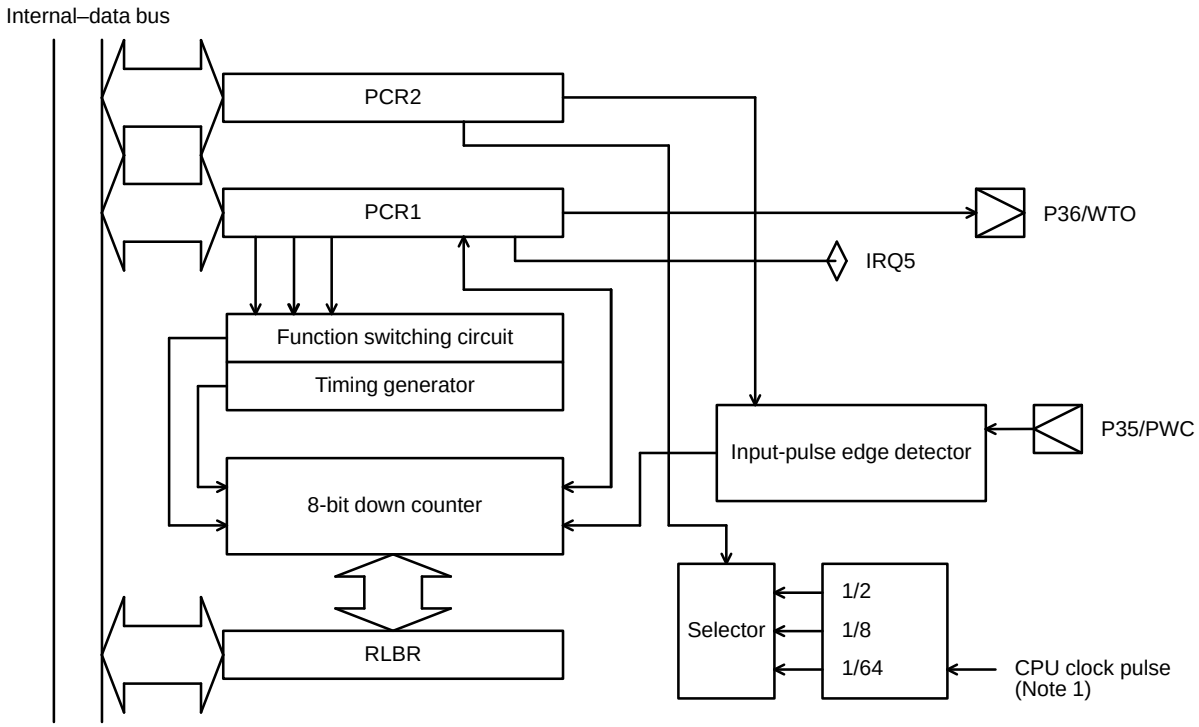
The TIR bit (bit 2) of the CNTR in the PWM operation mode has no meaning. No interruption occurs even if the TIE bit (bit 0) is 1.
The cycle of the PWM pulse can be changed by switching the count clock pulse. The count clock pulse can be selected from three clock pulses from the prescaler and from pulses from the internal timer by clock-pulse select bits P0 and P1 of the CNTR.

PULSE-WIDTH COUNT TIMER (TIMER 2)

2.6 PULSE-WIDTH COUNT TIMER (TIMER 2)

- This timer has timer and pulse-width measurement functions.
- The timer function has two modes: reload timer and one-shot timer.
- In the reload-timer mode, the set values are decremented repeatedly.
- In the one-shot-timer mode, decrementing is started from the set value and stops at the first underflow.
- The pulse-width measurement function allows measurement of High, Low, or one-cycle widths of pulses input from pins.

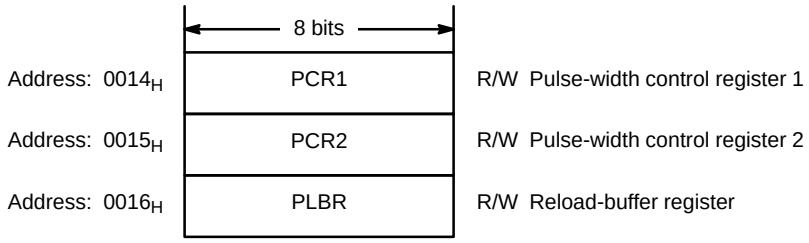
■ Block Diagram



Note 1: The CPU clock pulse is the pulse with 1/2 oscillation.

Fig. 2.20 Pulse-width Timer Block Diagram

■ Register List



PULSE-WIDTH COUNT TIMER (TIMER 2)

Address: 0014_H PCR1

Address: 0015_H PCR2

Address: 0016_H PLBR

■ Description of Register Details

(1) Pulse-width control register 1 (PCR1)

This PCR1 is used to enable and disable each function and to display the state of the timer.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0014_H	EN	TOE	IE	—	—	UF	IR	BF
	(R/W)	(R/W)	(R/W)			(R/W)	(R/W)	(R)
	Initial value $000XX000_B$							

[Bit 7] EN: Counter-operation enable bit

At the timer function, when 1 is written at this bit, the value of the data register is loaded to start the decrementing. At the pulse-width measurement function, when 1 is written at this bit, the measurement-enable state is set. Under this condition, decrementing starts when the edge of the measured pulse is detected. When 0 is written at this bit during measurement, the operation stops but the value of the counter is not transferred to the buffer (RLBR).

	Timer function	Pulse-width measurement function
0	Count-operation disable	Pulse-width measurement function stop/disable
1	Count-operation enable/start	Pulse-width measurement function enable/start

[Bit 6] TOE: TO bit output-enable bit

When Bit 6 is set to 1, the contents of the TO bit are output to port P36.

0	General-purpose port (P36)
1	TO bit output (WTO)

If this bit is set to 1 even after the DDR of P36 is set to input, the port functions as the TO bit output port.

[Bit 5] IE: Interrupt-enable bit

When Bit 5 is 1, an interrupt request is output if the interrupt-request flags (UF, IR, and BF) are set.

0	Interrupt disable
1	Interrupt enabled

[Bit 2] UF: Underflow interrupt-request bit

Bit 2 indicates the presence or absence of timer overflow. The meaning of each bit to be read is as follows:

0	Underflow does not occur.
1	Underflow occurs.

PULSE-WIDTH COUNT TIMER (TIMER 2)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 1] IR: Bit for interrupt request at measurement termination

When the IE bit (bit 5) of the PCR1 is 1, an interrupt occurs at termination of pulse measurement. The meaning of each bit to be read is as follows:

0	Pulse-width measurement not terminated
1	Pulse-width measurement terminated

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 0] BF: Buffer-full flag

When the IE bit (bit 5) of the PCR1 is 1, an interrupt occurs if any measured value is found in the RDBR. This bit is set when the pulse-width measurement is terminated, and is cleared when data in the buffer is read. The meaning of each bit to be read is as follows:

0	Pulse-width measured value not found
1	Pulse-width measured value found

Address: 0014_H PCR1

Address: 0015_H PCR2

Address: 0016_H PLBR

(2) Pulse-width control register 2 (PCR2)

The PCR2 is used to select the timer operation modes.
Rewriting is possible only when bit 7 (EN) of the PCR1 is 0.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0015_H	FC	RM	TO	—	C1	C0	W1	W0
	(R/W)	(R/W)	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)
				Initial value $000X0000_B$				

[Bit 7] FC: Function-select bit

Bit 7 is used to select the timer and pulse-width measurement functions.

0	Timer function
1	Pulse-width measurement function

PULSE-WIDTH COUNT TIMER (TIMER 2)

[Bit 6] RM: Timer mode-select bit

At the timer function, this bit is used to select the modes below.

0	Reload-timer mode
1	One-shot timer mode

[Bit 5] TO: Timer-output bit

The value of Bit 5 is reversed each time the counter underflows. When the TOE bit (bit 6 of PCR1) is 1, the contents of this bit are output from the WTO pin.

[Bits 3 and 2] C1 and C0: Counter clock-pulse select bits

Setting is made as shown below by a combination of these bits. These bits are not related to the value of the FC bit.

C1	C0	Count clock pulse
0	0	Internal clock pulse 1 instruction cycle
0	1	Internal clock pulse 1/4 instruction cycle
1	0	Internal clock pulse 1/32 instsruction cycle
1	1	Do not set.

[Bits 1 and 0] W1 and W0: Measured pulse-select bit

Setting is made as shown below by a combination of these bits. These bits are not relevant in the timer-operation mode (FC = 0).

W1	W0	Measured pulse width
0	0	High level
0	1	Low level
1	0	Rising edge - rising edge
1	1	Falling edge - falling edge

Address: 0014_H PCR1

Address: 0015_H PCR2

Address: 0016_H PLBR

(3) Reload buffer register (PLBR)

At the timer function, this register can be read and written. At the pulse-width measurement function, it functions as the read-only data buffer register used for holding the measured value. In this case, writing is impossible. Data is read to clear the BF flag (bit 0) of the PCR1.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0016_H								
At timer function ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
At pulse-width measurement function ⇒	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
				Initial value				
				$XXXXXXXX_B$				

PULSE-WIDTH COUNT TIMER (TIMER 2)

■ Description of Operation

(1) Timer function

This timer has the following two modes: reload timer and one-shot timer.

(a) Reload timer mode

Each time the counter underflows, the value written at the RLBR is reloaded to continue the decrementing. When the counter underflows, the interrupt flag UF (bit 2) is set. If the IE bit (bit 5) is set to 1, an interrupt request is output. If the TOE bit (bit 6) is set to 1, the value of the TO bit is reversed each time the timer underflows.

(b) One-shot timer mode

When an underflow occurs, the timer stops operation. When the counter underflows, the interrupt request flag UF (bit 2) is set. The EN bit (bit 7) is automatically set to 0 to stop counting.
In both modes, counting starts when 1 is written at the EN bit (bit 7), and it stops when 0 is written.

(2) Pulse-width measurement function

(a) Measurement start

Writing 1 at the FC bit (bit 7) and EN bit (bit 7) causes the counter to enter the operation-enable state. Counting starts when the edge of the measured pulse input is detected under this condition. At the pulse-width measurement function, decrementing is started from FF_H.

(b) Measurement end and measured value

When measurement is terminated, the counter transfers the measured value to the buffer, sets the measurement-end flag IR (bit 1) and buffer-full flag BF (bit 0), and then enters the operation-enable state again. At this time, an interrupt request is output if the IE bit (bit 5) is set to 1. However, if the previous measured value cannot be read after continuous pulse-width measurement, continue to set the BF flag to hold the previous measured value. The new measured value is discarded.

(c) Long pulse

If the counter undeflows during measurement, set the UF bit (bit 2) to continue counting. In this case, an interrupt request is also output if the IE bit (bit 5) is set to 1.

(d) Operation stop

Measurement stops when 0 is written at the EN bit (bit 7).

PULSE-WIDTH COUNT TIMER (TIMER 2)

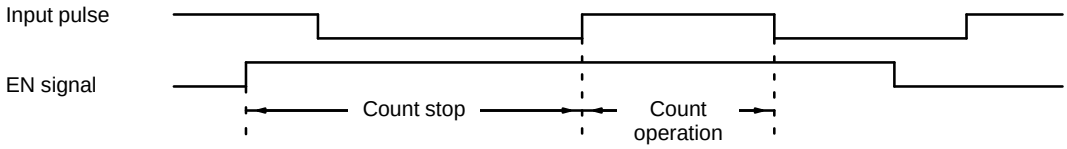
(e) Calculation of pulse width

The measured value to be transferred to the buffer is the same as that of the counter when measurement is terminated. Therefore, the pulse width should be calculated as follows:

Pulse width = [(256 - counter value) + (Number of TO reversed x 256)] x 1 cycle width of count clock pulse

(f) Others

The counter is in the operation-enable state even after the end of measurement, so continuous pulse-width measurement is enabled. The High width measurement is started from the changing edge of the input pulse. If the input pulse is already High, enable the EN bit (0 ⇒1) to perform counting after the next rising edge occurs.



High Width Measurement

■ Precautions for use

(1) When the EN bit is 1 (during timer operation or pulse-width measurement), do not rewrite the contents of the PCR2.

(2) When the mode is switched (the FC bit is rewritten), the state of each flag does not change. Therefore, clear each flag immediately after switching the mode.

(3) Read the measured value before the next underflow occurs. If the value is read after an underflow occurs, the TO bit is reversed, sometimes disabling calculation of the correct measured value.

(4) If the previous measured value cannot be read after continuous pulse-width measurement, hold the previous measured value without transferring the new one to the buffer.

16-BIT TIMER/COUNTER (TIMER 3)

2.7 16-BIT TIMER/COUNTER (TIMER 3)

- 16-bit binary timer/counter
- It is possible to select the timer function for count-clocking internal clock sources and the counter function for counting by detecting an arbitrary edge of the external pin input.
- An arbitrary byte value can be written from the data bus to the counter.
- An interrupt request can be output to the CPU by detecting counter overflow.

■ Block Diagram

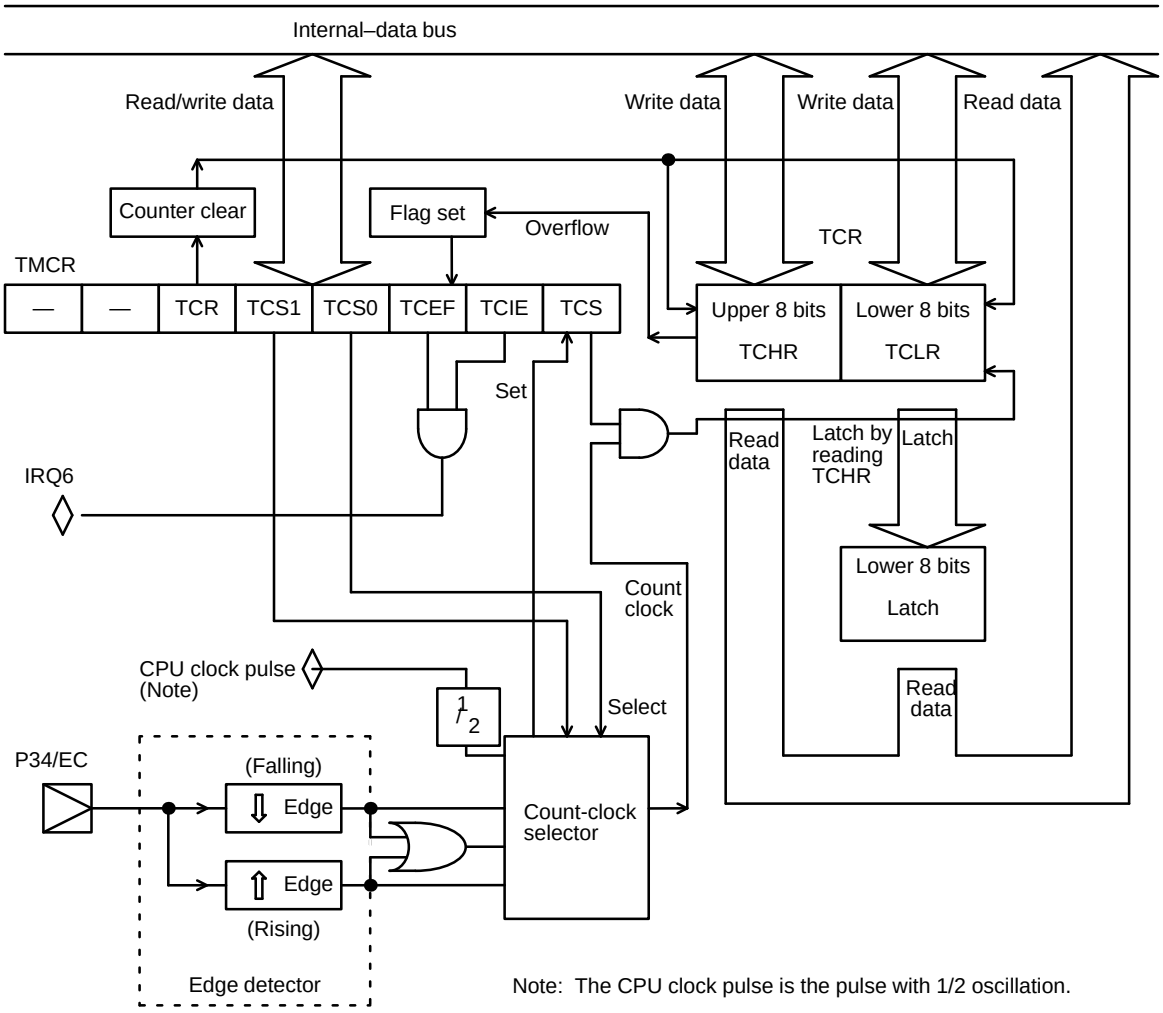
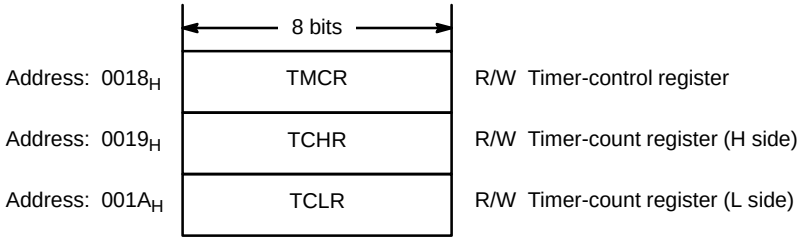


Fig. 2.21 16-bit Timer/Counter Block Diagram

16-BIT TIMER/COUNTER (TIMER 3)

■ Register List



■ Description of Register Details

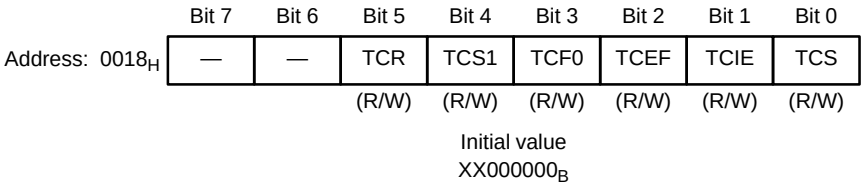
(1) Timer-control register (TMCR)

This 6-bit register selects and controls various operations of the counter, and controls interrupts.

Address: 0018_H TMCR

Address: 0019_H TCHR

Address: $001A_H$ TCLR



[Bit 5] TCR: Counter-clear bit

Bit 5 is used to clear the counter. The meaning of each bit to be written is as follows:

0	Counter cleared - The contents of the 16-bit counter are set to 0000_H.
1	Other counters not affected

The read value of this bit is always 1.

[Bits 4 and 3] TCS1 and TCS0: Timer/counter operation-mode select bits

These bits are used to select the timer/counter operation mode and to determine the detection edge of the external-count clock pulse to be detected in the counter- operation mode. The counter-operation mode and the detection edge of the external-count clock pulse are selected as shown below.

Table 2-7 Selection of Timer/Counter Operation Mode

TCS1	TCS0	Operation mode	
0	0	Timer mode (Internal clock source operation)	
0	1	Counter mode	Detect falling edge of external input.
1	0		Detect rising edge of external input.
1	1		Detect both edges of external input.

16-BIT TIMER/COUNTER (TIMER 3)

Note: The DDR of P34 must always be set to input when TSC0 and TCS1 are other than 00_B (using EC input).

[Bit 2] TCEF: Interrupt-request flag

Bit 2 is a flag for interrupt request due to counter overflow. The meaning of each bit to be read is as follows:

0	Counter does not overflow.
1	Counter overflows (counter value $FFFF_H \Rightarrow 0000_H$).

Note: 1 is always read when the Read Modify Write instruction is read. When interrupt-output is enabled (TCIE = 1), an interrupt request is output to the CPU if this bit is 1.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 1] TCIE: Interrupt-request output-enable bit

Bit 1 is used to enable and disable interrupt output to the CPU. When the bit is 1, an interrupt request is output if the interrupt flag TCEF (bit 2) is set to 1. When the bit is 0, interrupt-request output is disabled.

0	Interrupt-request output disabled.
1	Interrupt-request output disabled.

[Bit 0] TCS: Count start bit (counter-enable bit)

Bit 0 is used to start and stop the counter. When 1 is written at this bit, the TCR is enabled for counting and the value of the counter is incremented by the count clock. When 0 is written, the TCR stops counting to hold the value of the counter.

0	Count disabled
1	Count enabled

(2) Timer-count register (TCR)

The TCR is a 16-bit binary up counter. It is used for upper bytes; the TCLR is used for lower bytes. Writing to the counter should be performed when counting stops (TCS bit (bit 0) of TMCR = 0). To read the counter, always use the word transfer instructions (MOVW A, dir, etc.).

Address: 0018_H TMCR

Address: 0019_H TCHR

Address: $001A_H$ TCLR

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0019_H								
Address: $001A_H$								
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value	00000000_B							
	00000000_B							

16-BIT TIMER/COUNTER (TIMER 3)

■ Description of functions

(1) Operation modes

The operation modes of the 16-bit timer/counter can be selected from the timer and counter modes by a combination of bit 3 (TCS0) and bit 4 (TCS1) of the TMCR.

(a) Timer mode

Setting values other than $\mathbf{00_B}$ at bit 3 (TCS0) and bit 4 (TCS1) of the TMCR gives the timer mode. The TCR increments according to the internal clock source (1/4 oscillation or instruction cycle); external-count input is disabled at this time. Detecting an overflow enables generation of time intervals up to 2^{16} times the clock source (65536 instruction cycles). The maximum time intervals are 32.8 ms at 8 MHz oscillation.

(b) Counter mode

Setting values other than 00_B at bit 3 (TCS0) and bit 4 (TCS1) of the TMCR gives the counter mode. The edge polarities given in Table 2-5-1 can be selected according to the value to be set. The counter mode is divided into three according to the setting of the edge detection for the external-count input. In the counter mode, the TCR increments each time the arbitrary edge of the EC input for the external-count clock pin is detected. (The internal clock source is disabled at this time.) This enables counting with the number of external-count input events (arbitrary edges). The pulse width of the external-count clock input can be input at a minimum width of two instruction cycles.

(2) Count start/stop

The TCR starts counting when 1 is written at bit 0 (TCS) of the TMCR, and stops counting when 0 is written.

(3) Counting and interrupt occurrence

In the timer mode, the TCR is incremented every one instruction cycle of the clock source; in the counter mode, it is incremented each time the effective edge of the external-count input is detected. When the counter value changes from $\mathbf{FFFF_H}$ to $\mathbf{0000_H}$ (overflows), an overflow-interrupt request is output to the CPU if the interrupt flag TCEF (bit 2) of the TMCR is set to 1 and the interrupt-request output-enable bit TCIE (bit 1) is 1.

Any byte value can be set at the TCR. (This setting should be done when the counter stops (TCS = 0).) The value of the TCR can be read even during operation. To read, always use the word-transfer instructions (MOVW A, dir, etc.).

(4) Counter clear

The TCR is cleared to $\mathbf{0000_H}$ when 0 is written at bit 5 (TCR) of the TMCR. If clearing is performed concurrently with overflow, the interrupt flag is not set.

16-BIT TIMER/COUNTER (TIMER 3)

■ Precautions for use

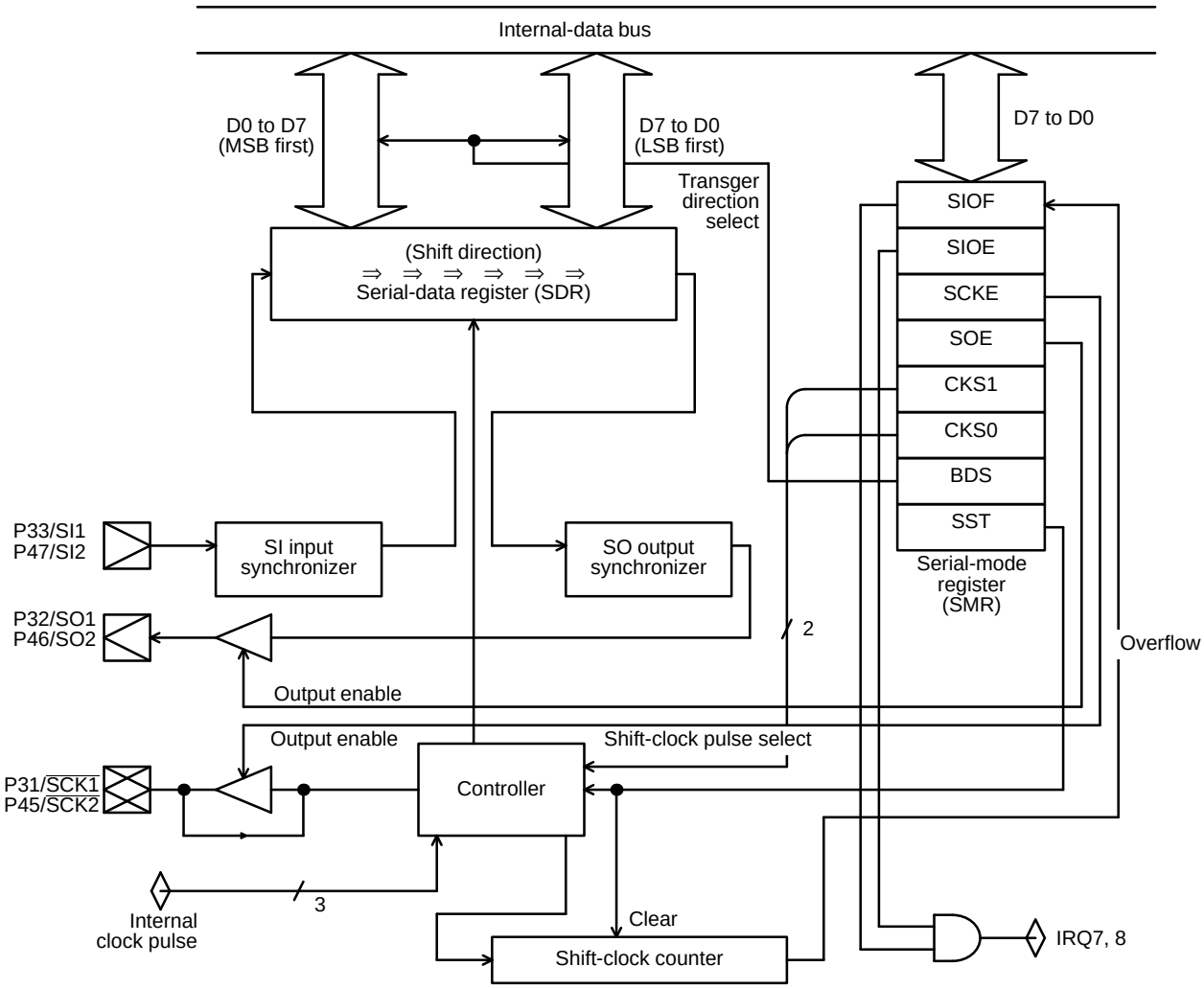
Interrupts should be disabled by the TCIE bit:
”With interrupt acceptance disabled by the I flag of the condition code register (CCR)”
”With interrupts for the 16 bit timer/counter disabled by the interrupt level register (ILR)”

8-BIT TIMER/COUNTER (TIMER 3)

2.8 8-BIT SERIAL I/O 1 AND 2

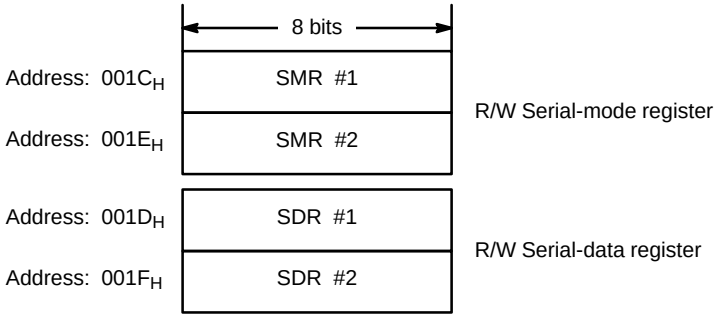
- 8-bit serial data transfer is possible by the clock synchronous method.
- LSB first or MSB first can be selected for data transfer.
- Four shift-clock modes (three internal and one external) can be selected.
- There are two-channel serial ports with the same functions.

■ Block diagram



8-BIT TIMER/COUNTER (TIMER 3)

■ Registers



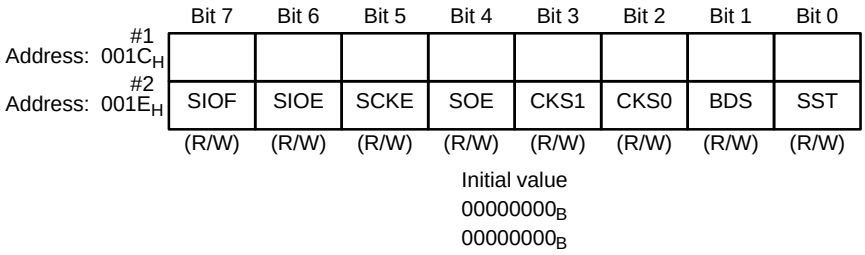
■ Description of Register Details

(1) Serial-mode register (SMR)

The SMR is used to control serial I/O.

Address: 001C$_H$ SMR #1

Address: 001E$_H$ SMR #2



[Bit 7] SIOF: Serial I/O interrupt-request flag

Bit 7 indicates the serial I/O transfer state.
The meaning of each bit to be read is as follows:

0	Serial data transfer not terminated
1	Serial data transfer terminated

Note that 1 is always read when the Read Modify Write instruction is read. If this bit is set when an interrupt is enabled (SIOE = 1), an interrupt request is output to the CPU.
The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

The end-of-transfer decision may be made by either the SST bit (bit 0) of the SMR or by this bit.

[Bit 6] SIOE: Serial I/O interrupt-enable bit

Bit 6 is used to enable a serial I/O interrupt request.

0	Serial I/O interrupt-output disable
1	Serial I/O interrupt-output enable

8-BIT TIMER/COUNTER (TIMER 3)

[Bit 5] SCKE: Shift-clock output-enable bit

Bit 5 is used to control the shift-clock I/O pins.

0	General-purpose port pins (P31, P45) or SCK input pin
1	SCK (shift clock) output pin

When using the P31/$\overline{SCK1}$ and P45/$\overline{SCK2}$ pins as external clocks, always set the DDR to input (bit 1 of DDR3 = 0, bit 5 of PDR4 = 1).

[Bit 4] SOE: Serial-data output-enable bit

Bit 4 is used to control the output pins for serial I/O.

0	General-purpose port pins (P32, P46)
1	SO (serial data) output pin

When using P33/SI1 and P47/SI2 pins as the SI pin, always set the DDR to input (bit 3 of DDR3 = 0, bit 7 of PDR4 = 1).

[Bits 3 and 2] CKS1 and CKS0: Shift-clock select bits

Bits 3 and 2 are used to select the serial shift-clock modes.

CKS1	CKS0	Mode (Clock rate)	SCK
0	0	Internal shift-clock mode (1/2 instruction cycle)	Output
0	1	Internal shift-clock mode (1/8 instruction cycle)	Output
1	0	Internal shift-clock mode (1/32 instruction cycle)	Output
1	1	External shift-clock mode (SCK)	Input

[Bit 1] BDS: Transfer direction select bit

At serial data transfer, Bit 1 is used to select whether data transfer is performed from the least significant bit first (LSB first) or from the most significant bit first (MSB first).

0	LSB first
1	MSB first

Note that when this bit is rewritten after writing data to the SDR, the data become invalid.

[Bit 0] SST: Serial I/O transfer-start bit

Bit 0 is used to start serial I/O transfer. The bit is automatically cleared to 0 when transfer is terminated.

0	Serial I/O transfer stop.
1	Serial I/O transfer start.

Before starting transfer, ensure that transfer is stopped (SST = 0).

8-BIT TIMER/COUNTER (TIMER 3)

Address: $001D_H$ SDR #1

Address: $001F_H$ SDR #2

(2) Serial-data register (SDR)

This 8-bit register is used to hold serial I/O transfer data. Do not write data to this register during the serial I/O operation.

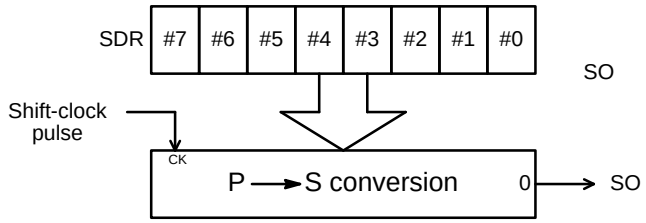
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
#1 Address: $001D_H$								
#2 Address: $001F_H$								
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value								
	$XXXXXXXX_B$							
	$XXXXXXXX_B$							

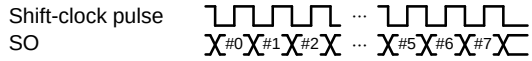
■ Description of operation

(1) Outline

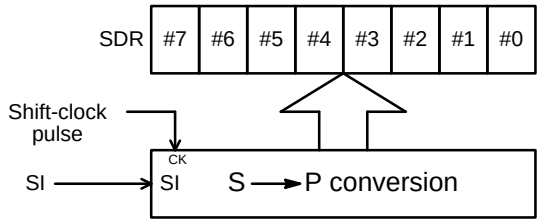
This module consists of the serial-mode register (SMR) and serial-data register (SDR). At serial output, data in the SDR is output in bit serial to the serial output pin (SO) in synchronization with the falling edge of a serial shift-clock pulse generated from the internal or external clock. At serial input, data is input in bit serial from the serial input pin (SI) to the SDR at the rising edge of a serial shift-clock pulse.

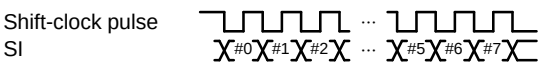
Serial output





Serial input





8-BIT TIMER/COUNTER (TIMER 3)

(2) Operation modes

The serial I/O has three internal shift-clock modes and one external shift-clock mode, which are specified by the SMR. Mode switching or clock selection should be made with serial I/O stopped (SST bit (bit 0) of SMR = 0).

(a) Internal shift-clock mode

Operation is performed by the internal clock. A shift-clock pulse with a duty of 50% is output from the SCK pin as a synchronous timing output. Data is transferred bit-by-bit at every clock pulse.

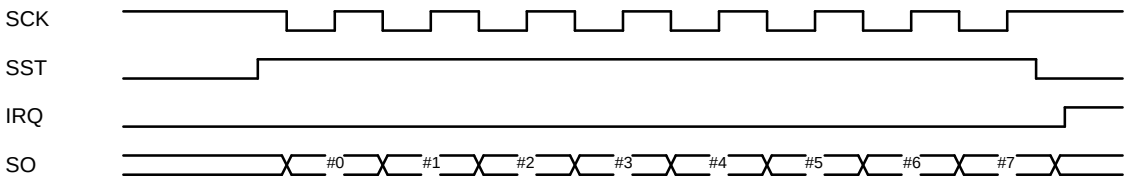
(b) External shift-clock mode

Data is transferred bit-by-bit at every clock pulse in synchronization with the external shift-clock pulse input from the SCK pin. The transfer speed can be from DC to 1/2 oscillation (two instruction cycles). When one instruction cycle is 0.4 μs (at 10 MHz oscillation), the transfer speed can be up to 1.25 MHz.

Do not write data to the SMR and SDR during the serial I/O operation in either mode.

(3) Interrupt functions

This module can output an interrupt request to the CPU. To output an interrupt request, set the SIOE bit (bit 6) of the SMR to 1 to enable an interrupt and then set the interrupt flag SIOF (bit 7) of SMR after 8-bit data transfer is terminated.

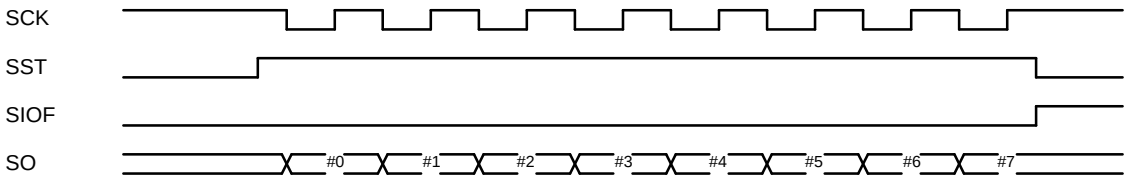


(4) Shift start/stop timing

Data transfer starts when 1 is written at the SST bit (bit 0) of the SMR, and stops when 0 is written. When data transfer is terminated, the SST bit is automatically cleared to 0, which stops the operation.

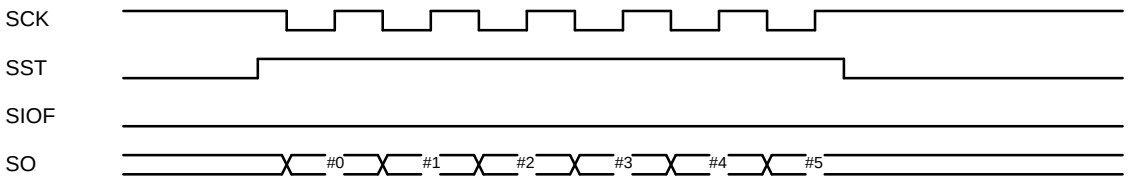
(a) Internal shift-clock mode (LSB first)

[When transfer terminated]



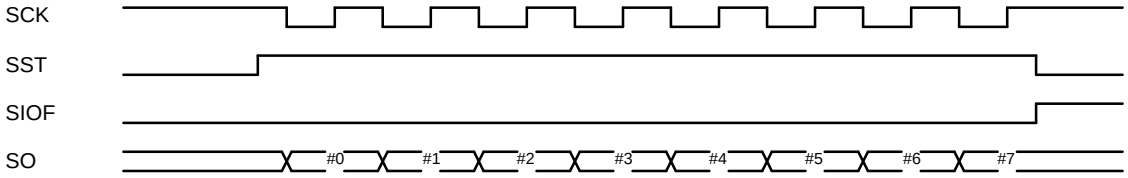
8-BIT TIMER/COUNTER (TIMER 3)

[When transfer suspended]

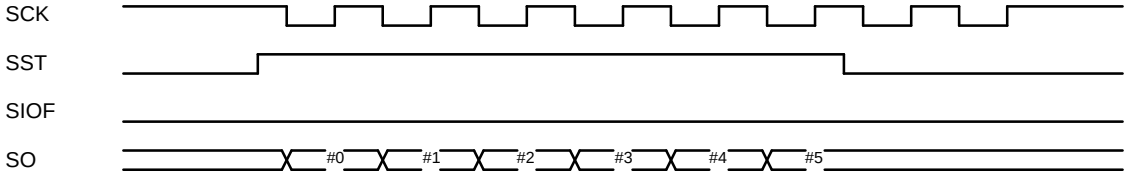


(b) External shift-clock mode (LSB first)

[When transfer terminated]



[When transfer suspended]



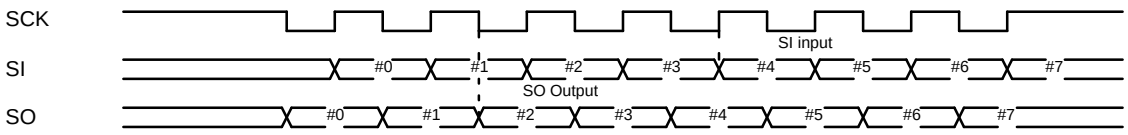
Note: When data is written at the SDR, the output data changes at the falling edge of the external-clock pulse.

Fig. 2.22 Shift Start/Stop Timing

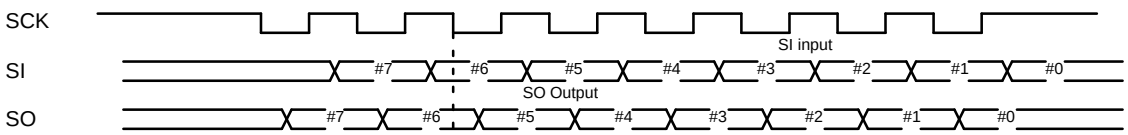
(5) Input/output shift timing

Data is output from the serial output pin (SO) at the falling edge of the shift-clock pulse, and is input from the serial input pin (SI) to the SDR at the rising edge of the shift-clock pulse.

(a) LSB first (BDS = 0)



(b) MSB first (BDS = 1)



DI7 to DI0 indicate input data, and DO7 to DO0 indicate output data.

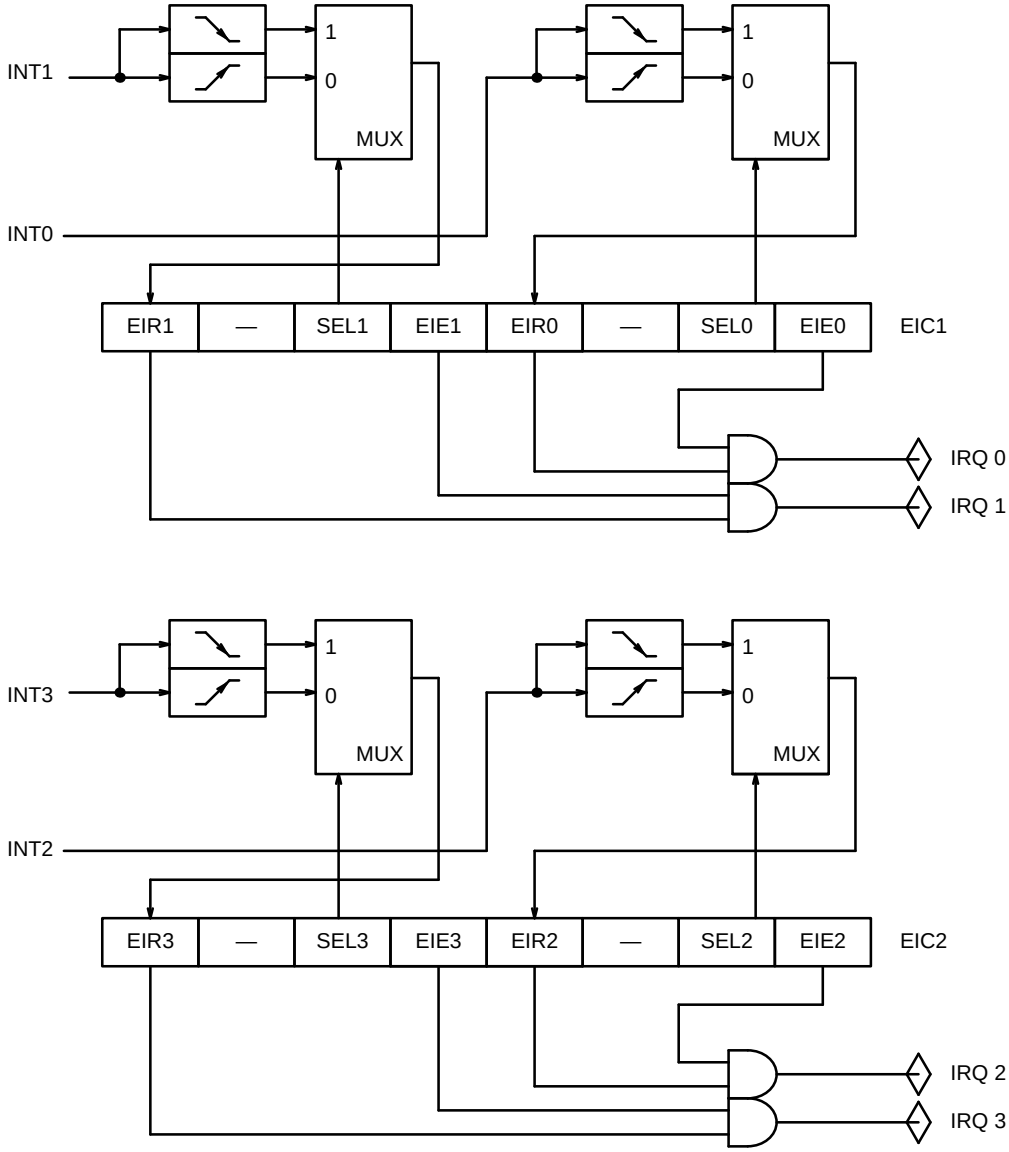
Fig. 2.23 Input/Output Shift Timing

EXTERNAL INTERRUPT CIRCUIT

2.9 EXTERNAL INTERRUPT CIRCUIT

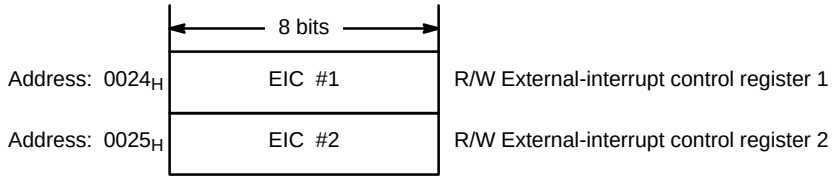
- The edges of four external-interrupt sources (INT0 to INT3) can be detected to set the corresponding flag.
- An interrupt can be generated at the same time the flag is set.
- The four interrupts can release the STOP or SLEEP mode.

■ Block diagram



EXTERNAL INTERRUPT CIRCUIT

■ Registers



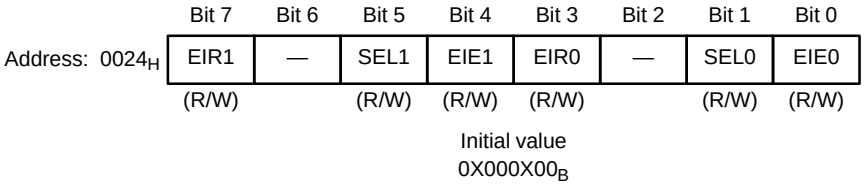
■ Description of registers

(1) External-interrupt control register 1 (EIC1)

The EIC1 controls interrupts by the INT0 and INT1 pins.

Address: 0024_H EIC

Address: 0025_H EIC



[Bit 7] EIR1: External-interrupt request flag

When the edge specified by the SEL1 bit is input to the INT1 pin, bit 7 is set to 1. When the EIE1 bit is 1, an interrupt request (IRQ1) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT1 pin
1	Specified edge input to INT1 pin (IRQ1 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 5] SEL1: Edge-polarity select bit

Bit 5 is used to control the input edge polarity of the INT1 pin.

0	Rising edge
1	Falling edge

[Bit 4] EIE1: Interrupt-enable bit

Bit 4 is used to enable an external-interrupt request by the INT1 pin.

0	Interrupt request disabled
1	Interrupt request enabled by EIR1 setting

[Bit 3] EIR0: External-interrupt request flag

EXTERNAL INTERRUPT CIRCUIT

When the edge specified by the SEL0 bit is input to the INT0 pin, bit 3 is set to 1. When the EIE0 is 1, an interrupt request (IRQ0) is output if this bit is set.
The meaning of each bit to be read is as follows:

0	Specified edge not input to INT0 pin
1	Specified edge input to INT0 pin (IRQ0 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 1] SEL0: Edge-polarity select bit
Bit 1 is used to control the input edge polarity of the INT0 pin.

0	Rising edge
1	Falling edge

[Bit 0] EIE0: Interrupt-enable bit
Bit 0 is used to enable an external-interrupt request by the INT0 pin.

0	Interrupt request disabled
1	Interrupt request enabled by EIR0 setting

(2) External-interrupt control register 2 (EIC2)

The EIC2 controls an interrupt by the INT2 and INT3 pins.

Address: 0024_H EIC

Address: 0025_H EIC

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0025_H	EIR3	—	SEL3	EIE3	EIR2	—	SEL2	EIE2
	(R/W)		(R/W)	(R/W)	(R/W)		(R/W)	(R/W)
				Initial value $0X000X00_B$				

[Bit 7] EIR3: External-interrupt request flag
When the edge specified by the SEL3 bit is input to the INT3 pin, bit 7 is set to 1. When the EIE3 bit is 1, an interrupt request (IRQ3) is output if this bit is set.
The meaning of each bit to be read is as follows:

0	Specified edge not input to INT3 pin
1	Specified edge input to INT3 pin (IRQ3 is output.)

EXTERNAL INTERRUPT CIRCUIT

1 is always read when the Read Modify Write instruction is read.
The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 5] SEL3: Edge-polarity select bit
Bit 5 is used to control the input edge polarity of the INT3 pin.

0	Rising edge
1	Falling edge

[Bit 4] EIE3: Interrupt-enable bit
Bit 4 is used to enable an external-interrupt request by the INT3 pin.

0	Interrupt request disabled
1	Interrupt request enabled by setting of EIR3

[Bit 3] EIR2: External-interrupt request flag
When the edge specified by the SEL2 bit is input to the INT2 pin, bit 3 is set to 1. When the EIE2 is 1, an interrupt request (IRQ2) is output if this bit is set.
The meaning of each bit to be read is as follows:

0	Specified edge not input to INT2 pin
1	Specified edge input to INT2 pin (IRQ2 is output.)

1 is always read when the Read Modify Write instruction is read.
The meaning of each bit to be written is as follows:

0	This bit is cleared.
1	This bit does not change nor affect other bits.

[Bit 1] SEL2: Edge-polarity select bit
Bit 1 is used to control the input edge polarity of the INT2 pin.

0	Rising edge
1	Falling edge

[Bit 0] EIE2: Interrupt-enable bit
Bit 0 is used to enable an external-interrupt request by the INT2 pin.

0	Interrupt request disabled
1	Interrupt request enabled by setting of EIR2

EXTERNAL INTERRUPT CIRCUIT

■ Precautions for external-interrupt circuit

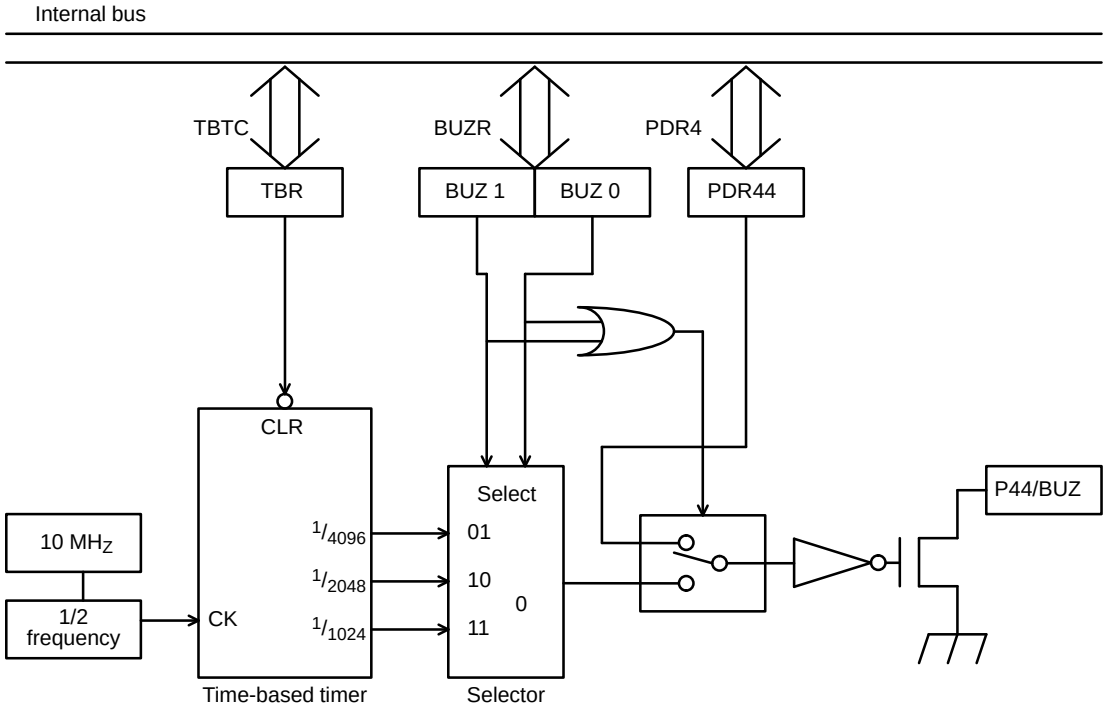
When enabling an interrupt after clearing reset, always clear the interrupt flag simultaneously. An interrupt request is output immediately when the interrupt flags (EIR3, EIR2, EIR1, EIR) are set to 1.

BUZZER OUTPUT CIRCUIT

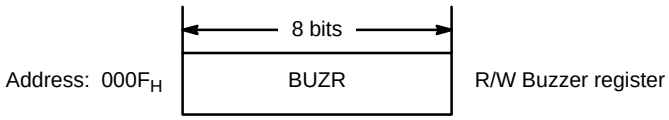
2.10 BUZZER OUTPUT CIRCUIT

- The buzzer output sound for checking key input can be output from port 44.
- Three frequencies can be output by setting the registers.

■ Block diagram



■ Registers



■ Detailed description of registers

(1) Buzzer register (BUZR)

This register enables buzzer output and selects the frequency.

Address: $000F_H$ BUZR

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $000F_H$	—	—	—	—	—	—	BUZ1	BUZ0
							(R/W)	(R/W)
Initial value								
$XXXXXX00_B$								

BUZZER OUTPUT CIRCUIT

[Bits 1 and 0] BUZ1 and BUZ0: Buzzer-select bits

Bits 1 and 0 are used to enable buzzer output and select the frequency. The buzzer output function is disabled by 00 and the port operates normally. In other cases, the frequencies listed in the table below are selected.

Table 2-8 Buzzer Output Frequencies (at 10 MHz Oscillation)

BUZ1	BUZ0	Buzzer output frequency
0	0	General-purpose port operation
0	1	1220 Hz
1	0	2441 Hz
1	1	4883 Hz

■ Description of operation

This circuit outputs a signal for use as a check sound. The buzzer register is used to enable buzzer output and select the frequency. When values other than 00 are set at the BUZR register, the square wave of the set frequency is output at the port.

■ Precautions for buzzer output circuit

Part of the time-based timer is used as the buzzer output.
Therefore, clearing the time-based timer affects the circuit.

3. DATA FORMAT

3.1 CLOCK PULSE GENERATOR

The MB89610 series of microcontrollers incorporate the system clock pulse generator. The crystal oscillator is connected to the X0 and X1 pins to generate clock pulses. Clock pulses can also be supplied internally by inputting externally-generated clock pulses to the X0 pin. The X1 pin should be kept open.

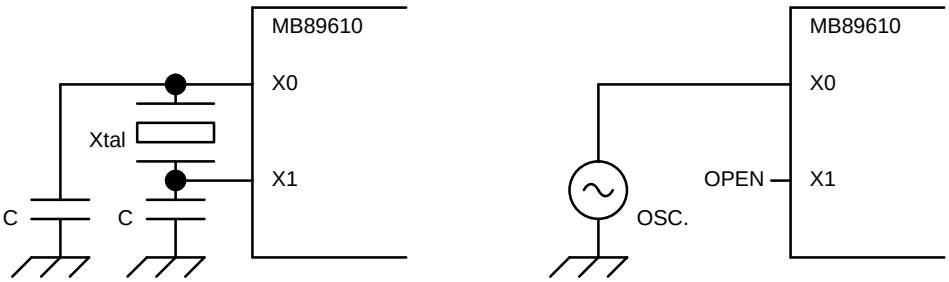


Fig. 3.1 Clock Pulse Generator

3.2 RESET

3.2.1 Reset Operation

When reset conditions occur, the MB89610 series of microcontrollers suspend the currently-executing instruction to enter the reset state. The contents written at the RAM do not change before and after reset. However, if a reset occurs during writing of 16-bit long data, data is written to the upper bytes and may not be written to lower bytes. If a reset occurs around write timing, the contents of the addresses being written are not assured.

When the reset conditions are cleared, the MB89610 series of microcontrollers are released from the reset state and start operation after fetching the mode data from address **0FFFD$_H$**, the upper bytes of the reset vectors from address **0FFFE$_H$**, and the lower bytes from address **0FFFF$_H$**, in that order. Figure 3.2 shows the flowchart for the reset operation.

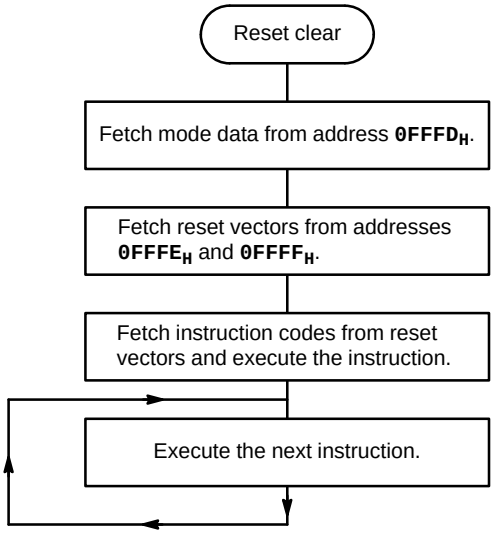


Fig. 3.2 Outline of Reset Operation

Table 3-1 indicates the structure of data to be stored in addresses **0FFFD$_H$**, **0FFFE$_H$**, and **0FFFF$_H$**.

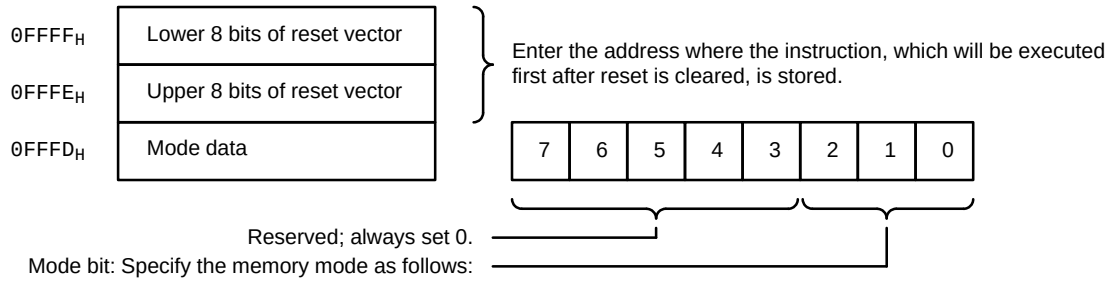


Table 3-1 Reset Vector Structure

T2	T1	T0	Operation
0	0	0	External-access disable (single chip)
0	0	1	External-access enable (external-bus enable)
Other than above			Reserved; do not set.

3.2.2 Reset Sources

The MB89610 series of microcontrollers have the following reset sources.

(1) External pin — A Low level is input to the $\overline{RST}$ pin.

(2) Specification by software — 0 is written at the RST bit of the standby-control register.

(3) Power-on — The power is turned on when the power-on reset option is selected.

(4) Watchdog function — The watchdog function is enabled by the watchdog-control register and reaccess to this register is not obtained within the specified time.

When the stop mode is cleared by reset or power-on reset (option selected), operation is started after elapse of the oscillation stabilization time.

Note: At other than the stopped state, external-reset input is sampled by internal clock pulses. Therefore, reset input is not accepted when the supply of external clock pulses to the MB89610 series of microcontrollers is stopped.

3.3 INTERRUPT

If the interrupt controller and CPU are ready to accept interrupts when an interrupt request is output from the resources or by an external-interrupt input, the CPU temporarily suspends the currently-executing instruction and executes the interrupt-processing program. Figure 3.3 shows the interrupt-processing flowchart.

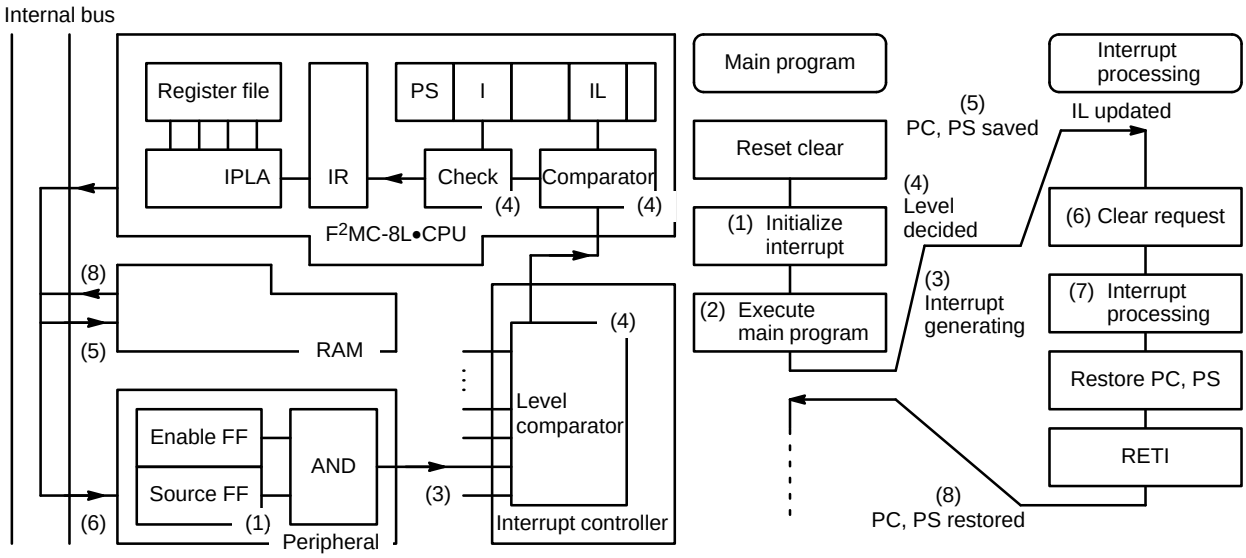


Fig. 3.3 Interrupt-processing Flowchart

All interrupts are disabled after a reset is cleared. Therefore, initialize interrupts in the main program (1). Each peripheral generating interrupts and the interrupt-level-setting registers (ILR1 - ILR3) in the interrupt controller corresponding to these interrupts are to be initialized. The levels of all interrupts can be set by the interrupt-level-setting registers (ILR1 - ILR3) in the interrupt controller. The interrupt level can be set from 1 to 3, where 1 indicates the highest level, and 2 the second highest level. Level 3 indicates that no interrupt occurs. The interrupt request of this level can be accepted. After initializing the registers, the main program executes various controls (2). Interrupts are generated from the resources (3). The highest-priority interrupt requests are identified from those occurring at the same time by the interrupt controller and are transferred to the CPU. The CPU then checks the current interrupt level and the status of the I-flag (4), and starts the interrupt processing.

The CPU performs the interrupt processing to save the contents of the current PC and PS in the stack (5) and fetches the entry addresses of the interrupt program from the interrupt vectors. After updating the IL value in the PS to the required one, the CPU starts executing the interrupt-processing routine.

Clear the interrupt sources (6) and process the interrupts in the user's interrupt-processing routine. Finally, restore the PC and PS values saved by the RETI instruction in the stack (8) to return to the interrupted instruction.

Note: Unlike the F^{2}MC-8, A and T are not saved in the stack at the interrupt time.

Table 3-2 lists the relationships between each interrupt source and interrupt vector.

Table 3-2 Interrupt Sources and Interrupt Vectors

Interrupt source	Upper vector address	Lower vector address
IRQ0 (External interrupt 0)	$FFFA_H$	$FFFB_H$
IRQ1 (External interrupt 1)	$FFF8_H$	$FFF9_H$
IRQ2 (External interrupt 2)	$FFF6_H$	$FFF7_H$
IRQ3 (External interrupt 3)	$FFF4_H$	$FFF5_H$
IRQ4 (8-bit PWM timer)	$FFF2_H$	$FFF3_H$
IRQ5 (Pulse-width count timer)	$FFF0_H$	$FFF1_H$
IRQ6 (16-bit timer/counter)	$FFEE_H$	$FFEF_H$
IRQ7 (8-bit serial I/O#1)	$FFEC_H$	$FFED_H$
IRQ8 (8-bit serial I/O#2)	$FFEA_H$	$FFEB_H$
IRQ9 (Unused)	$FFE8_H$	$FFE9_H$
IRQA (Interval timer)	$FFE6_H$	$FFE7_H$
IRQB (Unused)	$FFE4_H$	$FFE5_H$

3.4 MEMORY ACCESS MODE

When external access is enabled by setting bits 2 to 0 of the mode data at address $FFFD_H$, the ☐ areas in Figure 3.4 are externally accessed via the P0 to P2 pins.

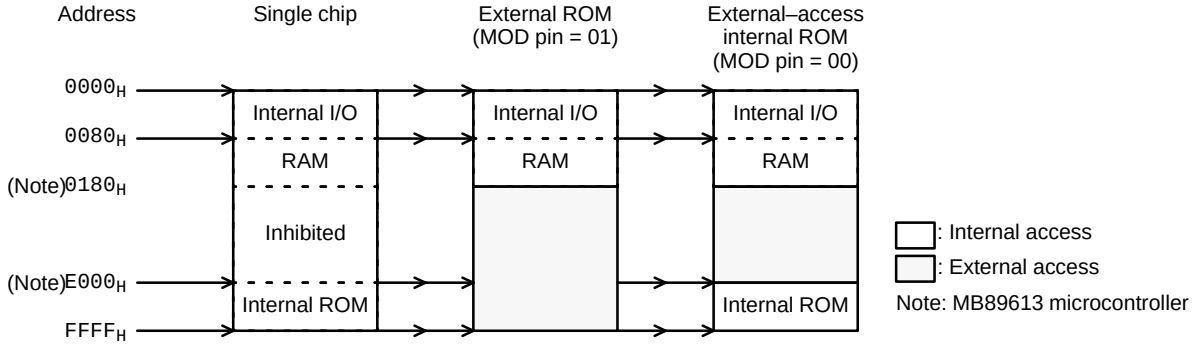


Fig. 3.4 Memory Map in Various Modes

As shown in Figure 3.5, when accessing by the external pins, specify the address of the external peripheral/memory to be accessed according to the access information to be output to the address and address-data pins. The lower 8 bits of the address are input and output by time-sharing with the data bus. Therefore, the external circuit should be created so that the address information can be latched at the falling edge of the ALE signal to be output to the ALE pin. For access, when reading, input data from the external peripheral/memory to the data pin in synchronization with the read strobes to be output to the $\overline{RD}$ pin; when writing, write the data to be output to the data pin to the external peripheral/memory in synchronization with the write strobes to be output to the $\overline{WR}$ pin.

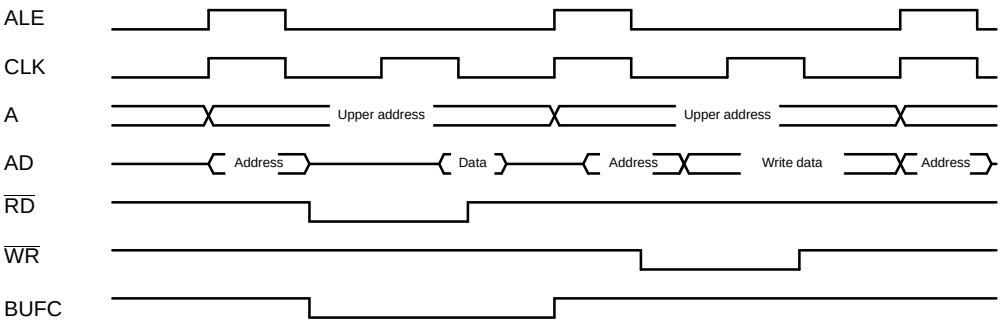


Fig. 3.5 External-access Timing Chart

The BUFC signal is used when the address-data bus has an external buffer. It controls the buffer direction. This signal can be used to facilitate buffer control.

Figure 3.6 shows an example of connecting the external peripheral/memory to the MB89610 series of microcontrollers. In this circuit, the external bus is used after enabling the operation of the $\overline{HAK}$ pin by the external ROM. When using the hold function, the pull-up resistor must be attached externally to the $\overline{HAK}$ pin.

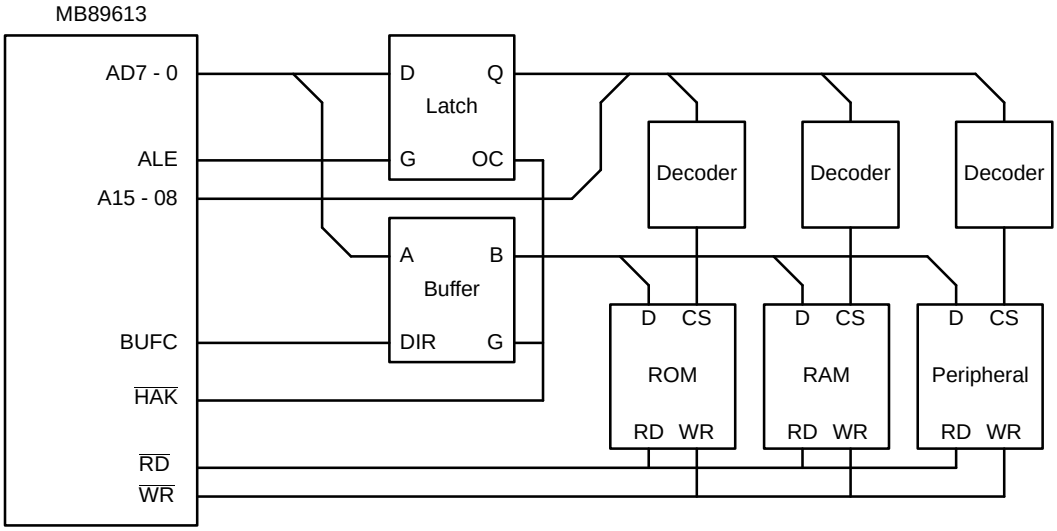
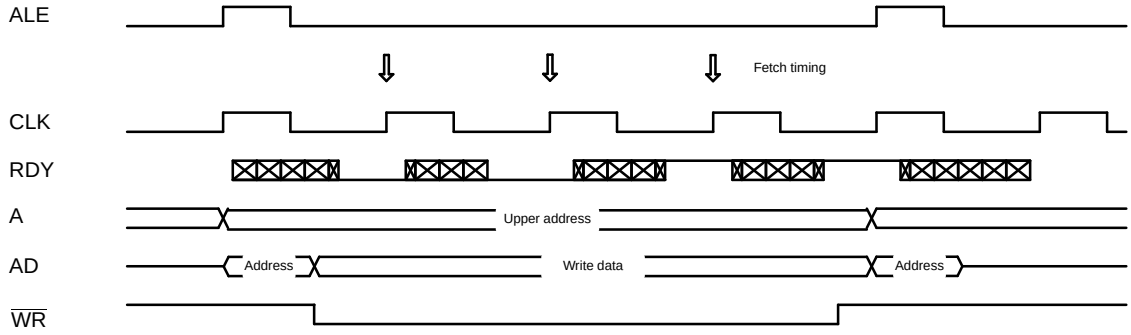


Fig. 3.6 External Peripheral/Memory Connection

3.5 READY AND HOLD FUNCTIONS

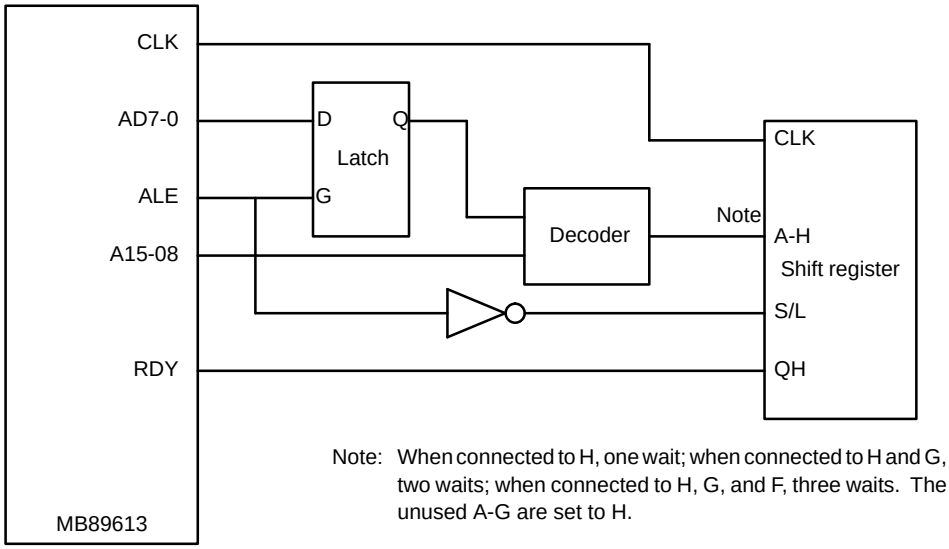
3.5.1 Ready Function

The RDY pin allows access to the low-speed memory and resources. When the RDY pin goes Low while the CPU is conducting external access, the CPU prolongs the last bus cycle by double oscillations. When the CPU conducts an internal access, the value of the RDY pin is ignored. As shown in Figure 3.7, the Ready signal is input near the center of the $\overline{RD}$ or $\overline{WR}$ pin. In the not-ready state, the Ready signal is input around the CLK rising edge. The Ready/Not-ready signal can be generated in the circuit as shown in Figure 3.8.



Note: The read cycle is also prolonged in the same manner.

Fig. 3.7 Ready Input Timing Chart (Write Cycle)



Note: When connected to H, one wait; when connected to H and G, two waits; when connected to H, G, and F, three waits. The unused A-G are set to H.

Fig. 3.8 Ready Generation Circuit

3.5.2 Hold Function

The CPU samples the user hold-request input to the HRQ pin at the boundary of each instruction and sets the $\overline{HAK}$ pin to Low to open the bus. When the CPU detects that the HRQ pin is active, it temporarily suspends operation to set the address, data, $\overline{RD}$, $\overline{WR}$, and BUFC pins to High impedance, and also enters the hold state after outputting a Low level from the $\overline{HAK}$ pin. Figure 3.9 shows the hold timing.

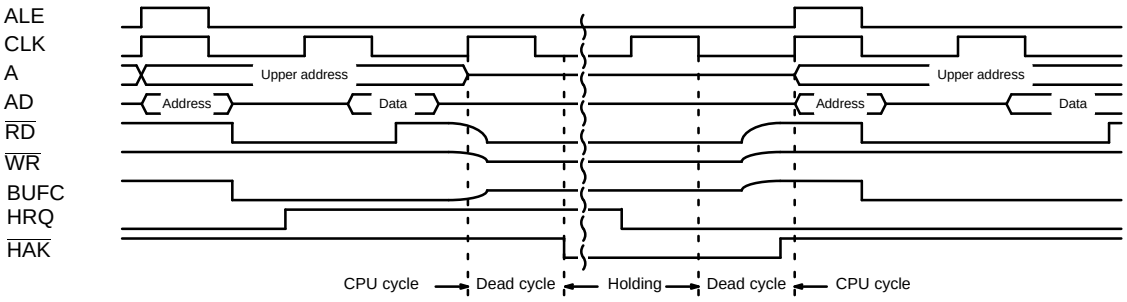


Fig. 3.9 Hold Timing

The CPU does not accept any hold requests in the stop and sleep modes. The use of the hold-acknowledge signal with an external buffer is shown in Figure 3.6.

3.6 LOW-POWER CONSUMPTION MODES

The MB89610 series of microcontrollers have two standby modes: sleep and stop, to reduce the power consumption. Writing to the standby-control register (STBC) gives these two standby modes. Clearing is performed by an interrupt or at reset. The CPU stops operation in the sleep mode but each resource continues to operate. In the stop mode, oscillation stops and data is held at the lowest power consumption.

<Sleep mode>

The CPU operation clock pulse stops, but the others operate. Writing 1 at the SLP bit (bit 6) and 0 at the STP bit (bit 7) of the STBC gives the sleep mode. In the sleep mode, all the contents of the registers and RAM immediately before executing the sleep operation are stored.

The sleep mode can be cleared by an interrupt request higher than level 11 or by reset input. If the sleep mode is cleared by an interrupt request, the operation varies depending on whether the interrupt is enabled or disabled. If the interrupt is enabled by the values of the I-flag and IL bit of the CPU, the operation jumps to the interrupt-processing routine after clearing. If the interrupt is disabled, operation is resumed from the instruction after the one at which the sleep mode was started.

<Stop mode>

When oscillations stop, data is held with the lowest power consumption. Setting the STP bit (bit 7) of the STBC gives the stop mode. In the stop mode, all the contents of registers and RAM immediately before executing the stop operation are stored.

The stop mode can be cleared by an interrupt request higher than level 11 or by reset input. If the stop mode is cleared by an interrupt request, the operation also varies depending on whether the interrupt is enabled or disabled. If the interrupt is enabled by the values of the I-flag and IL bit of the CPU, the operation jumps to the interrupt-processing routine after clearing. If the interrupt is disabled, the operation is resumed from the instruction after the one at which the stop mode was started. When clearing by interrupt and reset, the operation starts after the oscillation stabilization time shown in Table 3-3 has elapsed.

Table 3-3 Oscillation Stabilization Time

Number of counts for minimum instruction time	Time at 10 MHz oscillation	Remarks
About 2^{16} counts	About 26.2 ms	Option for crystal oscillator
About 2^{12}counts	About 1.64 ms	Option for ceramic oscillator

Figure 3.10 shows the state transition diagram in the low-power consumption mode.

Figure 3.11 shows the state transition diagram in the low-power consumption mode without power–on reset.

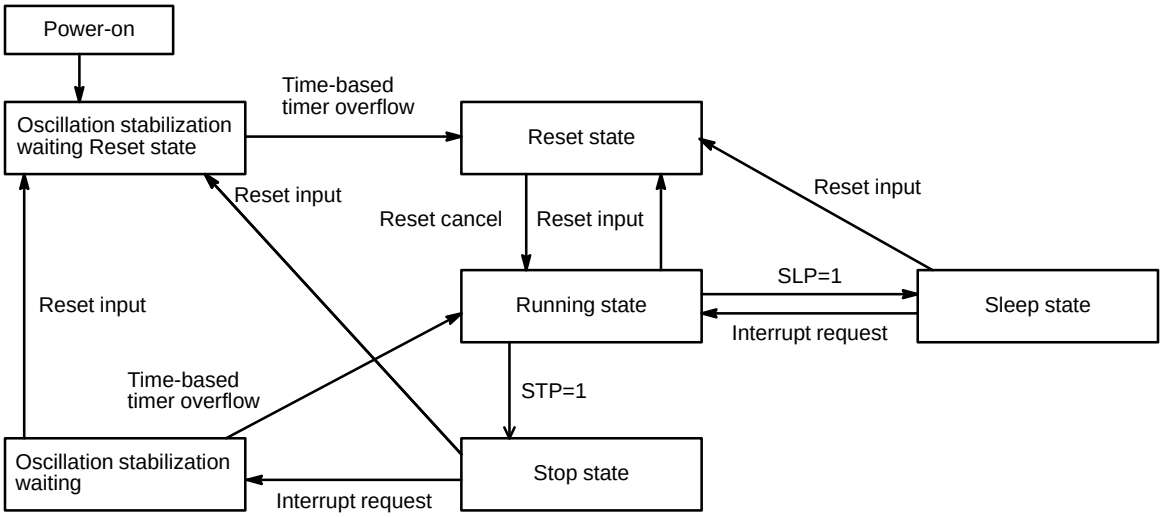


Fig. 3.10 State Transition Diagram at Low-power Consumption(with power–on reset)

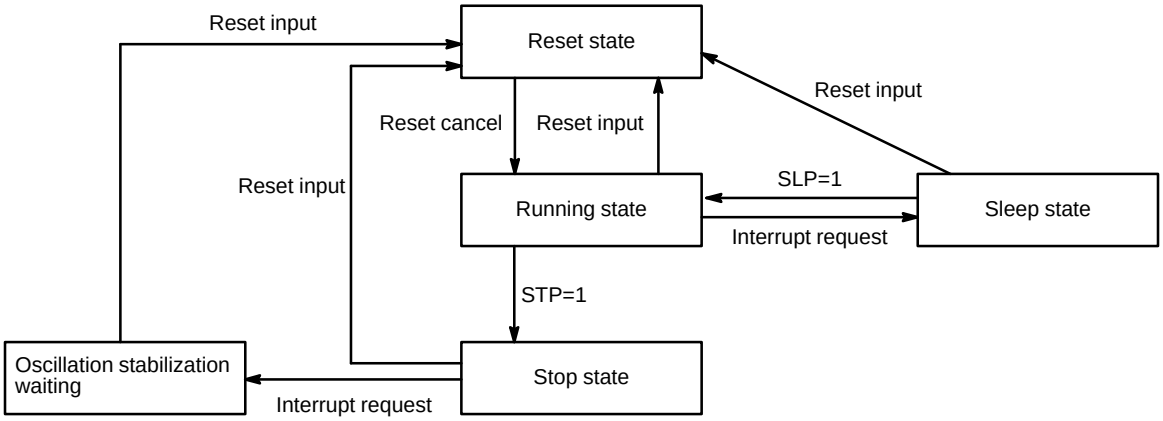


Fig. 3.11 State Transition Diagram in Low-power Consumption Modes(without power–on reset)

3.7 PIN STATES FOR SLEEP, STOP, HOLD, AND RESET

The state of each pin of the MB89610 series of microcontrollers at sleep, stop, hold, and reset is as follows:

(1) Sleep The pin state immediately before the sleep state is held.

(2) Stop The pin state immediately before the stop state is held when the stop mode is started and bit 5 of the standby-control register (STBC) is set to 0; the impedance of the output and input/output pins goes High when the bit is set to 1.

(3) Hold The impedance of the bus pins goes High.

(4) Reset When the MOD pin is 00, the impedance of all I/O and resource pins (excluding pins for pull-up option) goes High. When the MOD pin is 01, the ALE, CLK, RDY, and BUFC signals become active.

The detailed pin state in each mode is described on the following pages.

Normal Pins for MB89610 Series of Microcontrollers (in Single-Chip Mode)

Pin name	Normal	Sleep	Stop SPL = 0	Stop SPL = 1	Reset
P00/AD0 to P07/AD7	Port input/output	Port input/output	Port input/output	High impedance (Note 1)	High impedance
P10/A08 to P17/A15	Port input/output	Port input/output	Port input/output	High impedance (Note 1)	High impedance
X0	Input for oscillation	Input for oscillation	High impedance (Note 1)	High impedance (Note 1)	Input for oscillation
X1	Output for oscillation	Output for oscillation	H output	H output	Output for oscillation
MOD0 MOD1	Mode input	Mode input	Mode input	Mode input	Mode input
$\overline{RST}$	Reset input	Reset input	Reset input	Reset input	Reset input (Note 2)
P27/ALE	Port output	Port output	Port output	High impedance	High impedance
P26/$\overline{RD}$	Port output	Port output	Port output	High impedance	High impedance
P25/$\overline{WR}$	Port output	Port output	Port output	High impedance	High impedance
P24/CLK	Port output	Port output	Port output	High impedance	High impedance
P23/RDY	Port output	Port output	Port output	High impedance	High impedance
P22/HRQ	Port output	Port output	Port output	High impedance	High impedance
P21/$\overline{HAK}$	Port output	Port output	Port output	High impedance	High impedance
P20/BUFC	Port output	Port output	Port output	High impedance	High impedance
P30 to P37/PT0	Port/resource input/ output	Port/resource input/ output	Port/resource input/ output	High impedance (Note 1)	High impedance
P40 to P47/SI2	Port/resource input/ output	Port/resource input/ output	Port/resource input/ output	High impedance (Note 1)	High impedance
P50 to P57	Output port	Output port	Output port	High impedance	High impedance
P60/INT0 to P64	Port/resource input	Port/resource input	Port/resource input	High impedance	High impedance

Note 1: The input level is fixed to prevent leakage due to open input.

Note 2: The reset pin may serve as and output depending on the option setting.

Normal Pins for MB89610 Series of Microcontrollers (in External-ROM and External-Access Internal-ROM Modes)

Pin name	Normal	Hold	Sleep	Stop SPL = 0	Stop SPL = 1	Reset (MOD = 00)	Reset (MOD = 01)
P00/AD0 to P07/AD7	Address/data input/output	High impedance	Data output	Data output	High impedance (Note 1)	High impedance	Undefined
P10/A08 to P17/A15	Address output	High impedance	Address output	Address output	High impedance (Note 1)	High impedance	Undefined
X0	Input for oscillation	Input for oscillation	Input for oscillation	High impedance (Note 1)	High impedance (Note 1)	Input for oscillation	Input for oscillation
X1	Output for oscillation	Output for oscillation	Output for oscillation	H output	H output	Output for oscillation	Output for oscillation
MOD0 MOD1	Mode input	Mode input	Mode input	Mode input	Mode input	Mode input	Mode input
$\overline{RST}$	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input (Note 2)	Reset input (Note 2)
P27/ALE	ALE output	L output	L output	L output	High impedance	High impedance	L output
P26/$\overline{RD}$	$\overline{RD}$ output	High impedance	H output	H output	High impedance	High impedance	H output
P25/$\overline{WR}$	$\overline{WR}$ output	High impedance	H output	H output	High impedance	High impedance	H output
P24/CLK	CLK output	CLK output	CLK output	L output	High impedance	High impedance	CLK output
P23/RDY	RDY input	High impedance	High impedance	High impedance (Note 1)	High impedance	High impedance	RDY input
P22/HRQ	HRQ input (Note 3)	HRQ input (Note 3)	High impedance (Note 3)	High impedance (Notes 1 and 3)	High impedance (Note 1)	High impedance	Port output (Low level)
P21/$\overline{HAK}$	$\overline{HAK}$ output (Note 3)	L output (Note 3)	H output (Note 3)	H output (Note 3)	High impedance	High impedance	Port output (Low level)
P20/BUFC	BUFC output (Note 3)	High impedance (Note 3)	H output (Note 3)	H output (Note 3)	High impedance	High impedance	H output
P30 to P37/PT0	Port/resource input	Port/resource input	Port/resource input	Port/resource input	High impedance (Note 1)	High impedance	High impedance
P40 to P47/SI2	Port/resource input	Port/resource input	Port/resource input	Port/resource input	High impedance (Note 1)	High impedance	High impedance
P50 to P57	Output port	Output port	Output port	Output port	High impedance	High impedance	High impedance
P60/INT0 to P64	Port/resource input	Port/resource input	Port/resource input	Port/resource input	High impedance	High impedance	High impedance

Note 1: The input level is fixed to prevent leakage due to open input.

Note 2: The reset pin may serve as an output depending on the option setting.

Note 3: This may operate as a port depending on the setting of the bus-control register (BCTR).

APPENDIX

APPENDIX 1. MASK OPTIONS

Mask Options

No.	Type	MB89613 MB89615	MB89P625 MB89W625	MB89PV620
	Specification method	**Select when ordering mask.**	**Set by EPROM writer**	**Cannot be set (Fixed)**
1	Pull-up resistor P00 to P07, P10 to P17 P30 to P37, P40 to P47 P50 to P57, P60 to P64	Can be selected for each pin	Can be selected for each pin (Only P40 – P47 do not have the pull-up resistor.)	Pull-up resistor not provided
2	Power–on reset Power-on reset available Power-on reset not available	Can be selected	Can be set	Power–on reset available
3	Oscillation stabilization time selection Crystal oscillator (26.2 ms/10 MHz) Ceramic oscillator (1.64 ms/10 MHz)	Can be selected	Can be set	Crystal oscillator (26.2 ms/10 MHz)
4	Reset pin output Reset output available Reset output not available	Can be selected	Can be set	Reset output available

APPENDIX 2. I/O MAP

Addresses $00_H - 17_H$

Address	Read/Write	Register	Description of register
00_H	(R/W)	PDR0	Port-0 data register
01_H	(W)	DDR0	Port-0 direction register
02_H	(R/W)	PDR1	Port-1 data register
03_H	(W)	DDR1	Port-1 direction register
04_H	(R/W)	PDR2	Port-2 data register
05_H	(R/W)	BCTR	External bus-control register
06_H	—	—	—
07_H	—	—	—
08_H	(R/W)	STBC	Standby-control register
09_H	(R/W)	WDTC	Watchdog-timer control register
$0A_H$	(R/W)	TBTC	Time-based timer control register
$0B_H$	—	—	—
$0C_H$	(R/W)	PDR3	Port-3 data register
$0D_H$	(W)	DDR3	Port-3 direction register
$0E_H$	(R/W)	PDR4	Port-4 data register
$0F_H$	(R/W)	BUZR	Buzzer register
10_H	(R/W)	PDR5	Port-5 data register
11_H	(R)	PDR6	Port-6 data register
12_H	(R/W)	CNTR	PWM-control register
13_H	(W)	COMR	PWM-compare register
14_H	(R/W)	PCR1	PWC pulse-width control register 1
15_H	(R/W)	PCR2	PWC pulse-width control register 2
16_H	(R/W)	RLBR	PWC-reload buffer register
17_H	—	—	—

–: Empty area.

Address 18_H – $7F_H$

Address	Read/Write	Register	Description of register
18_H	(R/W)	TMCR	16-bit timer control register
19_H	(R/W)	TCHR	16-bit timer count register (H)
$1A_H$	(R/W)	TCLR	16-bit timer count register (L)
$1B_H$	—	—	—
$1C_H$	(R/W)	SMR1	Serial 1 mode register
$1D_H$	(R/W)	SDR1	Serial 1 data register
$1E_H$	(R/W)	SMR2	Serial 2 mode register
$1F_H$	(R/W)	SDR2	Serial 2 data register
20_H	—	—	—
21_H	—	—	—
22_H and 23_H	—	—	—
24_H	(R/W)	EIC1	External-interrupt control register 1
25_H	(R/W)	EIC2	External-interrupt control register 2
26_H to $7B_H$	—	—	—
$7C_H$	(W)	ILR1	Interrupt-level register 1
$7D_H$	(W)	ILR2	Interrupt-level register 2
$7E_H$	(W)	ILR3	Interrupt-level register 3
$7F_H$	Access disable	ITR	Interrupt-test register

–: Empty area.

APPENDIX 3. EPROM SETTING FOR MB89P625

In the EPROM mode, the MB89P625 microcontroller functions as the MBM27C256A or equivalent. Therefore, use of a dedicated socket permits writing by a general-purpose EPROM writer.

- Setting

(1) Set the EPROM writer to MBM27C256A.

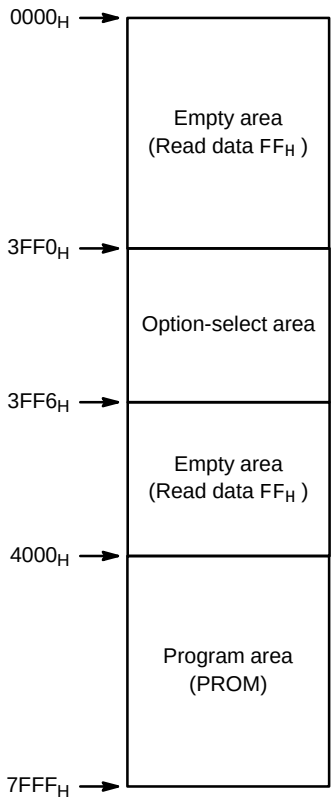
(2) Load the program data from address 4000_H to address $7FFF_H$.
(It should be noted that data is loaded from address **$0C000_H$** to address **$0FFFF_H$** in the operation mode, and from address 4000_H to address **$7FFF_H$** in the EPROM mode.)

(3) Load the option information from address **$3FF0_H$** to address **$3FF5_H$** of the EPROM writer.
(For the correspondence between the addresses and options, see the Bit Map on the next page.)

(4) Write the data with the EPROM writer.

The memory space in the EPROM mode is as follows:

- Address EPROM mode



• Bit Map for PROM Option

	7	6	5	4	3	2	1	0
$3FF0_H$	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Reset pin Output 1: Available 0:Unavailable	Oscillation stable time 1: Ctystal 0: Ceramic	Power-on reset 1: Available 0: Unavailable
$3FF1_H$	P07 Pull-up 1: Unavailable 0: Available	P06 Pull-up 1: Unavailable 0: Available	P05 Pull-up 1: Unavailable 0: Available	P04 Pull-up 1: Unavailable 0: Available	P03 Pull-up 1: Unavailable 0: Available	P02 Pull-up 1: Unavailable 0: Available	P01 Pull-up 1: Unavailable 0: Available	P00 Pull-up 1: Unavailable 0: Available
$3FF2_H$	P17 Pull-up 1: Unavailable 0: Available	P16 Pull-up 1: Unavailable 0: Available	P15 Pull-up 1: Unavailable 0: Available	P14 Pull-up 1: Unavailable 0: Available	P13 Pull-up 1: Unavailable 0: Available	P12 Pull-up 1: Unavailable 0: Available	P11 Pull-up 1: Unavailable 0: Available	P10 Pull-up 1: Unavailable 0: Available
$3FF3_H$	P37 Pull-up 1: Unavailable 0: Available	P36 Pull-up 1: Unavailable 0: Available	P35 Pull-up 1: Unavailable 0: Available	P34 Pull-up 1: Unavailable 0: Available	P33 Pull-up 1: Unavailable 0: Available	P32 Pull-up 1: Unavailable 0: Available	P31 Pull-up 1: Unavailable 0: Available	P30 Pull-up 1: Unavailable 0: Available
$3FF4_H$	P57 Pull-up 1: Unavailable 0: Available	P56 Pull-up 1: Unavailable 0: Available	P55 Pull-up 1: Unavailable 0: Available	P54 Pull-up 1: Unavailable 0: Available	P53 Pull-up 1: Unavailable 0: Available	P52 Pull-up 1: Unavailable 0: Available	P51 Pull-up 1: Unavailable 0: Available	P50 Pull-up 1: Unavailable 0: Available
$3FF5_H$	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	P64 Pull-up 1: Unavailable 0: Available	P63 Pull-up 1: Unavailable 0: Available	P62 Pull-up 1: Unavailable 0: Available	P61 Pull-up 1: Unavailable 0: Available	P60 Pull-up 1: Unavailable 0: Available

Note: Each bit is set to 1 after erase.

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