MB89630R HW manual (reference : CM25-10119-3E)

- p. 2-39 : the matrixes « SCx1, SCx0 » (x= 1 or 2) should show

SCx1	SCx0	CHx input-clock cycle
0	0	1 instruction cycle (0.4 µs) = 1/2 resource operation clock
0	1	8 instruction cycles (3.2 µs) = 1/16 resource operation clock
1	0	16 instruction cycles (6.4 µs) = 1/32 resource operation clock
1	1	64 instruction cycles (25.6 µs) = 1/128 resource operation clock

- p. 2-42 : the comment under addresses 2BH and 2CH should rather be

« Bit 7 is ignored in the high-speed mode ».

- P. 2-44 : the 3rd example for PWM operation should be for COMR = FFH and the PWM pulse output should be changed accordingly, i.e. the PWM pulse output goes high on 00H and goes low on FFH.

- p. 2-45 : the column « Selected clock » should be

Selected clock
1 instruction cycle
8 instruction cycles
16 instruction cycles
64 instruction cycles
Channel-1 toggle output

- p. 2-45 : typo in paragraph « (d) CH1-2 PWM mode »

TPE2 (instead of PTE2) is the correct flag name.

- p. 2-47 : paragraph « 2.2.3 Pulse-width Count timer »

the indication « Timer 3 » in the title should disappear.

- p. 2-47 : the input of the selector block should be « resource operation clock » instead of « CPU clock pulse ».

- p. 2-50 : typo in the « Count clock pulse » matrix

« 1/32 instruction cycle » (rather than « 1/32 instsruction cycle ») should be indicated.

- p. 2-58 : typos in the SIDR and SODR blocks

« REGISTER » (instead of « REGISTETR ») should be indicated.

- p. 2-58 : typo in the « SRC register » block

« SCS1/0 » (instead of « CS1/0») should be indicated.

- P. 2-59: The Mode control matrix must be set as follows:

MC1	MC0	Mode	Data length
0	0	0	7 (6)
0	1	1	8 (7)
1	0	2	Prohibited
1	1	3	9 (8)

- P. 2-77: Analog-input channel selection matrix
- All matrix (ANS3 … ANS0, Select channel). entries in the 5th column must be set to 1.

- p. 2-67 : the column « CLK synchronous (µs/baud) » of table 2-10 should be

CLK synchronous (µs / bauds)
13 / 76.9 k
26 / 38.4 k
52 / 19.2 k
104 / 9.6 k
208 / 4.8 k
416 / 2.4 k
2 / 500 k
16 / 62.5 k

and the indication « At 10-MHz oscillation » should be completed with « fch division = 4 ».

p. 2-67 : in the paragraph « (e) Baud rate calculation … », the formula example should be

Clock gear selection — fch : Crystal oscillator frequency

$$\frac{1}{\text{Baud rate}} = \boxed{\begin{matrix}64/fch\\16/fch\\8/fch\\4/fch\end{matrix}} \times 10/4 \quad \boxed{\text{SCS1, SCS0}} \quad \text{Clock division ratio} \qquad \boxed{\text{Baud rate selection (RC2, RC1, RC0)}}$$

(fch = 10 MHz)

$$\frac{1}{9615\ \text{bps}} = 0.4\ \mu s\ (4/fch) \times 10/4 \times 8\ (\text{Asynchronous mode}) \times 13\ (RC2= RC1= RC0= 0$$

- p. 2-68 : under the matrix « RC2, RC1, RC0 », the indication « Crystal oscillator frequency = 10 MHz » should be completed with « fch division = 4 ».

- p. 2-69 : the 1st equation should be corrected as follows

fch : Crystal oscillator frequency

(min= 8 x 2 / fch)

$$\frac{1}{\text{Baud rate value}} = \frac{1}{\text{External clock input}} \times \text{CR (16 if CR= 0, 64 if CR= 1)}$$

(ex)

(fch = 10 MHz)

$$\frac{1}{39\ \text{kbps}} = 1.6\ \mu s\ (\text{min value}) \times 16\ (CR=0)$$

P-3-7 Table 3-2 Interrupt Source and Interrupt Vector

Correction:

IRQ3 (8-Bit PWM Timer#1)	FFF4	FFF5
IRQ6 (16-Bit Timer / Counter)	FFEE	FFEF
IRQ7 (UART Receive)	FFEC	FFED
IRQ8 (UART Transmit)	FFEA	FFEB

- p. 2-69 : the 2nd equation should be corrected as follows

fch : Crystal oscillator frequency

$$\frac{1}{\text{Baud rate value}} = \underbrace{\boxed{\begin{array}{l}64/fch\\16/fch\\8/fch\\4/fch\end{array}}}_{\text{Clock gear selection}} \times \underbrace{\boxed{\begin{array}{l}1\ (SC11=0, SC10=0)\\8\ (SC11=0, SC10=1\\16\ (SC11=1, SC10=0)\\32\ (SC11=1, SC10=1)\end{array}}}_{\text{Input clock select …}} \times \cdots$$

(ex 1)

$$\frac{1}{78\ \text{kbps}} = \text{(fch = 10 MHz)}\ 0.4\ \mu s\ (4/fch) \times 1\ (SC11=0, SC10=0) \times 1\ (COMR1=0) \times 2 \times 16\ (CR=0)$$

(ex 2)

$$\frac{1}{19531\ \text{bps}} = \text{(fch = 10 MHz)}\ 0.4\ \mu s\ (4/fch) \times 10/4 \times 1\ (SC11=0, SC10=0) \times 4\ (COMR1=3) \times 2 \times 16\ (CR=0)$$