FUJITSU SEMICONDUCTOR
CONTROLLER MANUAL

CM25-10126-1E

F^2MC-8L
8-BIT MICROCONTROLLERS
MB89863 Series
HARDWARE MANUAL

FUJITSU

PREFACE

Thank you for choosing FUJITSU semiconductor products.

The MB89863 is a proprietary 8-bit single-chip microcontroller developed as a specific-application (inverter control) version of the F^{2}MC*-8L (MB89600 series) Family of microcontrollers, and is intended for use with ASIC (application-specific IC) and other low-voltage applications.

This manual describes the functions and operations of the MB89863 microcontroller. Please be sure to read it through carefully.

The following terms and definitions are used throughout this manual.

❍ One instruction cycle is equivalent to four oscillator clock cycles.

Oscillation at 4.2 MHz: 1 instruction cycle = 0.95 µs

Oscillation at 8 MHz: 1 instruction cycle = 0.50 µs

*: F^{2}MC is an abbreviation for FUJITSU Flexible Microcontroller

This manual is organized as follows.

Chapter 1 General

This chapter describes the model lineup of the MB89863 microcontrollers, with an overview of each model.

Chapter 2 Hardware Configuration

This chapter describes the internal configuration and operating modes of the F^{2}MC*-8L CPU and specifications for the hardware built into the MB89863 microcontroller.

Chapter 3 Operation

This chapter describes the use of the MB89863, including reset sequence, interrupts, external bus operation, and low-power consumption modes.

Chapter 4 Instruction Overview

This chapter describes instructions used with the F^{2}MC*-8L Family microcontrollers.

Chapter 5 Electrical Characteristics

This chapter describes absolute maximum ratings, recommended operating conditions, DC and AC standards, and electrical characteristics for the A/D converter unit.

Appendix I/O Map

The I/O map lists registers in the I/O area.

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CONTENTS

Chapter 1: OVERVIEW

The MB89863 is a single-chip microcontroller using the F²MC-8L core for low-voltage, high-speed operation, with built-in peripherals including a timer unit, a timer, UART, A/D converter, and external interrupt. This product is optimized for pulse output for the control of AC inverter motors.

1.1 Features

- F²MC-8L CPU Core

  Instruction set optimized for controller operation
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Instruction test and branch instructions
  - Bit manipulation instructions, etc.

- Timer Unit

  Outputs a non-overlapping 3-phase waveform for AC inverter motor control. Can also be used as PWM (4 channels).

- 8-bit PWM timer (2 channels)

  Can be used as a reload timer or a PWM.

- UART

  Full-duplex double buffer
  Transfers synchronous or asynchronous data.

- A/D Converter

  10-bit resolution, conversion time of 33 instruction cycles.
  Can be started by timer unit.

- External Interrupt Input (1 channel)

  Can also be used to wake from low-power consumption modes (includes edge detection function).

- Low-Power Consumption Modes

  Stop mode (oscillator stops, virtually no current consumed)
  Sleep mode (CPU stops, current consumption reduced to approximately one-third of normal)

1.2 Product Lineup

Table 1.2.1 lists the product lineup for the MB89863 and MB89P/W857 series of microcontrollers.

Table 1.2.1 MB89863 and MB89P/W857 Series Product Lineup

Part No.	MB89863	MB89P857	MB89W857
Type	Mass-producted (mask ROM) product	One-time/EPROM/evaluation products	
ROM size	8K × 8 bits, built-in	32K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	
RAM size	256 × 8 bits, built-in	1K × 8 bits, built-in	
CPU functions	Number of basic instructions: 136 instructions Instruction bit length: 8 bits Instruction length: 1-3 bytes Data bit length: 1, 8, 16 bits		
Minimum execution time	0.95 µs/4.2 MHz 0.5 µs/8 MHz	0.4 µs/10 MHz	
Interrupt processing time	8.57 µs/4.2 MHz 4.5 µs/8 MHz	3.6 µs/10 MHz	
I/O ports	Maximum 38 ports	Maximum 53 ports	
Timer unit	10-bit up/down counter timer × 1 Compare register with buffer × 4 Compare-clear register with buffer, zero detection pin control, 4 output channels, non-overlapping 3-phase waveform output, 3-phase independent dead-time timer		
PWM timer	8-bit reload timer operation (toggle output available, operating clock cycle: 1 to 64 instruction cycles) 8-bit resolution PWM operation (conversion cycle: 255 to 16,320 instruction cycles), 2 built-in channels		
UART	8-bit length, clock-synchronous/clock-asynchronous data transfer capability		
Serial I/O		8-bit length, LSB first/MSB first selection Transfer clock (selection of external signal: 2, 8, or 32 instruction cycles)	
A/D converter	10-bit resolution × 8 channels A/D conversion time: 33 instruction cycles External startup or continuous startup by timer unit compare channel 0 (no external startup on MB89863)		
External interrupts	1 channel	4 channels	
	Selection of rising or falling edge Can be used for wake-up from stop/sleep mode (edge detection also available in stop mode)		
Standby mode	Sleep mode, stop mode		
Process	CMOS		
Package	QFP-48	SHDIP-64	
Operating voltage	5V±10%	2.7 to 5.5 V	

1.3 Block Diagram

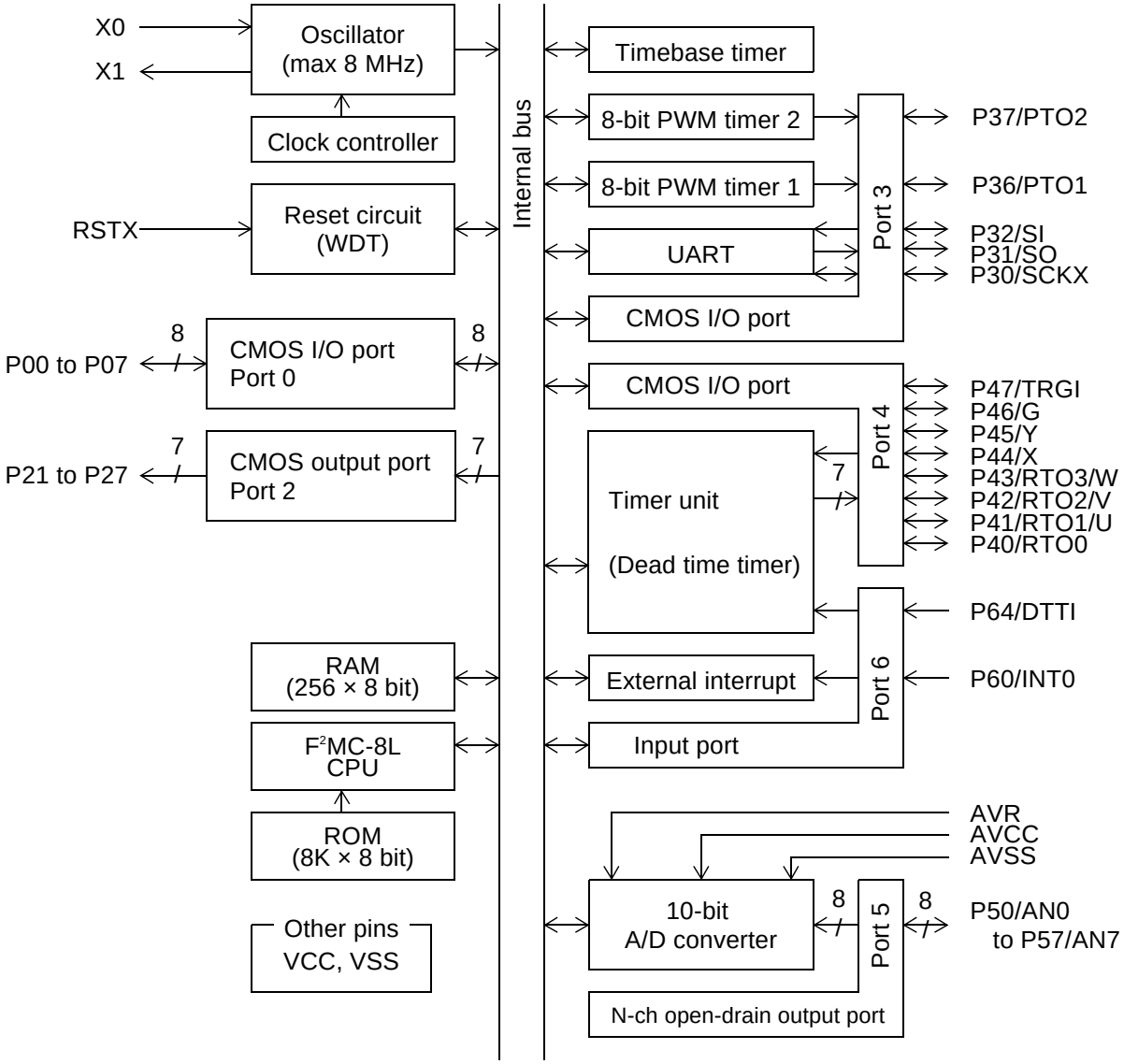


Fig. 1.3.1 Block Diagram (MB89863)

1.4 Pin Assignment

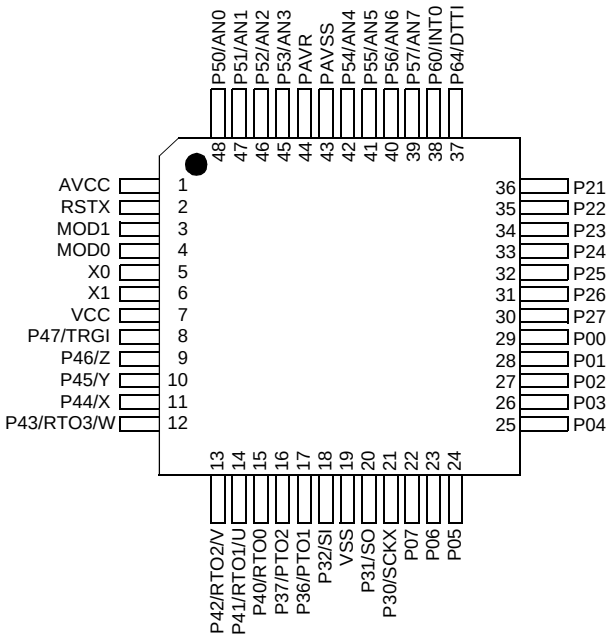
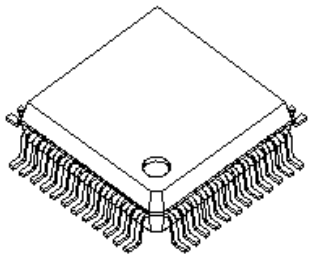


Fig. 1.4.1 MB89863 Pin Assignment

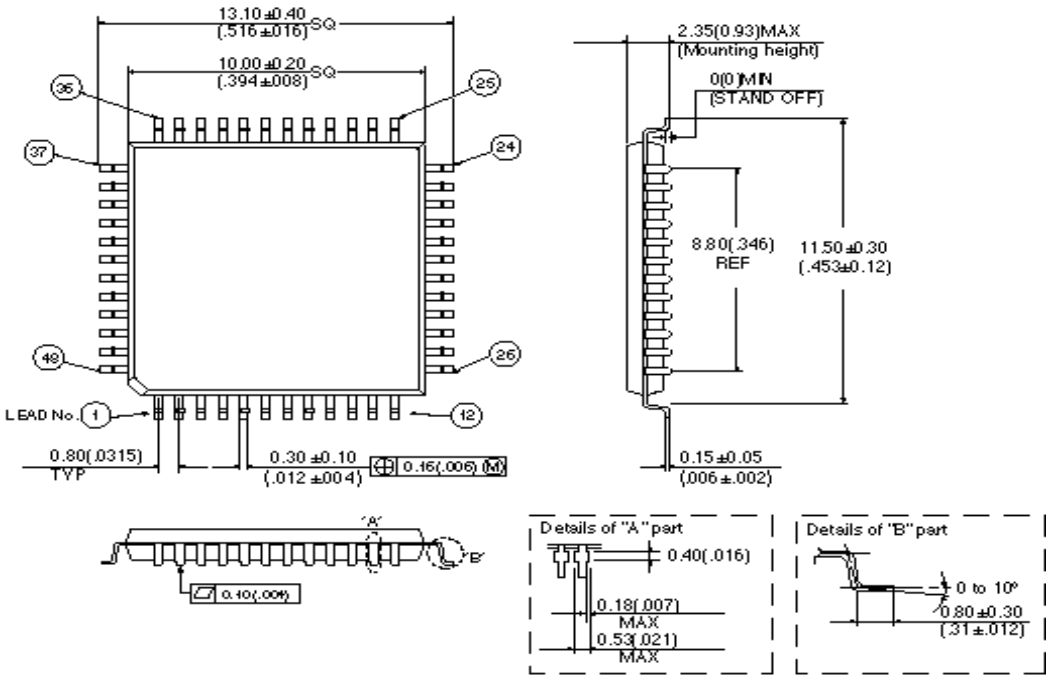
1.5 External Dimensions

FPT-48P-M04

EIAJ code: *QFP048-P-1010-1

48-pin Plastic QFP		
 (FPT-48P-M04)	Lead pitch	0.80 mm
	Package width × package length	10 × 10 mm
	Lead shape	Gull-wing
	Sealing method	Plastic mold

48-pin Plastic QFP
(FPT-48P-M04)



 Dimensions in mm (inches)

Note: External dimensions on specification diagrams are for reference purposes only. Users should consult directly for final information.

Fig. 1.5.1 External Dimensions (QFP48)

1.6 Pin Descriptions

Table 1.6.1 lists the pin functions, and I/O circuit diagrams are shown in Figure 1-6-1.

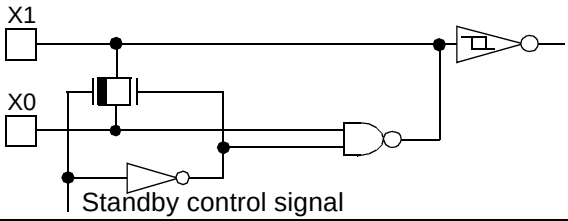
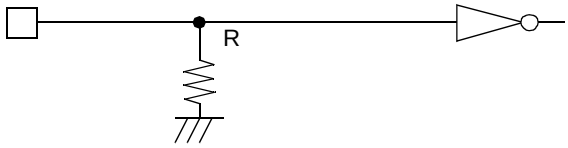
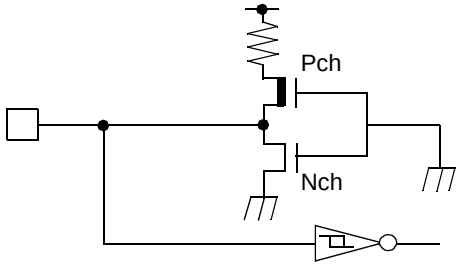
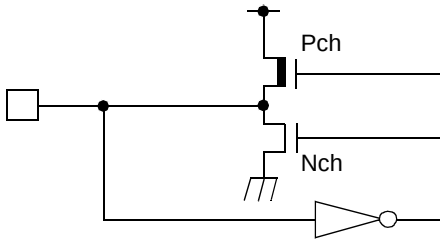
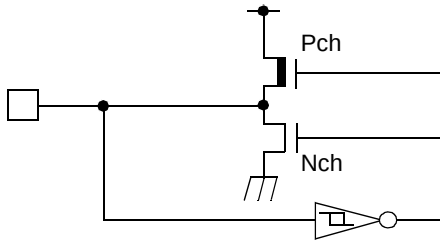
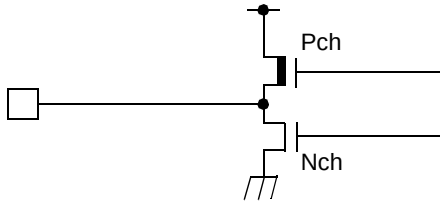
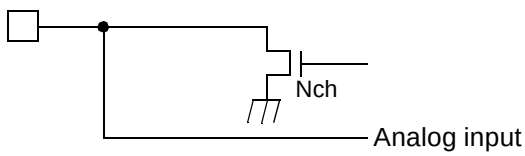
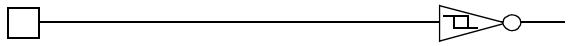
Table 1.6.1 Pin Description

Pin No. QFP48	Pin name	Circuit type	Function
5	X0	A	Crystal oscillator pins (max 8 MHz)
6	X1		
3	MOD0	B	Operating mode selection input pins. Connect directly to VSS. Internal pull-down resistor
4	MOD1		
2	RSTX	C	Reset input pin Low-level input signal initializes internal circuits. Hysteresis input, internal pull-up resistor
22 to 29	P07 to P00	D	General-purpose I/O ports
30 to 36	P27 to P21	F	General-purpose output ports
21	P30/SCKX	E	General-purpose I/O port. Also functions as UART clock I/O pin. Hysteresis input.
20	P31/SO	E	General-purpose I/O port. Also functions as UART data output pin. Hysteresis input.
18	P32/SI	E	General-purpose I/O port. Also functions as UART data input pin. Hysteresis input.
17	P36/PT-1	E	General-purpose I/O port. Also functions as 8-bit PWM ch1 pulse output pin. Hysteresis input.
16	P37/PT-2	E	General-purpose I/O port. Also functions as 8-bit PWM ch2 pulse output pin. Hysteresis input.
15	P40/RTO0	E	General-purpose I/O port. Also functions as timer unit pulse output pin. Hysteresis input.
14	P41/RTO1/U	E	General-purpose I/O port. Also functions as timer unit pulse output or non-overlapping 3-phase output pin. Hysteresis input.
13	P42/RTO2/V	E	General-purpose I/O port. Also functions as timer unit pulse output or non-overlapping 3-phase output pin. Hysteresis input.
12	P43/RTO3/W	E	General-purpose I/O port. Also functions as timer unit pulse output or non-overlapping 3-phase output pin. Hysteresis input.
11	P44/X	E	General-purpose I/O port. Also functions as non-overlapping 3-phase output pin. Hysteresis input.

Table 1.6.1 Pin Description *(Continued)*

Pin No. QFP48	Pin name	Circuit type	Function
10	P45/Y	E	General-purpose I/O port. Also functions as non-overlapping 3-phase output pin. Hysteresis input.
9	P46/Z	E	General-purpose I/O port. Also functions as non-overlapping 3-phase output pin. Hysteresis input.
8	P47/TRGI	E	General-purpose I/O port. Also functions as timer unit trigger input pin. Hysteresis input.
39 to 42 45 to 48	P57/AN7 to P54/AN4 P53/AN3 to P50/AN0	G	N-ch open-drain output ports. Also function as A/D converter analog input pins.
38	P60/INTO	H	General-purpose input port. Also functions as external interrupt input pins. Hysteresis input.
37	P64/DTTI	H	General-purpose input port. Also functions as dead time timer disable signal input pin. Hysteresis input. DTTI input function includes noise cancellation circuit.
7	VCC	–	Power supply pin.
19	VSS	–	Power supply (GND) pin.
1	AVCC	–	Power supply pin for A/D converter
44	AVR	–	Reference voltage input pin for A/D converter.
43	AVSS	–	Power supply pin for A/D converter. Use at same potential as VSS.

Fig. 1.6.1 I/O Circuit Type

Type	Circuit	Remarks
A		• Oscillation feedback resistor: Approx. 1 MΩ.
B		• CMOS input • Internal pull-down resistor
C		• Output pull-up resistor (Pch) • Hysteresis input
D		• CMOS output • CMOS input
E		• CMOS output • Hysteresis input
F		• CMOS output
G		• N-ch open-drain output • Analog input
H		• Hysteresis input

1.7 Handling Devices

(1) Preventing Latch-up

A phenomenon called latch-up may occur on CMOS IC devices if voltage higher than Vcc or lower than Vss is applied to input and output pins, or if voltage higher than the rated value is applied between Vcc and Vss.

When latch-up occurs, supply current levels increase rapidly and might result in thermal damage to elements.

Sufficient care must be taken to avoid exceeding maximum rated values at any time during operation.

(2) Handling Unused Input Pins

Unused input pins can cause devices to malfunction if left open, and should therefore be connected to a pull-up or pull-down resistor.

(3) Fluctuations in Power Supply Voltage

The operating range of Vcc power supply voltage is warranted according to specifications, however even within this range, sudden fluctuations in supply voltage may cause malfunctions, and therefore the supply voltage to the IC should be as stable as possible. As an indicator of stability, it is recommended that at commercial frequencies (50-60 Hz) the Vcc ripple effect in (P-P value) be within 10% of the typical V_{CC} value, and that instantaneous changes at power turn on or off be limited so that the transient fluctuation rate be no more than 0.1 V/ms.

(4) Precautions for Use of External Clock

Even when an external clock is used, an oscillation stabilization time is required for a power-on reset or wake-up from stop mode.

(5) Power Supply and Analog Signal Input for A/C Converter

When turning on or off the power supply to the analog system, care must be taken that the analog power supply (AVCC, AVR) and analog input signal do not exceed the level of the digital power supply (VCC).

(6) Handling Power Supply Pins on Microcontrollers with A/D Converter

When the A/D converter is not in use, connect to be $AV_{CC}=V_{CC}$, and $AV_{SS}=AVR=V_{SS}$.

1.8 Development Environment

The MB89863 is a mask ROM product.

In software development, the use of evaluation tools or OTPROM version chips requires the use of the MB89P/W857 chip and a pin array conversion adapter (Sun Hayato model: 64SD-48QF-8L) dedicated for the MB89863.

For programming to the MB89P/W857, refer to the 'F^2MC-8L Family MB89860 Series Data Sheet.'

Chapter 2: HARDWARE CONFIGURATION

2.1 CPU

2.1.1 Memory Space

The MB89863 series of microcontrollers has 64 Kbytes of memory space. All I/O, data, and program areas are located in this space. The I/O area is located near the lowest address and the data area is immediately above it. The data area may be divided into register, stack and direct addressing areas according to the individual applications. The program area is located at the opposite end of the memory space, near the highest address, and the interrupt reset vectors and vector call instruction tables are at the top of the highest address. Figure 2.1.1 shows the structure of the memory space for the MB89863.

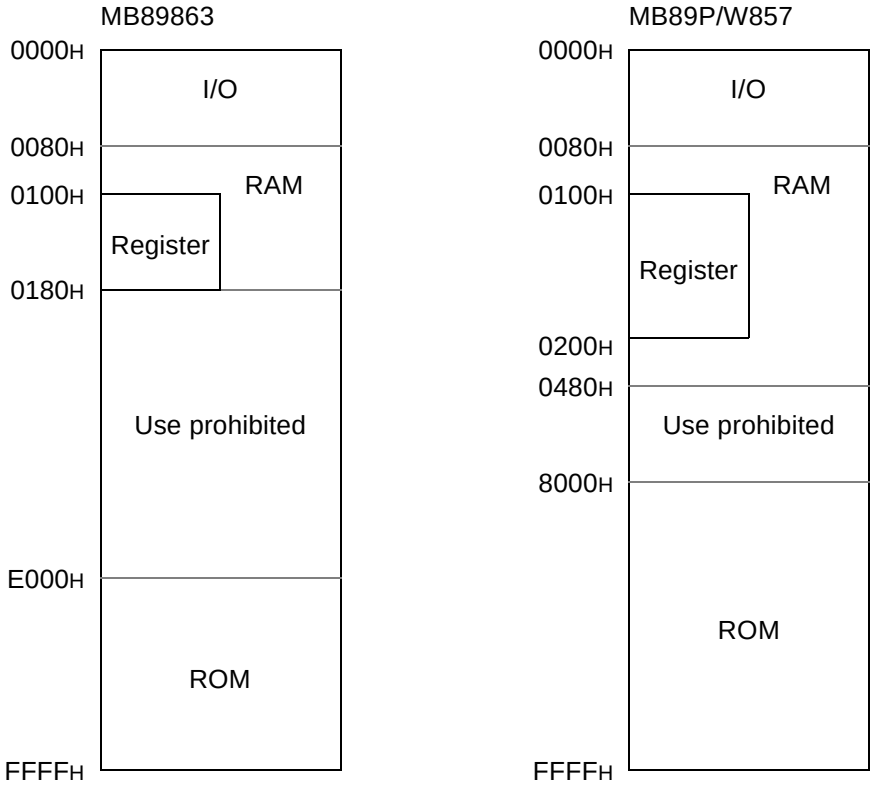


Fig. 2.1.1 Memory Space for MB89836 and MB89P/W857

❍ I/O Area

This area contains control registers for various peripheral devices, as well as data registers. The I/O area memory map is presented in Appendix 1.

❍ RAM Area

This area contains static RAM. The area from addresses 0100H to 0180H can also be used as the general-purpose register area.

❍ ROM Area

This area contains the internal ROM. The area from addresses FFC0H to FFFFH is also used for tables of interrupt and reset vectors and vector call instructions. Figure 2.1.2 shows the relation between each interrupt number or reset and the table addresses to be referenced for the MB89863 series microcontrollers.

	Table address	
	Upper data	Lower data
CALLV #0	FFC0H	FFC1H
CALLV #1	FFC2H	FFC3H
CALLV #2	FFC4H	FFC5H
CALLV #3	FFC6H	FFC7H
CALLV #4	FFC8H	FFC9H
CALLV #5	FFCAH	FFCBH
CALLV #6	FFCCH	FFCDH
CALLV #7	FFCEH	FFCFH

	Table address	
	Upper data	Lower data
Interrupt #11	FFE4H	FFE5H
Interrupt #10	FFE6H	FFE7H
Interrupt #9	FFE8H	FFE9H
Interrupt #8	FFEAH	FFEBH
Interrupt #7	FFECH	FFEDH
Interrupt #6	FFEEH	FFEFH
Interrupt #5	FFF0H	FFF1H
Interrupt #4	FFF2H	FFF3H
Interrupt #3	FFF4H	FFF5H
Interrupt #2	FFF6H	FFF7H
Interrupt #1	FFF8H	FFF9H
Interrupt #0	FFFAH	FFFBH
Reset mode	- - - - -	FFFDH
Reset vector	FFFEH	FFFFH

Note1: Address FFFCH is reserved.

Note2: The MB89863 has no interrupt source corresponding to interrupt numbers 6, 8, and 10.

Fig. 2.1.2 Reset and Interrupt Vector Tables

2.1.2 Locating Memory Space in 16-bit Data

The MB89863 handles 16-bit data in memory by assigning the data written in the lower address to the high byte and the data written in the next address to the low byte as shown in Figure 2.1.3.

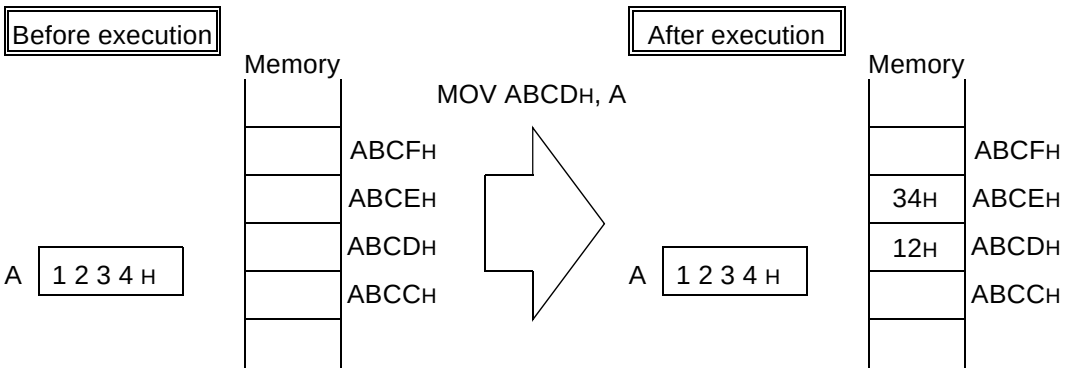


Fig. 2.1.3 Locating 16-bit Data in Memory

The same is true with an instruction operand designating 16-bit data, in which the values closest to the OP code are assigned to the high byte and the next adjacent values to the lower byte. The same treatment is used when the operand designates a memory address or 16-bit immediate data.

```
[Example]   MOV  A, 5678H          ; Extended address
            MOVW A,#1234H          ; 16-bit immediate data
```

Assemble

```
              :
XXXXH  XX XX
XXXXH  60  56  78      ; Extended address
XXXXH  E4  12  34      ; 16-bit immediate data
XXXXH  XX
              :
```

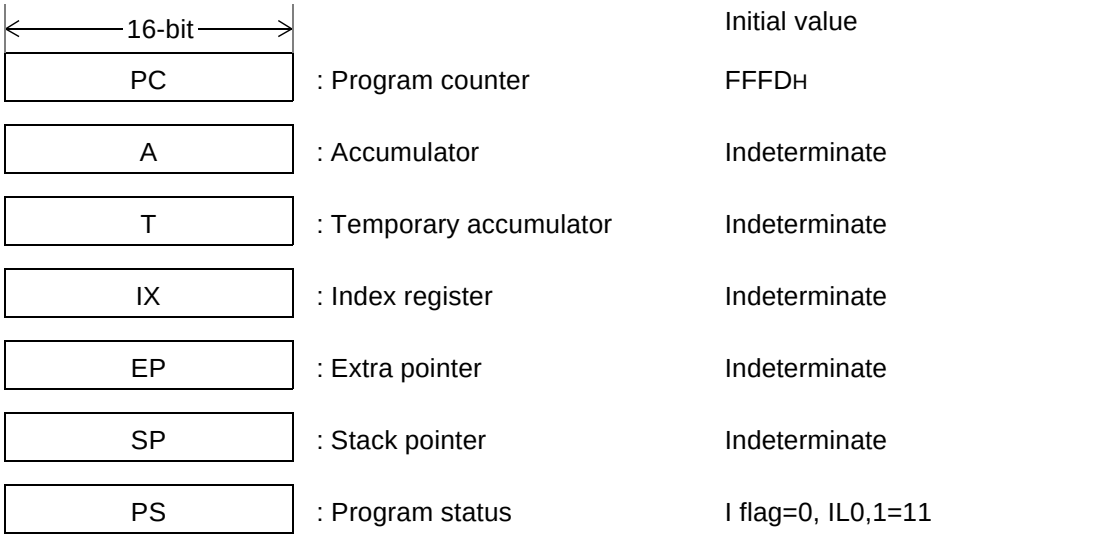
Fig. 2.1.4 Byte Order of 16-bit Data in Instructions

The same treatment is applied to data saved to stack following an interrupt.

2.1.3 Registers

The MB89863 registers are broadly divided into dedicated registers in the CPU and general-purpose registers in memory. The dedicated registers are as follows.

- Program counter (PC).....16-bit length, indicates locations where instructions are stored.
- Accumulator (A) .....16-bit length, used as a temporary storage register for calculations; lower byte used for 8-bit data processing instructions.
- Temporary accumulator (T) ...16-bit length, used for calculation in combination with the accumulator; lower byte used for 8-bit data processing instructions.
- Stack pointer (SP).....16-bit length, indicates a stack area.
- Program status (PS).....16-bit register used to store register pointers and condition codes.
- Index register (IX).....16-bit register used for index modification.
- Extra pointer (EP).....16-bit pointer used for memory addressing.



The 16 bits of the PS register can also be divided in to the upper 8 bits used for a register stack pointer and the lower 8 bits for a condition code register (CCR) (Figure 2.1.5).

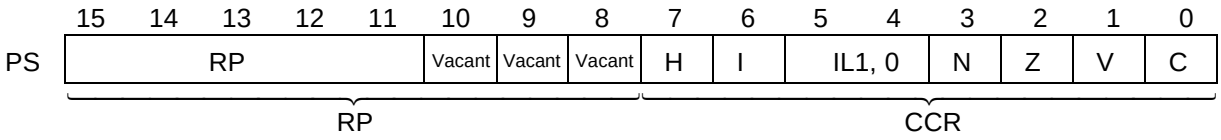


Fig. 2.1.5 Structure of Program Status Register

The RP register shows the address of the current register bank, so that the RP value and the actual address are related according to the conversion rule shown in Figure 2.1.6.

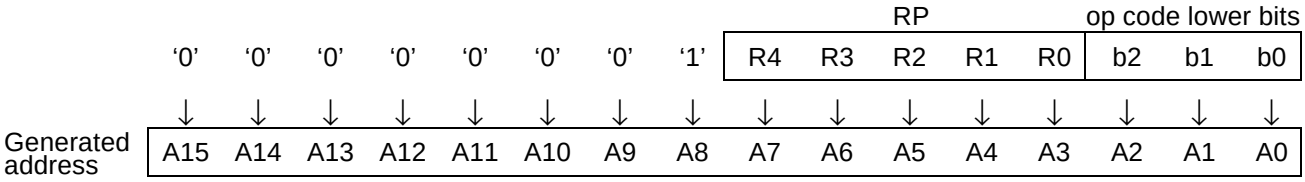


Fig. 2.1.6 Rule for Conversion of Actual Addresses the General-purpose Register Area

The CCR register consists of bits showing the results of arithmetic operations or the contents of transfer data, a bit controlling CPU operation during an interrupt.

- ❍ H flag..... Set when calculations cause a carry or borrow from bit 3 to bit 4 to occur; otherwise, cleared. This flag is used for decimal-correction instructions.
- ❍ I flag ..... Set to '1' to enable interrupts, and '0' to disable. Reset value is 0.
- ❍ IL1, IL0 ..... Indicate the level of the currently enabled interrupt. The CPU executes interrupt processing only for requests for interrupts with a level lower than the value of this bit.

IL1	IL0	Interrupt level	Priority level
0	0	1	High ↕ Low = no interrupt
0	1		
1	0	2	
1	1	3	

- ❍ N flag ..... Set when calculations cause the most significant bit (MSB) to be 1, and cleared when MSB is 0.
- ❍ Z flag ..... Set when calculations result in all bits set to 0, and otherwise cleared.
- ❍ V flag ..... Set when calculations result in a 2's complement overflow, and reset when no overflow occurs.
- ❍ C flag ..... Set when calculations result in a carry or borrow out of bit 7, and otherwise cleared. The value of the C flag is shifted out following a shift instruction.

The following general-purpose registers are provided.

- General-purpose registers .....8-bit length, used to store data.

The 8-bit general-purpose registers are located in the register banks in memory. One bank contains eight registers, and up to 16 banks are available for the MB89863 series of microcontrollers. The bank currently in use is indicated by the register bank pointer (RP).

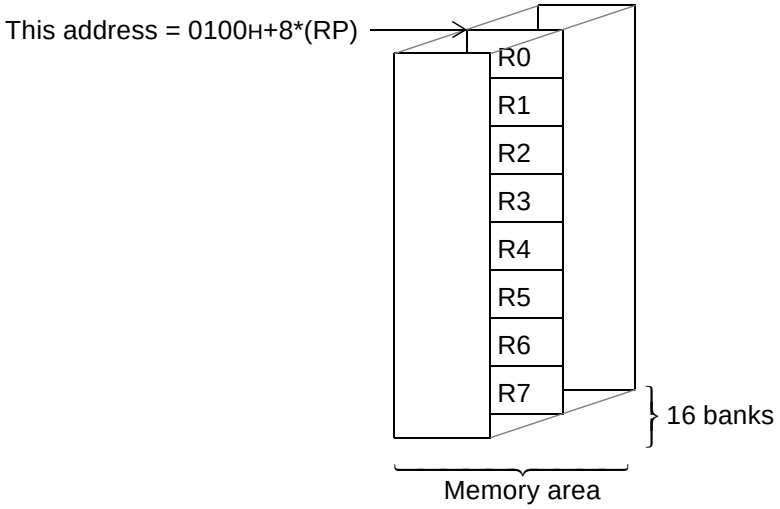


Fig. 2.1.7 Register Bank Configuration

2.1.4 Operating Modes

The MB89863 series of microcontrollers operates in single-chip mode.

The memory map is shown below.

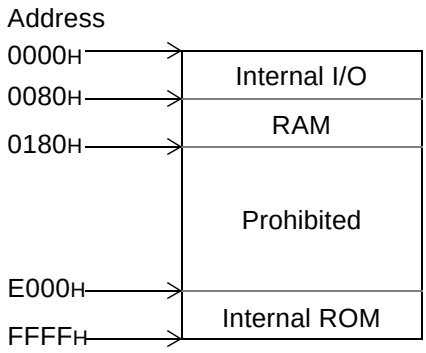
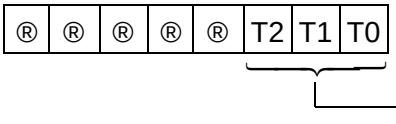


Fig. 2.1.8 Memory Map

The mode in which the device operates is ultimately determined by the setting of the mode pins and the contents of the mode data read during the last reset sequence. The relationship between mode pin settings and operating status is shown below. The MB89863 microcontroller accepts only the setting '00.'

MOD1	MOD0	Description
0	0	Reset vectors are read from internal ROM. External access functions not available.
All other		Reserved; do not set.

The following functions are determined by mode data setting values.



T2	T1	T0	Operation
0	0	0	Selects single-chip mode.
All other			Reserved; do not set.

2.1.5 Clock Controller

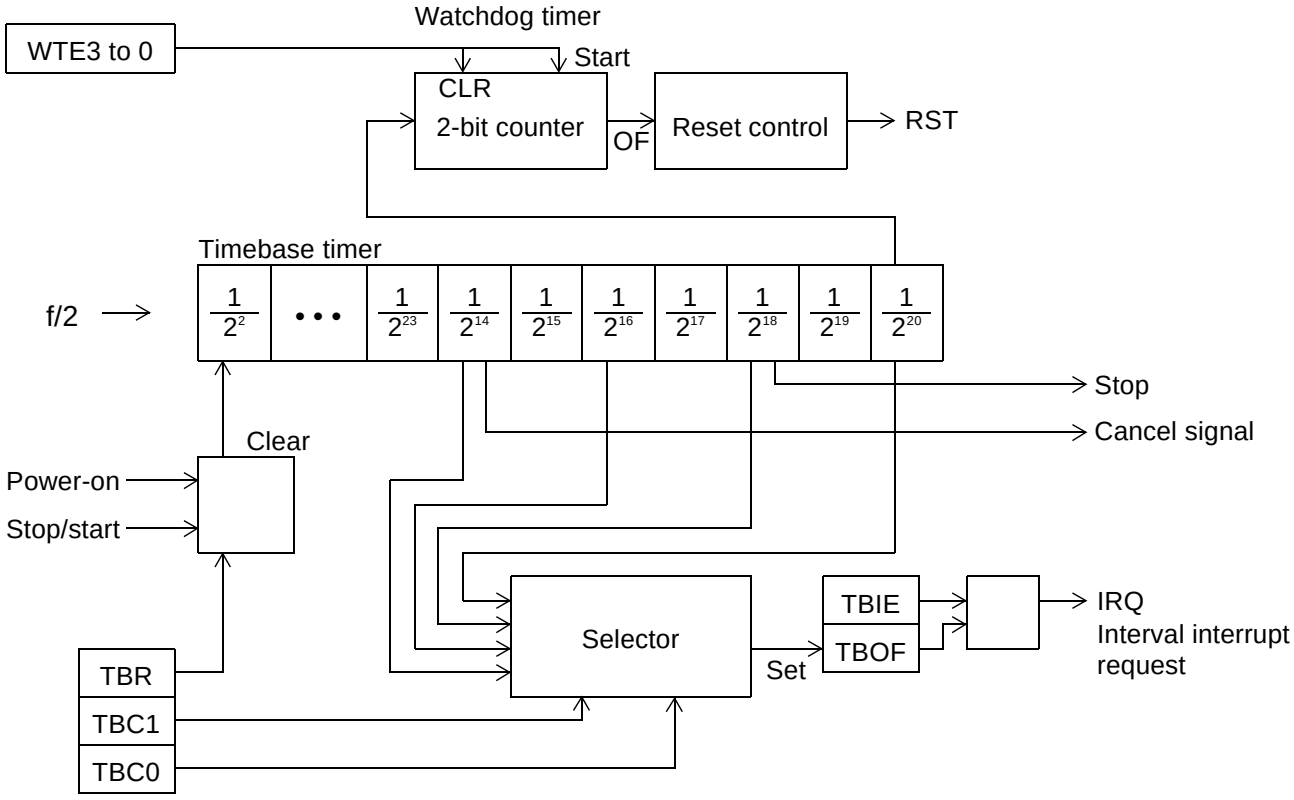
This block controls standby operations, and generation of software resets, in addition to the timebase timer and watchdog timer functions.

(1) Registers

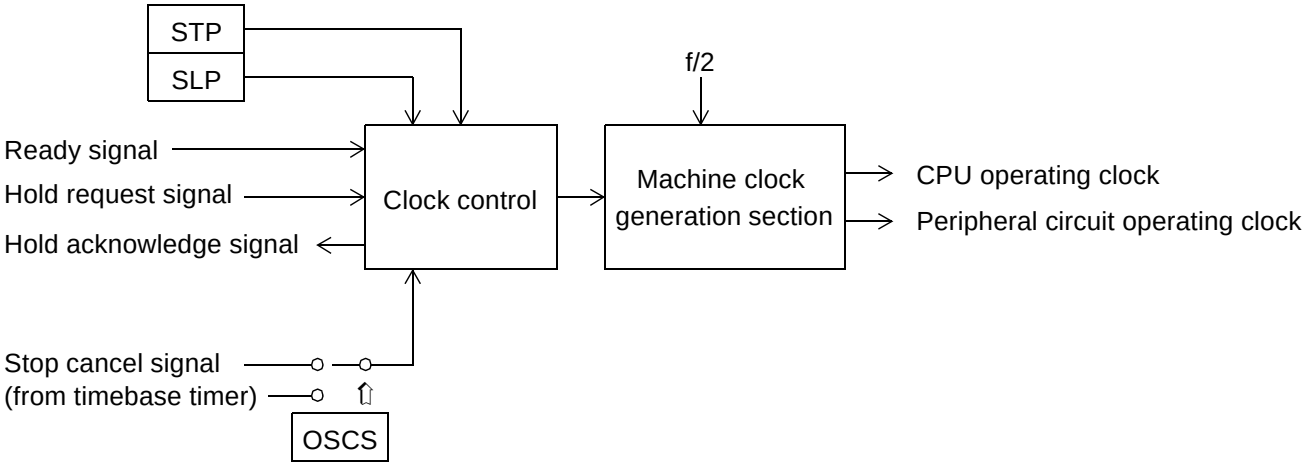
Bit	7	6	5	4	3	2	1	0	
Address: 0008H	STP	SLP	SPL	RST	–	OSCS	–	–	Standby control register (STBC)
Address: 0009H	–	–	–	–	WTE3	WTE2	WTE1	WTE0	Watchdog control register (WDTC)
Address: 000AH	–	–	–	TBIE	TBOF	TBR	TBC1	TBC0	Timebase timer control register (TBTC)

(2) Block diagram

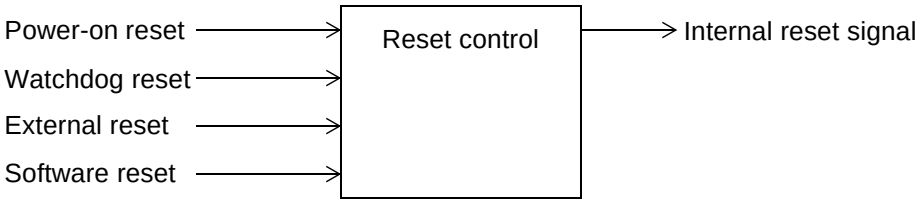
(a) Timebase timer and watchdog timer



(b) Machine clock controller



(c) Reset controller



(3) Register Descriptions

(3.1) STBC (Standby Control) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
STP	SLP	SPL	RST	–	OSCS	–	–	0001X0XXB
(W)	(W)	(R/W)	(W)		(R/W)			

The STBC register controls low-power consumption modes.

[Bit 7] STP: Stop bit

Bit 7 is used to specify switching to stop mode.

0	No operation
1	Stop mode

The bit is cleared at reset or wake-up from stop mode.

Writing '1s' simultaneously into STP and SLP bits enters the stop mode.

The read value of this bit is always '0.'

[Bit 6] SLP: Sleep bit

Bit 6 is used to specify switching to sleep mode.

0	No operation
1	Sleep mode

This bit is cleared at reset or wake-up from sleep mode or stop mode.

Writing ’1s’ simultaneously into STP and SLP bits enters the stop mode.

The read value of this bit is always '0.'

[Bit 5] SPL: Pin state select bit

Bit 5 is used to set the state of external pins when the MB89863 is in stop mode.

0	Holds the state and level immediately before stop mode.
1	High impedance state

This bit is cleared at reset.

[Bit 4]: Software reset bit

Bit 4 is used to specify a software reset.

0	Generates reset signal of 4 instruction cycles
1	No operation

The read value of this bit is always '1.'

[Bit 2] OSCS: Oscillation stabilization time select bit

This bit is used to select the length of the oscillation stabilization period.

OSCS	Counts for minimum execution time	Time at 4.2 MHz oscillation	Time at 8 MHz oscillation
0	approx. 2^{16} counts	approx. 62.3 ms	approx. 32.7 ms
1	approx. 2^{12} counts	approx. 3.90 ms	approx. 2.05 ms

This bit is initialized at zero at a power-on reset, but is not initialized by any other resets.

(3.2) WDTC (Watchdog Timer Control) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
–	–	–	–	WTE3	WTE2	WTE1	WTE0	XXXXXXXXB
				(W)	(W)	(W)	(W)	

This register controls the watchdog timer function.

[Bits 3 to 0] WTE3 to WTE0: Watchdog timer control bits

These bits control the watchdog timer functions.

❍ First write after reset

0101	Starts watchdog timer.
All other	No operation

❍ Second write after reset

0101	Clears watchdog timer counter.
All other	No operation

The watchdog timer can only be stopped by a reset.

The read value of bits 0-3 is '1111.'

(3.3) TBTC (Timebase Timer Control) Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
-	-	-	TBIE	TBOF	TBR	TBC1	TBC0	XXX00000B
			(R/W)	(R/W)	(W)	(R/W)	(R/W)	

The TBTC register controls the timebase timer and interval timer.

[Bit 4] TBIE: interval interrupt enable bit

Bit 4 is used to enable an interrupt from the interval timer.

0	Enables interval interrupt.
1	Disables interval interrupt.

This bit is cleared at reset.

[Bit 3] TBOF: Interval timer overflow bit

This bit is used to clear the interval timer overflow flag when writing.

0	Clear internal timer overflow flag.
1	No operation

❍ This bit indicates that an internal timer overflow occurred during reading.

0	No interval timer overflow occurred
1	Interval timer overflow occurred

The read value is '1' for all read-modify-write instructions.

An interrupt request is generated if this TBOF bit is set to '1' while the TBIE bit is '1.'

This bit is cleared at reset.

[Bit 2] TBR: Timebase timer initialize bit

This bit clears the timebase timer counter.

0	Clears timebase timer counter.
1	No operation

The read value of this bit is always '1.'

[Bits 1,0] TBC1,TBC0: Interval time setting bits

These bits are used to set the cycle of the interval timer.

TBC1	TBC0	Interval time at 4.2 MHz oscillation	Interval time at 8 MHz oscillation
0	0	7.8 ms	4.1 ms
0	1	31.2 ms	16.4 ms
1	0	124.6 ms	65.5 ms
1	1	498.1 ms	262.1 ms

These bits are cleared at reset.

(4) Description of operation

(4.1) Low-power consumption

There are two low-power consumption modes: sleep and stop. Table 2.1.1 lists the status of MB89863 components in each mode.

Table 2.1.1 Operating State in Low-Power Consumption Modes

Operating mode	Switching condition	Oscillation	Clock	CPU	Peripheral circuits	Pins	Exit method
Sleep	SLP=1	Operates	Operates	Stops	Operates	Operates	Reset/ interrupt
Stop (SPL=0)	STP=1	Stops	Stops	Stops	Stops	Holds	Reset/ interrupt
Stop (SPL=1)	STP=1	Stops	Stops	Stops	Stops	Hi-Z	Reset/ interrupt

- In sleep mode, only the CPU operating clock stops; other operations are continued.
- In stop mode, the oscillation stops, and data can be retained with the lowest power consumption.

(a) Sleep mode

❍ Switching into sleep mode

- Write '1' to the SLP bit (bit 6) of the STBC register to enter sleep mode.
- Sleep mode shuts down the clock signal on which the CPU operates. Only the CPU stops, and the peripheral circuits of the MB89863 continue to operate.
- If an interrupt has been requested when '1' is written to the SLP bit (bit 6), the CPU will continue to execute instructions without switching into sleep mode.
- The contents of registers and RAM are retained while the chip is in sleep mode.

❍ Wake-up from sleep mode

- The MB89863 exits sleep mode when a reset signal is input, or an interrupt is requested.
- A reset signal input while in sleep mode causes the MB89863 to switch to reset state, and to exit sleep mode.
- Any interrupt request lower than level 11 will cause the MB89863 to exit sleep mode.
- If the I flag and IL bits are set to accept interrupt requests after sleep mode, the CPU will start the interrupt processing. If they are set to ignore interrupt requests, the CPU will begin by processing the next instruction awaiting execution before transition to sleep mode.

(b) Stop mode

❍ Switching into stop mode

- Write '1' to the STP bit (bit 7) of the STBC register to enter sleep mode.
- Stop mode shuts down the oscillation and all MB89863 chip functions. In this mode, data can be retained at the lowest power consumption.
- While the chip is in stop mode, the SPL bit (bit 5) of the STBC register can be used to control whether the I/O pins and output pins retain their immediately previous settings or are set to high impedance.
- If an interrupt has been requested when '1' is written to the STP bit (bit 7), the CPU will continue to execute instructions without switching into stop mode.
- The contents of registers and RAM are retained while the chip is in stop mode.

❍ Wake-up from stop mode

- The MB89863 exits stop mode when a reset signal is input, or an interrupt is requested.
- A reset signal input while in sleep mode causes the MB89863 to switch to reset state, and to exit stop mode.
- Any interrupt request lower than level 11 will cause the MB89863 to exit stop mode.
- After wake-up from stop mode if the I flag and IL bits are set to enable interrupt processing after sleep mode, the CPU will begin by processing the interrupt as soon as the oscillation stabilization time has passed. If the I flag and IL bits are set to ignore interrupt requests, the CPU will begin by processing the next instruction awaiting execution before transition to stop mode.
- The OSCS bit in the STBC register can be used to select either of two stabilization time settings, as shown in Table 2.1.2.
- When a reset signal is used to exit stop mode, the MB89863 enters oscillation stabilization wait status, and the oscillator stabilization wait period must elapse before the reset is executed.

Table 2.1.2 Selection of Oscillator Stabilization Time

Counts for minimum execution time	Time at 4.2 MHz oscillation	Time at 8 MHz oscillation	Remarks
approx. 2^{16} counts	approx. 62.3 ms	approx. 32.7 ms	For crystal oscillators
approx. 2^{12} counts	approx. 3.90 ms	approx. 2.05 ms	For ceramic oscillators

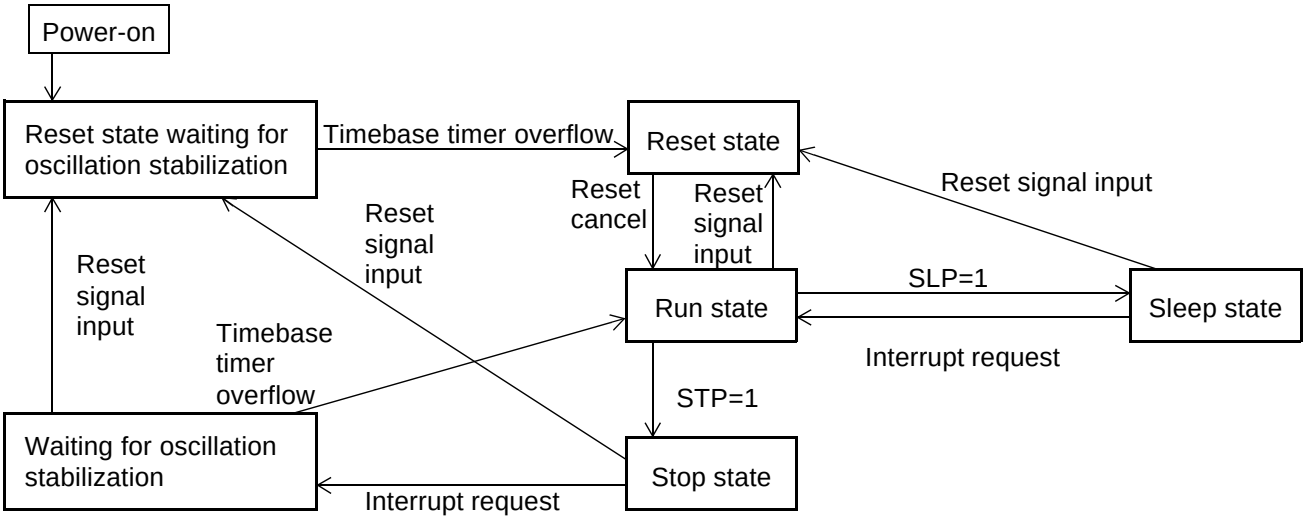


Fig. 2.1.9 State Transition in Lower-Power Consumption

(4.2) Watchdog timer

The watchdog timer function is used to detect program runaway (loop) conditions.

❍ Starting the watchdog timer

- The first writing of '0101' to the WTE3 to WTE0 bits (bits 3 to 0) immediately after a reset will activate the watchdog timer.

❍ Watchdog timer operations

- Once the timer has started, any second or later writing of '0101' to the WTE3 to WTE0 bits (bits 3 to 0) will clear the watchdog timer counter.
- If the watchdog timer counter is not cleared within the time specified in Table 2.1.3, a watchdog reset signal is generated and the chip is reset.
- Any transition to standby or hold status will clear the watchdog timer counter.
- Because the clock signal source for the watchdog timer is supplied from the timebase timer, the watchdog timer counter is simultaneously cleared whenever the timebase timer is cleared.
- Once started, the watchdog timer cannot be stopped until a reset signal is generated.

Table 2.1.3 Watchdog Timer Interval Time

Minimum time	Maximum time	Remarks
approx. 498.1 ms	approx. 996.2 ms	Oscillation at 4.2 MHz
approx. 262.1 ms	approx. 524.3 ms	Oscillation at 8 MHz

(4.3) Timebase timer

The timebase timer consists of 20-stage counters which use a 1/2 oscillation cycle as a clock source signal (see Figure 1). The timebase timer provides the signal for the watchdog timer, the oscillation stabilization timer, and the interval timer used to generate interrupt request at fixed intervals.

❍ Timebase timer control

- The timebase timer counter is cleared by writing '0' to the TBR bit (bit 2) of the TBTC register, or when the MB89863 enters stop mode.
- In all other cases the counter continues to count up for as long as the clock pulse continues.

❍ Interval timer functions

- The interval timer operates by setting the TBOF bit (bit 3) in the TBTC register at regular intervals set by the TBC1,0 bits (bit 1, 0).
- The interval time is initiated by a flag set based on the time the timebase timer counter is last cleared.
- The TBOF bit (bit 3) is also cleared when the MB89863 goes into stop mode, because the timebase timer is used as the counter for the oscillation stabilization time on exiting.
- An interval interrupt is generated if the TBIE bit (bit 4) is set to '1' while TBOF bit (bit 3) is set.
- The interrupt source is cleared by writing '0' to the TBOF bit (bit 3).

(4.4) Resets

The MB89863 provides four types of resets, as shown in Table 2.1.4.

Table 2.1.4 MB89863 Reset Sources

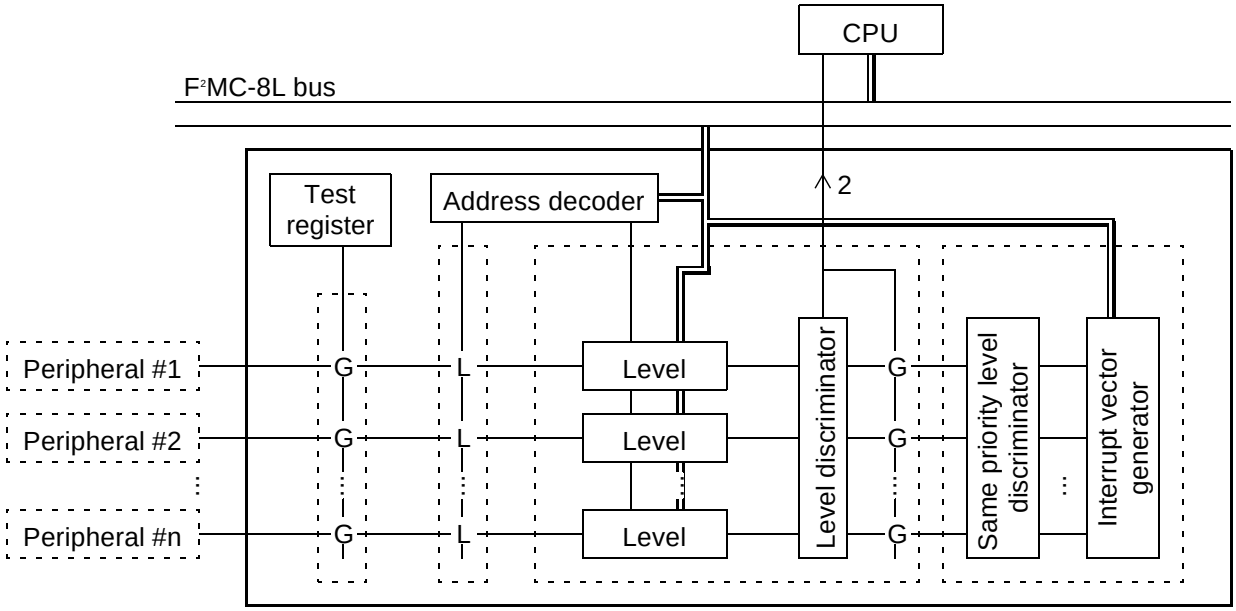
Reset	Description
External pin reset	Sets external reset pins to 'L' level
Software reset	Write '0' to RST bit (bit 4) of STBC register
Watchdog reset	Triggered by watchdog timer overflow
Power-on reset	Triggered by power-on

A power-on reset or any reset in stop mode require an oscillation startup, which must be followed by an oscillation stabilization time because the oscillator has been deactivated. This stabilization time is controlled by the timebase timer. In such cases, therefore the MB89863 will not start operation immediately even if the reset is canceled.

2.1.6 Interrupt Controller

The interrupt controller for the F²MC-8L CPU core is located between the CPU and the peripheral circuits. This controller receives interrupt requests from the peripherals, assigns priorities to them, and then transfers the requests to the CPU. During that process, the controller also determines the priority of interrupts of the same level.

(1) Block diagram



(2) Register list

Address	7	6	5	4	3	2	1	0	Name [Abbreviation]	(Initial value)
007CH	L31	L30	L21	L20	L11	L10	L01	L00	Interrupt level at register #1 [ILR1]	(11111111)
007DH	L71	L70	L61	L60	L51	L50	L41	L40	Interrupt level at register #2 [ILR2]	(11111111)
007EH	LB1	LB0	LA1	LA0	L91	L90	L81	L80	Interrupt level at register #3 [ILR3]	(11111111)
007FH	–	–	–	–	–	–	*	*	Interrupt test register [ITR]	(access prohibited)

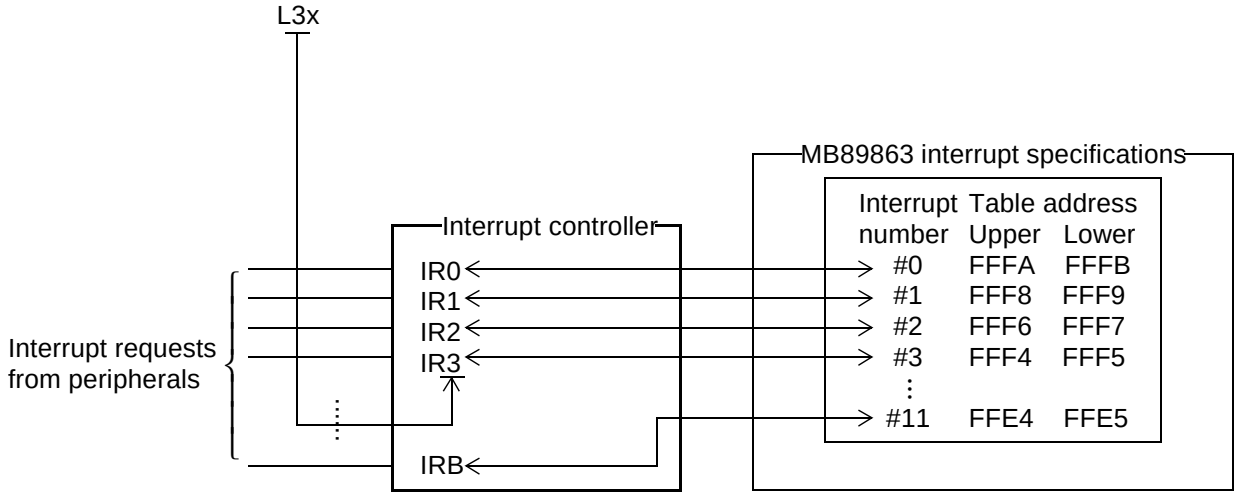
(3) Detailed description of register

(3.1) Interrupt level setting registers (ILRx: Interrupt Level Setting Register x)

	7							0			
ILR1	L31	L30	L21	L20	L11	L10	L01	L00	W	Reset value	(11111111)
ILR2	L71	L70	L61	L60	L51	L50	L41	L40	W	Reset value	(11111111)
ILR3	LB1	LB0	LA1	LA0	L91	L90	L81	L80	W	Reset value	(11111111)

The ILRx registers determine the interrupt levels assigned to each of the peripheral resources. The figure at the center of each bit corresponds to the interrupt number.

[Example]



Interrupt requests from peripherals are passed to the interrupt controller, which assigns an interrupt level based on the 2-bit setting in the corresponding IRLx register, and then transfers the request to the CPU. The relation between the 2-bit settings in the IRLx register and the interrupt request level is as follows:

Lx1	Lx0	Interrupt request level
0	x	1
1	0	2
1	1	3 (no interrupt)

(3.2) Interrupt test register (ITR)

	7							0	
ITR	---	---	---	---	---	---	*	*	–

ITR is a register for testing; it is unaccessible.

(4) Description of operation

(4.1) Interrupt functions

The MB89863 series of microcontrollers has 9 inputs for interrupt requests from peripherals. Each interrupt level is set by a 2-bit interrupt level register corresponding to an input signal. Interrupts requested by a peripheral are received by the interrupt controller and transferred to the CPU according to the level of the corresponding register. The overall procedure of interrupt processing by the MB89863 device is as follows.

(1) An interrupt source is generated inside a resource.

(2) If the interrupt enable bit for that peripheral is set to enable the interrupt, an interrupt request is output from that peripheral to the interrupt controller.

(3) After receiving the interrupt request, the interrupt controller determines the relative priority of any simultaneously requested interrupts, and then transfers the assigned interrupt levels for the applicable interrupts to the CPU.

(4) The CPU compares the level of the interrupt request to the IL bit in the program status register.

(5) If the comparison shows that the incoming interrupt level is higher than that of the current interrupt processing level, the value of the I flag in the program status register is checked.

(6) If the check in step (5) shows that the I flag is enabled for an interrupt, the value of the IL bit is set to the required level. As soon as execution of the current instruction is ended, the CPU processes the interrupt and transfers control to the appropriate interrupt processing routine.

(7) After the interrupt source in step (1) is cleared by software in the user's interrupt processing routine, interrupt processing ends.

Figure 2.1.10 shows an overview of interrupt processing on the MB89863.

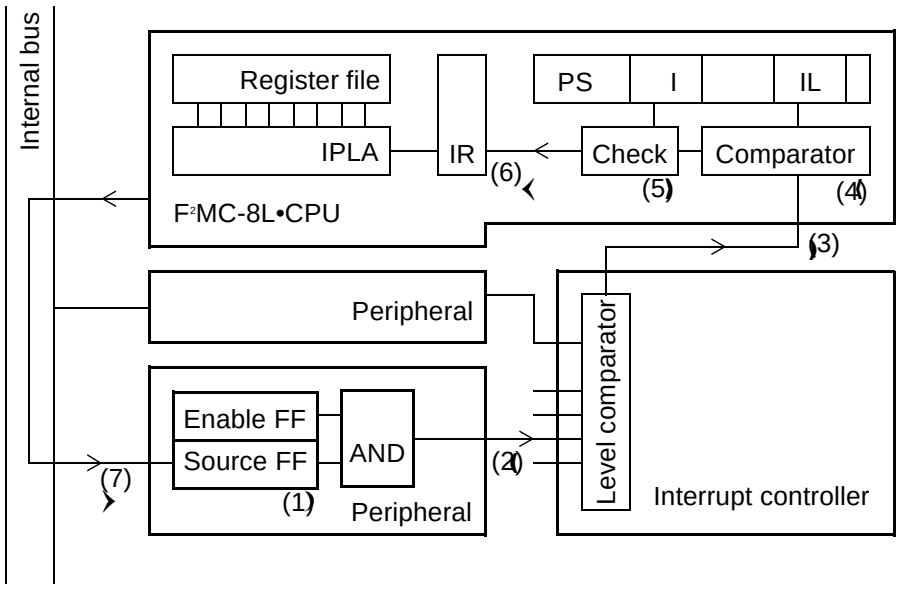


Fig. 2.1.10 Outline of MB89863 Interrupt Processing

2.2 Peripheral Functions

2.2.1 I/O Ports

(1) Overview

- The MB89863 series of microcontrollers has 6 parallel ports (38 pins).

  Ports 0 and 4 are 8-bit I/O ports, port 5 is an 8-bit output port, port 2 is a 7-bit output port, port 3 is a 5-bit I/O port, and port 6 is a 2-bit input port.

- Ports 3, 4 and 5 also function as peripherals. Ports 0 and 2 are dedicated ports.

Table 2.2.1 List of Ports and Functions

Pin no.	Input type	Output type	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P00 to P07	CMOS	CMOS push-pull	Parallel port 0	P07	P06	P05	P04	P03	P02	P01	P00
			Peripheral	–	–	–	–	–	–	v	–
P21 to P27	–	CMOS push-pull	Parallel port 2	P27	P26	P25	P24	P23	P22	P21	–
			Peripheral	–	–	–	–	–	–	–	–
P30 to P32	CMOS (Hyster-esis)	CMOS push-pull	Parallel port 3	P37	P36	–	–	–	P32	P31	P30
P36 to P37			Peripheral	PTO2	PTO1	–	–	–	SI	SO	SCKX
P40 to P47	CMOS (Hyster-esis)	CMOS push-pull	Parallel port 4	P47	P46	P45	P44	P43	P42	P41	P40
			Peripheral	TRGI	Z	Y	X	RTO3	RTO2	RTO1	RTO0
P50 to P57	Analog compa-rator	N-ch open-drain	Parallel port 5	P57	P56	P55	P54	P53	P52	P51	P50
			Peripheral	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
P60, P64	CMOS (Hyster-esis)	–	Parallel port 6	–	–	–	P64	–	–	–	P60
			Peripheral	–	–	–	DTTI	–	–	–	INT0

(2) Register list

Table 2.2.2 Port Registers

Register	Read/Write	Address	Initial value
Port 0 data register (PDR0)	R/W	0000H	XXXXXXX
Port 0 data direction register (DDR0)	W	0001H	00000000B
Port 2 data register (PDR2)	R/W	0004H	0000000XB
Port 3 data register (PDR3)	R/W	000CH	XXXXXXX
Port 3 data direction register (DDR3)	W	000DH	00XXX000
Port 4 data register (PDR4)	R/W	000EH	XXXXXXX
Port 4 data direction register (DDR4)	W	000FH	00000000B
Port 5 data register (PDR5)	R/W	0010H	11111111B
Port 6 data register (PDR6)	R	0012H	XXXXXXX

(3) Description of functions

P00 to P07: CMOS-type I/O ports

- Input/output switching

  Each port bit has a DDR (data direction register) and a PDR (port data register), enabling input or output to be selected independently for each bit. A pin with DDR set to '1' is set for output, and a pin with DDR set to '0' is set for input.

- Output port operation (DDR=1)

  When the DDR is set to '1,' the value written in the corresponding PDR is output to the pin with the DDR set to 1. Normally the PDR read value is the value of the pin, but not the contents of the output latch. However, in executing read-modify-write instructions, the contents of the output latch are read regardless of the DDR setting. Therefore bit processing instructions can be used even when input and output functions are both performed on the same pin. Data written to the PDR is held in the output latch irrespective of the DDR settings.

- Input port operation (DDR=0)

  When used as an input port, the output state is high impedance. Therefore the PDR read value is the value of the pin.

- Status at reset

  All pins are initialized to DDR=0 (with all bits for output at a high impedance) after a reset. The PDR is not initialized by reset, and retains the value it had before the DDR was reset for output.

- Status in stop mode

  In stop mode, when the SPL bit of the standby control register is set to '1,' the output is set to high impedance regardless of the value of the DDR.

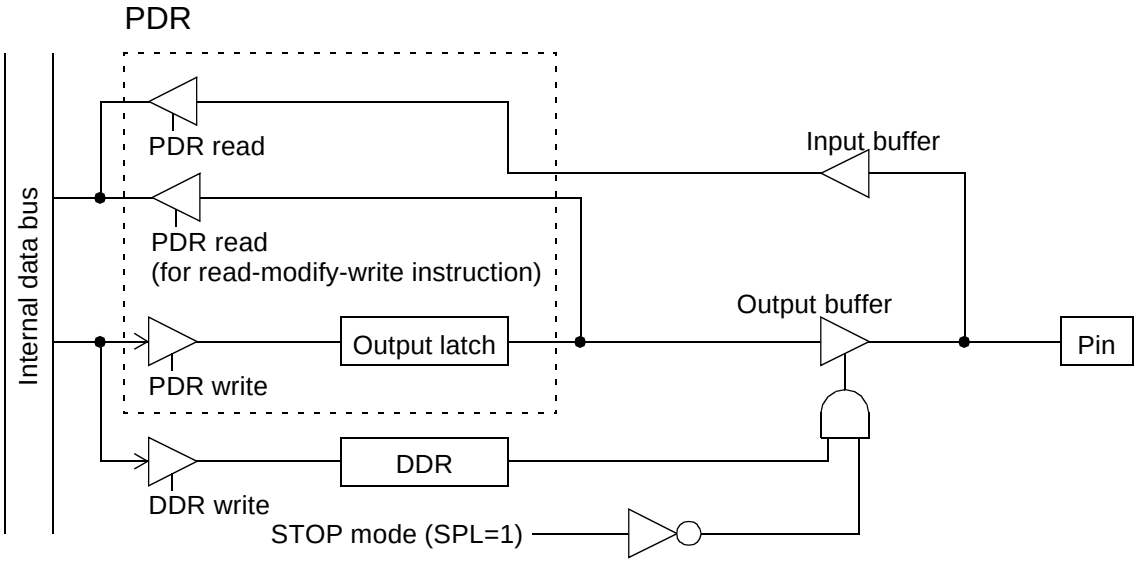


Fig. 2.2.1 Port 0

P21 to P27: CMOS-type output ports

- Operation at output port

  The value written to the PDR is output to the pin. Whenever the PDR is read the contents of the output latch are always read, so that bit processing instructions can be used even if the output level fluctuates due to load.

- Status at reset

  At a reset, pins are in high impedance status, so that port output is enabled as soon as a vector fetch is performed, and the port begins operation as an output port. Because the PDR is initialized to '0' at a reset, the signal output to the pin is at 'L' level.

- Status in stop mode

  In stop mode, when the SPL bit of the standby control register is set to '1,' the output is set to high impedance regardless of the value of the PDR.

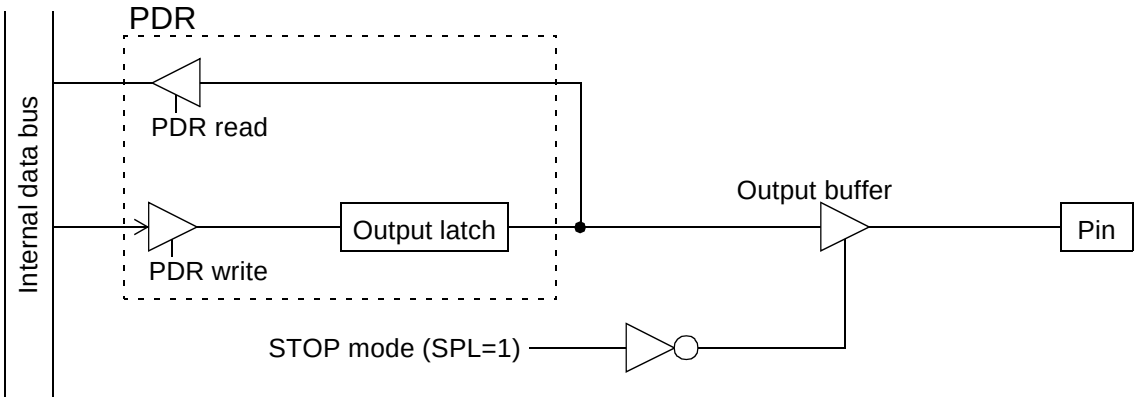


Fig. 2.2.2 Port 2

P30 to P32, P36 to P37: CMOS-type I/O ports (used as resource input/output pins)

- Input/output switching

  Each port bit has a DDR (data direction register) and a PDR (port data register), enabling input or output to be selected independently for each bit. A pin with DDR set to '1' is set for output, and a pin with DDR set to '0' is set for input. If the resource output enable bit is selected, the pin is set for output regardless of the DDR register value.

- Output port operation (DDR=1)

  When the DDR is set to '1,' the value written in the corresponding PDR is output to the pin with the DDR set to '1.' Normally the PDR read value is the value of the pin, but not the contents of the output latch. However, in executing read-modify-write instructions, the contents of the output latch are read regardless of the DDR setting. Therefore bit processing instructions can be used even when input and output functions are both performed on the same pin. Data written to the PDR is held in the output latch regardless of the DDR setting.

- Input port operation (DDR=0)

  When used as an input port, the output state is high impedance. Therefore reading the PDR value gives the value of the pin.

- Resource output operation

  Pins are used for resource output by setting the resource output enable bit (see individual resource descriptions). For input/output switching, the resource output enable bit has priority, so that resource output is selected as long as this bit is set, even when the DDR value is set to '0.' Parallel port reading is effective even when a pin is enabled to allow resource output to be read.

- Resource input operation

  Ports that double as resource inputs provide pin input values at all times regardless of the DDR or resource settings. If an external signal is used by a resource, the DDR should be set to input.

- Status at reset

  The DDR and resource output enable bits are initialized to 0 at a reset and all bits are set to high impedance output. The PDR is indeterminate at reset, and retains the value it had before the DDR was reset to output.

- Status in stop mode

  In stop mode, when the SPL bit of the standby control register is set to '1,' the output is set to high impedance regardless of the value of the DDR.

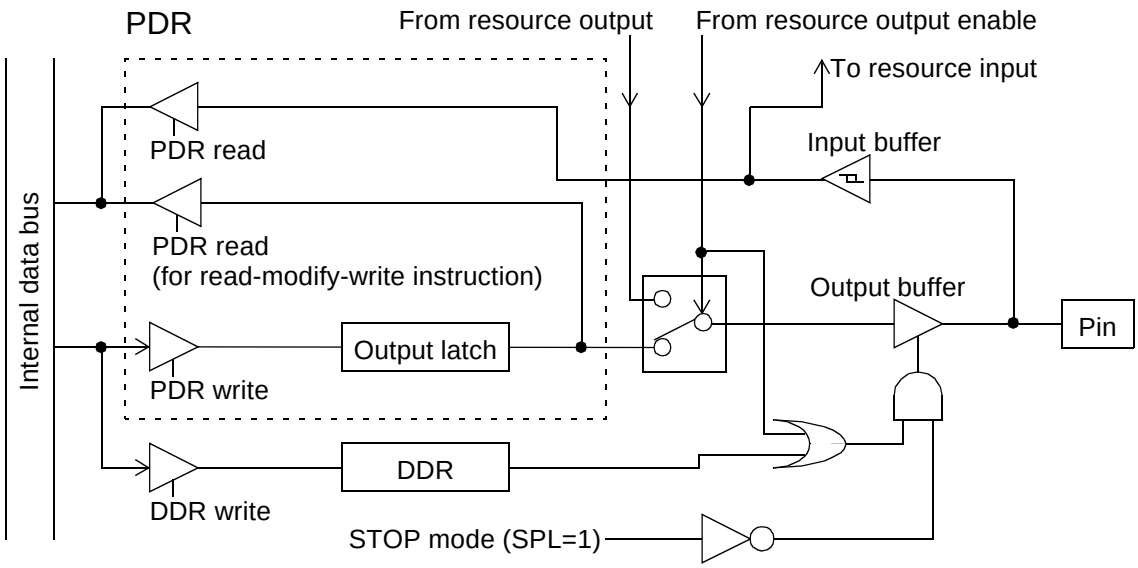


Fig. 2.2.3 Port 3

P40 to P47: CMOS-type output ports (also used as timer unit output)

- Output specification

  Each port bit has a DDR (data direction register) and a PDR (port data register), enabling input or output to be selected independently for each bit. A pin with DDR set to '1' is set for output, and a pin with DDR set to '0' is set for input. For port 4, the I/O setting is determined by the DDR regardless of the resource setting.

- Output port operation (DDR=1)

  When the DDR is set to '1,' the value written in the corresponding PDR is output to the pin with DDR set to '1.' Normally the PDR read value is the value of the pin, but not the contents of the output latch. However, in executing read-modify-write instructions, the contents of the output latch are read regardless of the DDR setting. Therefore bit processing instructions can be used even when input and output functions are both performed on the same pin. Regardless of the DDR setting, data written to the PDR is held in the output latch.

- Input port operation (DDR=0)

  When used as an input port, the output state is high impedance. Therefore the PDR read value is the value of the pin.

- Resource output operation

  When used as the output pin for the timer unit, control of the PDR is switched to the timer unit, even if the COER register of the timer unit is set. Therefore, output operation is designated by setting the DDR value of the corresponding pin for output.

  When used for non-overlapping three-phase waveform output, the X, Y, and Z signal is output as an inverted U, V, W signal rather than through the PDR. Output operation is designated by setting the DDR value of the corresponding pin for output.

  The RTO0 signal for starting the A/D converter uses the signal selected by the COER register, to be connected to the A/D converter. Therefore, the A/D converter can be started regardless of the setting of the DDR.

- Resource input operation

  Ports that double as resource inputs provide pin input values at all times regardless of the DDR or resource settings. If an external signal is used by a resource, the DDR should be set to input.

- Status at reset

  The DDR and resource output enable bits are initialized to 0 and all bits are set to output with high impedance after a reset. The PDR is indeterminate at reset, and retains the value it had before the DDR was reset to output.

- Status in stop mode

  In stop mode, when the SPL bit of the standby control register is set to '1,' the output is set to high impedance regardless of the value of the DDR.

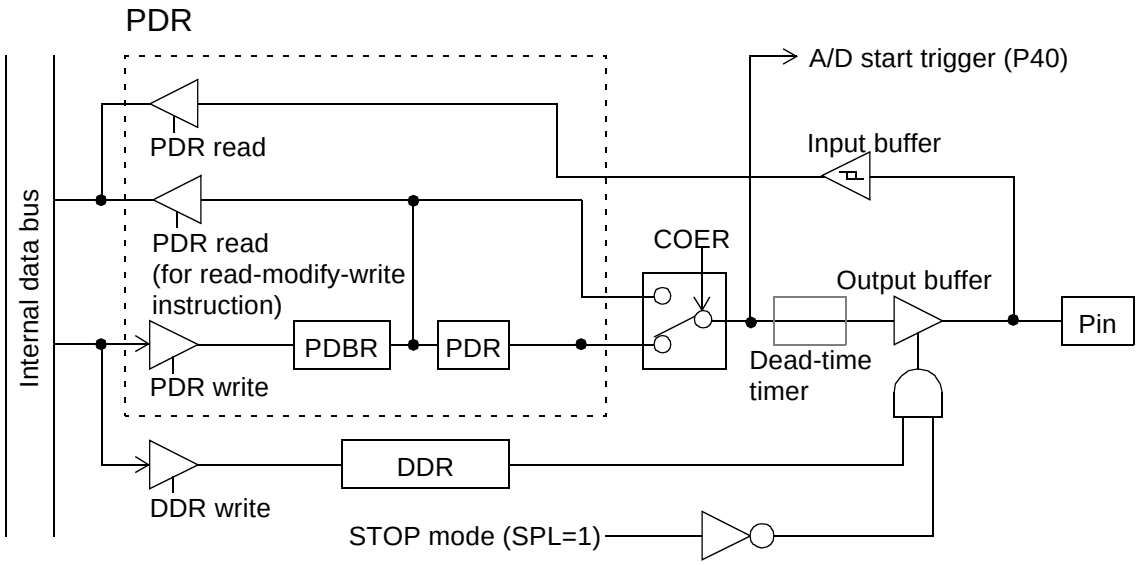


Fig. 2.2.4 Ports 40 to 43

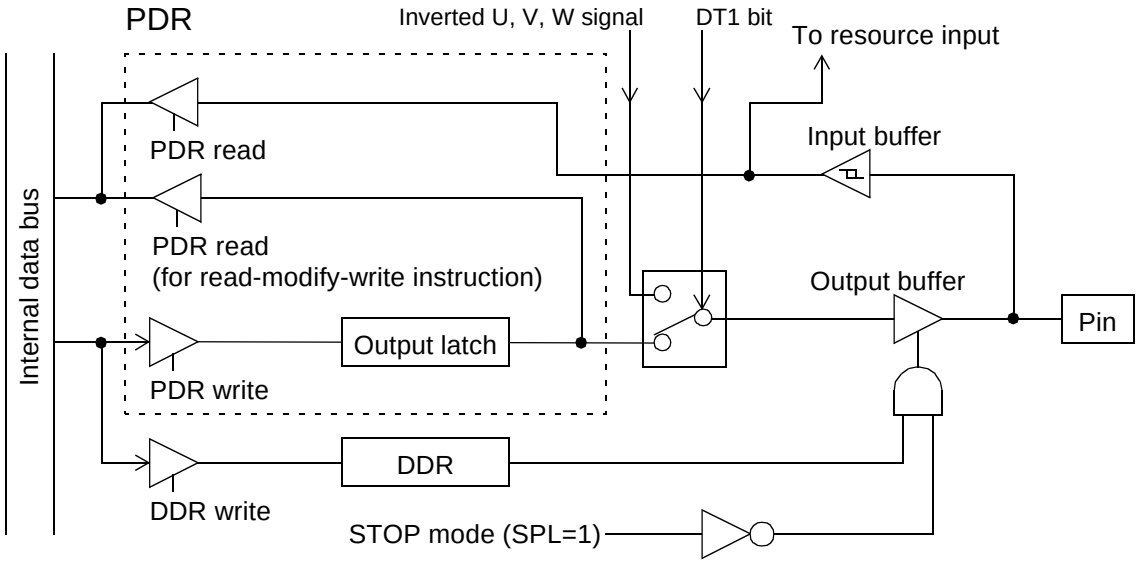


Fig. 2.2.5 Ports 44 to 47

P50 to P57: N-ch open drain-type output ports (also used as analog input)

- Output port operation

  The value written to the PDR is output to the pin. At these ports, the read value of the PDR is the contents of the output latch, so that the state of the pin itself cannot be read.

- Analog input operation

  When using these pins for analog input, The PDR is set to '1' to turn off the output transistor.

- Status at reset

  At a reset, the PDR is initialized to '1' and then output transistors for all bits are turned off.

- Status in stop mode

  In stop mode, when the SPL bit of the standby control register is set to '1,' the output is set to high impedance regardless of the value of the PDR.

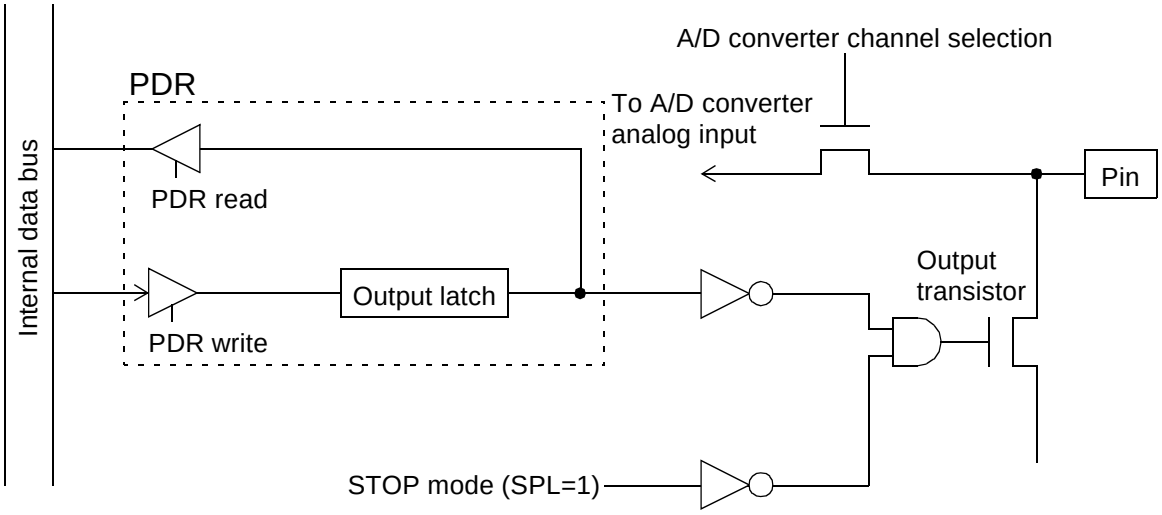


Fig. 2.2.6 Port 5

P60, P64: Input-only ports (also used as resource input)

- Input port operation

  The PDR for these ports can only be read, so that the read value is always the value of the pin. When used as a resource input, the read value is the value of the pin.

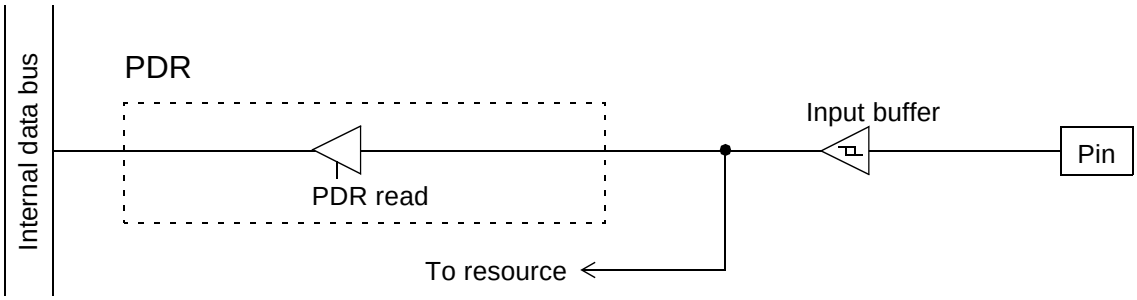


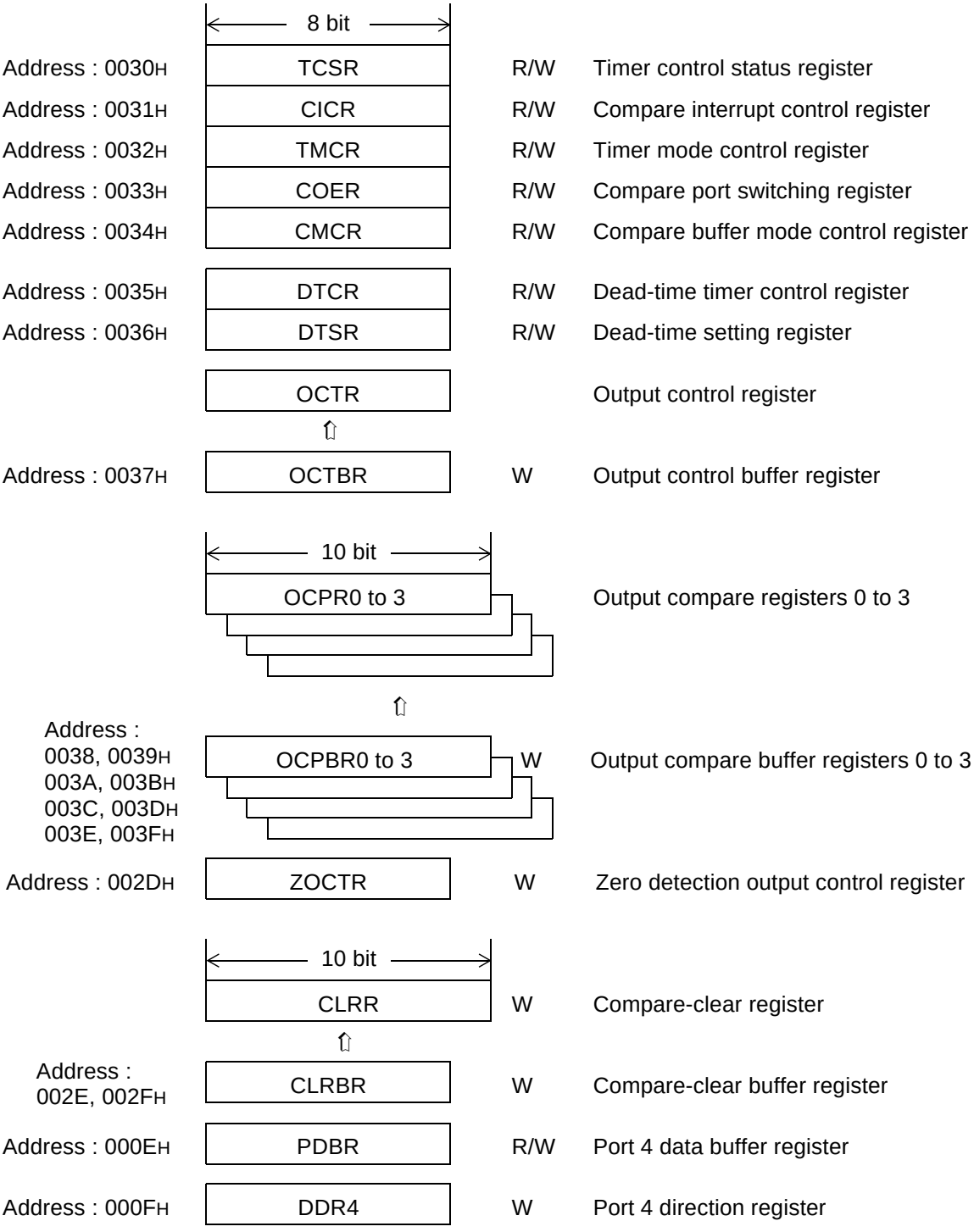
Fig. 2.2.7 Port 6

2.2.2 Timer Unit

Overview

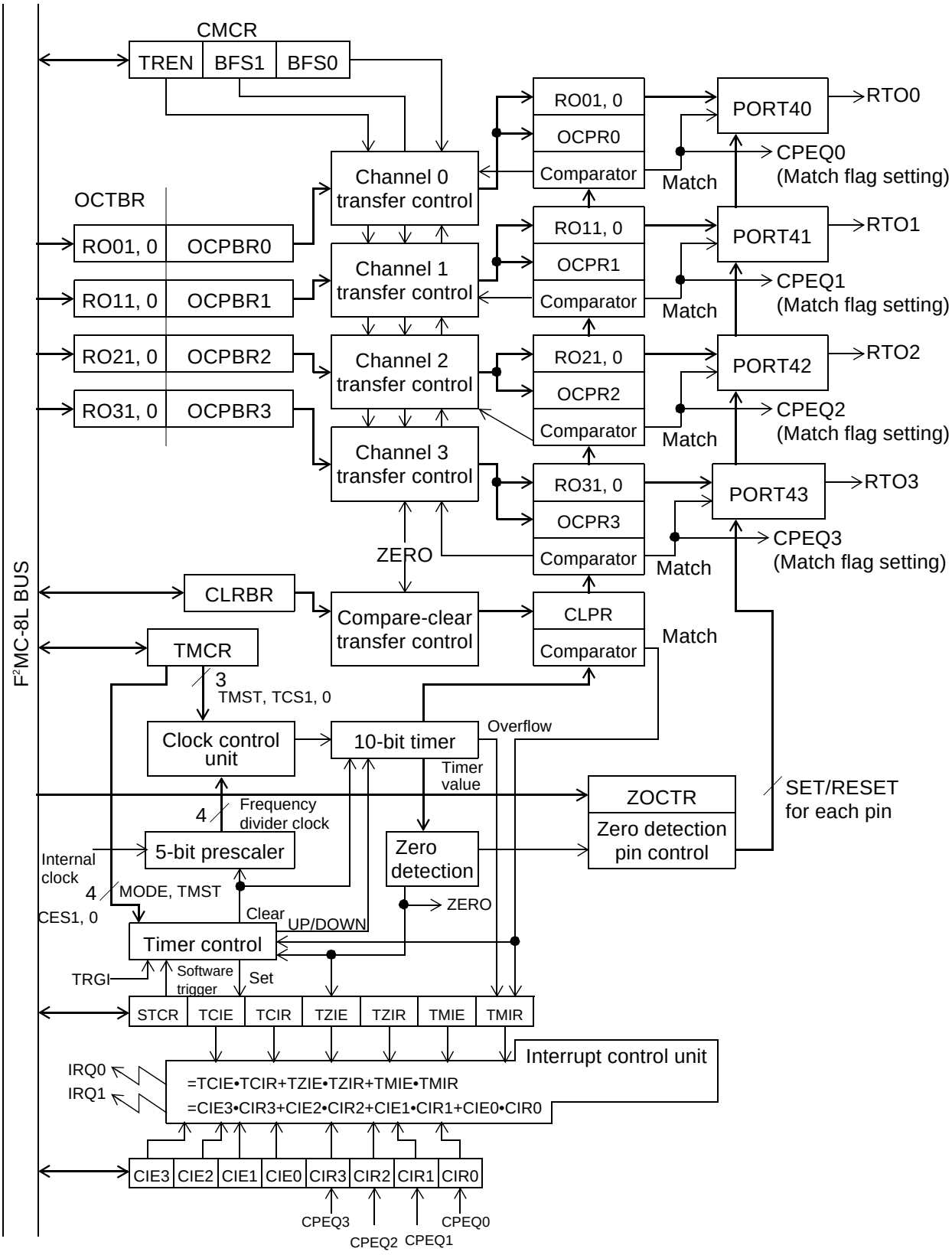
- This unit consists of one 10-bit up/down timer, one compare-clear register for cycle setting, four compare registers for output pin control, and one zero detection control register. It controls four realtime waveform output pins.
- There are two timer count modes: one for clearing the timer at detection of coincidence with the compare-clear register, and one for switching from increment to decrement counting. (In this mode, when the timer value goes to zero, decrementing is switched to incrementing.)
- The compare register and compare-clear register have buffer registers in which the next timer compare value is stored.
- The value in the buffer register is transferred to the compare register when the compare values match, or when timer value 000H is detected.
- Easy output of non-overlapping three-phase waveforms (U, V, W, X, Y, Z) for inverter motor control is available using the dead-time timers for each phase.
- External pins or software can be used for forced shutoff of the three-phase waveform output.
- The A/D converter can be started according to timing set up in the compare register.

(1) Register list

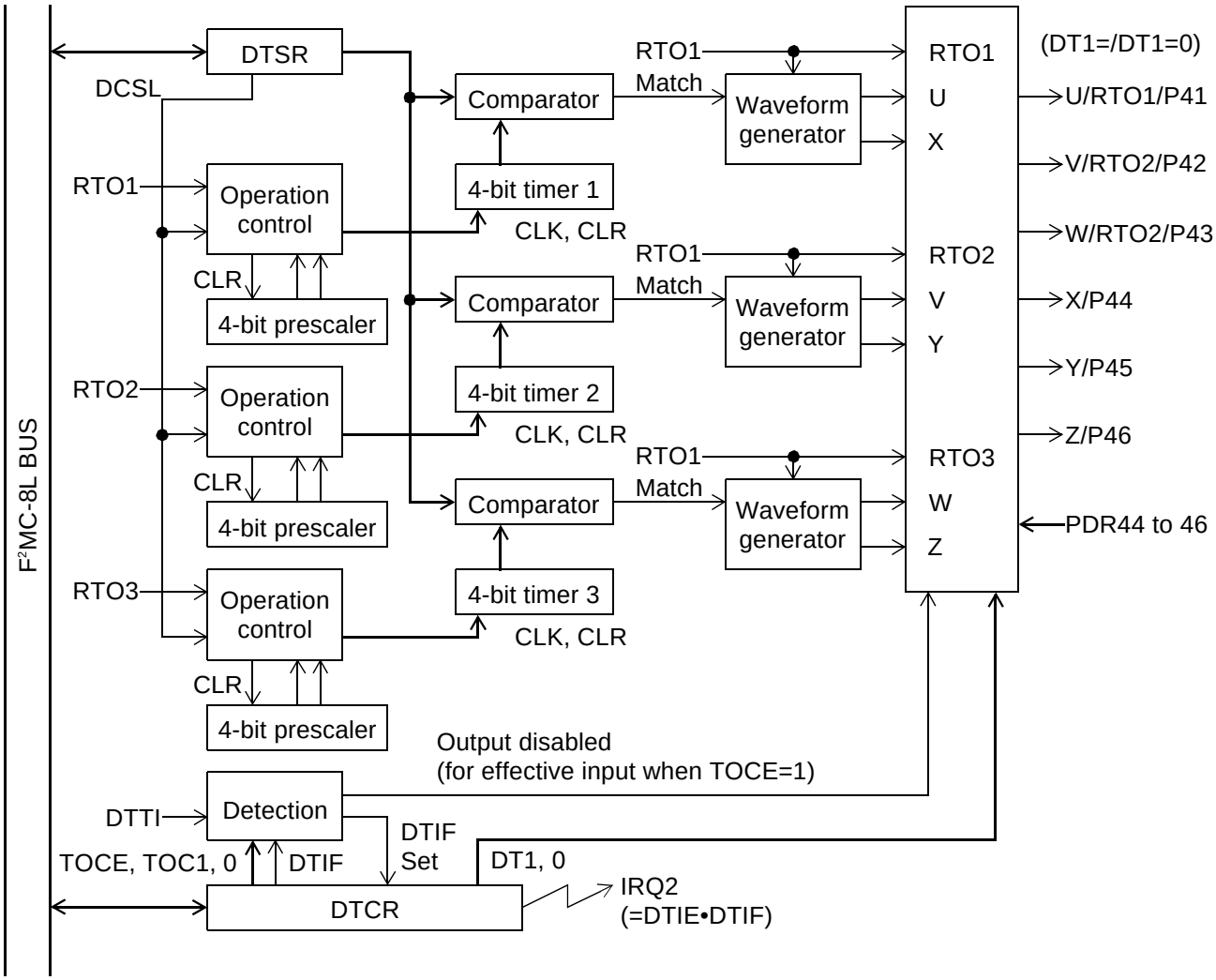


(2) Block diagrams

(2.1) Timer waveform generator block diagram



(2.2) Dead-time generator block diagram



(3) Description of registers

(3.1) TCSR (Timer Control Status) Register

This register is used to clear the timer by software instructions, to enable transfers to the compare buffer register, and to control the clear interrupt, zero detection interrupt, and overflow interrupt functions from trigger input.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0030H	STCR	–	TCIE	TCIR	TZIE	TZIR	TMIE	TMIR	1-000000B
	(W)		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] STCR: Software timer clear bit

Bit 7 is used to clear the timer count value. Write '0' to this bit to clear the timer and the prescaler.

Writing '1' to this bit is ignored and no operation is performed.

The read value of this bit is always '1.'

0	Clears timer and prescaler.
1	No operation

[Bit 5] TCIE: Timer clear interrupt enable bit

Bit 5 is used to enable an interrupt request when the timer is cleared by external trigger input (TRGI).

0	Disables timer clear interrupt by external trigger input
1	Enables timer clear interrupt by external trigger input

[Bit 4] TCIR: Timer clear interrupt request flag

This bit is an interrupt request flag used to clear the timer by external trigger input (TRGI). Set this bit to '1' to clear the timer from external trigger input.

Write '0' to clear this bit.

Writing '1' to this bit is ignored and the value of this bit is unchanged.

For read-modify-write instructions, the read value of this bit is always '1.'

0	No request for timer clear interrupt from external trigger input
1	Request for timer clear interrupt from external trigger input

[Bit 3] TZIE: Zero detection interrupt enable bit

This bit is used to enable zero detection interrupt requests, which originate when a timer value of zero is detected.

0	Disables zero detection interrupt request
1	Enables zero detection interrupt request

[Bit 2] TZIR: Zero detection interrupt request flag

This bit is an interrupt request flag for the timer zero detection interrupt. It is set to '1' when a timer value of zero is detected.

Write '0' to clear this bit.

Writing '1' to this bit is ignored and the value of this bit is unchanged.

For read-modify-write instructions, the read value of this bit is always '1.'

0	No request for zero detection interrupt
1	Request for zero detection interrupt

[Bit 1] TMIE: Timer interrupt request enable bit

This bit is used to enable timer overflow interrupts/compare-clear match detection interrupts.

0	Disables overflow/compare-clear match detection interrupts
1	Enables overflow/compare-clear match detection interrupts

[Bit 0] TMIR: Timer overflow/compare-clear match interrupt request flag

This bit is an interrupt request flag for timer overflow or compare-clear match interrupts.

Bit 0 is set to '1' when the timer overflows or when a match is detected between the values of the compare-clear register and timer.

Write '0' to clear this bit.

Writing '1' to this bit is ignored and the value of this bit is unchanged.

For read-modify-write instructions, the read value of this bit is always '1.'

0	No request for overflow/compare-clear match detection interrupts
1	Request for overflow/compare-clear match detection interrupts

(3.2) CICR (Compare Interrupt Control) Register

This register is used for control of compare match interrupts, which are separate interrupts originating from each channel in the compare register. The interrupt request sent to the CPU is the OR-product of the interrupts for the four channels.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0031H	CIE3	CIE2	CIE1	CIE0	CIR3	CIR2	CIR1	CIR0	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bits 7 to 4] CIE3 to CIE0: Compare match interrupt request enable bits

CIE3: Enables interrupt request to CIR3

CIE2: Enables interrupt request to CIR2

CIE1: Enables interrupt request to CIR1

CIE0: Enables interrupt request to CIR0

0	Disables interrupt request at compare match
1	Enables interrupt request at compare match

[Bits 3 to 0] CIR3 to CIR0: Compare match interrupt request flags

These bits are flags, set to '1' when a match is detected between the values of the corresponding compare register and timer.

Write '0' to clear the bit

Writing '1' is ignored and the values of the bits are unchanged.

For read-modify-write instructions, the read value of these bits is always '1.'

CIR3: Set to '1' when values of compare register 3 (OCPR3) and timer agree.

CIR2: Set to '1' when values of compare register 2 (OCPR2) and timer agree.

CIR1: Set to '1' when values of compare register 1 (OCPR1) and timer agree.

CIR0: Set to '1' when values of compare register 0 (OCPR0) and timer agree.

0	No request for interrupt at compare match
1	Request for interrupt at compare match

(3.3) COER (Compare/Port Switching) Register

This register is used to switch between the general-purpose port and timer unit-dedicated port functions.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0033H	–	–	–	–	RTO3	RTO2	RTO1	RTO0	----0000B
					(R/W)	(R/W)	(R/W)	(R/W)	

[Bits 3 to 0] RTO3 to RTO0: Realtime output set bits

Bits 3 to 0 are used to switch the functions of external pins.

0	Operates as general-purpose port
1	Operates as dedicated output port for timer unit

(3.4) TMCR (Timer Mode Control) Register

This register is used to set the operating mode of the timer, the transfer mode of the buffer register, the signal edge at which the timer is cleared, the timer start and stop signals, and the count clock pulse.

Rewriting of values in this register must be performed with the timer in the stop state.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0032H	TMST	MODE	TSTX	–	CES1	CES0	TCS1	TCS0	001-0000B
	(R/W)	(R/W)	(W)		(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 7] TMST: Timer start/stop bit

This bit is used to start and stop the timer.

When the timer is started, the prescaler is cleared to start counting.

0	Timer stops (default value)
1	Timer starts

[Bit 6] MODE: Timer count mode select bit

This bit is used to select the operating mode of the timer when a match is detected between values of the compare-clear register and the timer.

0	Sets timer to increment mode. When a match occurs, the timer is cleared to start counting up from 0000H.
1	Sets timer to increment/decrement mode When a match occurs, the timer is switched from increment to decrement. When zero is detected, the timer is switched from decrement to increment.

[Bit 5] TSTX: Test mode select bit

This bit is used to test the timer unit.

Set this bit to '1.'

[Bits 3,2] CES1, CES0: External trigger input edge select bits

These bits are used to select the signal edge at which the timer is cleared by external trigger input.

Both the timer and prescaler are cleared when input of the selected edge is detected.

CES1	CES0	Signal edge for timer clearing
0	0	No operation (timer clear disabled)
0	1	Timer cleared when rising edge is detected
1	0	Timer cleared when falling edge is detected
1	1	Timer cleared when either edge is detected

[Bits 1,0] TCS1, TCS0: Timer count clock pulse select bits

These bits are used to select the timer count clock pulse.

TCS1	TCS0	Timer clock source pulse
0	0	1 instruction cycles
0	1	2 instruction cycles
1	0	8 instruction cycles
1	1	16 instruction cycles

(3.5) CMCR (Compare Buffer Mode Control) Register

This register is used to control transfers from the compare buffer register to the compare register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0034H	–	–	–	–	–	TREN	BFS1	BFS0	-----100B
						(R/W)	(R/W)	(R/W)	

[Bit 2] TREN: Transfer enable bit

This bit is used to enable transfer of values in the compare buffer register and the compare-clear buffer register to the compare register and the compare-clear register, when the conditions determined by the buffer mode select bits BFS1 and BFS0 (bits 1 and 0 of this register) are detected.

0	Disables transfer from buffer register to compare register
1	Enables transfer from buffer register to compare register

[Bit 1] BFS1: Buffer mode select bit 1

Bit 1 is used to select the mode of transfer from the compare buffer registers to the compare registers for compare channels 1 to 3. This bit must not be overwritten during operation.

0	Transfers value from buffer register to compare register when compare values agree.
1	Transfers value from buffer register to compare register when count value is 000H.

[Bit 0] BFS0: Buffer mode select bit 0

Bit 0 is used to select the mode of transfer from the compare buffer registers to the compare registers for compare channel 0. This bit must not be overwritten during operation.

0	Transfers value from buffer register to compare register when compare values agree.
1	Transfers value from buffer register to compare register when count value is 000H.

Note: While the timer is stopped, values from the buffer are transferred to the compare register regardless of the indicated buffer mode (when the transfer is enabled).

(3.6) DTCR (Dead-time Timer Control) Register

This register is used to control the dead-time timer for non-overlapping three-phase waveform output, used to control the AC inverter motor.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0035H	DMOD	TOCE	TOC1	TOC0	DTIE	DTIF	DT1	DT0	XXXX0000B
	(W) *	(W) *	(W) *	(W) *	(R/W)	(R/W)	(W) *	(R/W)	

Note: * indicates bits for which only the first write data is valid.

[Bit 7] DMOD: Three-phase waveform output mode select bit

This bit is used to select the polarity when generating non-overlapping signal.

This bit has no meaning unless three-phase waveform output is specified (DT1 bit set to '0').

0	Positive-polarity non-overlapping signal generated
1	Negative-polarity non-overlapping signal generated

[Bit 6] TOCE: Three-phase waveform output stop input enable bit

This bit is used to enable the DTTI pin value to be input to control three-phase waveform output.

This bit has no meaning unless three-phase waveform output is specified (DT1 bit set to '0').

0	No control by DTTI pin
1	Control by DTTI pin

[Bits 5,4] TOC1,TOC0: DTTI pin input condition setting bits

These bits are used to set the input conditions for control of three-phase waveform output through the value of the DTTI pin input.

The DTIF bit is set when the conditions specified by these pins are input. If the TOCE bit is set to '1,' 6 three-phase waveform output pins are fixed at inactive level.

TOC1	TOC0	Conditions for output control by DTTI pin
0	0	While '0' is input
0	1	While '1' is input
1	0	From input at falling edge until DTIF pin is cleared by falling edge detection
1	1	From input at rising edge until DTIF pin is cleared

[Bit 3] DTIE: DTTI pin input interrupt enable bit

This bit is used to enable an interrupt request from the DTTI pin input.

0	Disables interrupt request from DTTI pin input
1	Enables interrupt request from DTTI pin input

[Bit 2] DTIF: DTTI pin input interrupt request flag

This bit is set to '1' when the conditions set by the TOC1,TOC0 bits are input to the DTTI input pin.

Write '0' to this bit to clear flag.

Writing '1' to this bit is ignored and the value of this bit is unchanged.

For read-modify-write instructions, the read value of this bit is always '1.'

0	No request for interrupt from valid DTTI pin input
1	Request for interrupt from valid DTTI pin input

[Bits 1,0] DT1,DT0: Dead-time timer control bits

These bits are used to switch the function of the output pins for the dead-time timer and to control the operation of non-overlapping signal generation.

DT1	DT0	Pin	Function
0	0	General-purpose port/ timer unit output	Dead-time timer stopped
0	1		
1	0	Three-phase waveform output	Fixed at inactive level
1	1	Three-phase waveform output	Non-overlapping three-phase waveform signal output

(3.7) DTSR (Dead-time Setting) Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0036H	DCSL	NRSL	-	-	DTC3	DTC2	DTC1	DTC0	X---XXXXB
	(W) *	(W) *			(W)	(W)	(W)	(W)	

Note: * indicates bits for which only the first write data is valid.

[Bit 7] DCSL: Dead-time timer clock source select bit

Bit 7 is used to select the clock source for the dead-time timer.

0	1 instruction cycle
1	8 instruction cycles

[Bit 6] NRSL: Noise cancellation function select bit

This bit is used to control selection of the noise cancellation function for DTTI pin input.

0	Inputs signal directly into the circuit without passing through noise cancellation circuits.
1	Inputs signal into the circuit after passing through noise cancellation circuits.

[Bits 3 to 0] DTC3 to DTC0: Dead-time count registers

These bits are used to store the compare values for the dead-time count generator counter.

The non-overlapping time interval is determined by the compare values that are common to all three dead-time timers.

(3.8) OCTR, OCTBR (Output Control Register, Output Control Buffer Register)

These registers are used to control the output compare operation. When compared values agree, the operation of controlling each pin is set according to the values in these registers.

When the timer is operating, transfer of values from the buffer register to the compare register is performed for each channel according to the conditions determined by the BFS bit in the CMCR register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
	RO31	RO30	RO21	RO20	RO11	RO10	RO01	RO00	11111111B
	⇧		⇧		⇧		⇧		
Address: 0037H	RO31	RO30	RO21	RO20	RO11	RO10	RO01	RO00	11111111B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bits 7 to 0] ROX1,ROX0: Realtime output function select bits (X=3, 2, 1, 0)

Bits 7 to 0 are used to determine the realtime output operation when the designated compare values agree.

UP count mode (MODE=0)

ROX1	ROX0	Realtime output operation when compare values agree
0	0	Reset to '0'
0	1	Set to '1'
1	0	Transfers value of PDBR register
1	1	Holds values before match occurred

UP/DOWN count mode (MODE=1)

ROX1	ROX0	Realtime output operation when compare values agree
0	0	Set to '0' during UP count and to '1' during DOWN count
0	1	Set to '1' during DOWN count and to '0' during UP count
1	0	Transfers value of PDBR register
1	1	Holds values before match occurred

(X = 0, 1, 2, 3)

(3.9) OCPR0-OCPR3, OCPBR0-OCPBR3 (Output Compare Registers 0-3, Output Compare Buffer Registers 0-3)

These registers are used to store the compare values for the output compare function.

When the timer is operating, transfer of values from each buffer register to the compare register is controlled by the BFS bit of the CMCR register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
	–	–	–	–	–	–	CPR9	CPR8	------XXB
Address: 0038H 003AH 003CH 003EH	–	–	–	–	–	–	CPR9 (W)	CPR8 (W)	------XXB

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
	CPR7	CPR6	CPR5	CPR4	CPR3	CPR2	CPR1	CPR0	XXXXXXXXB
Address: 0039H 003BH 003DH 003FH	CPR7 (W)	CPR6 (W)	CPR5 (W)	CPR4 (W)	CPR3 (W)	CPR2 (W)	CPR1 (W)	CPR0 (W)	XXXXXXXXB

The registers and buffer registers are used to store the compare values for the output compare function.

When the timer is operating, transfer of values from each buffer register to its compare register is controlled according to the buffer mode set in the CMCR register. When the timer is stopped, the value of the buffer register is transferred to the compare register regardless of the buffer mode setting (if transfer enabled).

(3.10) ZOCTR (Zero Detection Output Control Register)

This register is used to control pin output when a timer value of 0 is detected.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 002DH	–	–	–	ZOSC (W)	ZSB3 (W)	ZSB2 (W)	ZSB1 (W)	ZSB0 (W)	---X0000B

[Bit 4] ZOSC: Zero detection output control function select bit

Bit 4 is used to set the operation of the realtime output function when a timer value of 0 is detected.

If this function is selected, all pins are controlled.

If this function is selected simultaneously with the output compare function, the output compare function takes precedence.

0	Resets to '0' all pins set by ZSB3 to ZSB 0.
1	Resets to '1' all pins set by ZSB3 to ZSB 0.

[Bits 3 to 0] ZSB3 to ZSB0: Selection bits for pins controlled by zero detection function

Bits 3 to 0 are used to select pins for control of realtime output when a timer value of 0 is detected. The bits ZSB3 to ZSB0 correspond to RTO3 to RTO0.

0	Pins not controlled at zero detection
1	Pins controlled at zero detection

(3.11) CLRBR, CLRR (Compare-Clear Buffer Register, Compare-Clear Register)

These registers and buffer registers are used to store the compare values for the compare-clear function.

The timer is cleared or set to down-count operation when the values of these registers and the timer match.

When the timer is operating, transfer from the buffer register to the compare register is performed whenever the timer value is 000H.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
	–	–	–	–	–	–	CLR9	CLR8	------00B
					⇧				
Address: 002EH	–	–	–	–	–	–	CLR9	CLR8	------00B
							(W)	(W)	

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
	CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0	00000000B
					⇧				
Address: 002FH	CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0	00000000B
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	

When a match is detected between the value of this register and the timer, the timer will be cleared if the MODE bit of the timer mode control register (TMCR) is '0.' If the MODE bit is set to '1,' the timer will switch from increment to decrement and begin counting down.

If the match occurs simultaneously with an output compare event, both functions will be performed: pin control according to the output compare setting, and compare-clear processing.

If the match occurs simultaneously with an output compare in UP/DOWN mode, pin control is performed during downcounting.

Matches between the values of the compare-clear register and the timer are not detected when the value of this register is 000H.

(3.12) PDR4, PDBR (Port 4 Data Register and Port Data Buffer Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 000EH	PDR7	PDR6	PDR5	PDR4	PDR3	PDR2	PDR1	PDR0	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Address: 000EH	-	-	-	-	PDR3	PDR2	PDR1	PDR0	----XXXXB
					(R/W)	(R/W)	(R/W)	(R/W)	

The PDBR is a buffer register for the PDR4 register.

The bits selected as the general-purpose port function by the COER register for any of PDR4 bits 4-7 and bits 0-3, the PDBR register behave as a normal I/O port.

For the bits set by the COER register to function as a timer unit output port, writing to address 000EH is effectively the same as writing to the PDBR register. Read values are the values of the respective pins, and during read-modify-write operations the values of the PDBR register are read.

Also, if the dead-time timer is operating and non-overlapping three-phase output generated, the values of bits 4-6 in the PDR4 register are not output to the pins, but are switched to output of inverted waveforms for pins P41-P43.

(4) Description of operation

(4.1) Timer unit operation

The timer unit on the MB89863 series of microcontrollers consists of a 10-bit up/down counter, a prescaler for generation of clock source signals, and a timer operation control unit (count clock generation, run/stop, clear, increment/decrement, and overflow detection functions).

(a) Timer run/stop control

The timer enters operating state when the TMST bit of the TMCR register is set to '1.'

At this point, counting begins from the value at which the timer last stopped.

When the TMST bit is set to '0,' the timer stops.

At reset, the timer is initialized to 000H and stops.

(b) Timer count clock pulse

The count clock pulse signal used by the timer is selected by the TSC1 and TCS0 bits of the TMCR register.

These bits can be set to select the internal clock pulse from 1, 2, 8 and 16 instruction cycles.

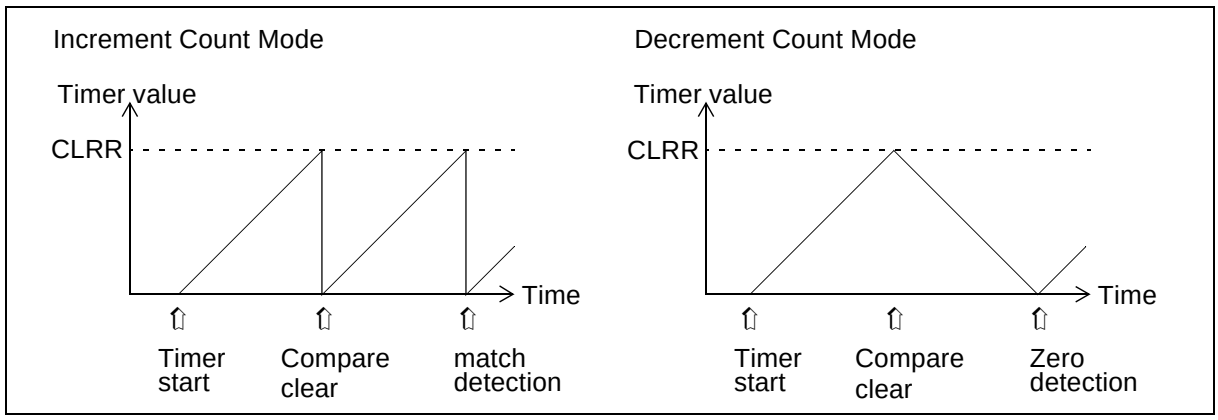
The prescaler for internal clock pulse generation is initialized each time the timer is started and cleared by a trigger signal.

(c) Timer count modes

When the MODE bit of the TMCR register is set to '0,' the timer operates in increment mode. In increment mode, each time a match is detected between the values of the compare-clear register and the timer, the timer is cleared and counting continues from 000H.

When the MODE bit is set to '1,' the timer operates in increment/decrement mode.

In this mode, each time a match is detected between the values of the compare-clear register and the timer, the timer switches direction from increment to decrement counting. When the timer value 000H is detected, the direction switches from decrement to increment counting.



(d) Timer clear function

The timer can be cleared by a software, by external pin trigger input, and when a match is detected between the values of the compare-clear register and the timer value during increment counting.

Clearing by software occurs when '0' is written to the STCR bit of the TCSR register, which immediately clears the timer and prescaler and counting continues from timer value 000H.

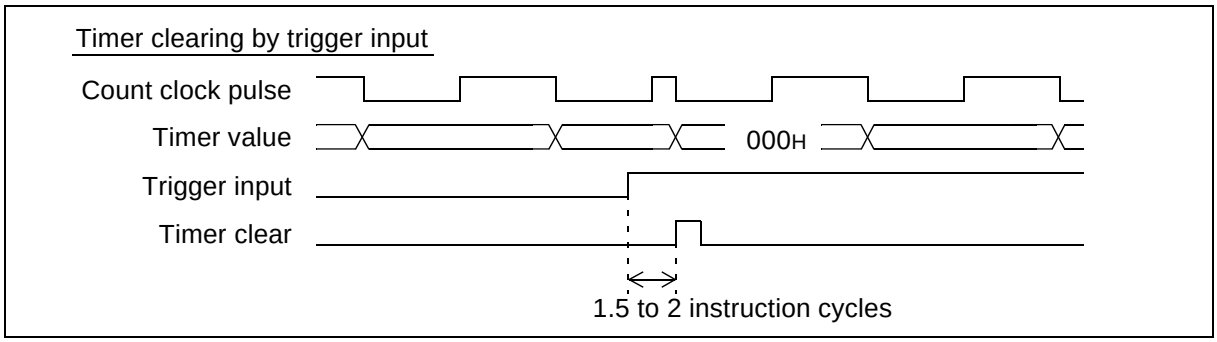
Clearing by external pin trigger input operates using a valid edge, determined by setting the CES1 and CES0 bits of the TMCR register.

When a valid edge signal is input and detected, the timer and prescaler are cleared and counting continues from timer value 000H. The TCIR bit of the TCSR register is set at this time.

1.5 to 2 instruction cycles are required from edge input detection to clear signal generation.

In clearing the timer when a match is detected between the timer value and the value in the compare-clear register, the timer value is cleared to 000H at the next count clock pulse after the pulse on which the match was detected. At this timing, however, the prescaler is not cleared.

The TMIR bit of the TCSR register is set at this time, and counting continues.



(e) Overflow

An overflow condition occurs when the timer value changes from 3FFH to 000H during increment counting.

The timer continues to count from 000H.

An overflow will not occur when the value of the compare-clear register is other than 000H (when a match is detected between the values of the compare-clear register and the timer).

(4.2) Compare match detection unit operation

The compare match detection unit consists of compare buffer registers, compare registers, transfer control unit, and comparators.

(a) Compare match detection

Each time a match is detected between the values of the timer and the OCPR register after random comparisons, the compare match detection unit outputs a match signal to each transfer control unit and pin control unit and sets the CIR bit in the CICR register corresponding to the compare register.

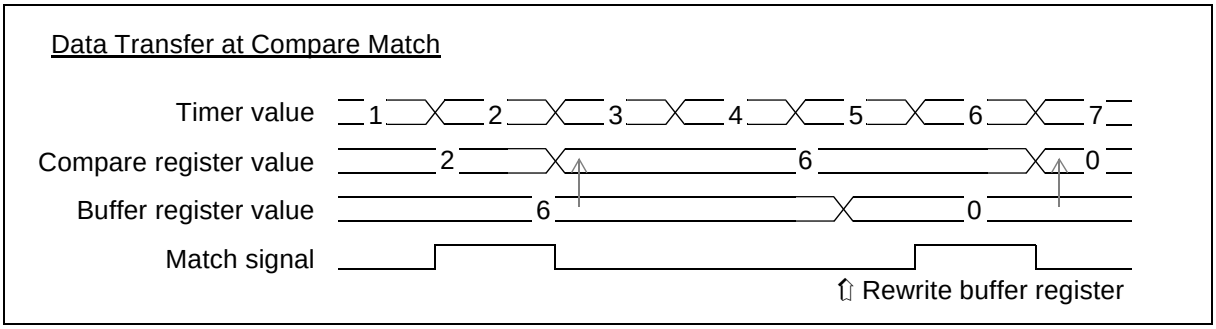
(b) Operation of compare buffer register and transfer control unit

While the timer is operating, the transfer of values from the compare buffer registers to the compare registers is controlled by the buffer mode select bits (BFS1 and BFS0) of the CMCR register.

When the timer is stopped, values are written to the buffer register and simultaneously transferred to the compare register.

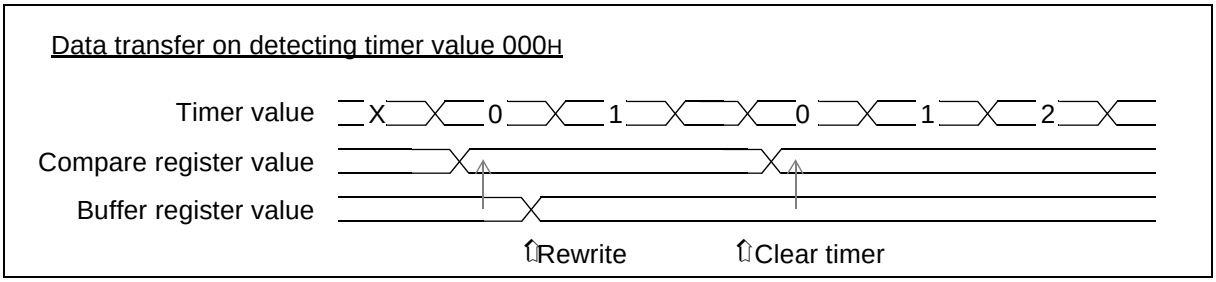
The buffer mode for compare channels 1 to 3 is selected by the BFS1 bit, and the buffer mode for compare channel 0 is controlled by the BFS0 bit.

If a compare-match occurs simultaneously with the input of a setting for transfer from the buffer register to the compare register, the transfer of the value in the buffer register (for the channel where the match has occurred) to the compare register takes place on the following count timing.



If the mode is set for transfer to occur when the timer count is 000H, the value in the buffer register will be transferred to the compare register simultaneously with zero detection.

Therefore the timer value 000H will be compared with the data after transfer.



Note: The initial value of the compare register is indeterminate. If the timer is activated without designating a value for the compare register, the compare-match function will compare the timer value with an indeterminate value for initial state.

(c) Buffer transfer enable bit

Setting the TREN bit of the CMCR register to '0' will disable all transfers from the compare buffer register to the compare register, as well as all transfers from the compare-clear buffer register to the compare clear register. All transfer sources occurring while the TREN bit is set to '0' are ignored.

After '1' is written to the TREN bit, transfers from buffer registers are executed when the transfer sources are generated.

This bit controls transfer operations even when the timer is stopped.

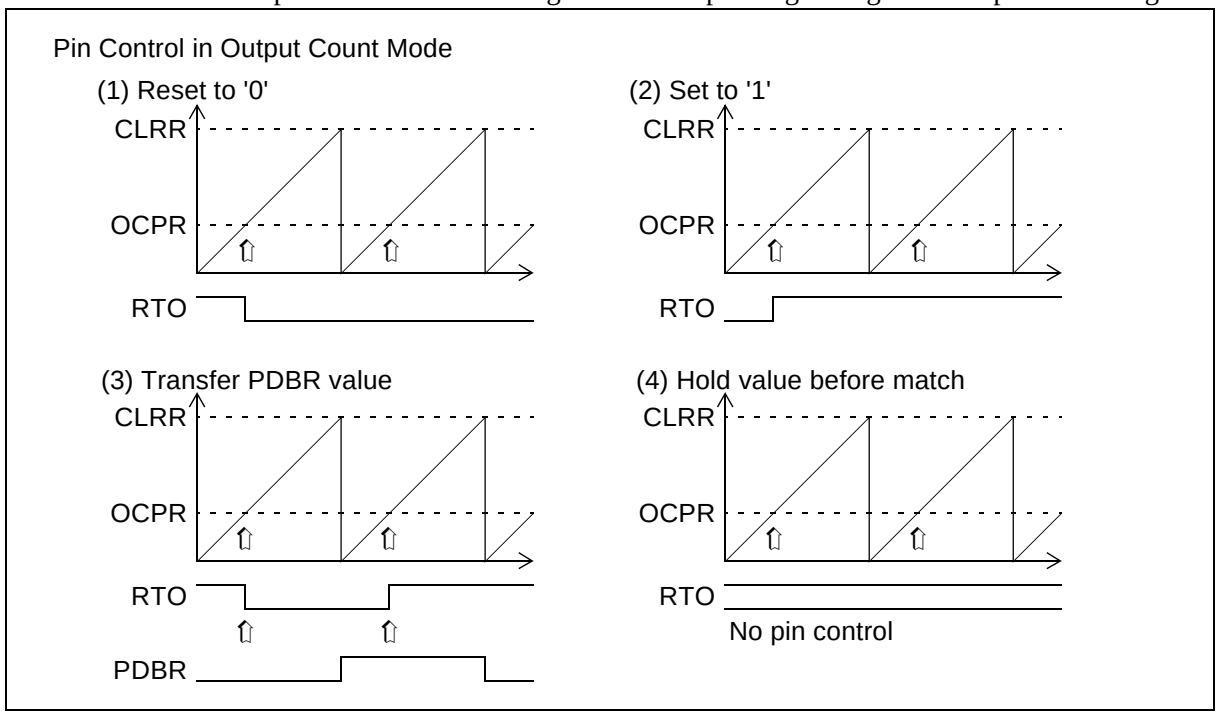
(4.3) Pin control unit operation

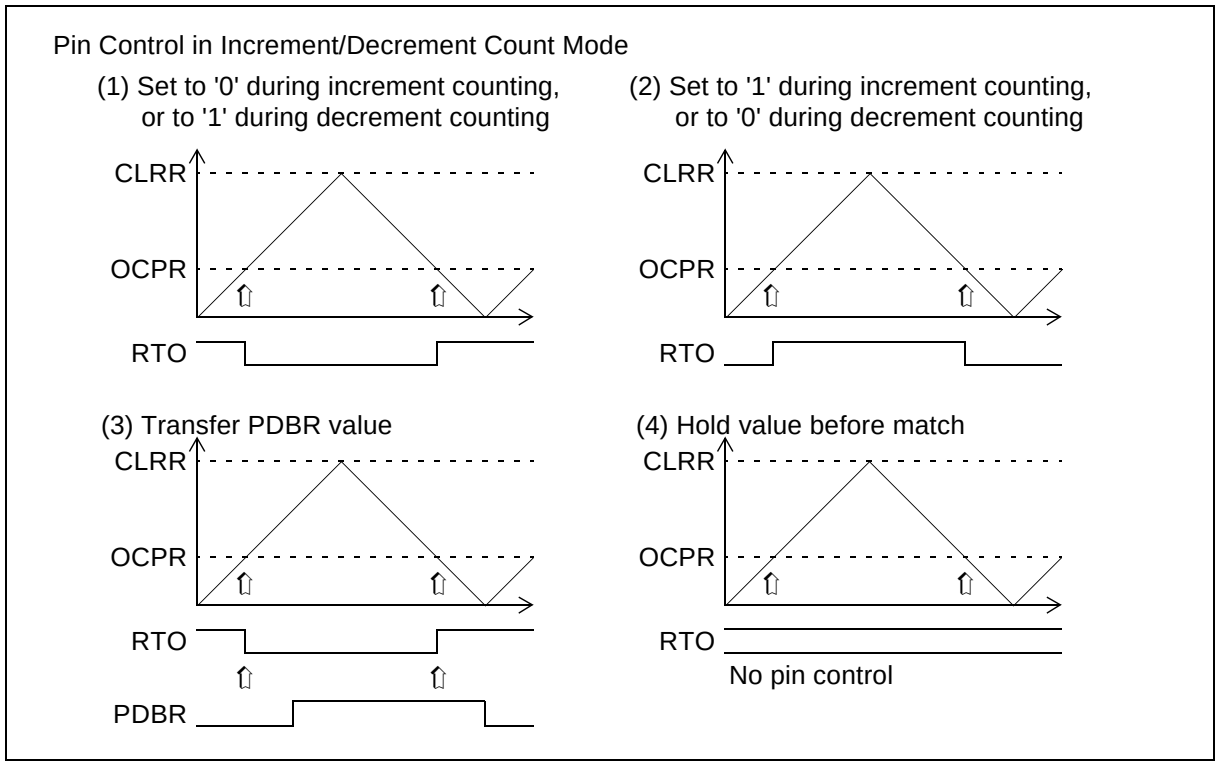
The pin control unit controls the RTO signal after receipt of the compare match detection signal.

(a). Output control operation

A pin control unit is provided for each realtime output pin, and the output compare registers 0 to 3 control the signals RTO0 to RTO3.

When a match signal is sent from the compare match detection unit to any of the pin control units, the action of the related pin is executed according to the corresponding setting in the output control register.





Pin control functions in increment/decrement count mode are equivalent to increment count mode controls with respect to timer values 00H, and to decrement count mode controls with respect to compare-clear register values.

(b) Compare/port switching operation

The COER register is used to select whether the internal signals RTO0 to RTO3 function as general-purpose port signals or as realtime output pin signals.

This register controls the internal signals RTO0 to RTO3. Thus, if the dead-timer timer is activated for three-phase waveform output, the resulting non-overlapping waveforms are created and supplied through the selected RTO1 to RTO3 signals for output to six ports 41 to 46.

COER	DT1	DDR	External pin operation
X	X	0	Functions as input port at high impedance
0	0	1	Functions as general-purpose port output
1	0	1	Functions as realtime output pin
0	1	1	Provides dead-time control for general-purpose port signal output
1	1	1	Provides dead-time control for realtime signal output

Note: The initial value of the realtime output signal is the value set in the PDR register before realtime output is selected in the COER register.

(4.4) Zero detection unit operation

Whenever the timer value is 000H, the zero detection unit sends a zero-detection signal to the transfer control unit and zero-detection pin control unit, and simultaneously sets the TZIR bit of the TCSR register.

Upon receiving the zero-detection signal, the zero detection pin control unit causes the pins designated by the ZSB0 to ZSB3 bits to operate as specified by the ZOSC bit of the ZOCTR register.

The timing of the zero-detection pin control function is the same as that of pin control by the output compare register.

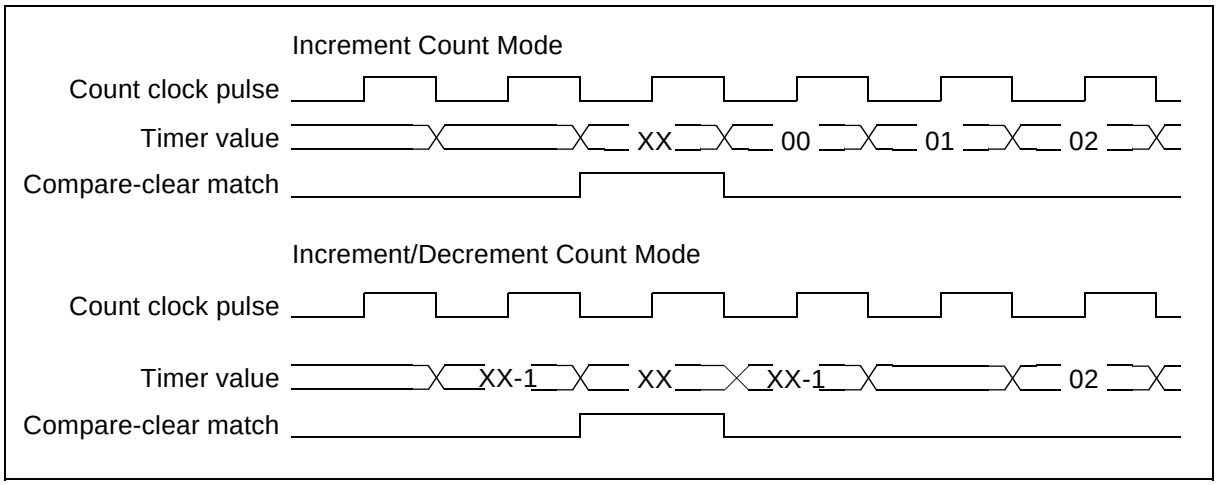
Note that if zero detection pin control occurs simultaneously with an output compare match, the zero detection pin control signal is masked regardless of the corresponding output operation setting, and pin control is applied by the output compare register.

(4.5) Compare clear operation

Whenever a match is detected between the values of the compare-clear register and the timer, a match signal is output to the timer control section. The timer count is controlled and the TMIR bit of the TCSR register is set.

When the timer is in increment count mode, this compare-clear match event causes the timer count to be cleared to 000H at the next count, after which the timer continues counting up.

When the timer is in increment/decrement count mode, this compare-clear match event causes the timer to start counting down at the next count.

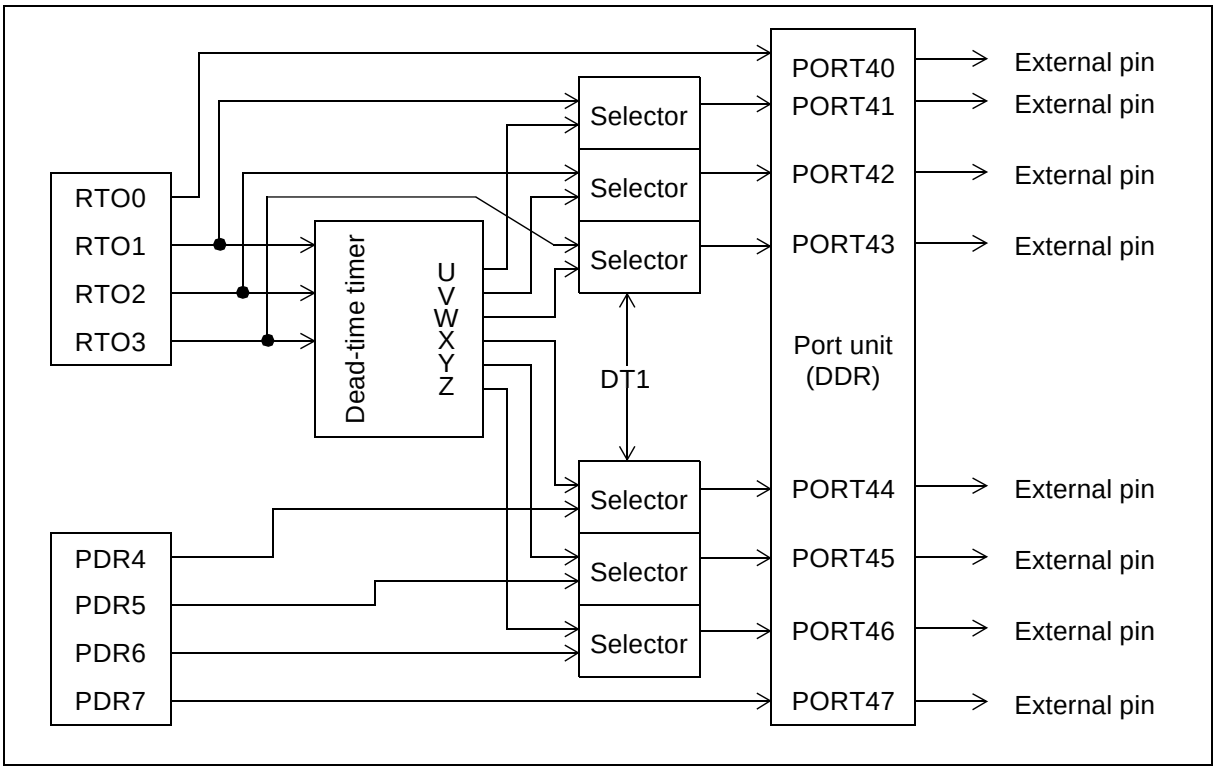


The compare-clear register has a buffer register. If the timer is stopped, the value from the buffer register is transferred to the compare-clear register simultaneously with writing of a new value to the buffer register. When the timer is operating, transfer is performed simultaneously with the zero detection of a timer value of 000H.

(4.6) Dead-time generator unit operation

The dead-time generator unit provides a realtime output pulse for the RTO1 to RTO3 signals. When the DT1 bit in the DTCR register is '0,' the RTO1 to RTO3 signals are output directly to the port unit.

If the DT1 bit is '1' the dead-time generator generates non-overlapping signals of RTO1 to RTO3 signals and their inverse signals, and outputs these to the port unit.

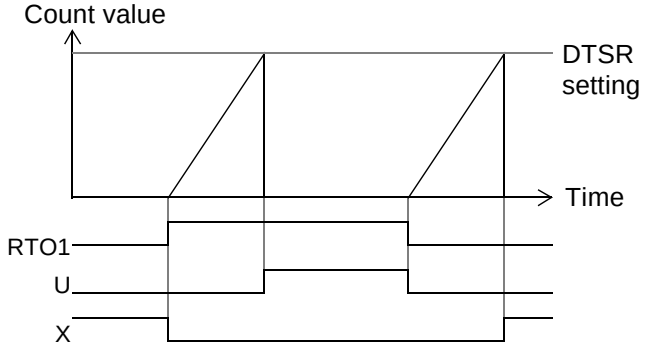


(a) Non-overlapping signal generation

When a positive-polarity non-overlapping signal is specified, a delay is applied at the rising edges of the RTO1 to RTO3 signals and their inverse signals. The non-overlapping signal delay time is set by the DTSR register.

If the pulse width of RTO1 to RTO3 signals is smaller than the designated non-overlapping delay time, the 4-bit counter applies a delay count at the next edge. Thus the signal is unchanged.

Non-Overlapping Signal Generation (Positive Polarity)

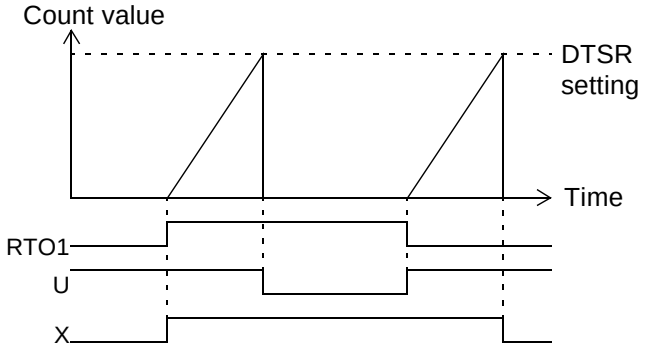


Pin name	Output signal
U	Signal with delay applied at rising edge of RTO1
V	Signal with delay applied at rising edge of RTO2
W	Signal with delay applied at rising edge of RTO3
X	Inverse signal with delay applied at falling edge of RTO1
Y	Inverse signal with delay applied at falling edge of RTO2
Z	Inverse signal with delay applied at falling edge of RTO3

When a negative-polarity non-overlapping signal is specified, a delay is applied at the falling edges of the RTO1 to RTO3 signals and their inverse signals. The non-overlapping signal delay time is set by the DTSR register.

If the pulse width of RTO1 to RTO3 signals is smaller than the designated non-overlapping delay time, the 4-bit counter applies a delay count at the next edge. Thus the signal is unchanged.

Non-Overlapping Signal Generation (Positive Polarity)



Pin name	Output signal
U	Inverted signal with delay applied at rising edge of RTO1
V	Inverted signal with delay applied at rising edge of RTO2
W	Inverted signal with delay applied at rising edge of RTO3
X	Signal with delay applied at falling edge of RTO1
Y	Signal with delay applied at falling edge of RTO2
Z	Signal with delay applied at falling edge of RTO3

Note: The following table lists settings for the DTC3 to DTC0 bits and the corresponding non-overlapping delay time.

Note that a setting of 0000B produces a non-overlapping delay of 0.5 instruction cycles, not a delay of zero.

DTC3 to DTC0	Non-overlapping time (instruction cycles)
0000	0.5
0001	1 × clock source
0010	2 × clock source
~	
1110	14 × clock source
1111	15 × clock source

(b) Operation Control

The dead-time timer is started by setting the DT1 bit to '1' at the first write cycle after canceling a reset to the DTCR register.

When the DT1 bit is set o '0,' the dead-time timer cannot be started.

At the second and subsequent write accesses, only the DTIE, DTIF and DT0 bits can be rewritten.

(c) Three-phase waveform output disable bit operation

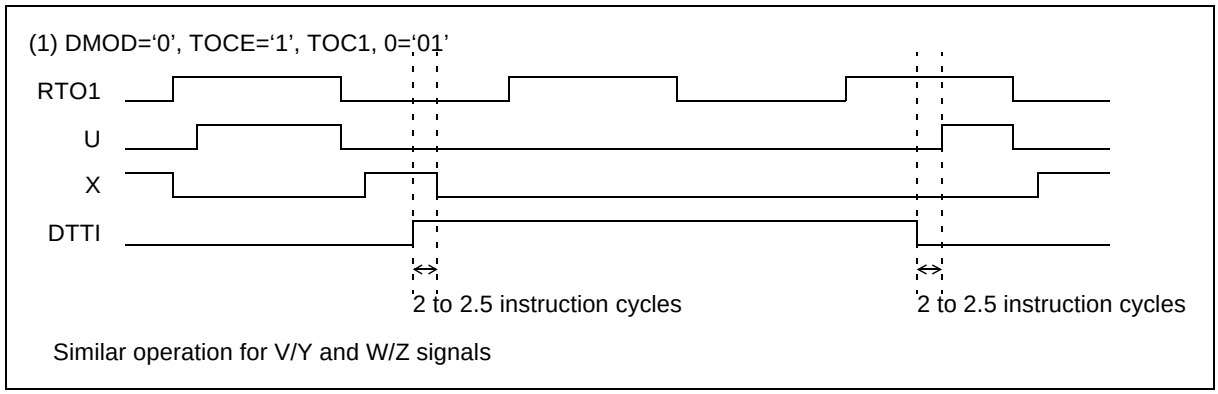
The non-overlapping three-phase waveform output can be held at inactive level by setting the DT0 bit of the DTCR register to '0' while three-phase waveform output is enabled. The three-phase waveform output will be held at inactive level until the DT0 bit is set to '1.'

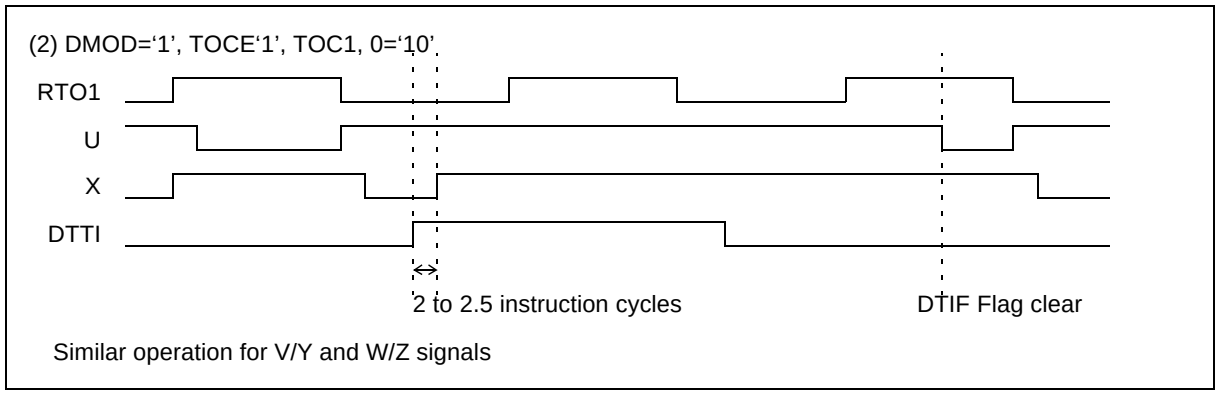
(d) Dead-time timer disable input pin operation

The DTTI pin input signal can be used to control the three-phase waveform output, by setting the TOCE bit of the DTCR register to '1' to enable this control feature.

Three-phase waveform output will be held at inactive level whenever the input signal to the DTTI pin satisfies the conditions set by the TOC1 and TOC0 bits. The time interval required from DTTI pin input to pin output control is 2 to 2.5 instruction cycles.

Note that the timer unit will continue to operate while generating waveform signals even when the pins are held at inactive level by DTTI pin input.





(e) DTTI Pin Noise Cancellation Function

The noise cancellation circuit for DTTI pin input is enabled by setting the NRSL bit of the DTSR register to '1.' Selection of the noise cancellation function may introduce a delay in the timing of control applied to hold the output pin at inactive level (maximum delay of 0.5 instruction cycles).

(4.7) Interrupts

Three interrupt request channels, IRQ0 to IRQ2, are allocated for interrupt requests from the timer unit to the CPU.

The interrupt sources may be any of the following: timer clear trigger, zero detection, timer overflow, compare-clear match, output compare match, and DTTI pin input.

(a) Trigger input interrupt

When the external trigger input pin receives a valid signal edge as defined by the CES1 and CES0 bits of the TMCR register, the TCIR flag bit of the TCSR register is set to indicate an interrupt request. At this time if the TCIE bit is set to '1' (interrupt enabled), the timer unit will output an IRQ0 signal to the CPU.

(b) Zero detection interrupt

When the timer value reaches 000H the TZIR flag bit of the TCSR register is set. At this time, if the TZIE bit is set to '1' (interrupt enabled), the timer unit will output an IRQ0 signal to the CPU.

(c) Timer overflow/compare-clear match interrupt

When a timer value overflow or compare-clear match occurs, the TMIR flag bit of the TCSR register is set. At this time if the TMIE bit is set to '1' (interrupt enabled), the timer unit will output an IRQ0 signal to the CPU.

(d) Output compare match interrupt

When an output compare match occurs on a particular compare channel, the corresponding CIR flag bit in the CICR register is set. At this time, if the CIE bit for that compare channel is set to '1' (interrupt enabled), the timer unit will output an IRQ1 signal to the CPU.

(e) DTTI pin input interrupt

When the DTTI input pin receives the input signal defined by the TOC1 and TOC0 bits of the DTCR register, the DTIF flag bit is set. At this time, if the DTIF bit is set to '1' (interrupt enabled), the timer unit will output an IRQ2 signal to the CPU. This interrupt has no relation to the TOCE bit value.

(5) Usage examples

(5.1) Control of a sine-wave approximation PWM inverter

The following example illustrates use of the timer unit to control a sine-wave approximation PWM inverter.

Registers in the timer unit are set as follows:

TCSR=0X001000B

- Timer initialization before start ⇒ STCR=0
- Compare-clear interrupt ⇒ Disable (TCIE=0)
- Zero detection interrupt ⇒ Enable (TZIE=1), buffer rewrite in interrupt routine
- Timer interrupt ⇒ Disable (TMIE=0)

CICR=00000000B

- Compare match interrupt ⇒ Disable (CIE0 to CIE3=0)

COER=XXXX1110B

- Compare output/port switching ⇒ Use P43 to P41 as compare output pins (RTO1 to RTO3=1, RTO0=0)

TMCR=01XX0000B

- Timer count mode ⇒ Increment/decrement count mode
- External trigger ⇒ Not used (CES1, CES0=00)
- Timer count clock pulse ⇒ 1 instruction cycle, (TCS1, TCS0=00)
  [0.95 µs at f=4.2 MHz, 0.50 µs at f=8 MHz]

CMCR=XXXXX110B

- Buffer register transfer mode (compare 1 to 3) ⇒ Transfer when timer value is 0000B (BFS1=1)
- Buffer register transfer mode (compare 0) ⇒ Transfer at compare match (BFS0=0)

DTSR=00XX1100B

- Dead-time setting ⇒ 0.95 × 12 = 11.4 µs [at f=4.2 MHz]
  0.50 × 12 = 6.0 µs [at f=8 MHz]

DTCR=00111010B

- Three-phase waveform mode ⇒ Positive polarity (DMOD=0)
- Output control by DTTI ⇒ No control (TOCE=0)
- DTTI pin input conditions ⇒ Rising edge (TOC1, TOC0=11)
- DTTI interrupt ⇒ Enable (DTIE=1)
- Dead-time timer ⇒ Start/output fixed at inactive level (DT1, DT0=10)

OCTBR=01010111B

- Compare output operation ⇒ RTO1 to RTO3 set to '1' during increment counting and to '0' during decrement counting

OCPBR

- Compare value ⇒ Set according to desired output waveform

ZOCTR=XXX01110B

- Zero detection pin control ⇒ Reset RTO1 to RTO3 at zero detection occurrence (ZOSC=0, ZSB=1110)

CLRR=0FAH(250D)

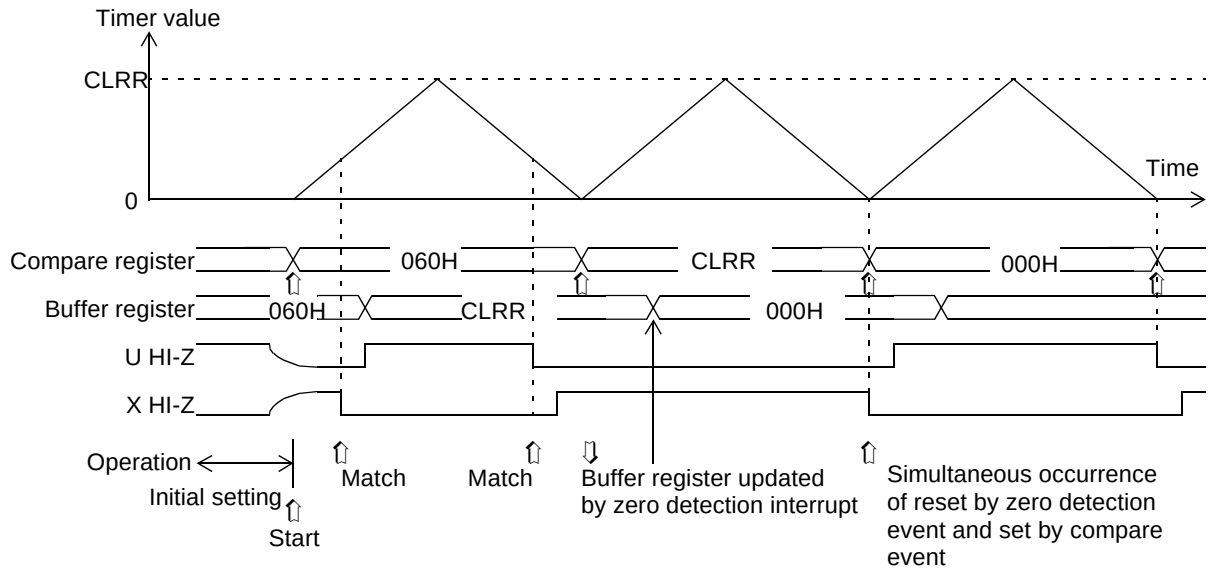
- Compare-clear value ⇒ Set to half of carrier cycle

After making the above settings, set the timer start bit TMST to '1,' the dead-time timer output enable bit DT0 to '1,' and specify external pin output (DDR41 to DDR46=1).

Initial settings

←Start

The following diagram illustrates the operation of the MB89863 with the settings on the previous page.



Compare Register Values and Output Waveforms for the Above Settings

Compare register setting	Output waveform	Pulse width at f=4.2 MHz	Pulse width at f=8 MHz
000H		475 µs	250 µs
001H		473.1 µs	249 µ
≀	≀	≀	≀
CLRR-1		1.9 µs	1.0 µs
CLRR		0 µs	0 µs

(5.2) Four-Channel PWM Output

The following example illustrates use of the timer unit for 4-channel independent PWM output.

Registers in the timer unit are set as follows:

TCSR=0X001000B

- Timer initialization before start ⇒ STCR=0
- Compare-clear interrupt ⇒Disable (TCIE=0)
- Zero detection interrupt ⇒Disable (TZIE=0)
- Timer interrupt ⇒Disable (TMIE=0)

CICR=11110000B

- Compare match interrupt ⇒Enable (CIE0 to CIE3=1)

COER=XXXX1111B

- Compare output/port switching ⇒Use all ports as compare output pins (RTO0 to RTO3=1)

TMCR=00XX0001B

- Timer count mode ⇒Increment count mode
- External trigger ⇒Not used (CES1, CES0=00)
- Timer count clock pulse ⇒2 instruction cycles, (TCS1, TCS0=01)
  [1.9 µs at f=4.2 MHz, 1.0 µs at f=8 MHz]

CMCR=XXXXX100B

- Buffer register transfer mode (compare 0 to 3)=> Transfer at compare match (BFS1, 0=00)

DTCR=00000000B

- Dead-time timer ⇒ Disable

OCTBR

- Compare output operation ⇒ Set according to desired output waveform

OCPBR

- Compare value ⇒ Set according to desired output waveform

ZOCTR=XXX00000B

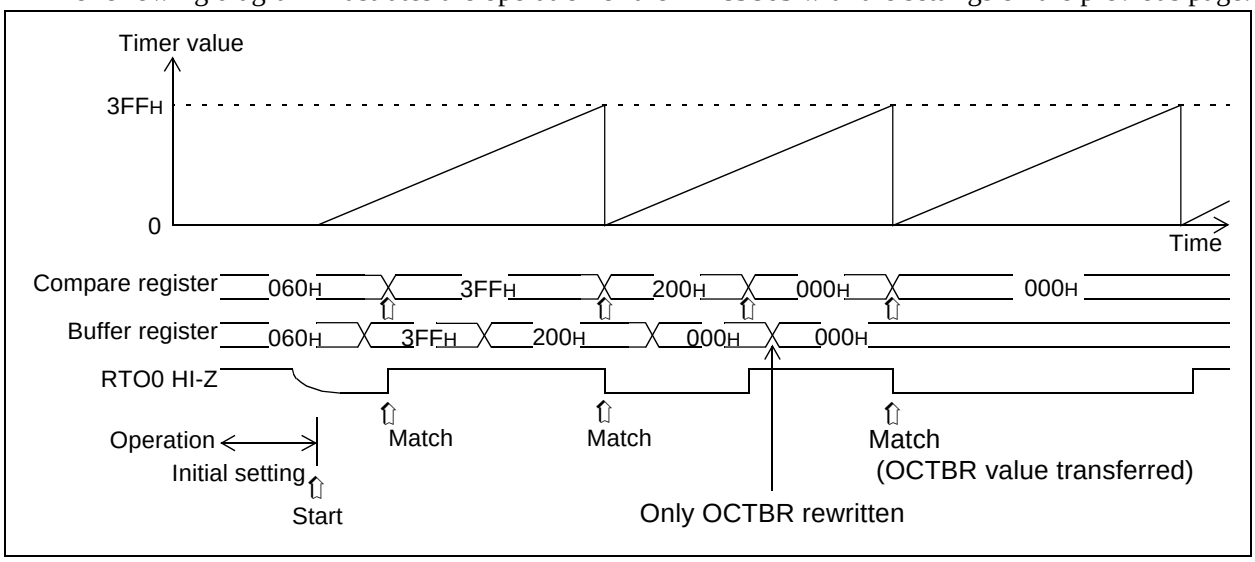
- Zero detection pin control ⇒ No pin control

CLRR=000H

- Compare-clear value ⇒ Disable compare-clear operation

After making all the above settings, set the timer start bit TMST to '1,'
and specify external pin output (DDR41 to DDR43=1).

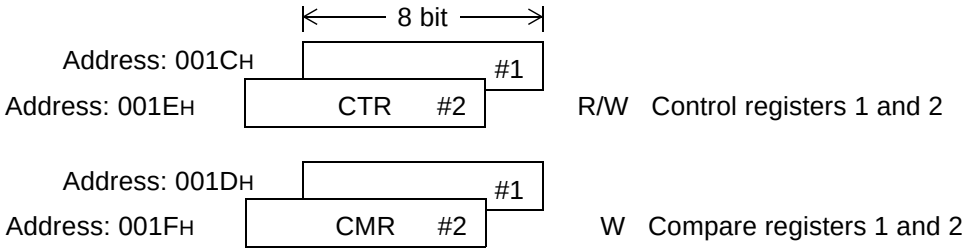
The following diagram illustrates the operation of the MB89863 with the settings on the previous page.



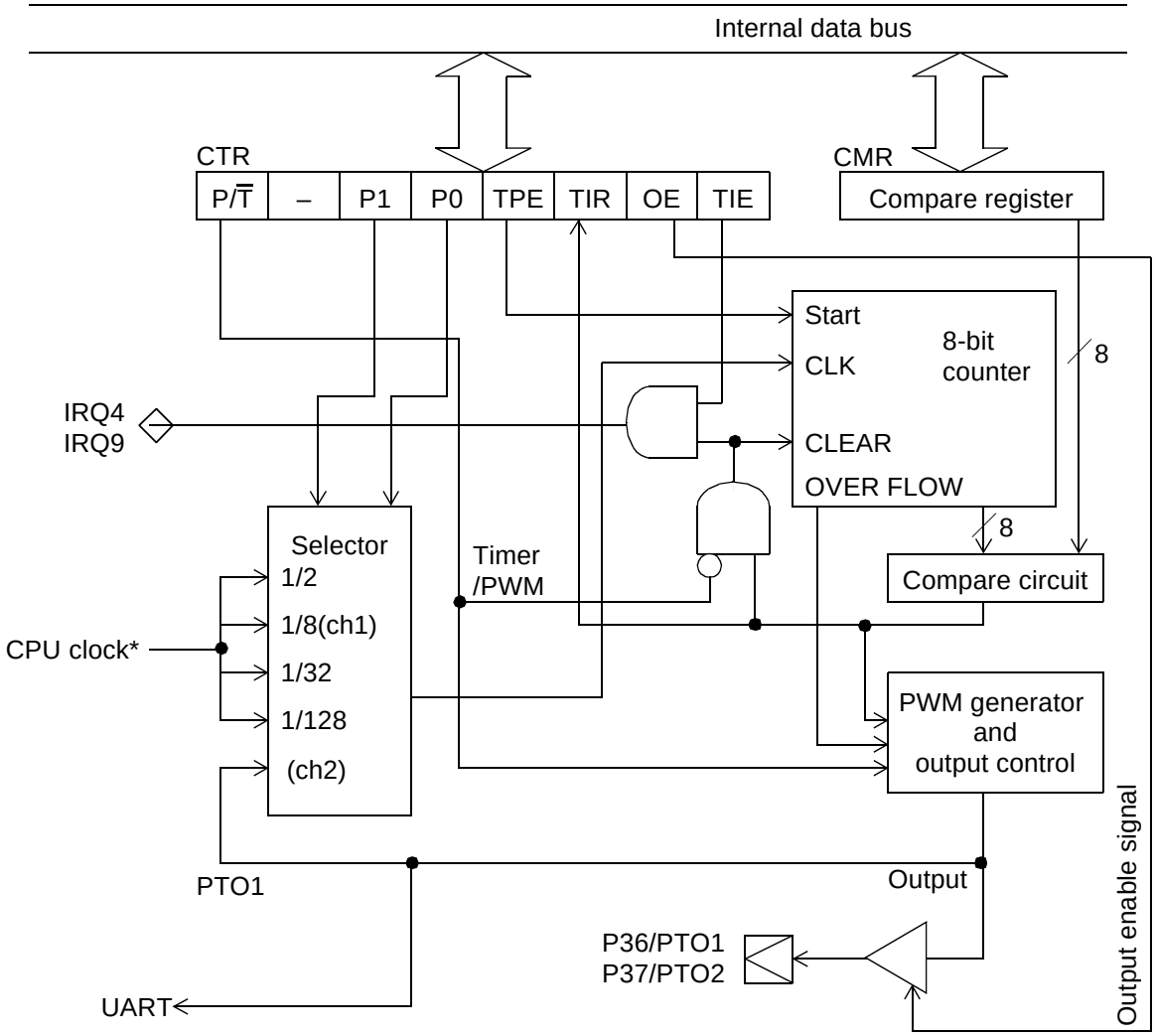
2.2.3 8-Bit PWM Timers 1 and 2

- Can be used either as 8-bit timers or 8-bit PWM control circuits with 8-bit resolution.
- Selection of 4 types of clock pulse
- Toggle output from Timer 1 can be used as count clock for Timer 2

(1) Registers



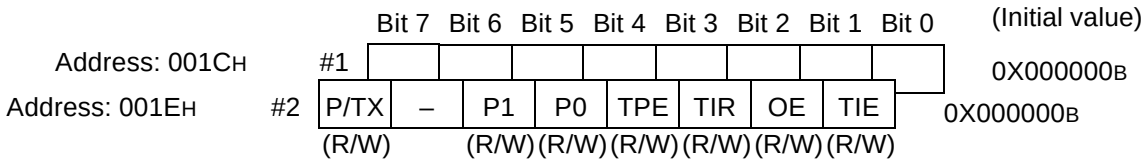
(2) Block diagram



*: The CPU clock operates on the oscillation frequency divided by 2. After a reset is canceled, the clock enters free-run operation.

(3) Register Descriptions

(3.1) CTR (Control Register)



[Bit 7] P/TX: Timer/PWM operation mode switching bit

The unit operates as a timer when this bit is '0' and as a PWM control circuit when this bit is set to '1.'

0	Timer
1	PWM control circuit

Switching between timer and PWM operating modes should be performed when the count is stopped (TPE=0) the interrupt is disabled, and the interrupt request flag is cleared (TIR=0).

[Bits 5,4] P1, P0: Clock select bits

Bits P1 and P0 determine whether the clock pulse is taken from the prescaler or the TPO1 signal output from PWM timer 1.

P1	P0	PWM timer 1 clock cycle
0	0	Internal clock, 1 instruction cycles
0	1	Internal clock, 4 instruction cycles
1	0	Internal clock, 16 instruction cycles
1	1	Internal clock, 64 instruction cycles

P1	P0	PWM timer 2 clock cycle
0	0	Internal clock, 1 instruction cycles
0	1	Internal clock, 16 instruction cycles
1	0	Internal clock, 64 instruction cycles
1	1	PTO1 signal output from PWM timer 1

Note that these bits must not be rewritten when the counter is operating (TPE=1). To select the PTO1 signal from timer 2, timer 1 must be set for timer operation.

[Bit 3] TPE: Counter operation enable bit

When this bit is set to '1,' the timer or PWM control circuit starts operation.

0	Counter operation stop
1	Counter operation start

[Bit 2] TIR: Interrupt request flag bit

When an interrupt source has occurred, this bit is set to '1.' To clear the interrupt source, writ e'0' to this bit. This bit has the following read values:

0	Values of counter and CMR do not match
1	Values of counter and CMR match

For read-modify-write instructions, the read value of this bit is always '1.'

This bit has the following write values:

0	Bit cleared
1	Writing '1' causes no change, no effect on other functions

Note: In PWM mode, there is no significance to either the read or write values of this bit.

[Bit 1] OE: Output signal control bit

When this bit is '1,' the port signals serve as timer or PWM output signals. In timer mode, the signal is inverted each time the counter and compare register values match. In PWM mode, the PWM signal is output.

0	General-purpose ports (P36, P37)
1	Counter/PWM output pins (PTO0, PTO1)

If this bit is set to '1,' the port functions as the counter/PWM output pin even if the DDR register of ports P36 and P37 is set for input (bits 6, 7 of DDR3=0).

[Bit 0] TIE: Interrupt enable bit (timer mode)

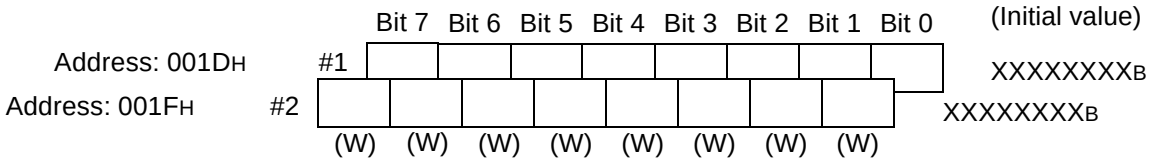
This bit is set to '1' to enable an interrupt request when the values of the counter and compare register match.

0	Counter interrupt output disabled
1	Counter interrupt output enabled

However, no interrupt will be generated in PWM mode regardless of the value of this bit.

(3.2) CMR (Compare Register)

This register is used to set the value for comparison with the timer. When the counter value matches the value of this register, the timer counter is cleared. In PWM mode, this register can be used to specify the value of the 'H' pulse width.



(4) Description of operation

(4.1) Timer operation

The P/TX bit (bit 7) of the CTR register is set to '0' to specify timer mode. The counter begins to count up from 00H when the TPE bit is set to '1.' When the value of the counter matches the value set in the CMR register, the counter is cleared on the next count clock pulse, and begins counting up again. Thus if the value '00H' is set up in the compare (CMR) register, the TIR bit is set and the output pin signal is inverted at every cycle of the count clock. And if the compare register is set to 'FFH,' the TIR bit is set and the output pin signal is inverted at every 256 cycles of the count clock. (As long as the TPE bit is set to '0,' the output pin signal remains fixed at 'L' level.)

If the value of the compare register is rewritten while operating in timer mode, the new value becomes effective from the next cycle. (If the value of the counter is 00H, the value of the CMR register will be transferred to the comparator circuit latch.)

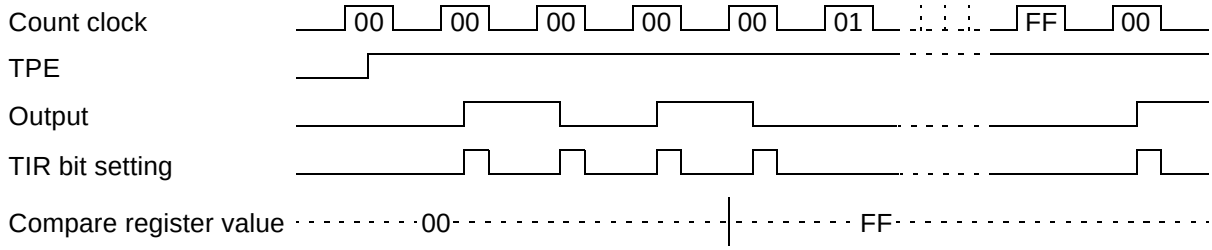


Fig. 2.2.8 Timer Operation

When the TIE bit in the CTR register is set to '1,' an interrupt is generated each time the values of the counter and CMR register agree. During interrupt processing the TIR bit is used as the interrupt flag. The TIR bit value has no effect on the value of the TIE bit, however, the TIR bit is reset to '1' each time a match occurs, even when the interrupt signal itself is disabled.

To clear an interrupt source or the TIR bit itself, write '0' to the TIR bit. Also, the TIR is designed to have a read value of '1' to prevent erroneous clearing by read-modify-write instructions.

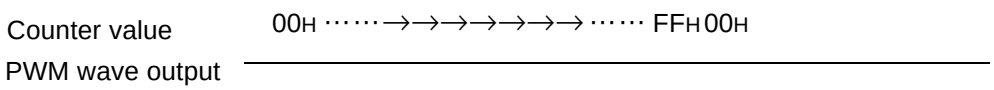
The CTR register clock select bits P0 and P1 are used to select any one of four available count clock pulses from the prescaler (three prescaler signal types from PWM timer ch2, and one output signal from PWM timer ch1).

(4.2) PWM Operation

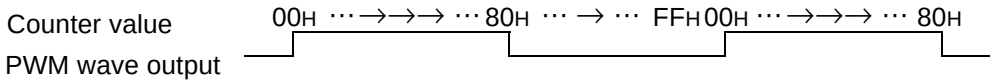
PWM mode is selected by setting the P/TX bit in the CTR register to '1.' The CMR register specifies the duty ratio of the output pulse, which can be output with 1/256 resolution and a duty ratio range of 0 to 99.6%. Write zero (00H) to the CMR register for a PWM output with duty ratio of 0%, write 128 (80H) for 50%, and 225 (FFH) for 99.6%.

Whenever the value of the counter is 00H, the value of the CMR register is transferred to the comparator latch. If the value of the compare register is rewritten while operating in PWM mode, the new value becomes effective from the next cycle.

- Compare register = 00H



- Compare register = 80H



- Compare register = FFH

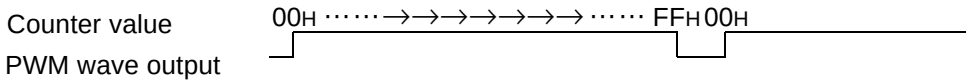


Fig. 2.2.9 PWM Waveforms Output

In PWM operation, there is no significance to the TIR bit in the CTR register. No interrupt will occur even when the TIE bit is set to '1.'

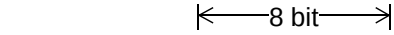
The PWM pulse cycle and frequency can be changed by switching the count clock signal. The count clock can be selected from four types of prescaler signals, using the clock pulse select bits P0 and P1 in the CTR register. (There are three prescaler signal types from PWM timer ch2, and one output signal from PWM timer ch1.)

2.2.4 UART

Outline

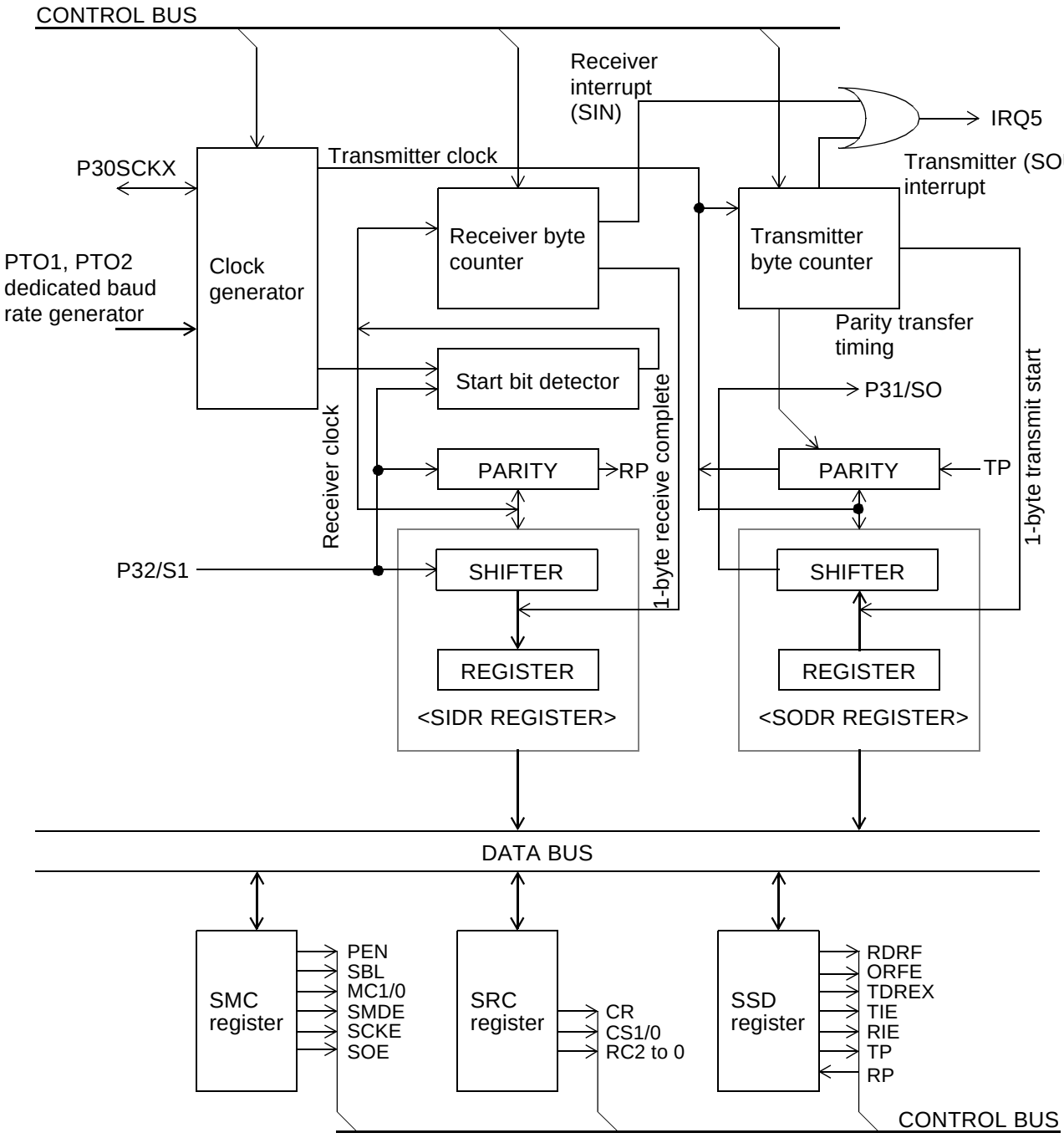
- Full-duplex double buffer
- CLK-synchronous and -asynchronous data transfer capability
- 14 baud rates (using internal clock). Additional baud rates may be set freely by using an external clock or input from the internal timer.
- Variable data length
- NRZ transfer format

(1) Registers



Address: 0020H	SMC	R/W	Serial mode control register
Address: 0021H	SRC	R/W	Serial rate control register
Address: 0022H	SSD	R/W	Serial status and data register
Address: 0023H	SIDR	R	Serial input data register
Address: 0023H	SODR	W	Serial output data register

(2) Block Diagram



(3) Description of registers

(3.1) SMC (Serial Mode Control Register)

This register is used to select UART operating modes.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0020H	PEN	SBL	MC1	MC0	SMDE	–	SCKE	SOE	00000-00B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)		(R/W)	(R/W)	

[Bit 7] PEN (Parity Enable):

This bit is used to determine whether to append a parity bit (when transmitting) or detect it (when receiving) for serial data input/output operation.

0	No parity (Default)
1	Parity (odd or even parity selection is controlled by TD8/TP bits in the SSD register)

[Bit 6] SBL (Stop Bit Length):

This bit is used to determine the stop bit length for outgoing data. At the receiving end, only the first bit of the stop bit is recognized. Second and subsequent bits are ignored (default: 0)

0	2-bit length (Default)
1	1-bit length

[Bits 5,4] MC1, MC0 (Mode Control):

These bits are used to select the transfer mode (data length).

MC1	MC0	Mode	Data length
0	0	0	7(6)
0	1	1	8(7)
1	0	2	8+1
1	1	3	9(8)

(Default)

Values in parentheses ( ) indicate data length with parity bit

Note: The receive interrupt in mode 2 differs from that in other modes. In mode 2, a UART receive interrupt request is sent to the CPU when the RIE bit is '1,' the RDRF bit or ORFE bit is '1,' and the SI pin is also '1.' (See the description of operation.)
This mode is used when more than one slave CPUs are connected to one host CPU.

[Bit 3] SMDE:

0	Synchronous transfer (default)
1	Asynchronous transfer

[Bit 1] SCKE (SCLK enable bit):

When '1' is written to this bit, a port pin is switched to the UART serial clock output pin to output a synchronous clock pulse to the outside.

If the CS1 and CS0 bits in the SRC register are used to select synchronous clock pulse input from outside the MB89863, that clock signal can also be read using this port as the input pin.

0	Port functions as general-purpose input/output port, no serial clock pulse output. When the port is set to input mode (DDR=0), it also functions as a serial clock input pin. (default)
1	Port functions as UART serial clock input/output pin.

When using the MB89863 in external clock input mode, set this bit to '0.'

[Bit 0] SOE (Serial output enable)

When '1' is written to this bit, the port switches to UART serial data output pin, in order to enable serial data output.

0	Port pin functions; no serial data output (default)
1	UART serial data output pin (SO) functions

(3.2) SRC (Serial Rate Control Register)

This register is used to control the data transfer speed (baud rate) of the UART.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0021H	-	-	CR	CS1	CS0	RC2	RC1	RC0	--011000B
			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

[Bit 5] CR (Clock rate)

This bit selects the asynchronous transfer clock rate. However if the CS1 and CS0 bits are set to '11B,' a clock rate of 1/8 is selected regardless of the value of this bit.

0	1/16 of clock input	(Default)
1	1/64 of clock input	

Note: Regardless of the value of the CR bit, the synchronous transfer clock rate is as follows:

Clock source: — Internal clock 1/2 ..... 1/2
└ External clock, dedicated baud rate generator 1/1

[Bits 4,3] CS1, CS0 (Clock select):

These bits are used to select the clock signal input for the UART port. If the clock input is either an external or internal clock signal the baud rate is either a 1/16 or 1/64 clock frequency according to the value of the CR bit (default: 11B). For details, see section (4.4) 'Transfer Clock' in the following 'Description of Operation.'

[Bits 2 to 0] RC2, RC1, RC0:

Bits 2 to 0 are needed only when generating a serial clock pulse using the dedicated baud rate generator. These bits can be used in combination to select fourteen baud rates (default: 000B).

For baud rate settings, see section (4.4) 'Transfer Clock' in the following 'Description of Operation.'

(3.3) SSD (Serial Status and Data Register)

This register is used to indicate the current status of the UART port. The most significant data bit (bit 8) is included when the data communication length is 9 bits.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0022H	RDRF	ORFE	TDRE	TIE	RIE	–	TD8/TP	RD8/RP	00100-1XB
	(R)	(R)	(R/W)	(R/W)	(R/W)		(R/W)	(R)	

[Bit 7] RDRF:

This bit is a flag indicating the data status of the SIDR (serial input data) register.

0	Vacant (default)
1	Data present

Reading SSD in a state of RDRF=1, and then SIDR (serial data input register) clears RDRF. RDRF, if reset to 1, causes receive interrupt request.

[Bit 6] ORFE:

This bit is a flag indicating that an overrun or framing error has occurred. This bit is initialized to '0' at reset.

0	Normal
1	Error

If this bit is set, data will not be transferred from the receive shift register to the SIDR register.

Once the SIDR register is read following reading of the SSD register with the ORFE flag set to '1,' the ORFE flag will be cleared. A receive interrupt request can also be output when this flag is set.

The RDRF and ORFE flags indicate the status of input data, as follows:

RDRF	ORFE	SIDR data status
0	0	Vacant
0	1	Framing error (RDRF will not be set if new data is input in this state.)
1	0	Normal data
1	1	Overrun (previous data remains)

[Bit 5] TDRE:

This bit is a flag used to indicate the status of the serial output data register (SODR).

0	Data present
1	Vacant (Default)

When data is written to the SODR register, after reading the SSD register with this flag set to '1,' serial data is output from the SO pin.

A transmitter interrupt request is output when the TDRE flag is set to '1.'

[Bit 4] TIE: Transmitter interrupt request enable bit

This bit is used to enable the transmitter interrupt request.

0	Interrupt disabled (Default)
1	Interrupt enabled

[Bit 3] RIE: Receiver interrupt request enable bit

This bit is used to enable the receiver interrupt request.

0	Interrupt disabled (Default)
1	Interrupt enabled

[Bit 1] TD8/TP:

When no parity bit is used, bit 1 is treated as bit 8 of the SODR (serial output data) register. When a parity bit is present, this bit is used to determine whether the parity of serial output data is even or odd.

0	Odd parity (Default)
1	Even parity

[Bit 0] RD8/RP:

When no parity bit is used, bit 0 is treated as bit 8 of the SIDR (serial input data) register. When a parity bit is present, this bit is used to determine whether the parity of serial output data is even or odd. (Default: undefined)

0	Odd parity
1	Even parity

(3.4) SIDR (Serial Input Date Register)

SODR (Serial Output Data Register)

SIDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0023H								
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)

The SIDR (Serial Input Date Register) is used for serial data input (default: undefined).

SODR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0023H								
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

The SODR (Serial Output Data Register) is used for serial data output (default: undefined).

(4) Description of operation

(4.1) Operating modes

The UART provides the modes listed in Table 1. Mode selections can be switched through the serial mode control register (SMC).

Table 1 UART Operating Modes

Mode	Parity	Data length	Clock mode	Stop bit length
0	Provided	6	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	7	Asynchronous/synchronous	1 bit or 2 bits
1	Provided	7	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	8	Asynchronous/synchronous	1 bit or 2 bits
2	Not provided	8+1	Asynchronous/synchronous	1 bit or 2 bits
3	Provided	8	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	9	Asynchronous/synchronous	1 bit or 2 bits

Note that stop bit length can be specified only for the transmitter channel. The receiver channel is always 1-bit length.

(4.2) Interrupt generation and flag setting conditions

The UART has three flags and two interrupt sources.

The three flags are the ORFE, RDRF and TDRE flags. The ORFE flag is an overrun/framing error flag, and is set when an error occurs during reception. The RDRF flag indicates that receiving data is present in the SIDR register. The TDRE flag indicates that writing is enabled to the transmit data register (SODR).

For two interrupt sources, one is for receiving, and the other for transmitting. Receiving interrupts are requested by the RDRF or ORFE flag. Sending interrupts are requested by the TDRE flag.

The conditions and timing for setting each flag vary according to the operating mode. Conditions and timing for interrupt requests also vary. The interrupt flag set timing in each mode is described below.

(4.2.1) Receiving in Modes 0, 1 and 3

Both the RDRF (receive data register full) and ORFE (overrun/framing error) flags are set when receiving and transfer are completed and the last stop bit is detected. An interrupt request is then output to the CPU. When the RDRF flag is active, the received data is transferred to the SIDR (serial data input) register.

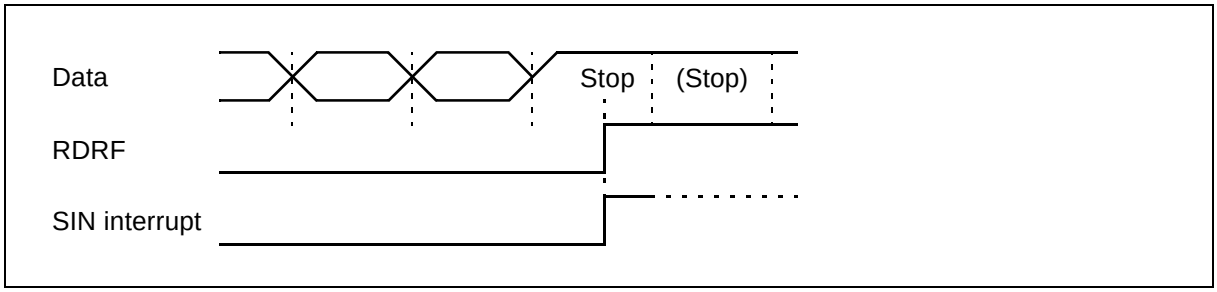


Fig. 1 RDRF Flag Set Timing

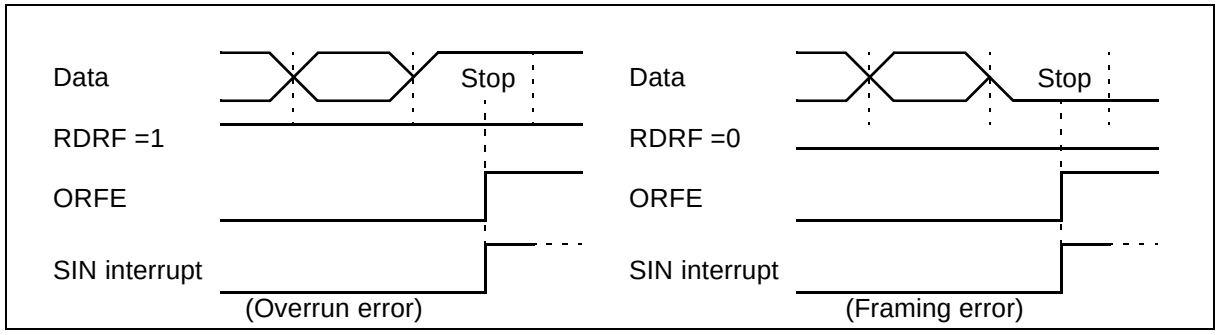


Fig. 2 ORFE Flag Set Timing

(4.2.2) Receiving in Mode 2

Both the RDRF (receive data register full) and ORFE (overrun/framing error) flags are set when receiving and transfer are completed with the last data bit (D8) set to '1' and the last stop bit is detected. However, when a framing error occurs, the flags are set regardless of the value of the last data bit. An interrupt request is sent to the CPU after the flags are set and input data goes to '1.'

(See description of mode 2 uses (7).)

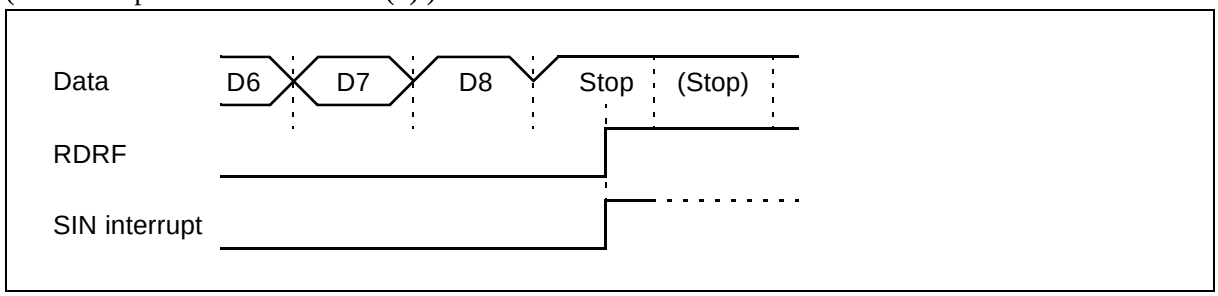


Fig. 3 RDRF Flag Set Timing

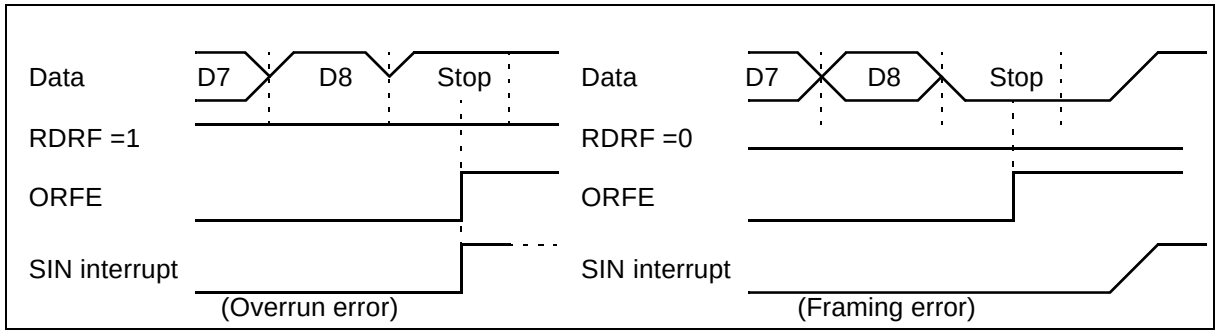


Fig. 4 ORFE Flag Set Timing

(4.2.3) Transmission

Each time data written to the serial output data register (SODR) has been transferred to the interrupt shift register, and the next data is ready to write, the TDRE (transmit data register empty) flag is set as active and an interrupt request is output to the CPU.

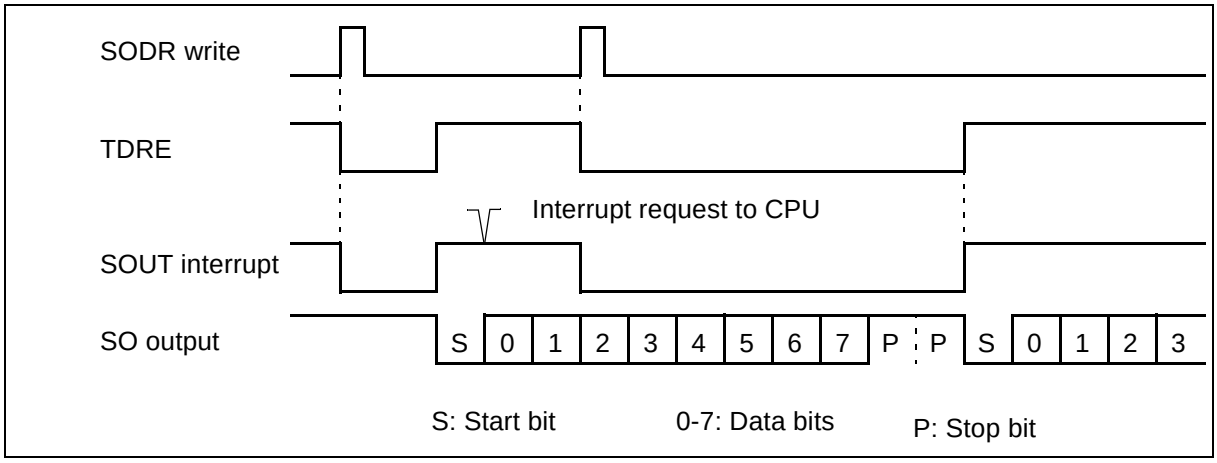


Fig. 5 TDRE Flag Set Timing (Mode 0)

(4.3) Transfer data format

The UART can handle only data in NRZ (non-return to zero) format. The relation between transmitter/ receiver clocks and data is shown in Figure 6.

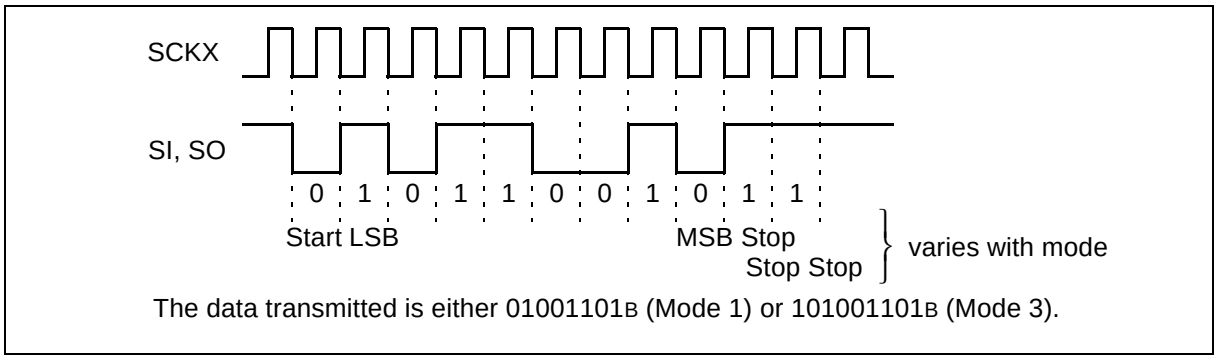


Fig. 6 Transfer Data Format

As shown in Figure 6, data transfer always starts with a start bit ('L' level data), followed by transfer of the data bit-length specified by the LSB first format, and then ends at the stop bit ('H' level data).

Note that in asynchronous transfer, the relation between the SCKX and SI signals is not as shown above. Note also that the relation shown above does not apply even when the SCLK pin is set for input.

(4.4) Transfer clock selection

The transfer clock may be selected from the external clock signal (SCKX pin), two internal clocks (PTO1 and PTO2), or the dedicated baud rate generator. The selection is made using the CS0, SC1 and CR bits of the SRC (serial rate control) register. The divide ratios are listed in Table 2.

Table 2 Clock Divide Ratio

CS1	CS0	Clock input source	CR	Asynchronous	Synchronous
0	0	External clock	0	1/16	1/1
			1	1/64	
0	1	PWM timer 1	0	1/16	1/2
			1	1/64	
1	0	PWM timer 2	0	1/16	1/2
			1	1/64	
1	1	Dedicated baud rate generator	–	1/8	1/1

Tables 3-1 and 3-2 list transfer clock signals used with the dedicated baud rate generator.

Table 3-1 Baud Rate Selection (at 4.2 MHz Oscillation)

RC2	RC1	RC0	CLK-asynchronous (µs/baud)	CLK-synchronous (µs/baud)
0	0	0	247/4048	2.375/421K
0	0	1	494/2024	4.75/210K
0	1	0	988/1012	9.50/105K
0	1	1	1976/506	19.00/52.6K
1	0	0	3952/253	38.00/26.3K
1	0	1	7904/126	76.00/13.1K
1	1	0	38/26315	4.75/210K
1	1	1	304/3289	38.00/26.3K

Table 3-2 Baud Rate Selection (at 8 MHz Oscillation)

RC2	RC1	RC0	CLK-asynchronous (µs/baud)	CLK-synchronous (µs/baud)
0	0	0	130/7692	12.5/800K
0	0	1	360/2777	2.50/400K
0	1	0	720/1389	5.00/200K
0	1	1	1440/694	10.00/100K
1	0	0	2880/347	20.00/50.0K
1	0	1	5760/173	40.00/25.0K
1	1	0	20/50000	2.50/400K
1	1	1	160/6250	20.00/50.0K

The following formula can be used to determine baud rate when using the PWM timer output signals.

Baud rate = f / A × 2 ×(n + 1) × k × 4 [bps]

f: frequency used

A: For asynchronous transfer, use the figure '16' for CR=0, '64' for CR=1. For synchronous transfer, use the figure '2.'

n: CMR (compare register) setting, in decimal notation

k: PWM timer clock frequency (in instruction cycles)

Table 4 Sample Baud Rate Settings with PWM Timer

PWM timer clock cycle	1 instruction cycle (k=1)	
CR value	0 (asynchronous mode) (A=16)	
Frequency used	4 MHz ($f = 4 \times 10^6$)	8 MHz ($f = 8 \times 10^6$)
Baud rate (figures in ( ) are CMR register values)	2403.8 (n = 12)	2403.8 (n = 25)
	1201.9 (n = 25)	1201.9 (n = 51)
	600.9 (n = 51)	600.9 (n = 103)

(4.5) Sample use of Mode 2

In mode 2, the receive interrupt operates differently than in other modes. The UART receiver interrupt request is output to the CPU when the RIE bit is '1,', the RDRF or ORFE bit is '1' and the SI pin value is '1.'

This mode is used when more than one slave CPUs are connected to one host CPU (see Figure 7).

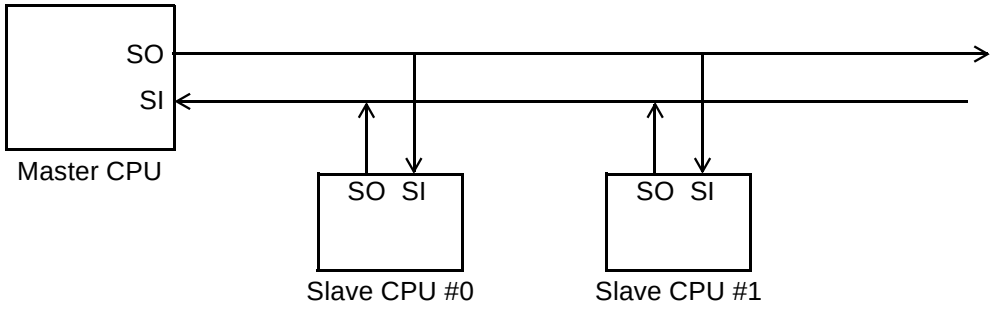


Figure 7 System Configuration Example in Mode 2

Communication begins with the transfer of address data from the CPU. Address data is data in which bit 9 (=D8) is set to '1,' selecting the slave CPU as the destination of the communication. Once a slave CPU is selected, communication with the master CPU is performed according to user-defined rules. Normally data with D8 set to '0' is used. The non-selected slave CPU(s) wait until the next communication is started. Figure 8 shows a flow chart of this process.

In mode 2, the parity check function cannot be used, and therefore the PEN bit should be set to '0.'

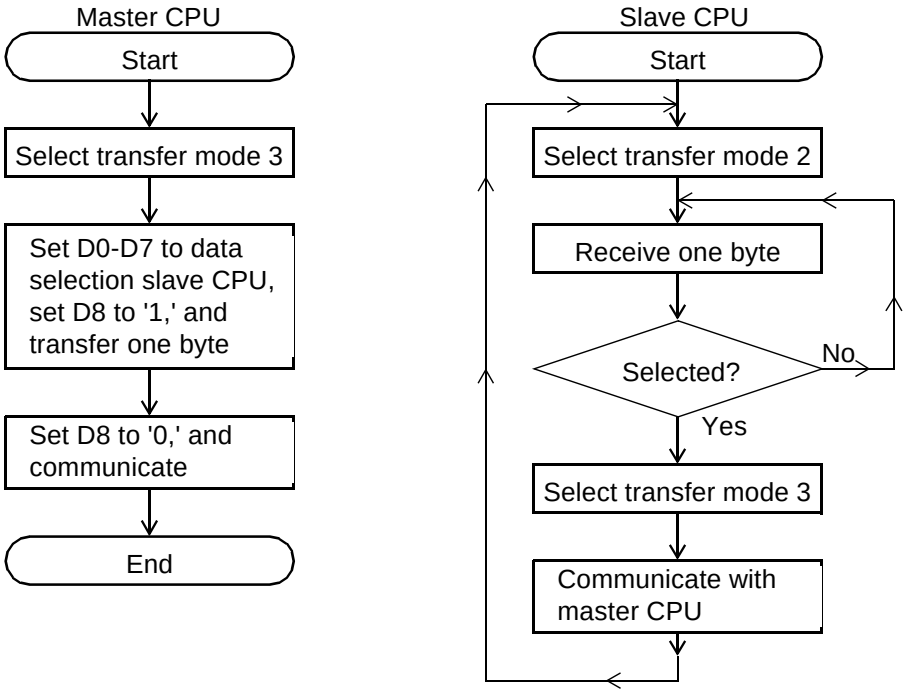


Figure 8 Communication Flowchart Using Mode 2

After the slave CPU completes communication with the master CPU, the timing for disabling SO output can be determined by the following three methods:

(1) Write the last data to the SODR register, wait for 11 shift clock cycles after the TDRE flag is set, and then disable SO output.

(2) Disable SO output after receiving the last data from the master CPU.

(3) Use wired-OR configuration for the signal line connected to the SO output of the slave CPU. In this case there is no need to disable SO output.

Note: If a register initialization has been canceled by a reset, 11 shift clock cycles are required to initialize the internal control section.

2.2.5 A/D Converter

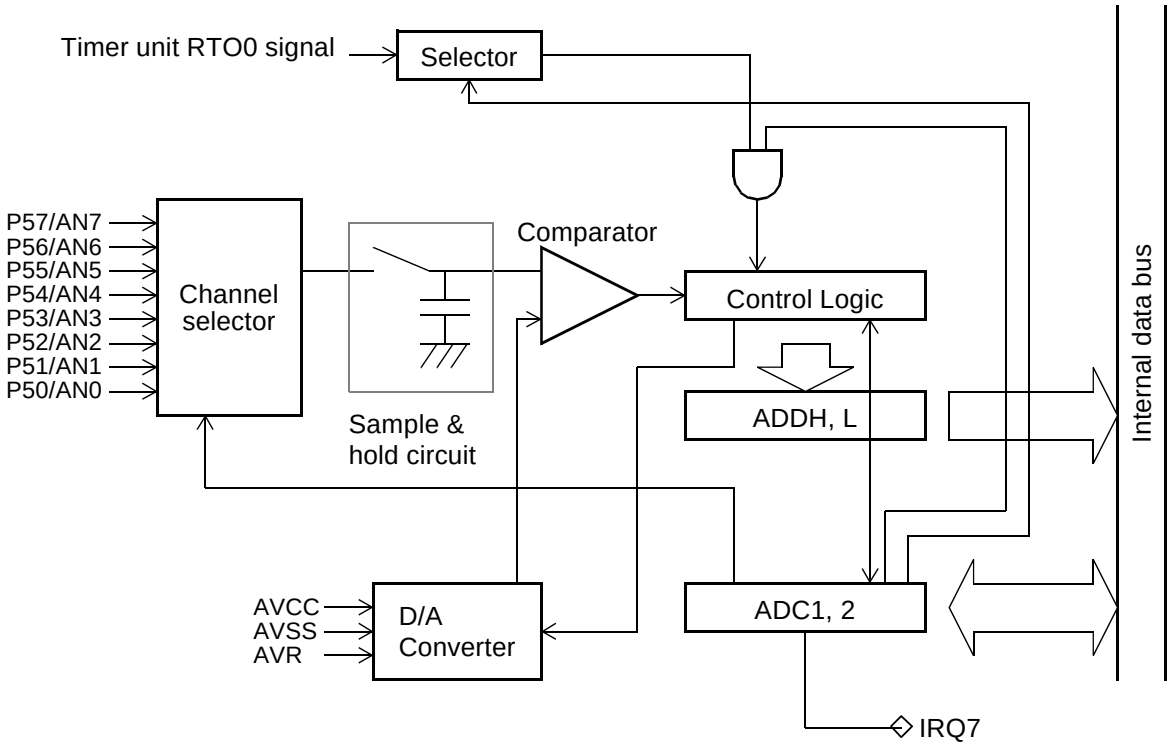
Outline

- Conversion time: 33 instruction cycles
- 10-bit resolution
- RC-type successive approximation conversion method with sample & hold circuit.
- 8-channel analog input selection by program
- Conversion end detected by interrupt or software polling
- Start by software, or timer unit.

(1) Register list

	8 bit		
Address: 0028H	ADC1	R/W	ADC control status register 1
Address: 0029H	ADC2	R/W	ADC control status register 2
Address: 002AH	ADDH	R	ADC data register (H)
Address: 002BH	ADDL	R	ADC data register (L)

(2) Block diagram



(3) Description of registers

(3.1) ADC1 (A/D Converter Control Status Register 1)

This register is used to control the A/D converter and display its status.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0028H	–	ANS2	ANS1	ANS0	ADIE	ADI	ADMV	AD	-0000000B
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R)	(R/W)	

[Bits 6 to 4] ANS2 to ANS0: Analog input channel select bits

These three bits are used to select the analog input channel.

ANS2	ANS1	ANS0	Channel to be selected	ANS2	ANS1	ANS0	Channel to be selected
0	0	0	AN0	1	0	0	AN4
0	0	1	AN1	1	0	1	AN5
0	1	0	AN2	1	1	0	AN6
0	1	1	AN3	1	1	1	AN7

[Bit 3] ADIE: A/D conversion end interrupt enable bit

This bit is used to enable an interrupt at the completion of A/D conversion.

0	A/D conversion end interrupt disabled
1	A/D conversion end interrupt enabled

[Bit 2] ADI: A/D conversion end flag bit

This bit is a flag used to indicate that A/D conversion is ended.

0	A/D conversion not ended
1	A/D conversion ended

Write '0' to clear this bit.

Writing '1' to this bit is ignored and the value of this bit is unchanged.

Note that when this bit is set with the ADIE bit (bit 3) set to '1,' an interrupt request is output.

For read-modify-write instructions, the read value of this bit is always '1.'

[Bit 1] ADMV: A/D conversion on flag bit

This bit is used to indicate that A/D conversion is in progress.

0	A/D conversion not in progress
1	A/D conversion in progress

[Bit 0] AD: A/D conversion start bit

When the ESL1 and ESL0 bits (bit 1, 0) of the ADC2 register are set to '00B,' writing '1' to this bit starts A/D conversion. Writing '0' to this bit has no meaning. The read value is always '0.'

The write values of this bit have the following significance.

0	No change
1	Start A/D conversion

(3.2) ADC2 (A/C Converter Control Status Register 2)

This register is used to control the A/D converter.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0029H	TST1	TST0	–	–	–	SELT	ESL1	ESL0	11---000B
	(R/W)	(R/W)				(R/W)	(R/W)	(R/W)	

[bits 7,6] TST1, TST0: Test bits

These two bits are used only for testing. The write value should always be '1.' The read value is always '1.'

[Bit 2] SELT: A/D conversion start trigger signal select bit

This bit is used to select the trigger signal for starting A/D conversion other than by software. (The ESL1 and ESL0 bits must be other than '00B.')

With the MB89863 series of microcontrollers, this bit should always be set to '0.'

0	Start by RTO0 signal of timer unit
1	Setting prohibited

[Bits 1,0] ESL1, ESL0: A/D conversion start source (trigger signal start edge) select bits

These two bits are used to select the trigger signal edge used as the start source for A/D conversion.

Used together, the ESL1 and ESL0 bits have the following value.

ESL1	ESL0	Start conditions
0	0	Software start (using AD (bit 0) in the ADC1 register)
0	1	Start at falling edge of A/D conversion start trigger signal
1	0	Start at rising edge of A/D conversion start trigger signal
1	1	Start at either edge of A/D conversion start trigger signal

(3.3) ADDH, ADDL (A/D Converter Data Registers H and L)

There registers are used to store the results of digital conversion.

The upper 2 bits of the conversion results are stored in the ADDH register, and the lower 8 bits in the ADDL register.

ADDH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 002AH	–	–	–	–	–	–	9	8	000000XXB
							(R)	(R)	

ADDL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 002BH	7	6	5	4	3	2	1	0	XXXXXXXXB
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

The values of these registers are updated at the end of each A/D conversion cycle. Therefore after A/D conversion is ended and these registers have been read, write '0' to the ADI bit (bit 2) of the ADC1 register to clear the A/D conversion end flag before the end of the next A/D conversion.

(4) Description of operation

(4.1) Starting by software

(a) Start

Start conversion by writing '00B' to the ESL1 and ESL0 bits (bits 1, 0 of the ADC2 register) and writing '1' to the AD bit (bit 0) of the ADC1 register.

(b) Restart

A/D conversion can be restarted at any time, even during operation.

(c) End

Once started, A/D conversion is terminated after 33 instruction cycles (31.43 µs at f=4.2 MHz or 16.5 µs at f=8 MHz) unless a restart is made. When A/D conversion is terminated, the ADI bit (bit 2) of the ADC1 register is set. At this time, if the ADIE bit (bit 3) of the ADC1 register is '1' (interrupt enabled), an interrupt request is output.

(4.2) Start by timer unit

(a) Start

Use the ESL1 and ESL0 bits (bits 1, 0 of the ADC2 register) to select the trigger signal edge, and A/D conversion will start when the corresponding trigger signal edge is input.

(b) Restart

A/D conversion can be restarted at any time by input of the starting source (trigger edge), even during operation.

(c) End

Once started, A/D conversion is terminated after 33 instruction cycles (31.43 µs at f=4.2 MHz or 16.5 µs at f=8 MHz) unless a restart is made. When A/D conversion is terminated, the ADI bit (bit 2) of the ADC1 register is set. At this time, if the ADIE bit (bit 3) of the ADC1 register is '1' (interrupt enabled), an interrupt request is output.

(5) Precautions for use

(a) The contents of the ADDH and ADDL registers are rewritten immediately after A/D conversion is ended. After conversion has ended, the contents of the ADDH and ADDL registers will be held until the end of the next A/D conversion.

(b) If the ESL1 and ESL0 bits (bits 1, 0 of the ADC2 register) are set to any value other than '00B' (start by timer unit), A/D conversion cannot be started by the AD bit (bit 0) of the ADC 1 register.

(c) When a reset is applied, A/D conversion stops and all registers are initialized.

(d) When stop mode is applied, A/D conversion stops and the ADMV flag (bit 1) of the ADC1 register is initialized.

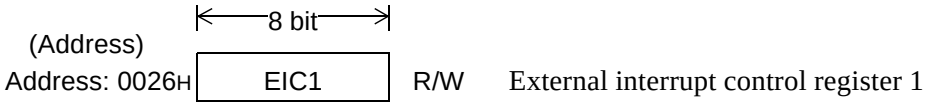
(e) Start and analog channel selection may be made simultaneously. In other words, when '1' is written to the AD bit (bit 0) of the ADC1 register, the ANS2 to ANS0 bit (bits 6 to 4) selection can be made at the same time. However, if the timer unit is designated as the start source, it is necessary to stop A/D conversion to make these settings.

(f) Do not switch A/D channels during conversion. If the timer unit is designated as the start source, first set the start source for a software start (setting the ESL1 and ESL0 bits in the ADC2 register to '00B') and then set the ADMV bit (bit 1) of the ADC1 register to '0' before changing the channel selection.

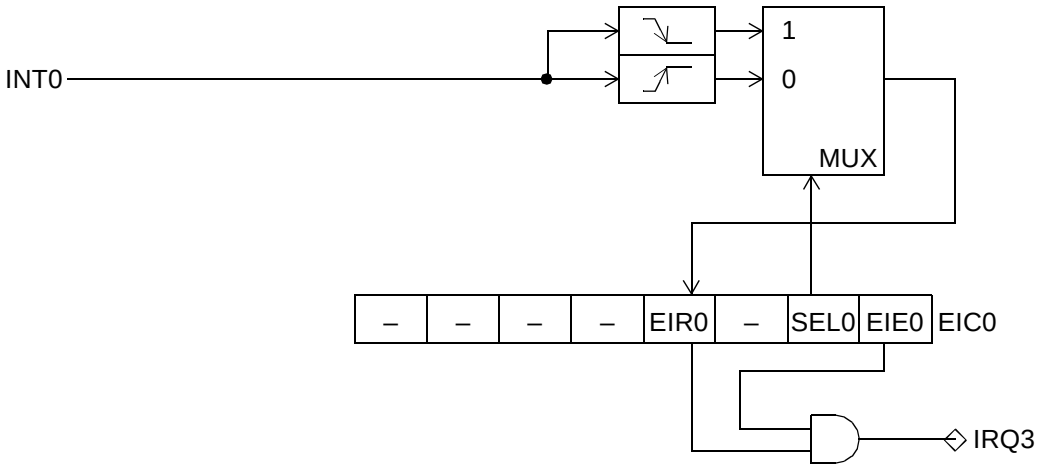
2.2.6 External Interrupt Circuit

- The edge of the external interrupt source signal INT0 can be detected to set the corresponding interrupt flag.
- A source can both set a flag and generate an interrupt.
- The interrupt function can be used to escape from stop mode or sleep mode.

(1) Register list



(2) Block diagram



(3) Description of registers

(3.1) EIC1 (External interrupt control register 1)

This register controls interrupts by the INT0 pin.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Initial value
Address: 0026H	–	–	–	–	EIR0	–	SEL0	EIE0	XXXX0X00B
					(R/W)		(R/W)	(R/W)	

[Bit 3] EIR0: External interrupt request flag

Then the edge specified by the SEL0 bit is detected at the INT0 pin, this bit is set to '1.' If the EIE1 bit is '1' (interrupt enabled), an interrupt request (IRQ3) is output. The read value is as follows:

0	Specified edge not detected at INT0 pin
1	Specified edge detected at INT0 pin (IRQ3 generated).

For read-modify-write instructions, the read value of this bit is always '1.'

The write value is as follows:

0	This bit is cleared
1	No change to this bit, no effect on other bits

[Bit 1] SEL1: Edge-polarity select bit

This bit is used to control the edge polarity of the INT0 pin.

0	Rising edge
1	Falling edge

[Bit 0] EIE0: Interrupt enable bit

This bit is used to enable an interrupt request from the INT0 pin.

0	Interrupt request disabled
1	Interrupt request enabled when EIR0 bit is set

(4) Precautions for use

When enabling an interrupt after clearing a reset, always clear the interrupt flag at the same time. An interrupt request will be output immediately whenever the interrupt flag (EIR0) is set to '1.'

Chapter 3: OPERATION

3.1 Clock Pulse Generator

The MB89863 series of microcontrollers features a built-in system clock pulse generator. Clock signal pulses are generated by a crystal oscillator connected to the X0 and X1 pins. Clock pulses can also be produced internally by connecting externally generated clock pulses to the X0 pin. The X1 pin should be kept open

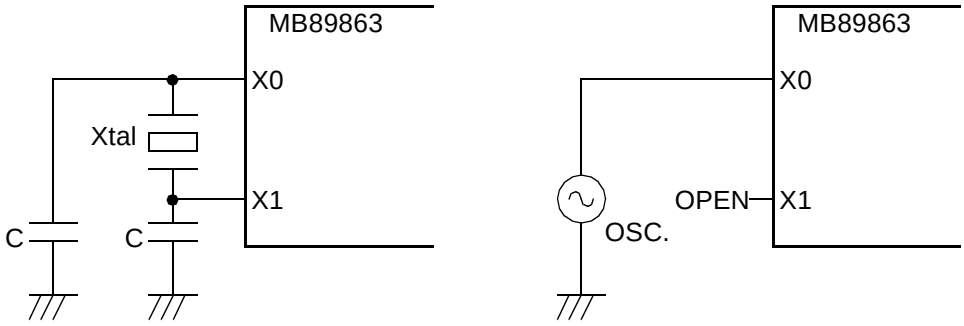


Fig. 3.1.1 Clock Pulse Generator Circuit

3.2 Reset

3.2.1 Reset Operation

When a reset condition occurs, the MB89863 series of microcontrollers suspends execution of the current instruction and enters reset state. The contents of RAM do not change during or after reset. However if a reset occurs during writing of 16-bit data, some data may be written to upper byte addresses and not to lower byte addresses. If a reset occurs during the timing of a write access operation, the contents of the destination addresses are not assured.

When the reset is cleared, the MB89863 series of microcontrollers are released from reset state. Before operation begins, mode data must be obtained from address FFFDH, the upper bytes of the reset vectors from address FFFEH, and the lower bytes from address FFFFH. Figure 3.2.1 shows the flowchart for a reset cancellation sequence.

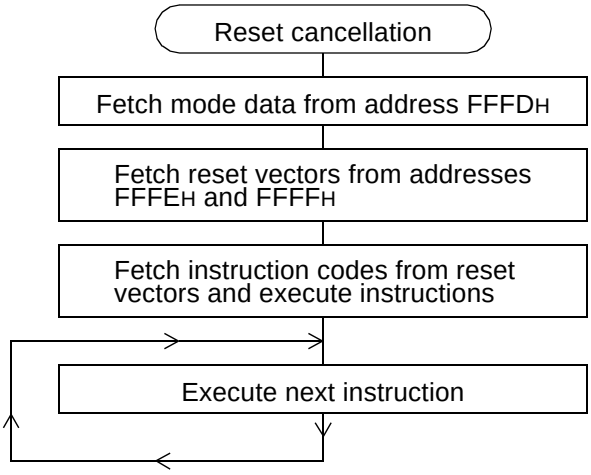
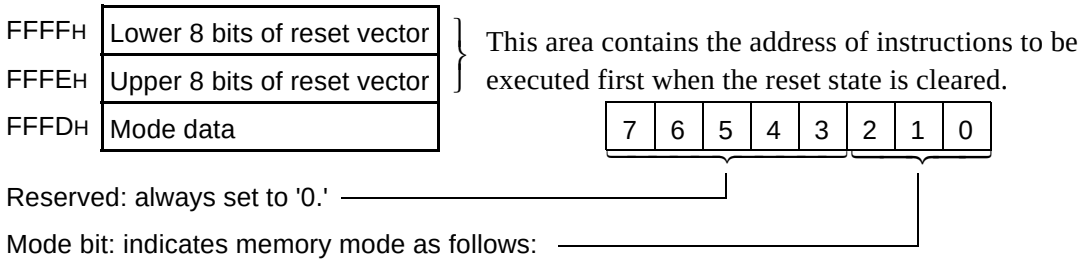


Fig. 3.2.1 Outline of Reset Release Sequence

Figure 3.2.2 indicates the structure of data stored in addresses FFFDH, FFFEH and FFFFH .



T2	T1	T0	Operation
0	0	0	External access disabled (single-chip mode)
Other values			Reserved: do not use

Fig. 3.2.2 Reset Vector Structure

3.2.2 Reset Conditions

The MB89863 series of microcontrollers have the following reset sources:

(1) External pin originated: A low level signal input to the RSTX pin.

(2) Software originated: '0' is written to the RST bit of the standby control register

(3) Power-on: The power supply is turned on.

(4) Watchdog function: The watchdog function is enabled by the watchdog control register, and reaccess to this register does not occur within the specified time.

Following wake-up from stop mode or a power-on reset, the oscillation stabilization time must elapse before operation resumes.

Note: In any state other than stop mode, external reset input is sampled by internal clock pulses. Therefore reset input is not accepted when the supply of external clock pulses to the MB89863 series of microcontrollers is stopped.

3.3 Interrupts

If the interrupt controller and CPU are ready to accept interrupts when an interrupt request is output from internal resources or by an external interrupt signal, the CPU temporarily suspends the execution of the current instruction and executes the interrupt processing program. Figure 3-3-1 shows the interrupt processing flowchart.

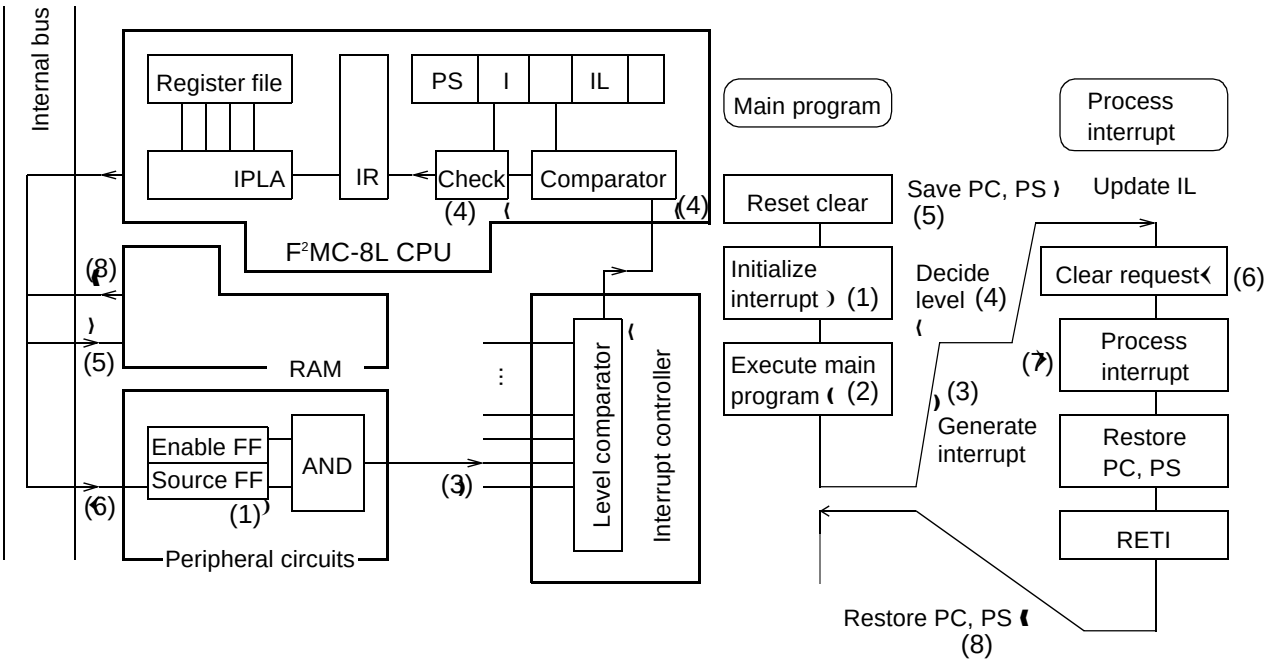


Fig. 3.3.1 Interrupt Processing Flowchart

Initially all interrupts are in disabled status. Therefore, interrupts must be initialized in the main program(1). Initialization must be made for each peripheral generating an interrupt, and the interrupt level setting registers (ILR1 to ILR3) in the corresponding interrupt controllers, where the levels of all interrupts can be designated. Each interrupt level can be set from 1 to 3, where 1 indicates the highest level and 2 the second highest level. Level 3 indicates that no interrupt occurs, and therefore interrupts set at this level are prohibited from causing interrupt requests.

After making the peripheral register settings, the main program executes various controls (2). During operation, interrupts are generated from various resources (3). When interrupt requests occur at the same time, those having the highest priority are identified by the interrupt controller and are transferred to the CPU. The CPU then checks the current interrupt level and the status of the related I-flag (4) and starts interrupt processing.

In interrupt processing, the CPU saves the contents of the current PC and PS registers in the stack (5) and reads the interrupt vectors to get the entry addresses of the interrupt program. After updating the IL in the PS register to the currently required value, the CPU begins executing the interrupt processing routine.

Once the interrupt source is cleared by the user-defined interrupt processing routine (6), the CPU executes a RETI instruction to restore the PC and PS values saved to the stack (9), and returns to the interrupted instruction.

Note: Unlike the F²MC-8, the contents of the A and T registers are not saved to the stack during interrupt processing.

Figure 3.3.2 shows the relation between each interrupt source and the corresponding interrupt vector.

Interrupt source	Upper vector address	Lower vector address
IRQ0 (Timer unit 1)	FFFAH	FFFBH
IRQ1 (Timer unit 2)	FFF8H	FFF9H
IRQ2 (Timer unit 3)	FFF6H	FFF7H
IRQ3 (External interrupt)	FFF4H	FFF5H
IRQ4 (PWM timer 1)	FFF2H	FFF3H
IRQ5 (UART)	FFF0H	FFF1H
IRQ6	–	–
IRQ7 (A/D converter)	FFECH	FFEDH
IRQ8	–	–
IRQ9 (PWM timer 2)	FFE8H	FFE9H
IRQ10	–	–
IRQ11 (Interval timer)	FFE4H	FFE5H

Note: No interrupt sources are established for IRQ 6, 8, and 10.

Fig. 3.3.2 Interrupt Sources and Interrupt Vectors

3.4 Low Power Consumption Modes

The MB89863 series of microcontrollers supports two standby modes: sleep mode and stop mode. Transition to either of these modes is made by writing to the standby control register (STBC). Wake-up is performed by an interrupt or reset signal. In sleep mode, the CPU stops operation but each resource continues to operate. In stop mode, the oscillator stops and data is held at the lowest possible level of power consumption.

<Sleep mode>

The CPU operating clock pulse stops, but other signals continue to operate. Transition to sleep mode is initiated by writing '1' to the SLP bit (bit 6) and '0' to the STP bit (bit 7) in the STBC register. The contents of all registers and RAM are retained as they were immediately before entering sleep mode.

Wake-up from sleep mode is initiated by an interrupt request higher than level '11' or by a reset signal. If an interrupt request is already pending when the sleep mode starts, the transition to sleep mode is delayed until the instruction or interrupt processing is executed. When sleep mode is ended by an interrupt request, the operation varies depending on whether the interrupt is enabled or disabled. If the interrupt is enabled according to the values of the I flag and IL bit of the CPU, execution will jump to the interrupt processing routine after the wake-up from sleep mode. If the interrupt is disabled, operation resumes with execution of the next instruction following the instruction during which sleep mode was started.

<Stop mode>

The oscillator stops, and power consumption is reduced to the lowest level at which data can be retained. Transition to stop mode is initiated by setting the STP bit (bit 7) in the STBC register. The contents of all registers and RAM are retained as they were immediately before entering stop mode.

Wake-up from stop mode is initiated by an interrupt request higher than level '11' or by a reset signal. If an interrupt request is already pending when the stop mode starts, the transition to stop mode is delayed until the instruction or interrupt processing is executed. When stop mode is ended by an interrupt request, the operation varies depending on whether the interrupt is enabled or disabled. If the interrupt is enabled according to the values of the I flag and IL bit of the CPU, execution will jump to the interrupt processing routine after the exit from stop mode. If the interrupt is disabled, operation resumes with execution of the next instruction following the one during which stop mode was started. After escaping from stop mode, either by interrupt or reset, the oscillation stabilization time shown in Table 3.4.1 must elapse before processing begins.

Table 3.4.1 Oscillation Stabilization Time

Minimum execution time, counts	Time at 4.2 MHz oscillation	Time at 8 MHz oscillation	Remarks
Approx. 2^{16} counts	Approx. 62.3 ms	Approx. 32.7 ms	For crystal oscillators
Approx. 2^{12} counts	Approx. 3.90 ms	Approx. 2.05 ms	For ceramic oscillators

Figure 3.4.1 is a state transition diagram for MB89863 series of microcontrollers in low-power consumption modes.

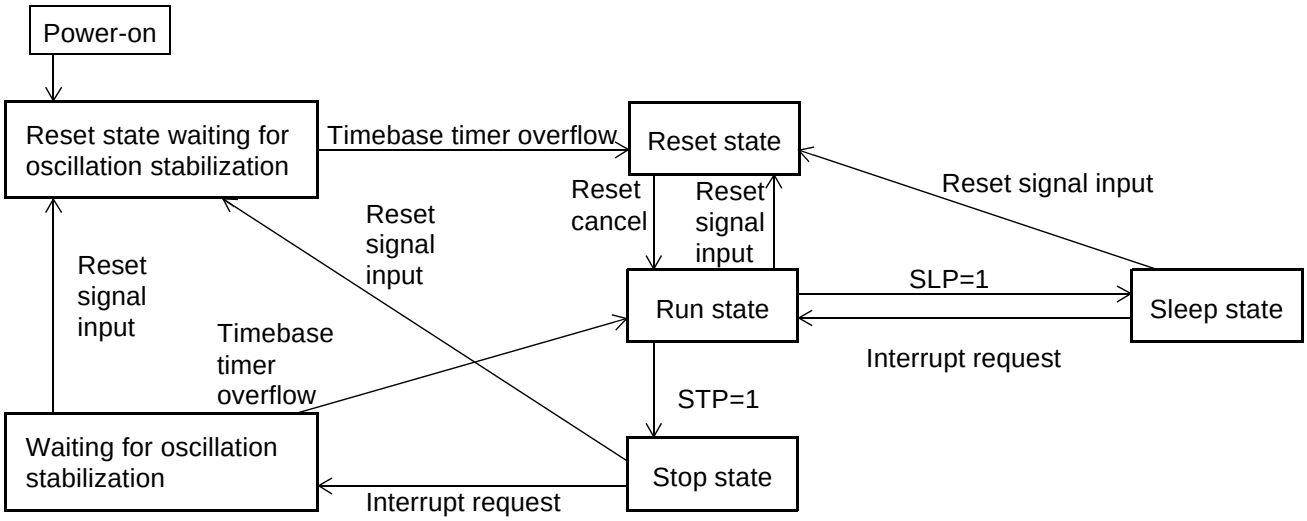


Fig. 3.4.1 Low-Power Consumption Mode State Transition Diagram

3.5 Pin States in Sleep, Stop, Hold and Reset Modes

The state of each pin of the MB89863 series of microcontrollers in sleep, stop, hold and reset modes is as follows:

(1) Sleep: Pins retain the state immediately before sleep mode is entered.

(2) Stop: Pins retain the state immediately before stop mode is entered if the SPL bit (bit 5) of the standby control register (STBC), is set to '0.' If the SPL bit is set to '1,' all output and I/O pins go to high impedance state.

(3) Reset: If the MOD pins have the value '00,' all I/O pins and resource pins go to high impedance state.

The table on the following pages provides detailed information about pin states.

Normal Pin States for MB89863 Series of Microcontrollers (Single-Chip Mode)

Pin name	Normal	Sleep	Stop, SPL=0	Stop, SPL=1	Reset
P00 to P07	Port input/output	Port input/output	Port input/output	High impedance (Note)	High impedance
X0	Oscillator input	Oscillator input	High impedance (Note)	High impedance (Note)	Oscillator input
X1	Oscillator output	Oscillator output	H level output	H level output	Oscillator output
MOD0 MOD1	Mode input	Mode input	Mode input	Mode input	Mode input
RSTX	Reset input	Reset input	Reset input	Reset input	Reset input
P21 to P27	Port output	Port output	Port output	High impedance	High impedance
P30 to P32 P36 to P37	Port/resource input/output	Port/resource input/output	Port/resource input/output	High impedance (Note)	High impedance
P40/RTO0 to P47/TRGI	Port/resource input/output	Port/resource input/output	Port/resource input/output	High impedance (Note)	High impedance
P50/AN0 to P57/AN7	Port/resource input/output	Port/resource input/output	Port/resource input/output	High impedance	High impedance
P60/INT0, P64/DTTI	Port/resource input	Port/resource input	Port/resource input	High impedance	High impedance

Note: Input level is fixed to prevent leakage from open input conditions.

Chapter 4: INSTRUCTION TABLES

4.1 Transfer-Related Instructions

NO	MNEMONIC	~	#	Operation	TL	TH	AH	NZVC	OP CODE
1	MOV dir,A	3	2	(dir)←(A)	–	–	–	----	45
2	MOV @IX=off,A	4	2	((IX)+off)←(A)	–	–	–	----	46
3	MOV ext,A	4	3	(ext)←(A)	–	–	–	----	61
4	MOV @EP,A	3	1	((EP))←(A)	–	–	–	----	47
5	MOV Ri,A	3	1	(Ri)←(A)	–	–	–	----	48 to 4F
6	MOV A,#db8	2	2	(A)←d8	AL	–	–	++--	04
7	MOV A,dir	3	2	(A)←dir	AL	–	–	++--	45
8	MOV Adir,#db8	4	2	(A)←((IX)+off)	AL	–	–	++--	46
9	MOV @IX=off,#d8	4	3	(A)←(ext)	AL	–	–	++--	60
10	MOV A,@A	5	1	(A)←((A))	AL	–	–	++--	92
11	MOV A,@EP	3	1	(A)←((EP))	AL	–	–	++--	07
12	MOV A,Ri	3	1	(A)←(Ri)	AL	–	–	++--	08 to 0F
13	MOV dir,#d8	4	3	(dir)←d8	–	–	–	----	85
14	MOV @IX+off,#d8	5	3	((IX)+off)←d8	–	–	–	----	86
15	MOV @EP,#d8	4	2	((EP))←d8	–	–	–	----	87
16	MOV Ri,#d8	4	2	(Ri)←d8	–	–	–	----	88 to 8F
17	MOVW dir,A	4	2	(dir)←(AH),(dir+1)←(AL)	–	–	–	----	D5
18	MOVW @IX+off,A	5	2	((IX)+off)←(AH), ((IX)+off+1)←(AL)	–	–	–	----	D6
19	MOVW ext,A	5	3	(ext)←(AH),(ext+1)←(AL)	–	–	–	----	D4
20	MOVW @EP,A	4	1	((EP))←(AH),((EP)+1←(AL)	–	–	–	----	D7
21	MOVW EP,A	2	1	(EP)←(A)	–	–	–	----	E3
22	MOVW A,#d16	3	3	(A) ←d16	AL	AH	dH	++--	E4
23	MOVW A,dir	4	2	(AH)←(dir),(AL)←(dir+1)	AL	AH	dH	++--	C5
24	MOVW A,@IX+off	5	2	(AH)←((IX)+off), (AL)←((IX)+off+1)	AL	AH	dH	++--	C6
25	MOVW A,ext	5	3	(AH)←(ext),(AL)←(ext+1)	AL	AH	dH	++--	C4
26	MOVW A,@A	4	1	(AH)←((A)),(AL)←((A)+1)	AL	AH	dH	++--	93
27	MOVW A,@EP	4	1	(AH)←((EP)),(AL)←((EP)+1)	AL	Ah	dH	++--	C7
28	MOVW A,EP	2	1	(A) ←(EP)	–	–	dH	----	F3
29	MOVW EP,#d16	3	3	(EP)←d16	–	–	–	----	E7
30	NOVW IX,A	2	1	(IX)←(A)	–	–	–	----	E2
31	MOVW A,IX	2	1	(A) ←(IX)	–	–	dH	----	F2
32	MOVW SP,A	2	1	(SP)←(A)	–	–	–	----	E1
33	MOVW A,SP	2	1	(A) ←(SP)	–	–	dH	----	F1
34	MOV @A,T	3	1	((A))←(T)	–	–	–	----	82
35	MOVW @A,T	4	1	((A))←(YH),((A)+1)←(TL)	–	–	–	----	83
36	MOVW IX,#d16	3	3	(IX)←d16	–	–	–	----	E6
37	MOVW A,PS	2	1	(A) ←(PS)	–	–	dH	----	70
38	MOVW PS,A	2	1	(PS)←(A)	–	–	–	++++	71
39	MOVW SP,#d16	3	3	(SP)←d16	–	–	–	----	E5
40	SWAP	2	1	(AH)⇔(AL)	–	–	AL	----	10
41	SETB dir:n	4	2	(dir):n←1	–	–	–	----	A8 to AF
42	CLRB dir:n	4	2	(dir):n←0	–	–	–	----	A0 to A7
43	XCH A,T	2	1	(AL)⇔(TL)	AL	–	–	----	42
44	XCHW A,T	3	1	(A) ⇔(T)	AL	AH	dH	----	43
45	XCHW A,EP	3	1	(A) ⇔(EP)	–	–	dH	----	F7
46	XCHW A,IX	3	1	(A) ⇔(IX)	–	–	dH	----	F6
47	XCHW A,SP	3	1	(A) ⇔(SP)	–	–	dH	----	F5
48	MOVW A,PC	2	1	(A)←(PC)	–	–	dH	----	F0

*1: For byte transfer to A, T←A is used for low bytes only.

*2: Operands used by multiple-operand instructions are stored in mnemonic order (reverse of F²MC-8 order).

4.2 Operation-Related Instructions

NO	MNEMONIC	~	#	Operation	TL	TH	AH	NZVC	OP CODE
1	ADDC A,Ri	3	1	(A)←(A)+(Ri)+C	–	–	–	++++	28 to 2F
2	ADDC A,#d8	2	2	(A)←(A)+d8+C	–	–	–	++++	24
3	ADDC A,dir	3	2	(A)←(A)+(dir)+C	–	–	–	++++	25
4	ADDC A,@IX+off	4	2	(A)←(A)((IX)+off)+C	–	–	–	++++	26
5	ADDC A,@EP	3	1	(A)←(A)((EP))+C	–	–	–	++++	27
6	ADDZW A	3	1	(A)←(A)+(T)+C	–	–	dH	++++	23
7	ADDC A	2	1	(AL)←(AL)+(TL)+C	–	–	–	++++	22
8	SUBC A,Ri	3	1	(A)←(A)-(Ri)-C	–	–	–	++++	38 to 3F
9	SUBC A,#d8	2	2	(A)←(A)-d8-C	–	–	–	++++	34
10	SUBC A,dir	3	2	(A)←(A)-(dir)-C	–	–	–	++++	35
11	SUBC A,@IX+off	4	2	(A)←(A)-((IX)+off)-C	–	–	–	++++	36
12	SUBC A,@EP	3	1	(A)←(A)-((EP))-C	–	–	–	++++	37
13	SUBCW A	3	1	(T)←(T)-(A)-C	–	–	dH	++++	33
14	SUBC A	2	1	(AL)←(TL)-(AL)-C	–	–	–	++++	32
15	INC Ri	4	1	(Ri)←(Ri)+1	–	–	–	+++-	C8 to CF
16	INCW EP	3	1	(EP)←(EP)+1	–	–	–	----	C3
17	INCW IX	3	1	(IX)←(IX)+1	–	–	–	----	C2
18	INCW A	3	1	(A)←(A)+1	–	–	dH	++--	C0
19	DEC Ri	4	1	(Ri)←(Ri)-1	–	–	–	+++-	D8 to DF
20	DECW EP	3	1	(EP)←(EP)+1	–	–	–	----	D3
21	DECW IX	3	1	(IX)←(IX)-1	–	–	–	----	D2
22	DECW A	3	1	(A)←(A)-1	–	–	dH	++--	D0
23	MULU A	19	1	(A)←(AL)*(TL)	–	–	dH	----	01
24	DIVU A	21	1	(A)←(T)/(AL),MOD→(T)	dL	00	00	----	11
25	ANDW A	3	1	(A)←(A)∧(T)	–	–	dH	++R-	63
26	ORW A	3	1	(A)←(A)∨(T)	–	–	dH	++R-	73
27	XORW A	3	1	(A)←(A)∀(T)	–	–	dH	++R-	53
28	CMP A	2	1	(TL)←(AL)	–	–	–	++++	12
29	CMPW A	3	1	(T)←(A)	–	–	–	++++	13
30	RORC A	2	1		–	–	–	++-+	03
31	ROLC A	2	1		–	–	–	++-+	02
32	CMP A,#d8	2	2	(A)←d8	–	–	–	++++	14
33	CMP A,dir	3	2	(A)←(dir)	–	–	–	++++	15
34	CMP A,@EP	3	1	(A)←((EP))	–	–	–	++++	17
35	CMP A,@IX+off	4	2	(A)←((IX)+off)	–	–	–	++++	16
36	CMP A,Ri	3	1	(A)←(Ri)	–	–	–	++++	18 to 1F
37	DAA	2	1	decimal adjust for addition	–	–	–	++++	84
38	DAS	2	1	decimal adjust for subttaction	–	–	–	++++	94
39	XOR A	2	1	(A)←(AL)∀(TL)	–	–	–	++R-	52
40	XOR A,#d8	2	2	(A)←(AL)∀ d8	–	–	–	++R-	54
41	XOR A,dir	3	2	(A)←(AL)∀(dir)	–	–	–	++R-	55
42	XOR A,@EP	3	1	(A)←(AL)∀((EP))	–	–	–	++R-	57
43	XOR A,IX+off	4	2	(A)←(AL)∀((IX)+off)	–	–	–	++R-	56
44	XOR A,Ri	3	1	(A)←(AL)∀(Ri)	–	–	–	++R-	58 to 5F
45	AND A	2	1	(A)←(AL)∧(TL)	–	–	–	++R-	62
46	AND A,#d8	2	2	(A)←(AL)∧ d8	–	–	–	++R-	64
47	AND A,dir	3	2	(A)←(AL)∧(dir)	–	–	–	++R-	65
48	AND A,@EP	3	1	(A)←(AL)∧((EP))	–	–	–	++R-	67
49	AND A,@IX+off	4	2	(A)←(AL)∧((IX)+off)	–	–	–	++R-	66
50	AND A,Ri	3	1	(A)←(AL)∧(Ri)	–	–	–	++R-	68 to 6F
51	OR A	2	1	(A)←(AL)∨(TL)	–	–	–	++R-	72
52	OR A,#d8	2	2	(A)←(AL)∨ d8	–	–	–	++R-	74
53	OR A,dir	3	2	(A)←(AL)∨(dir)	–	–	–	++R-	75
54	OR A,@EP	3	1	(A)←(AL)∨((EP))	–	–	–	++R-	77
55	OR A,@IX+off	4	2	(A)←(AL)∨((IX)+off)	–	–	–	++R-	76
56	CMP A,Ri	3	1	(A)←(AL)∨(Ri)	–	–	–	++R-	78 to 7F
57	CMP dir,#d8	5	3	(dir) –d8	–	–	–	++++	95
58	CMP @EP,#d8	4	2	((EP))–d8	–	–	–	++++	97
59	CMP @IX+off,#d8	5	3	((IX)+off)-d8	–	–	–	++++	96
60	CMP Ri,#d8	4	2	(Ri)–d8	–	–	–	++++	98 to 9F
61	INCW SP	3	1	(SP)←(SP)+1	–	–	–	----	C1
62	DECW SP	3	1	(SP)←(SP)-1	–	–	–	----	D1

4.3 Branch-Related Instructions

NO	MNEMONIC	~	#	Operation	TL	TH	AH	NZVC	OP CODE
1	BZ/BEQ rel	3	2	if Z=1 then PC←PC+rel	–	–	–	----	FD
2	BNZ/BNE rel	3	2	if Z=0 then PC←PC+rel	–	–	–	----	FC
3	BC/BLO rel	3	2	if C=1 then PC←PC+rel	–	–	–	----	F9
4	BNC/BHS rel	3	2	if C=0 then PC←PC+rel	–	–	–	----	F8
5	BN rel	3	2	if N=1 then PC←PC+rel	–	–	–	----	FB
6	BP rel	3	2	if N=0 then PC←PC+rel	–	–	–	----	FA
7	BLT rel	3	2	if V∀N=1 then PC←PC+rel	–	–	–	----	FF
8	BGE rel	3	2	if V∀N=0 then PC←PC+rel	–	–	–	----	FE
9	BBC dir:b,rel	5	3	if (dir:b)=0 then PC←PC+rel	–	–	–	-+--	B0 to B7
10	BBS dir:b,rel	5	3	if (dir:b)=1 then PC←PC+rel	–	–	–	-+--	B8 to BF
11	JMP @A	2	1	(PC)←(A)	–	–	–	----	E0
12	JMP ext	3	3	(PC)←etc	–	–	–	----	21
13	CALLV #vct	6	1	vector call	–	–	–	----	E8 to EF
14	CALL ext	6	3	subroutine call	–	–	–	----	31
15	XCHW A,PC	3	1	(PC)←(A),(A)←(PC)+1	–	–	dH	----	F4
16	RET	4	1	return from subroutine	–	–	–	----	20
17	RETI	6	1	return from interrupt	–	–	–	restore	30

4.4 Other Instructions

NO	MNEMONIC	~	#	Operation	TL	TH	AH	NZVC	OP CODE
1	PUSHW A	4	1		–	–	–	----	40
2	POPW A	4	1		–	–	dH	----	50
3	PUSHW IX	4	1		–	–	–	----	41
4	POPW IX	4	1		–	–	–	----	51
5	NOP	1	1		–	–	–	----	00
6	CLRC	1	1		–	–	–	---R	81
7	SETC	1	1		–	–	–	---S	91
8	CLRI	1	1		–	–	–	----	80
9	SETI	1	1		–	–	–	----	90

4.5 Instruction Map

F²MC-8L Instruction Map

L\H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir :0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir :1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir :2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir:3	BBC dir :3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir :4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir :5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC @IX+dA,	SUBC A,@IX+d	MOV @IX+d,A	XOR A,@IX+d	AND A,@IX+d	OR A,@IX+d	MOV IX+d,#d8	CMP IX+d,#d8	CLRB dir:6	BBC dir :6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @E,#d8P	CMP @E,#d8P	CLRB dir:7	BBC dir :7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir :0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir :1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir :2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir :3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir :4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir :5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir :6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir :7,rel	INC R7	DEC R7	CALLV #7	BLT rel

Chapter 5: ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

(AVss = Vss = 0.0 V)

Item	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Supply voltage	Vcc	Vss-0.3	Vss+7.0	V	
	AVcc	Vss-0.3	Vss+7.0	V	Not to exceed Vcc (Note)
	AVR	Vss-0.3	Vss+7.0	V	Not to exceed AVcc +0.3 V
Input voltage	V_I	Vss-0.3	Vss+0.3	V	
Output voltage	V_O	Vss-0.3	Vss+0.3	V	
'L' level output current	I_{OL}	–	20	mA	
'L' level average current	I_{OLAV1}	–	4	mA	P00 to P07, P21 to P27, P30 to P32, P36, P37, P50 to P57
'L' level average current	I_{OLAV2}	–	15	mA	P40 to P47
'L' level total output average current	ΣI_{OLAV1}	–	15	mA	P00 to P07, P21 to P27, P30 to P32, P36, P37, P50 to P57
'L' level total output average current	ΣI_{OLAV2}	–	45	mA	P40 to P47
'H' level output current	I_{OH}	–	-20	mA	
'H' level average current	I_{OHAV}	–	-4	mA	
'H' level total output average current	ΣI_{OH}	–	-20	mA	
Power consumption	Pd	–	230	mW	
Operating temperature	Ta	-40	+85	°C	
Storage temperature	Tstg	-55	+150	°C	

Note: AVcc and Vcc should be used at the same potential level.

Use at levels exceeding absolute maximum ratings may cause permanent damage to the LSI and reduce its life.

Normal use should not exceed the recommended operating conditions, limits over which the reliability of the LSI may be adversely affected.

5.2 Recommended Operating Conditions

(AVss = Vss = 0.0 V)

Item	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Supply voltage	Vcc AVcc	4.5	5.5	V	
	AVR	0.0	AVcc	V	
Operating temperature	Ta	-40	+85	°C	

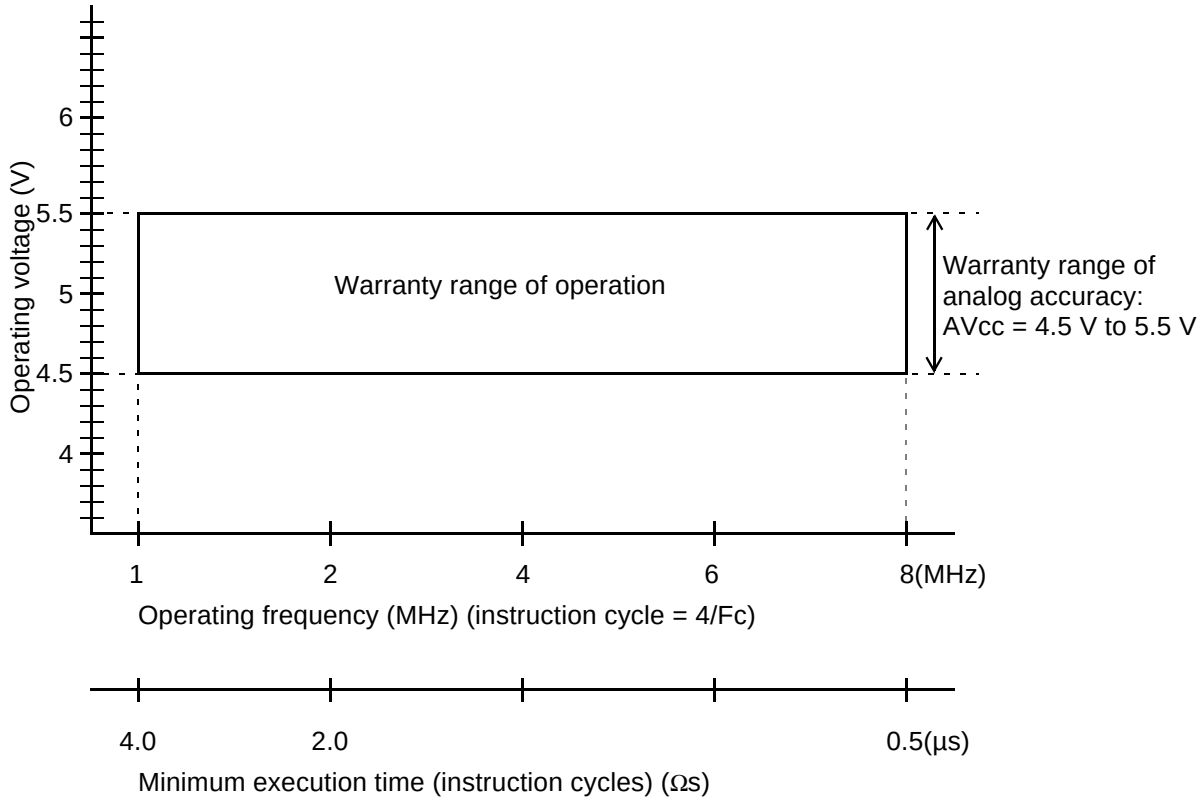


Fig. 1 Range of Assured Operation

5.3 DC Standards

Table 3.4.2 (Ta = -40 to 85°C, AVcc = Vcc = 5.0 V, AVss = Vss = 0.0 V)

Item	Symbol	Pin	Condition	Rated value			Unit	Remarks
				Min.	Typ.	Max.		
Input 'H' voltage	V_{IH}	P00 to P07	–	0.7 Vcc	–	Vcc+0.3	V	
	V_{IHS}	RSTX, P30 to P32, P36 to P37, P40 to P47, P60, P64	–	0.8 Vcc	–	Vcc+0.3	V	
Input 'L' voltage	V_{IL}	P00 to P07	–	Vss-0.3	–	0.3 Vcc	V	
	V_{ILS}	RSTX,P30 to P32, P36 to P37, P40 to P47, P60, P64	–	Vss-0.3	–	0.2 Vcc	V	
Output 'H' voltage	V_{OH}	P00 to P07, P21 to P27, P30 to P32, P36 to P37, P40 to P47	I_{OH} = -2.0 mA	2.4	–	–	V	
Output 'L' voltage	V_{OL1}	P00 to P07, P21 to P27, P30 to P32, P36 to P37, P50 to P57	I_{OL}= 1.8 mA	–	–	0.4	V	
	V_{OL2}	P40 t oP47	I_{OL} = 15 mA	–	–	1.5	V	
Input leak current	I_{L11}	P00 to P07, P21 to P27, P30 t oP32, P36 to P37, P40 to P47, P50 to P57, P60, P64	0.45 V < V_I < Vcc	–	–	±5	µA	
Pull-up resistance	R_{PULL}	RSTX	V_I= 0.0 V	25	50	100	kΩ	
Supply current	Icc	Vcc	Fc = 4.2 MHz	–	5	15	mA	In normal operation (external clock)
			Fc = 8 MHz	–	7	18	mA	
	I_{CCS}		Fc = 4.2 MHz	–	1	8	mA	In sleep mode (external clock)
			Fc = 8 MHz	–	2	10	mA	
	I_{CCH}		Ta = 25°C	–	–	10	µA	In stop mode
	I_A	AVcc	Fc = 8 MHz	–	6	–	mA	At start of AD conversion
Input capacitance	C_{IN}	other than AVcc, AVss, Vcc, Vss	f = 1 MHz	–	10	–	pF	

Note: The MOD0 and MOD1 pins should be connected directly to VSS.

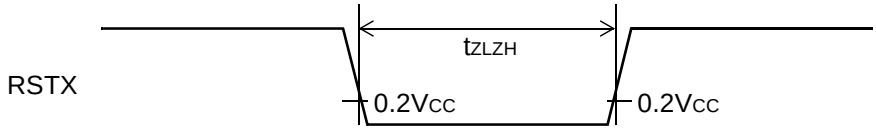
5.4 AC Standards

❍ Reset Timing

(Ta = -40 to 85°C, Vcc = 5.0 V±10%, AVss = Vss = 0.0 V)

Item	Symbol	Condition	Rating		Unit	Remarks
			Min.	Max.		
RSTX 'L' pulse width	t_{ZLZH}	–	$16t_{XCYL}$	–	ns	

Note: t_{XCYL} represents the oscillation cycle of input to the X0 pin (1/Fc).

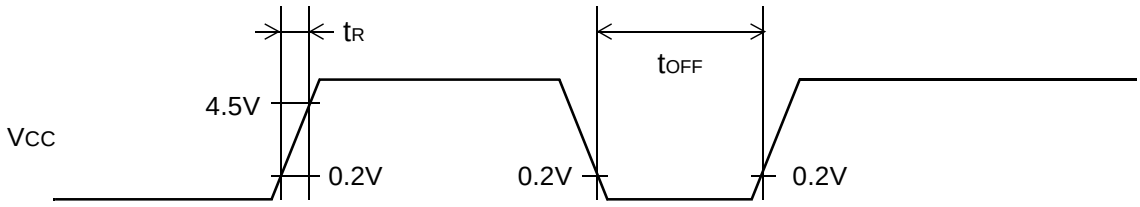


❍ Power-On Reset

(Ta = -40 to 85°C, Vcc = 5.0 V±10%, AVss = Vss = 0.0 V)

Item	Symbol	Condition	Rating		Unit	Remarks
			Min.	Max.		
Power supply rise time	t_R	–	–	50	ms	
Power supply shutoff time	t_{OFF}		1	–	ms	Repetitive operation

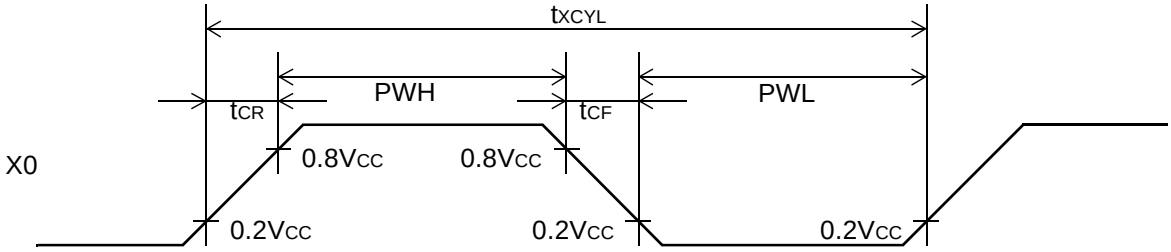
Note: Be sure the power supply rise time is less than the selected oscillation stabilization time. Also, it is recommended that changes in voltage during operation be kept as smooth as possible.



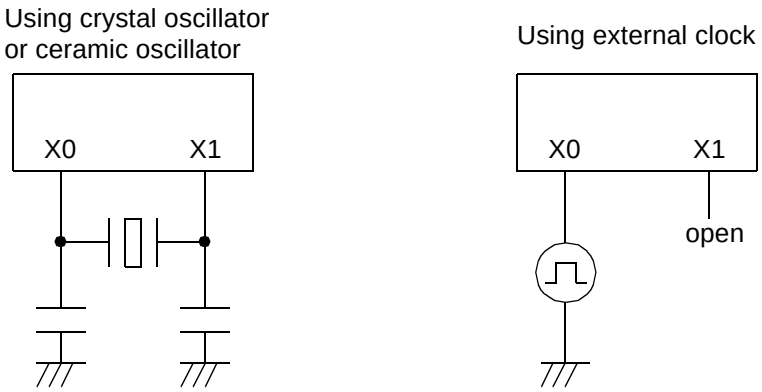
❍ Clock Timing Standards

(Ta = -40 to 85°C, AVss = Vss = 0.0 V)

Item	Symbol	Pin	Condition	Rating		Unit	Remarks
				Min.	Max.		
Clock frequency	Fc	X0, X1	–	1	8	MHz	
Clock cycle time	t_{XCYL}	X0, X1	–	125	1000	ns	
Input clock pulse width	PWH PWL	X0	–	35	–	ns	With external clock
Input clock rise/fall time	t_{CR} t_{CF}	X0	–	–	10	ns	With external clock



Clock signal application conditions



❍ Instruction Cycle Time

Table 3.4.3 (Ta = -40 to 85°C, Vcc = 5.0 V±10%, AVss = Vss = 0.0 V)

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Minimum execution time (instruction cycle time)	t_{inst}		0.50	–	4	µs	

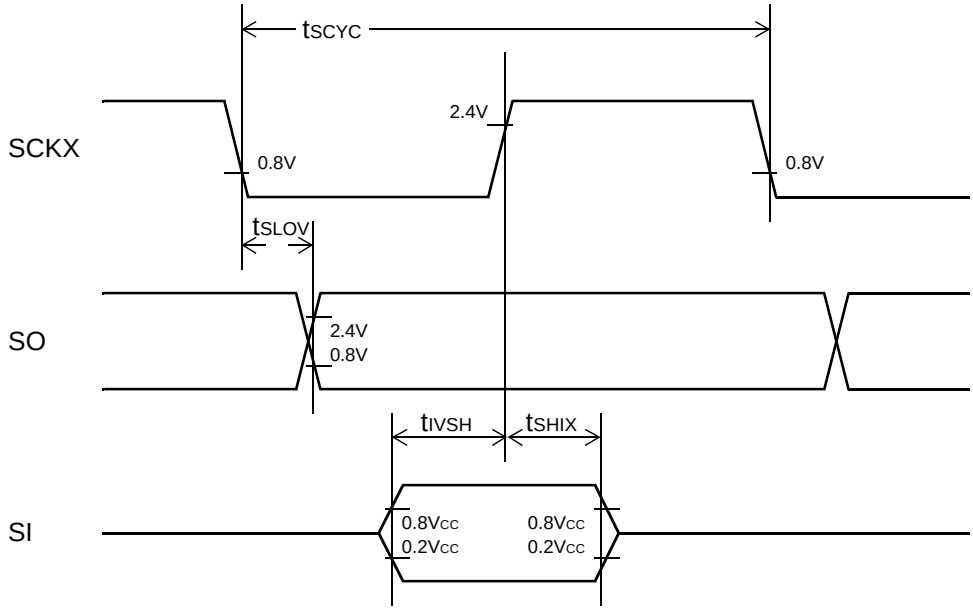
❍ UART

Table 3.4.4 (Ta = -40 to 85°C, Vcc = 5.0 V±10%, AVss = Vss = 0.0 V)

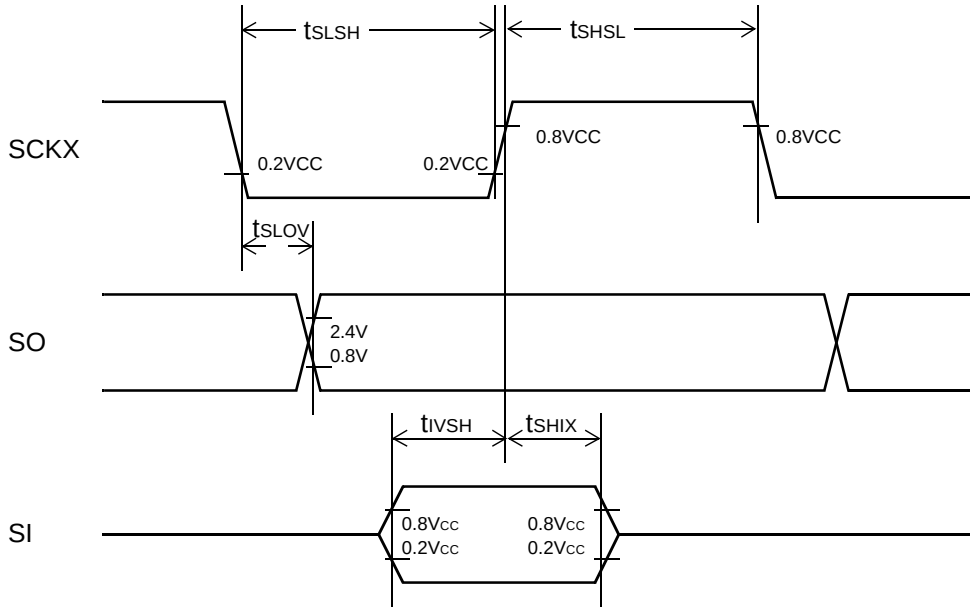
Item	Symbol	Pin	Condition	Rating		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCKX	Internal clock operation	$2t_{inst}$*	–	µs	
SCKX fall ↓ to SO time	t_{SLOV}	SCKX, SO		-200	200	ns	
Valid SI to SCKX rise ↑	t_{IVSH}	SI, SCKX		$1/2t_{inst}$	–	µs	
SCKX rise ↑ to valid SI hold time	t_{SHIX}	SCKX, SI		$1/2t_{inst}$	–	µs	
Serial clock 'H' pulse width	t_{SHSL}	SCKX	External clock operation	t_{inst}	–	µs	
Serial clock 'L' pulse width	t_{SLSH}	SCKX		t_{inst}	–	µs	
SCKX fall ↓ to SO time	t_{SLOV}	SCKX, SO		0	200	ns	
Valid SI to SCKX rise ↑	t_{IVSH}	SI, SCKX		$1/2t_{inst}$	–	µs	
SCKX rise ↑ to valid SI hold time	t_{SHIX}	SCKX, SI		$1/2t_{inst}$	–	µs	

*: For t_{inst}, see 'Instruction Cycle Time.'

Internal Shift Clock Mode



External Shift Clock Mode



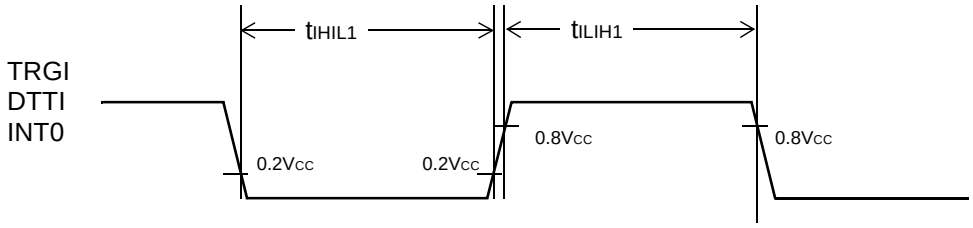
❍ Peripheral Input Timing

(Ta = -40 to 85°C, Vcc = 5.0 V±10%, AVss = Vss = 0.0 V)

Item	Symbol	Pin	Condition	Rating		Unit	Remarks
				Min.	Max.		
Peripheral input 'H' level pulse width 1	t_{ILIH1}	TRGI, DTTI, INT0		$2t_{inst}$*	–	µs	
Peripheral input 'L' level pulse width 1	t_{IHIL1}	TRGI, DTTI, INT0		$2t_{inst}$	–	µs	

*: For t_{inst}, see 'Instruction Cycle Time.'

Peripheral Input Timing Diagram



5.5 A/D Converter Electrical Characteristics

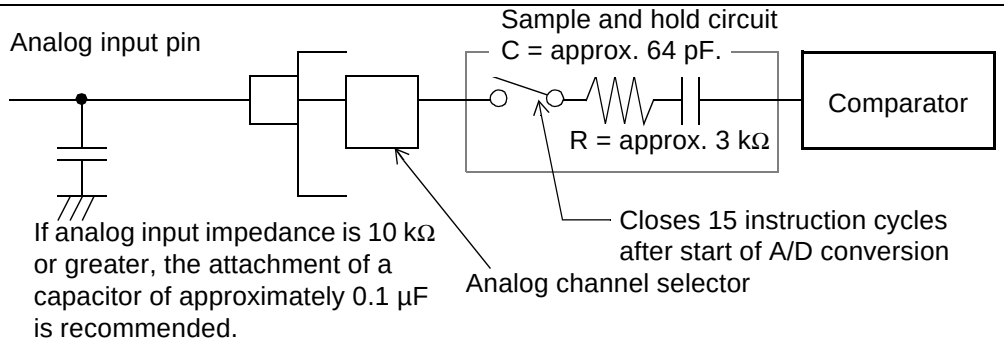
(Ta = -40 to 85°C, AVcc = Vcc = 5.0 V±10%, Fc = 4.2 MHz, AVss = Vss = 0.0 V)

Item	Symbol	Pin	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	–	–	–	–	10	bit	
Linearity error	–	–	–	–	±2.0	LSB	
Differential linearity error	–	–	–	–	±1.5	LSB	
Total error	–	–	–	–	±3.0	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVss - 1.5LSB	AVss +0.5LSB	AVss +2.5LSB	LSB	
Full-scale transition voltage	V_{FST}	AN0 to AN7	AV_R -3.5LSB	AV_R -1.5LSB	AV_R +0.5LSB	LSB	
Variation between channels	–	–	–	–	4	LSB	
AD conversion time	–	–	–	33	–	t_{inst}*	
Analog port input current	I_{AIN}	AN0 to AN7	–	–	10	µA	
Analog input voltage	–	AN0 to AN7	0	–	AV_R	V	
Reference voltage	–	AV_R	0	–	AV_{CC}	V	
Reference voltage supply current	I_R	AV_R	–	200	–	µA	AV_R = 5.0 V

*: For t_{inst}, see 'Instruction Cycle Time.'

Note:

- Input Impedance of Analog Input Pins
  The A/D converter has a sample & hold circuit as shown below, which uses a sample-and-hold capacitor to obtain the voltage at the analog input pin for 15 instruction cycles following the start of A/D conversion. For this reason if the external circuits providing the analog input signal have high output impedance, the analog input voltage may not stabilized within the analog input sampling time. It is therefore recommended that the output impedance of external circuits be reduced to 10 kΩ or less.
  If it is not possible to reduce the output impedance of the external circuits, it is recommended that an 0.1 µF capacitor be externally connected to the analog input pin.



Note: Values shown are intended for reference purposes only.

Sample analog input circuit

- Margin of error:

  As the value |AVR - AVss| decreases, the relative margin of error increases.

- A/D Converter Terms and Definition

  Resolution

  The level of analog variation that can be distinguished by the A/D converter.

  10-bit resolution implies that analog voltage can be resolved into 2^{10} or 1024 levels.

  Linearity error (unit: LSB)

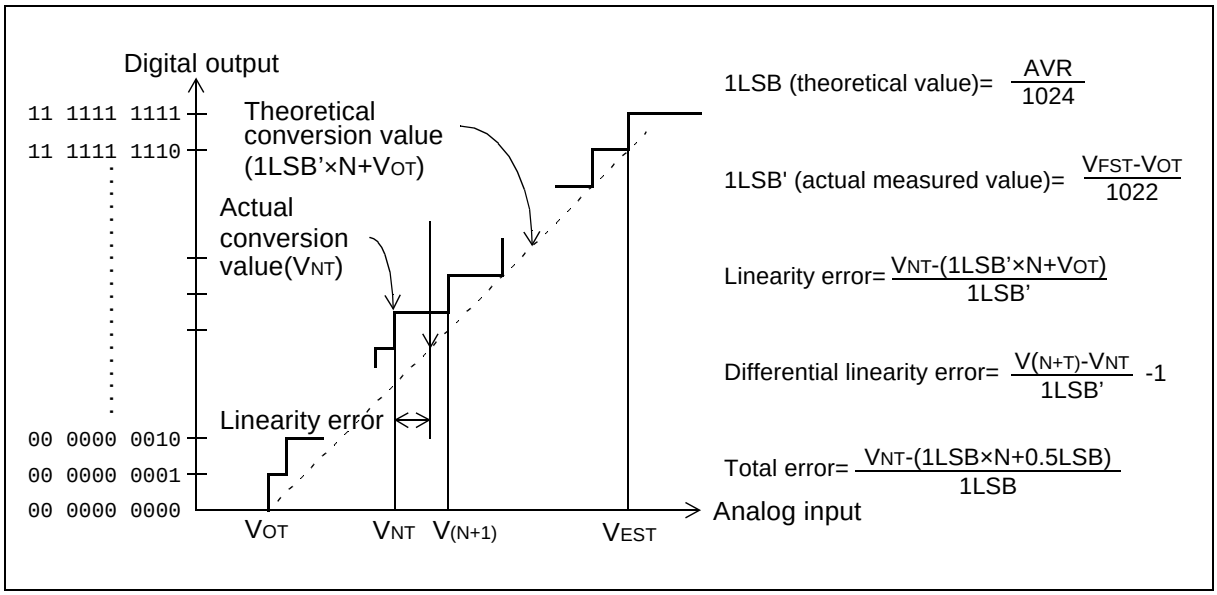
  The deviation between the value along a straight line connecting the zero transition point ("00 0000 0000"←→ "00 0000 0001") of a device and the full-scale transition point ("11 1111 1111" ←→ "11 1111 1110"), compared with the actual conversion values obtained.

  Differential linearity error

  The deviation from the theoretical input voltage required to produce a change of 1 LSB in output code.

  Total error

  The difference between theoretical conversion value and actual conversion value



Appendix 1 I/O MAP

Addresses 00H to 23H

Address	Write/Read	Register	Register contents
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 direction register
02H	Vacant		
03H	Vacant		
04H	(R/W)	PDR2	Port 2 data register
05H	Vacant		
06H	Vacant		
07H	Vacant		
08H	(R/W)	STBC	Standby control register
09H	(W)	WDTC	Watchdog control register
0AH	(R/W)	TBTC	Clock interrupt control register
0BH	Vacant		
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 direction register
10H	(R/W)	PDR5	Port 5 data register
11H	Vacant		
12H	(R)	PDR6	Port 6 data register
13H	Vacant		
14H	Vacant		
15H	Vacant		
16H	Vacant		
17H to 1BH	Vacant		
1CH	(R/W)	CTR1	PWM control register 1
1DH	(W)	CMR1	PWM compare register 1
1EH	(R/W)	CTR2	PWM control register 2
1FH	(W)	CMR2	PWM compare register 2
20H	(R/W)	SMC	UART serial mode control register
21H	(R/W)	SRC	UART serial write control register
22H	(R/W)	SSD	UART serial status/data register
23H	(R/W)	SIDR/SODR	UART serial data register

Note: Vacant spaces should not be used.

Addresses 24H to 7FH

Address	Write/Read	Register	Register contents
24H	Vacant		
25H	Vacant		
26H	(R/W)	EIC1	External interrupt control register 1
27H	Vacant		
28H	(R/W)	ADC1	A/D control register 1
29H	(R/W)	ADC2	A/D control register 2
2AH	(R/W)	ADDH	A/D data register (H)
2BH	(R/W)	ADDL	A/D data register (L)
2CH	Vacant		
2DH	(W)	ZOCTR	Zero detection output control register
2EH	(W)	CLRBRH	Compare-clear buffer register (H)
2FH	(W)	CLRBRL	Compare-clear buffer register (L)
30H	(R/W)	TCSR	Timer control status register
31H	(R/W)	CICR	Compare interrupt control register
32H	(R/W)	TMCR	Timer mode control register
33H	(R/W)	COER	Compare/port switching register
34H	(R/W)	CMCR	Compare buffer mode control register
35H	(R/W)	DTCR	Dead-time timer control register
36H	(W)	DTSR	Dead-time setting register
37H	(R/W)	OCTBR	Output control buffer register
38H	(W)	OCPBR0H	Output compare buffer register 0 (H)
39H	(W)	OCPBR0L	Output compare buffer register 0 (L)
3AH	(W)	OCPBR1H	Output compare buffer register 1 (H)
3BH	(W)	OCPBR1L	Output compare buffer register 1 (L)
3CH	(W)	OCPBR2H	Output compare buffer register 2 (H)
3DH	(W)	OCPBR2L	Output compare buffer register 2 (L)
3EH	(W)	OCPBR3H	Output compare buffer register 3 (H)
3FH	(W)	OCPBR3L	Output compare buffer register 3 (L)
40H to 7BH	Vacant		
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH	Vacant		

Note: Vacant spaces should not be used.

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