F² MC-8L Family
MICROCONTROLLER
MB89940 *Series*
Hardware Manual

Revision 0.91a

F^{2}MC-8L Family

MCROCONTROLLER

MB89940 Series

Hardware Manual

Revision 0.91a May,1996

Preliminary information

1 Table of Contents

2 Revision History

Date	Modification
24/May,1996	Revision 0.91a derived from Revision 0.91

3 Overview

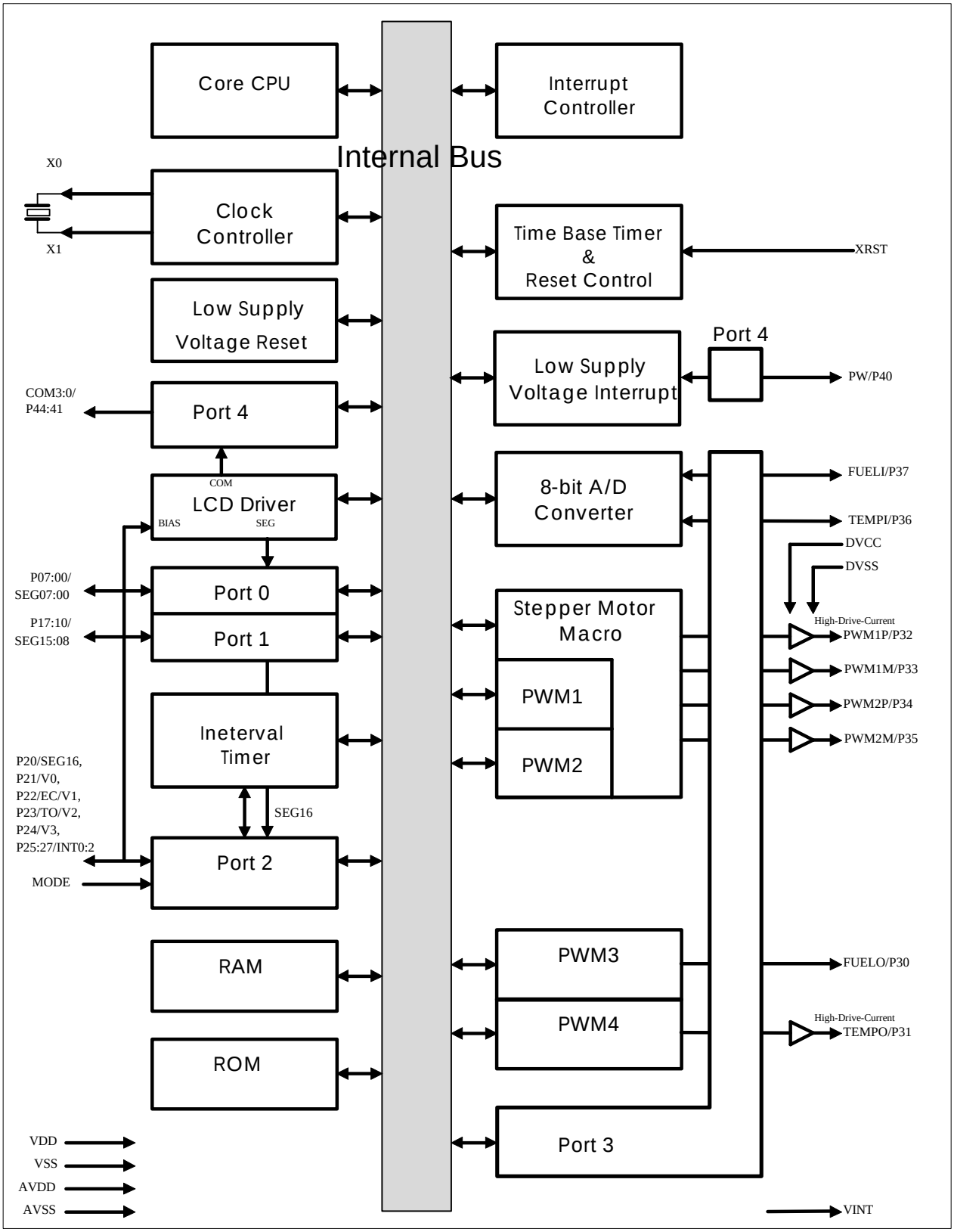
3.1 Features

The MB89940 Series is specially designed for automotive instrumentation applications. It features a combination of two PWM pulse generators and four high-drive-current outputs for stepper motor control. It also contains two analog inputs, two PWM pulse generators and 10-digit LCD controller/driver for various sensor/indicator devices. The MB89940 Series is manufactured with a high performance CMOS technologies and packaged in a 48-pin QFP.

- ✓ 8-bit core CPU; 4MHz system clock (8MHz external, 500ns instruction cycle)
- ✓ 21-bit watchdog timer
- ✓ Clock generator/controller
- ✓ 16-bit interval timer
- ✓ Two PWM pulse generators with four high-drive-current outputs
- ✓ Two-channel 8-bit A/D converter
- ✓ 3-level external interrupt
- ✓ Low supply voltage reset
- ✓ Low supply voltage interrupt
- ✓ Two more PWM pulse generators for indicator device control
- ✓ 4-common 17-segment LCD driver/controller
- ✓ 48-pin QFP
- ✓ 5V single power supply (V_{PP} required for MB89P945)
- ✓ 0.8um CMOS technology(MB89PV940 and MB89P945)
- ✓ 0.5um CMOS technology (MB89943)
- ✓ On-Chip Voltage Regulator for the internal 3V power supply (MB89943)

Memory configuration	RAM	ROM
MB89PV940	1k bytes	32k bytes (External) (Piggy back interface)
MB89P945	512k bytes	16k bytes (One Time PROM)
MB89943	256 bytes	8k bytes

3.2 Block Diagram

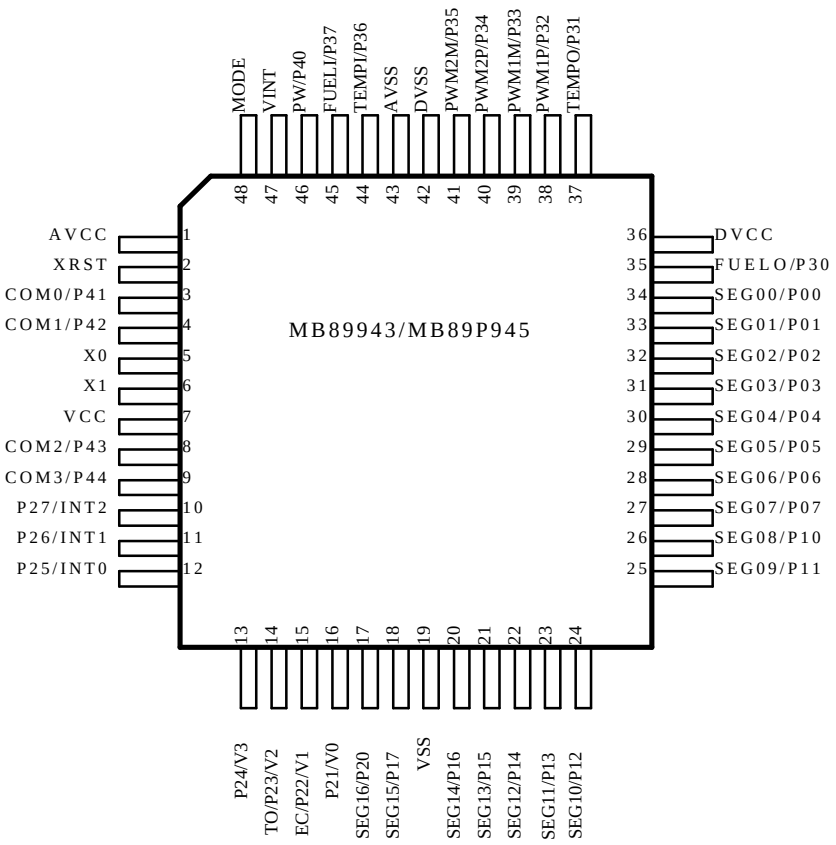


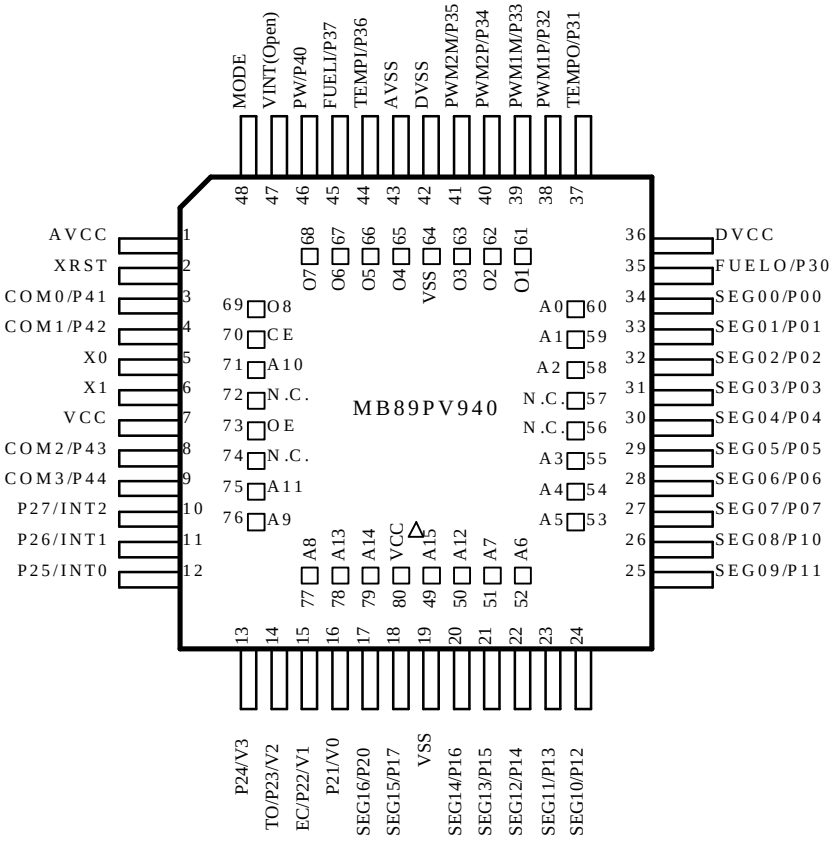
Preliminary information

3.3 Pin assignment

Pin No.	Pin Name	Input buffer	Output buffer
1	AVCC		
2	XRST	CMOS schmitt trigger.	Open Drain Iol=4mA.
3	COM0/P41		Open Drain Iol=4mA. LCD output.
4	COM1/P42		Open Drain Iol=4mA. LCD output.
5	X0	Oscillator input.	
6	X1		Oscillator output.
7	VCC		
8	COM2/P43		Open Drain Iol=4mA. LCD output.
9	COM3/P44		Open Drain Iol=4mA. LCD output.
10	P27/INT2	CMOS schmitt trigger.	CMOS Iol/Ioh=4/-2mA.
11	P26/INT1	CMOS schmitt trigger.	CMOS Iol/Ioh=4/-2mA.
12	P25/INT0	CMOS schmitt trigger.	CMOS Iol/Ioh=4/-2mA.
13	P24/V3	CMOS schmitt trigger. External bias input.	CMOS Iol/Ioh=4/-2mA.
14	TO/P23/V2	CMOS schmitt trigger. External bias input.	CMOS Iol/Ioh=4/-2mA.
15	EC/P22/V1	CMOS schmitt trigger. External bias input.	CMOS Iol/Ioh=4/-2mA.
16	P21/V0	CMOS schmitt trigger. External bias input.	CMOS Iol/Ioh=4/-2mA.
17	SEG16/P20	CMOS schmitt trigger.	CMOS Iol/Ioh=4/-2mA. LCD output.
18	SEG15/P17	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
19	VSS		
20	SEG14/P16	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
21	SEG13/P15	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
22	SEG12/P14	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
23	SEG11/P13	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
24	SEG10/P12	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.

Pin No.	Pin Name	Input	Output
25	SEG09/P11	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
26	SEG08/P10	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
27	SEG07/P07	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
28	SEG06/P06	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
29	SEG05/P05	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
30	SEG04/P04	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
31	SEG03/P03	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
32	SEG02/P02	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
33	SEG01/P01	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
34	SEG00/P00	CMOS input.	CMOS Iol/Ioh=4/-2mA. LCD output.
35	FUELO/P30	CMOS input.	CMOS Iol/Ioh=4/-2mA.
36	DVCC		
37	TEMPO/P31	CMOS input.	CMOS high drive current.
38	PWM1P/P32	CMOS input.	CMOS high drive current.
39	PWM1M/P33	CMOS input.	CMOS high drive current.
40	PWM2P/P34	CMOS input.	CMOS high drive current.
41	PWM2M/P35	CMOS input.	CMOS high drive current.
42	DVSS		
43	AVSS		
44	TEMPI/P36	CMOS input. Analog input.	CMOS Iol/Ioh=4mA/-2mA.
45	FUELI/P37	CMOS input. Analog input.	CMOS Iol/Ioh=4mA/-2mA.
46	PW/P40	Analog input	CMOS open drain Iol=4mA.
47	VINT		External pin for capacitor stabilizer.
48	MODE	CMOS schmitt trigger.	



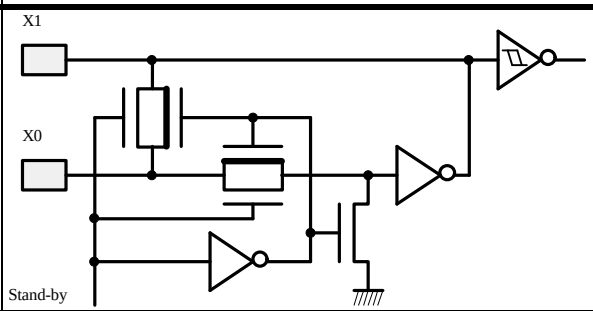
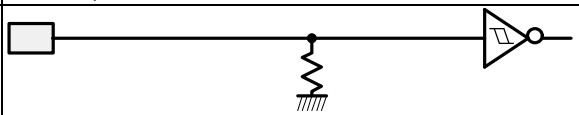
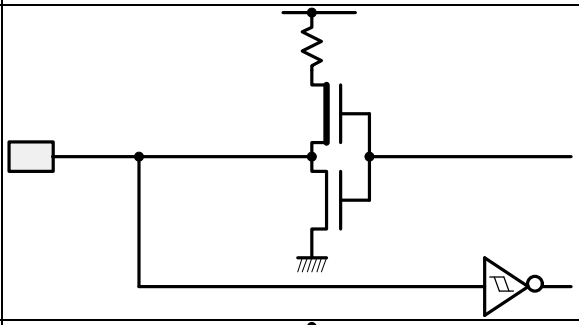
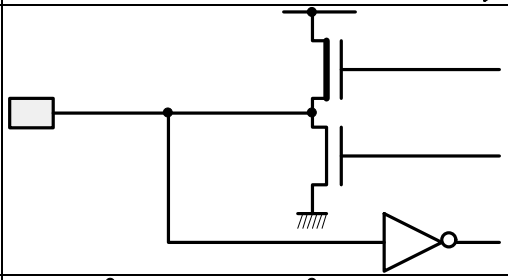
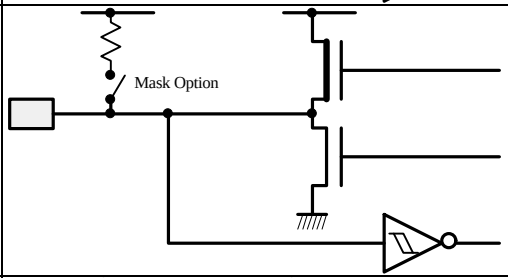
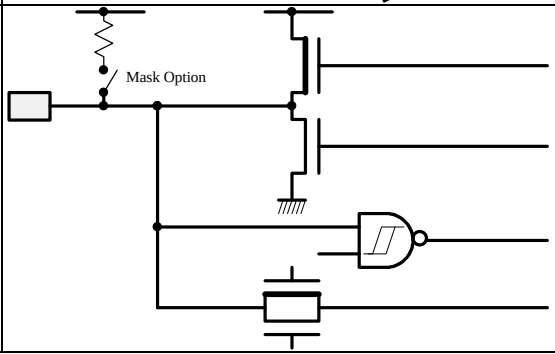


Preliminary information

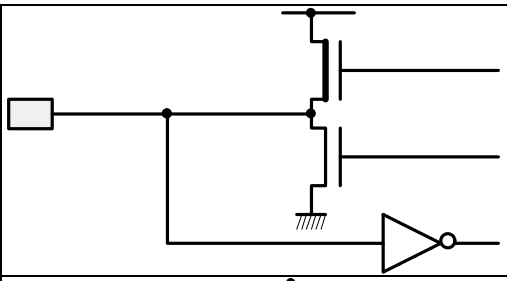
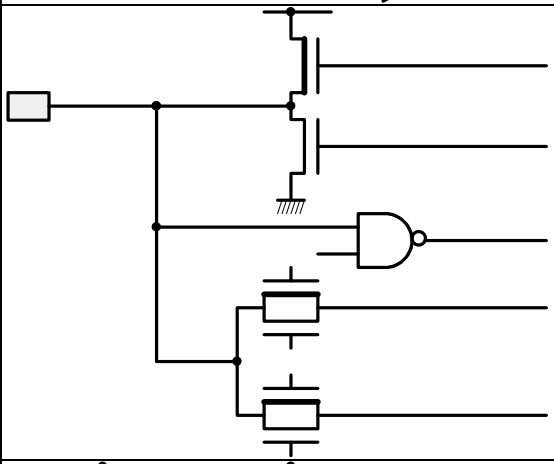
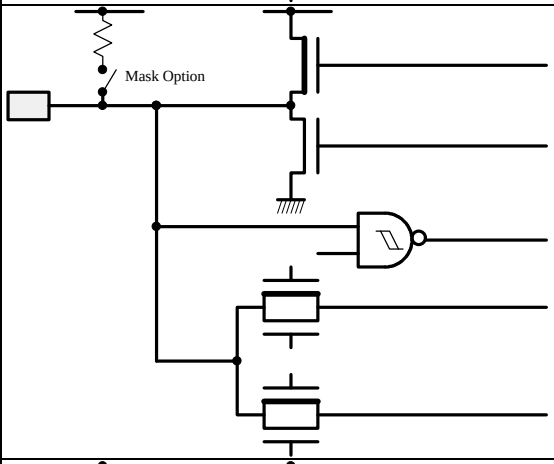
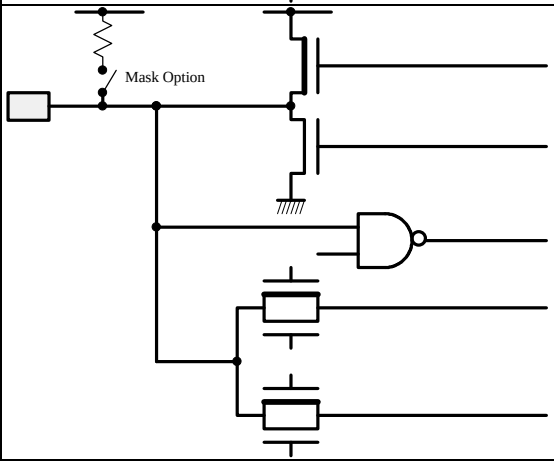
3.4 Pin function

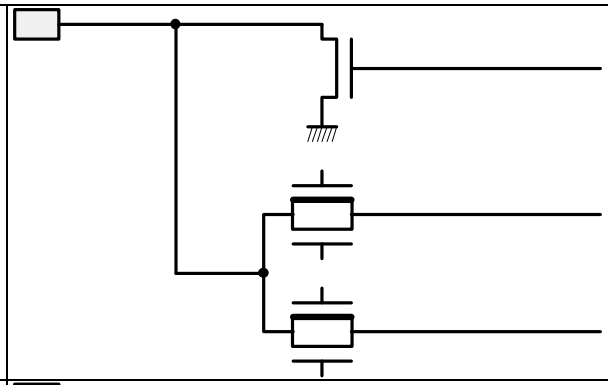
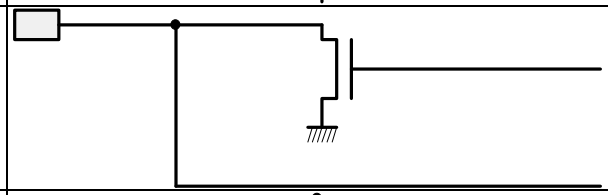
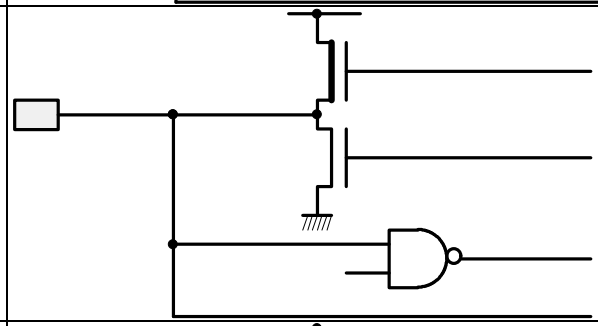
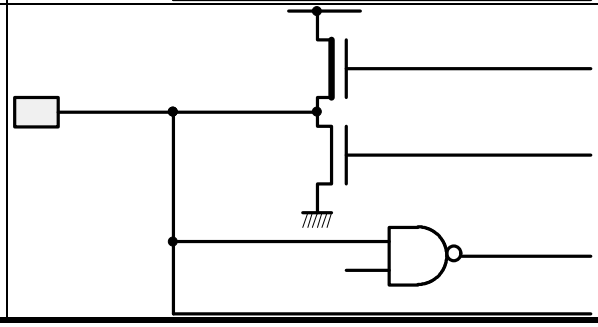
Pin Name	Circuit Type	Function
AVCC/AVSS		The power supply pins for the analog circuit. The same voltage should be applied as VCC/VSS.
XRST	C	Applying a reset pulse to this pin forces the MPU to enter the initial state. XRST is active low and drives low state when an internal reset occurs. Reset pulses of the duration less than the specified time may cause the MCU to enter undefined states.
FUELO/P30	D	This pin can be used for the bit 0 of Port 3 or the output from PWM3. The function of this pin can be switched by setting the internal register of PWM3.
TEMPO/P31	F	This pin can be used for the bit 1 of Port 3 or the output from PWM4. The function of this pin can be switched by setting the internal register of PWM4. This output has a high drive-current capability.
X0,X1	A	These pins are used for crystal oscillation. X0 and X1 can be directly connected to a crystal oscillator. When the oscillation clock is provided to X0 externally, X1 should be left open.
COM[3:0]/ P[44:41]	I	These pins are the LCD common signal outputs. When LCD is not used, these pins can be also used for Port 4.
P[27:25]/ INT[2:0]	E	These pins are used for Port 2. They can also be used for external interrupt inputs.
P24/V3	E’	This pin can be used as the bit 4 of Port 2 or an external LCD bias voltage input.
P23/TO/V2	E’	This pin can be used as the bit 3 of Port 2 or the output for the interval timer. Its function can be switched by setting the internal register of the interval timer. This pin can also be used for an external LCD bias voltage input.
P22/EC/V1	E’	This pin can be used as the bit 2 of Port 2 or the external clock input for the interval timer. This pin can also be used for an external LCD bias voltage input.
P21/V0	E’	This pin is the bit 1 of Port 2. This pin can also be used for an external LCD bias voltage input.

P20/SEG15	H	This pin can be used as the bit 0 of Port 2 or an LCD segment signal output by setting the internal register of the LCD controller.
P[10:17]/ SEG[08:15]	H'	These pins have two functions. Their functions can be switched between Port 1 and LCD segment signal outputs by setting the internal registers of the LCD controller.
P[00:07]/ SEG[00:07]	G	These pins have two functions. Their functions can be switched between Port 0 and LCD segment signal outputs by setting the internal registers of the LCD controller.
PWM1P/P32,PWM1M/ P33	F	These pins are the pair of high-current driver outputs for one of two motor coils. They can be also used for the bits 2 and 3 of Port 3 by setting the internal register of the stepper motor controller.
PWM2P/P34,PWM2M/ P35	F	These pins are the pair of high-current driver outputs for one of two motor coils. They can be also used for the bits 4 and 5 of Port 3 by setting the internal register of the stepper motor controller.
FUELI/P37	K	This analog input is connected to channel 0 of the A/D converter. It can also be used for the bit 7 of Port 3 when this A/D Input Enable register bit is set '0'.
TEMPI/P36	K	This analog input is connected to channel 1 of the A/D converter. It can also be used for the bit 6 of Port 3 when this A/D Input Enable register bit is set '0'.
P40/PW	J	This pin has two functions. When this pin is used as an open-drain output of Port 4, the Power Fail Detector should be in the power down mode. When it is used as the PW input of Power Fail Detector, the corresponding bit of the Port Data register should be set '1'.
VINT		An external capacitor should be connected to this pin for stabilizing the internal 3V power supply. For MB89PV940 and MB89P945, this pin should be left open.
MODE	B	The mode input is used for entering the MPU into the test mode. In user applications, MODE is connected to VSS.
VCC/VSS		VCC/VSS
DVCC/ DVSS		The dedicated power supply pins for the high-current driver outputs. The same voltage should be applied as VCC/VSS.

Type	Circuit	Remark
A		Oscillator input/output. With feedback resistor of approx. 2M ohm.
B		Schmitt-trigger input. (Pull-down resistance only for MB89943)
C		Open Drain output with pull-up resistor (Approx. 50K ohm). Schmitt-trigger input.
D		CMOS input/output.
E		CMOS input/output. (Schmitt trigger)
E’		CMOS input/output. (Schmitt trigger) External bias input

Preliminary information

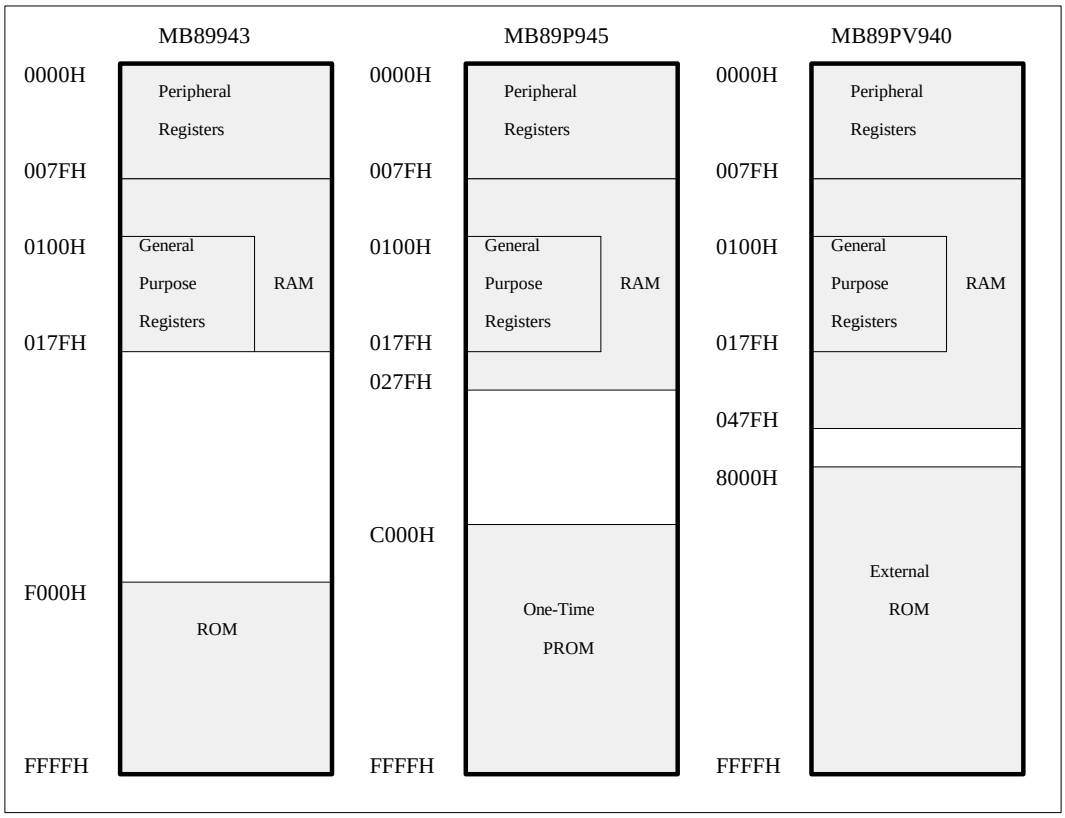
F		CMOS input/output. (High output current)
G		CMOS input/output. LCD driver output.
H		CMOS input/output. (Schmitt trigger) LCD driver output.
H’		CMOS input/output. (Schmitt trigger) LCD driver output. Pull-up options are not available for P11/SEG09 and P10/SEG08.

I		N-ch Open Drain output. LCD driver output.
J		N-ch Open Drain output. Analog input.
K		CMOS input/output. Analog input.
L		CMOS input/output. (High output current) Analog input.

4 CPU Architecture

4.1 Memory Space

The MB89940 Series has a memory space of 64K bytes. All peripheral registers, RAM and ROM areas are mapped onto the 0000H to FFFFH range. The peripheral registers address below 007FH and the RAM addresses range 0080H to 017FH (0080H to 027FH for MB89PV940 and 0080H to 0047FH for MB89P945). A part of this RAM area is also assigned as the general purpose registers. The ROM addresses above F000H. The One-Time PROM addresses the range above C000H. The external ROM for the piggy sample addresses the range above 8000H. The reset vector, interrupt vectors and vectors for vector-call instructions are stored in the highest addresses of the memory space.



■ Vector addresses

In the highest addresses of the ROM area, the reset vector and other information are stored. The table below shows these addresses.

Item	Upper byte address	Lower byte address
Reset Vector	FFFEH	FFFFH
Reset Mode📖	FFFCH (Unused)	FFFDH
Interrupt Level 0 Vector	FFFAH	FFFBH
Interrupt Level 1 Vector	FFF8H	FFF9H
Interrupt Level 2 Vector	FFF6H	FFF7H
Interrupt Level 3 Vector	FFF4H	FFF5H
Interrupt Level 4 Vector	FFF2H	FFF3H
Interrupt Level 5 Vector	FFF0H	FFF1H
Interrupt Level 6 Vector	FFEEH	FFEFH
Interrupt Level 7 Vector	FFECH	FFEDH
Interrupt Level 8 Vector	FFEAH	FFEBH
Interrupt Level 9 Vector	FFE8H	FFE9H
Interrupt Level 10 Vector	FFE6H	FFE7H
Interrupt Level 11 Vector	FFE4H	FFE5H
CALLV #7 Vector	FFCEH	FFCFH
CALLV #6 Vector	FFCCH	FFCDH
CALLV #5 Vector	FFCAH	FFCBH
CALLV #4 Vector	FFC8H	FFC9H
CALLV #3 Vector	FFC6H	FFC7H
CALLV #2 Vector	FFC4H	FFC5H
CALLV #1 Vector	FFC2H	FFC3H
CALLV #0 Vector	FFC0H	FFC1H

The Reset Mode data and Reset vector are used in the reset sequence. Refer to the section for more.

Interrupt Vectors are when an interrupt occurs. Refer to the section for more.

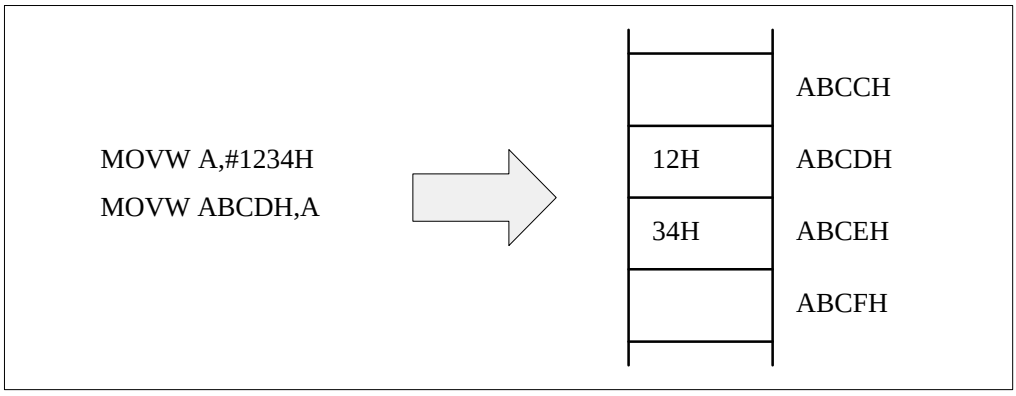
CALL Vectors are used for the vector call instructions. Details should be found in software documents.

📖 In user applications, the Reset Mode data should be 00H.

4.2 16-bit data alignment

The MB89940 Series supports a 2-byte data format and uses the Big-endian convention for storing 2-byte data. A 2-byte data is stored in two consecutive addresses of the memory space. The upper byte data is stored in the lower address and the lower byte data is stored in the higher address.

The same convention applies to the instruction coding. 16-bit extended address operands and 16-bit immediate data

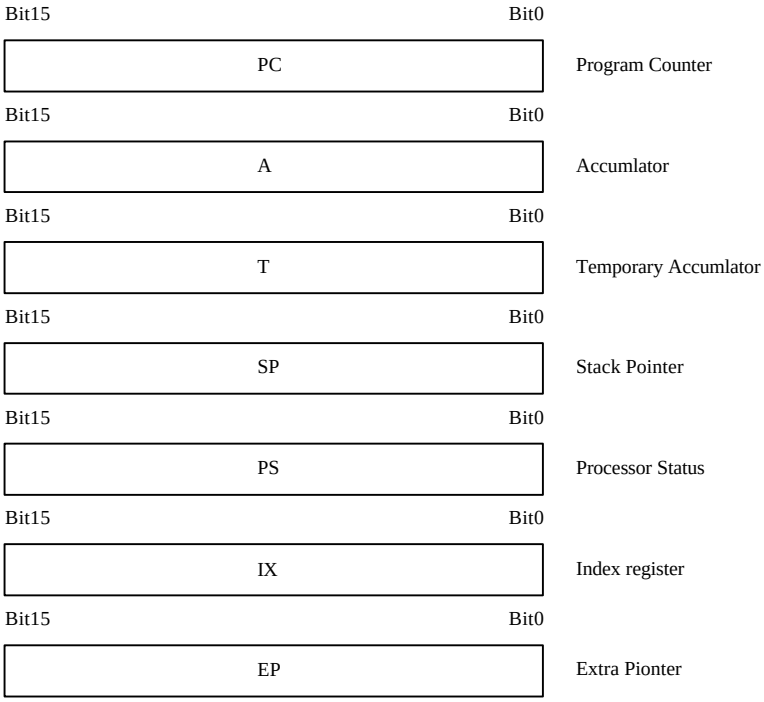


operands are treated in the same manner. Stack operations also follow the convention.

4.3 Internal Registers

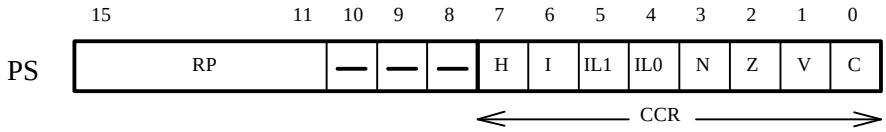
The MB89940 Series has a set of general purpose registers and application-specific registers. The general purpose registers reside in the RAM space with the size of 8-byte 16-bank. The application-specific registers consist of the following registers.

- Program Counter (PC)
  A 16-bit register storing the current instruction address.
- Accumulator (A)
  A 16-bit register for numeric operations. The Accumulator stores the result of the last numeric operation. One-byte operations only affect the lower byte of the Accumulator.
- Temporary Accumulator (T)
  A 16-bit register used for the numeric operations with the Accumulator. One-byte operations only use the lower byte of the Temporary Accumulator (TL). A transfer operation to the Accumulator automatically saves the existent data to the Temporary Accumulator. In the case of a one-byte transfer, the upper byte of the Temporary Accumulator (TH) remains unchanged.
- Stack Pointer (SP)
  A 16-bit register indicating the address for the top of the stack.
- Processor Status (PS)
  A 16-bit register storing the register bank pointer and processor status.
- Index register (IX)
  A 16-bit register used for the index addressing. The index addressing uses IX in conjunction with a one-byte offset. The target address is the sum of the content of IX and the offset.
- Extra Pointer (EP)
  A 16-bit register used for the pointer addressing. EP indicates the target address for the pointer addressing instructions.



4.3.1 Processor Status register (PS)

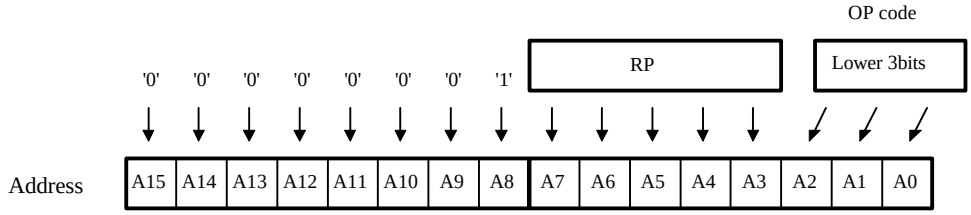
PS comprises the register bank pointer (RP) and the condition code register (CCR)



Default value : XXXXXXXX X011XXXXB

- Register Bank Pointer

  RP stores the pointer to the current bank of the general purpose registers. The address of the target register is generated by combining the content of RP and the lower three bits of the operation code.



- H flag (Half carry)

  When the H flag is set, it indicates that a carry or a borrow is occurred between bit 3 and bit 4 as a result of a numeric operation. Otherwise this flag is reset. The H flag is used for the decimal-correction instructions.

- I flag (Interrupt enable)

  If the I flag is set, interrupt operations are enabled. If it is reset, the CPU does not accept interrupt requests.

- IL1 and IL0 (Interrupt priority)

  IL1 and IL0 indicate the level of the currently-enabled interrupt priority. The CPU accepts the interrupt requests with the priority higher than the setting of these bits.

IL1	IL0	Interrupt Priority
0	0	Higher
0	1	
1	0	Lower
1	1	Interrupt disabled

- N flag (Negative)

  If a numeric operation results in setting the most significant bit, the N flag is set. Otherwise it is reset.

- Z flag (Zero)

  If a numeric operation results in zero, the Z flag is set. Otherwise it is reset.

- V flag (Two's complement overflow)

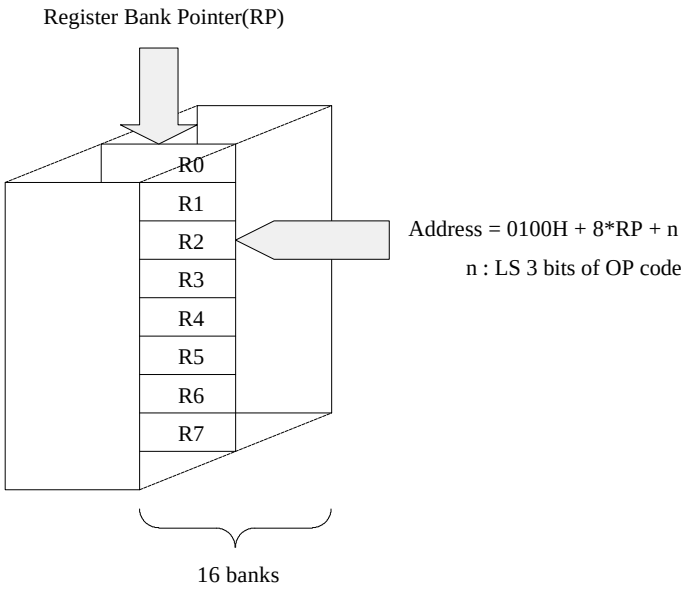
  When a two's complement overflow is occurred as a result of a numeric operation, the V flag is set. Otherwise it is reset.

- C flag (Carry)

  When a carry/borrow from/into bit 7 is occurred, the C flag is set. Refer to software documents for more.

4.3.2 General Purpose registers

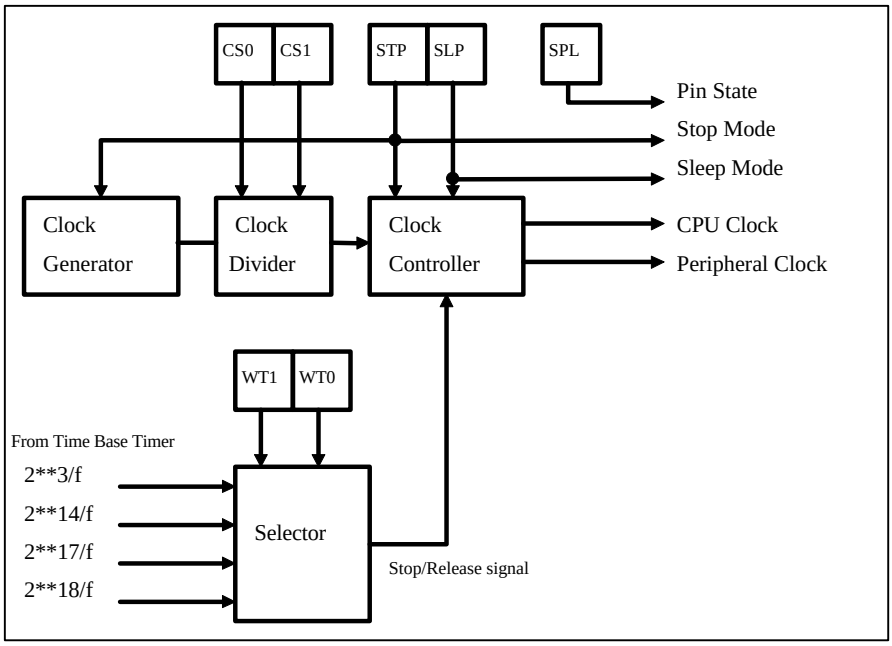
The MB89940 Series has a set of 8-bit 8-word 16-bank general purpose registers. These general purpose registers are located in the RAM area. The register bank pointer indicates the current register bank.



4.4 Clock Controller

The Clock Controller supervises the operation modes of the MCU and provides the system clock and reset signal.

■ Block Diagram



4.5 System Clock Control register

System Clock Control

Address 0007H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	—	WT1	WT0		CS1	CS0
			R/W	R/W		R/W	R/W

Default value XXXMM100B M: Mask option(11 for Piggy)

*Important : Bit 2 must always be set to '1'

By setting the WT1 and WT0 bits of the System Clock Control register, Oscillation Stabilization Time can be selected between four choices. This stabilization time is the wait cycles required for stabilizing the clock oscillation after the power-on. The default value for these bits is selected by user option.

WT1,WT0	Stabilization time (f_{osc} : Oscillation frequency)	Stabilization time with 8MHz oscillation
11	Approx. 2**18/f_{osc}	Approx. 32.8ms
10	Approx. 2**17/f_{osc}	Approx. 16.4ms
01	Approx. 2**14/f_{osc}	Approx. 2.0ms
00	Approx. 2**3/f_{osc}	Approx. 0ms

The CS1 and CS0 bits determine the divide number for the clock divider. The system clock frequency can be changed by setting these bits. The system clock frequency is the oscillation clock frequency times the selected divide number. One instruction cycle consists of two system clock cycles.

CS1,CS0	Divide number	System Clock	Instruction Cycle
11	1/2	f_{osc}*1/2	1/(f_{osc}*1/4)
10	1/4	f_{osc}*1/4	1/(f_{osc}*1/8)
01	1/8	f_{osc}*1/8	1/(f_{osc}*1/16)
00	1/32	f_{osc}*1/32	1/(f_{osc}*1/64)

f_{osc} : Oscillation clock frequency

4.6 Standby Control register

Standby Control

Address 0008H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STP	SLP	SPL	RST		—	—	—
W	W	R/W	W				

Default value 00010XXXB

*Important : Bit 3 must always be set to '0'

The•@STP bit switches the MPU into the Stop mode when it is set. This bit is reset upon a system reset or an external interrupt request. Reading this bit always returns ‘0’. See also the following section for more.

The SLP bit switches the MPU into the Sleep mode. This bit is reset upon a system reset or an interrupt request. Reading this bit always returns ‘0’. See also the following section for more.

The SPL bit used for specifying the external pin state in the Stop mode. If it is set, the external pins go into high-impedance state in the Stop mode. Otherwise the external pins maintain the last states before entering the Stop mode. This bit is reset at system reset.

The RST bit is for generating the software reset. When it is reset, the Clock Control block generates a 4-instruction-cycle reset pulse. Reading this bit always returns ‘1’.

4.7 Operation Mode summary

The MB89940 Series has three operation modes for reducing its power dissipation. In the Run mode the CPU and other peripheral blocks operate normally. In the Sleep mode, the Clock Controller stops providing the CPU clock however the other peripheral blocks continue their operations. In the Stop mode, the MCU only maintains the data stored and the clock oscillation is stopped.

Mode	Clock Generator	CPU	Time Base Timer	Peripheral Blocks	Wake-up source
Run	Oscillation	Operation	Operation	Operation	N/A
Sleep	Oscillation	Stop	Operation	Operation	Interrupt
Stop	Stop	Stop	Stop	Stop	External interrupt

- Sleep mode

  Writing '1' in the SLP bit forces the MPU to enter the Sleep mode. If a write '1' to the SLP bit is performed while an interrupt request is awaiting for the acceptance(to clear the interrupt flag of the source block), the MPU will not enter the Sleep mode and the SLP bit will not be changed. In the Sleep mode, various registers and the RAM maintain their states.

  When a reset or an interrupt request is occurred, the MPU resumes to the Run mode. Any interrupt request with the level higher than 3(IL1,IL0='11') awakes the MPU regardless of the settings of the I, IL1 and IL0 bits of the Processor Status register. If this interrupt request is disabled by these settings, the CPU starts processing the main routine.

- Stop mode

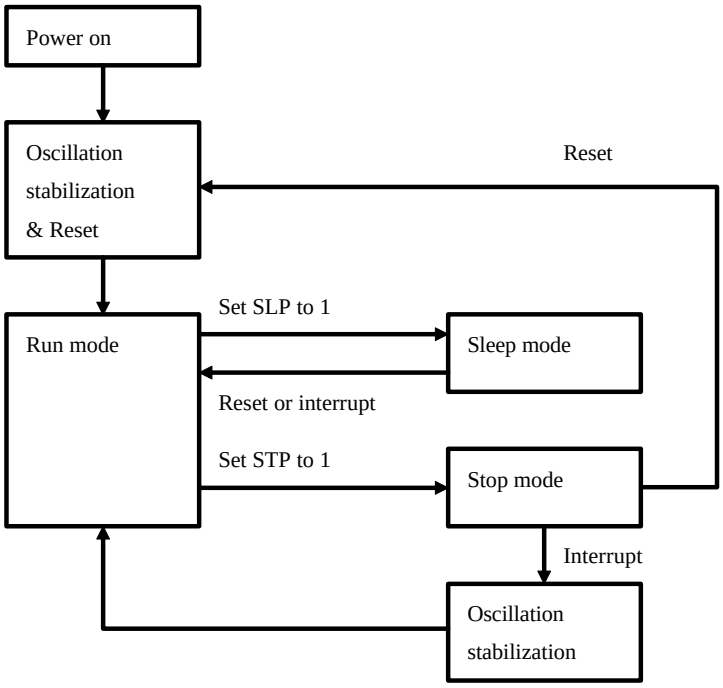
  Writing '1' to the STP bit forces the MPU to enter the Stop mode. In Stop mode, all the external outputs maintain their states or switch to high impedance states(or weak high states for those pins with pull-up options) depending on the setting of the SPL bit. If a write '1' to the STP bit is performed while an interrupt request is awaiting for the acceptance(to clear the interrupt flag of the source block), the MPU will not enter the Stop mode and the STP bit will not be changed. Before entering the Stop mode, the interrupt enable bit of the Time Base Timer should be reset to avoid any unexpected interrupt after resuming back to the Run mode.

  If a reset or an external interrupt is occurred in the Stop mode, the MPU resumes to the Run mode. While this mode transition, there will be an oscillation stabilization time before the CPU starts its operation.

  Since the clock signal is not provided to the peripheral blocks in the Stop mode, there will not be any interrupt request from those blocks. If the interrupt request which caused a mode transition is disabled by the setting of the processor status register, the CPU starts processing the main routine.

  The mode transition from Stop to Run may cause unstable operations of the peripheral blocks.

This is because they re-start from a mid-operation state. Therefor it is generally recommended that all the blocks are once initialized.



4.8 Interrupt Controller

The Interrupt Controller supports up to 12 levels of interrupt requests. Each interrupt level is assigned one of the three levels of the interrupt priority and this can be done by software. When a peripheral block signals an interrupt request, the Interrupt Controller diverts the request to the CPU in accordance with the setting of the ILR registers then generates the interrupt vector address. If more than two requests occur simultaneously, the request with the higher interrupt priority will be handled first. In case of simultaneous interrupts with the same interrupt priority, the lower interrupt level will have higher priority (IRQ0 has the highest priority).

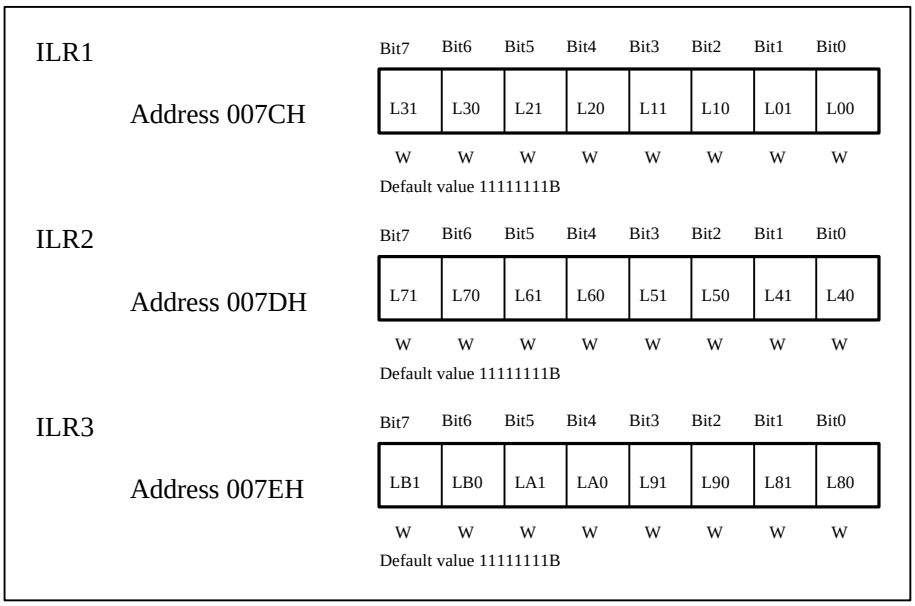
4.8.1 Interrupt Level Summary

Level	Peripheral	Interrupt Priority Setting in ILR	Vector Address	
			Upper byte	Lower byte
IRQ0	External interrupt (INT0)	L01,L00	FFFAH	FFFBH
IRQ1	External interrupt (INT1)	L11,L10	FFF8H	FFF9H
IRQ2	External interrupt (INT2)	L21,L20	FFF6H	FFF7H
IRQ3	Reserved for device test.	L31,L30	FFF4H	FFF5H
IRQ4	Low Supply Voltage	L41,L40	FFF2H	FFF3H
IRQ5	Interval Timer	L51,L50	FFF0H	FFF1H
IRQ6	Reserved	L61,L60	FFEEH	FFEFH
IRQ7	Time Base Timer	L71,L70	FFECH	FFEDH
IRQ8	PWM3 Timer	L81,L80	FFEAH	FFEBH
IRQ9	PWM4 Timer	L91,L90	FFE8H	FFE9H
IRQA	A/D Converter	LA1,LA0	FFE6H	FFE7H
IRQB	Unused	LB1,LB0	FFE4H	FFE5H

4.8.2 ILR Registers

The ILR registers store the interrupt priority setting for the all interrupt levels. Every two bits are assigned for specifying the interrupt priority of the corresponding interrupt request level. When the interrupt controller diverts a interrupt signal to the core CPU, it also passes this interrupt priority data. The CPU compare the received interrupt priority with the priority setting in the Processor Status register to determine whether to accept the request.

Any bit operation (i.e. SET bit, CLR bit instructions) can not be performed on the ILR registers.



LB1-L01	LB0-L00	Interrupt Priority
0	X	1 (Higher)
1	0	2 (Lower)
1	1	3 (Interrupt Disabled)

When Lx1 and Lx0 are set to '11', the corresponding interrupt request will not be passed to the CPU.

4.8.3 Interrupt Service sequence

A. After the MPU is reset, all the interrupt requests are disabled. To enable the interrupt operation, the peripheral block, Processor Status register and ILR register should be set to the appropriate value.

B. Upon an interrupt request from the peripheral block, the Interrupt Controller handles the request in the described manner.

C. The CPU then compares the received interrupt priority with the IL1 and IL0 bits and checks the I flag in the Processor Status register(PS). If the I flag is set and interrupt priority is higher than the setting of IL1 and IL0, the CPU then accept the request.

D. The CPU pushes the contents of the Program Counter(PC) and PS onto the stack then stores the interrupt vector address to the PC.

E. The CPU also changes the contents of IL1 and IL0 in the PS to the accepted interrupt priority. Therefor further interrupt request with the priority lower-than/equal-to the current interrupt priority will not be accepted.

F. When the CPU returns to the main routine by the RETI instruction, the contents of the PC and PS is restored from the stack. Before returning to the main routine, the interrupt flag of the current interrupt source should be reset.

4.8.4 Multiple interrupt

A multiple interrupt (interrupt in interrupt routine) can be performed if a further interrupt request has the higher priority than the current interrupt priority.

i.e. The CPU accepts the interrupt request of the priority-1 when a priority-2 interrupt routine is under execution.

4.8.5 Interrupt Acknowledge Time

The CPU requires nine instruction cycles as the interrupt acknowledge time. During this period, the CPU performs the following operations.

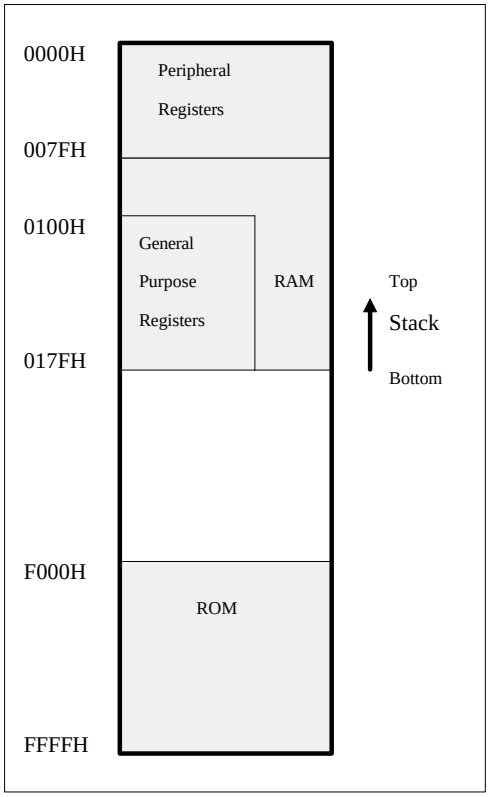
- Pushes PC and PS to the stack
- Stores Vector Address to PC
- Changes IL1 and IL0 in PS to the current priority

It should be noted that the CPU recognizes a presence of an interrupt request at the end of the last instruction execution. Thus the time period between an interrupt event and the execution of the first interrupt instruction will be longer than 9 instruction cycles.

For example, the divide instruction (DIVU) requires 21 instruction cycles. If this instruction is under its process while an interrupt request is awaiting, it takes 30 instruction cycles (9 + 21 cycles) before the CPU starts the first interrupt instruction at worst.

4.9 Stack Operation

The Subroutine Call instructions, Vector Call instructions, Push/Pop instructions and interrupt service perform stack operation. The stack area is located in the internal RAM. The Stack Pointer points to the top item in the stack and it is automatically decremented/ incremented by the stack operation. It is generally recommended to set the bottom address of the stack to the highest address of the RAM area.



4.10 Time Base Timer

The Time Base Timer (TBT) periodically signals an interrupt request. It consists of a 21-bit free-run timer counter and TBTC register. The timer counter operates with the 1/2 oscillation clock and it also provides interval signals for the Clock Controller, Watchdog Timer and other peripheral blocks.

4.10.1 TBTC Register

TBTC

Address 000AH

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBOF	TBIE	—	—	—	TBC1	TBC0	TBR
R/W	R/W				R/W	R/W	W

Default value 00XXX000B

The TBOF bit is the counter overflow flag. This bit is set when the counter overflow at the specified bit of the timer counter occurs. The TBC1 and TBC0 specify this overflow bit(See table below). The TBIE bit is the interrupt enable bit. The TBT generates an interrupt request, if TBIE is '1' and TBOF is set by the counter overflow. Prior to setting the TBIE bit, it is recommended to reset the TBOF bit. Writing '0' to the TBR bit clears the timer counter.

TBC1	TBC0	Overflow Bit	Overflow Interval
0	0	Bit 12	2**13/f_{osc}
0	1	Bit 14	2**15/f_{osc}
1	0	Bit 17	2**18/f_{osc}
1	1	Bit 21	2**22/f_{osc}

f_{osc} = Oscillation frequency

Writing '0' to the TBOF resets this bit. Writing '1' to the TBOF and TBR has no effect. Reading the TBR bit always returns '1'. Any Read-Modify-Write operation performed on the TBOF bit always results in reading '1'.

4.10.2 Time Base Timer Operation

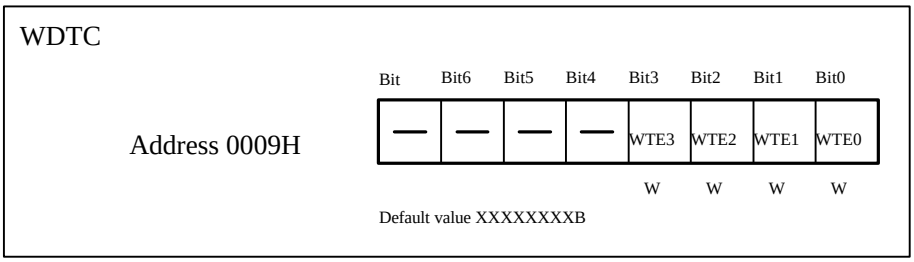
The timer counter in the TBT continues count-up operation as long as the oscillation clock is supplied. This count-up operation starts from '0' after the counter is reset by the TBR bit, Power On Reset or by the mode transition from Run to Stop. The periodical interrupt request occurs on this time basis and other peripheral blocks (i.e. Clock Controller, Watchdog Timer, Low Supply Voltage Reset and Power Fail Detector) use time interval signals from this timer counter.

Note that if the specified overflow interval is shorter than the Oscillation Stabilization Time specified by the System Clock Control register, the TBT will generate an interrupt request while the MPU is resuming from Stop mode to Run mode with the stabilization time. Therefore the TBIE bit should be reset before entering the Stop mode.

4.11 Watchdog Timer

The Watchdog Timer helps prevent the CPU entering the finite loop. Once the operation of the Watchdog Timer is started, the CPU must keep clearing the timer periodically. If the CPU fails to clear the timer within the predetermined interval, the Watchdog Timer generates a reset pulse for 4 instruction cycles. Since the Watchdog Timer uses the interval signal from the Time Base Timer, this reset interval varies depending on the timing (relative to the interval signal) when the Watchdog Timer is cleared. The table below shows the range of the reset interval.

Watchdog Timer	Reset interval from Watchdog Timer clear
Minimum Time	2**22/f_{osc}
Maximum Time	2*2**22/f_{osc}



The WDTC register is used to start and clear the Watchdog Timer. Once the Watchdog Timer is started, it can be stopped only by the MPU reset. Writing ‘XXXX0101’ in the WDTC register starts/clears the Watchdog Timer.

WTE3/WTE2/WTE1/WTE0	Operation
0101	For the first write after the reset, the Watchdog Timer starts its operation. For the second and later writes, the Watchdog Timer is cleared.

Note that clearing the Time Base Timer and the mode transitions to Stop and Sleep mode also clear the Watchdog Timer.

4.12 MPU Reset

There are five types of reset source. When one of the five sources generates a reset pulse, the MPU initializes the contents of the registers and performs the Mode Data fetch (Address FFFDH) and then Reset Vector fetch (Address FFFE/FFFFH). The Mode Data is used for describing the operation mode of the MPU. However this data should be 00H for user applications. The Reset Vector indicates the location of the first user instruction. Note that the oscillation stabilization time will be taken for Power On Reset and External Reset with the Power On Reset option activated.

Reset source		Oscillation stabilization time	Duration of reset output (Optional)
Power On Reset (Optional)		Yes	Oscillation stabilization time (+ Regulator stabilization time for MB89943)
Software Reset		No	4 instruction cycles
Watchdog Reset		No	4 instruction cycles
External Reset	With Power On Reset option	Yes	Oscillation stabilization time
	Without Power On Reset option	No	No output
Low Supply Voltage Reset	With Power On Reset option	Yes	Oscillation stabilization time
	Without Power On Reset option	No	No output

Important notes

- Clock signal is required for the initialization of the MPU.
- If the Power On Reset option is not activated, the External Reset does not invoke the oscillation stabilization time. Therefor the reset signal must be kept asserted until the oscillation is stabilized.
- The reset operation may collapse the content of the internal RAM if it is performed while a two-byte write is under execution. In this case, the upper byte will be written correctly however the lower byte write may be incomplete.
- To initialize the MPU after the power-on, the profile of the power supply voltage should follow the DC/AC specification. Refer to section 0.
- For MB89P945, the external reset signal must be applied for correct initialization when power-on.

4.13 External Interrupt

The MB89940 Series supports three levels of edge-sensitive externally-triggered interrupts. These interrupts can be enabled/disabled by the External Interrupt registers. The INT[2:0] pins are used for the trigger sources for the IRQ[2:0] interrupt requests respectively.

4.13.1 External Interrupt Control registers

The External Interrupt Control registers select the polarity of the trigger transitions and enable/disable the interrupt request signals.

External Interrupt Control 1

Address 002FH

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EIR1	—	SEL1	EIE1	EIR0	—	SEL0	EIE0
R/W		R/W	R/W	R/W		R/W	R/W

Default value XX00XX00B

External Interrupt Control 2

Address 0030H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	—			EIR2	—	SEL2	EIE2
R/W		R/W	R/W	R/W		R/W	R/W

Default value XXX0XX00B

Bit 4 should always be set to '0'.

- EIE bits

  EIE0 through EIE2 are the interrupt enable flags for IRQ0 through IRQ2 respectively. When they are set to '1', interrupt requests are generated upon external events. Otherwise the external interrupt requests are disabled. It is recommended to clear the interrupt flag (EIR bit) prior to enabling the external interrupt.

  In STOP mode, EIE bits also disable the input buffer in order to reduce the leakage current. Therefor the interrupt flag (EIR bit) is not affected by external event in STOP mode if the EIE bit is set to '0'.

- SEL bits

  SEL0 through SEL2 specify the polarities of the trigger transition for IRQ0 through IRQ2 respectively. When they are set to '1', the transition from a logic high to a logic low is selected as the trigger source. Otherwise low-to-high transition is selected.

- EIR bits

  EIR0 through EIR2 are the interrupt flags for IRQ0 through IRQ2 respectively. The external event specified by the SEL bit sets the flag except•@when the EIE bit is '0' in STOP mode. When the EIE bit is set and the EIR bit is set, an interrupt request occurs. Writing '0' into these bits clears the flags. Writing '1' into these bits do not have any effect. Any read-modify-write operation to the EIR bit always results in reading '1'.

5 Stepper Motor Controller

The Stepper Motor Controller consists of two PWM Pulse Generators, four motor drivers and Selector Logic. The four motor drivers have high output drive capabilities and they can be directly connected to the four ends of two motor coils. The combination of the PWM Pulse Generators and Selector Logic is designed to control the operation of the motor rotor. A synchronization mechanism assures the synchronous operations of the two PWMs.

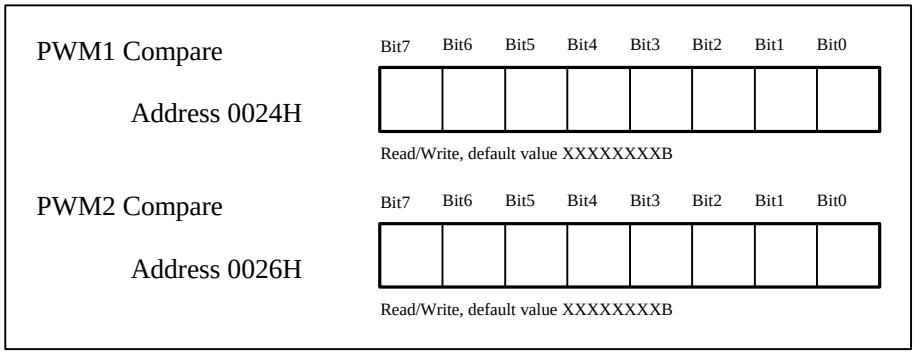
5.1 PWM Pulse Generators

The two PWM Pulse Generators generate 8-bit precision PWM pulses. Each generator provides PWM pulses for each one of two motor coils. (PWM1 can be connected to either PWM1P or PWM1M outputs. PWM2 can be connected to either PWM2P or PWM2M outputs. The Selector Logic switches these connections. See also section 0)

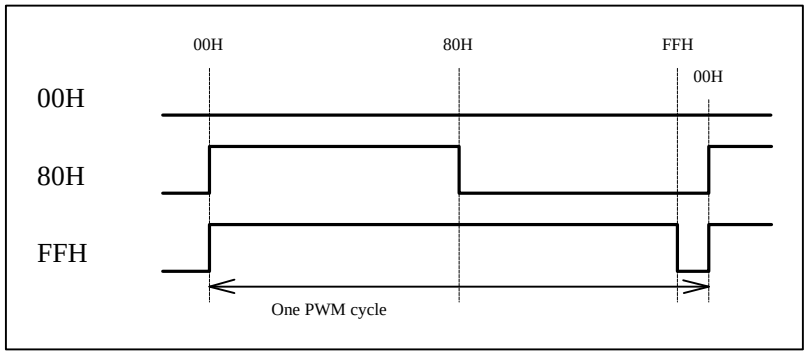
- Compare registers

  The contents of the two 8-bit Compare registers determine the widths of the PWM pulses.

  The stored value of 00H represents the PWM duty of 0% and FFH represents the duty of 99.6%. The



  registers are accessible at any time, however the duty stays unchanged until the BS bit of PWM2 Select register is set and the PWM generator completes the current PWM cycle. (See also section 0)



- Control register

  There is a 8-bit register for controlling the operation of the two PWM generators. By setting the P0 and P1 bits of this register, the operational clock can be selectively chosen between four different clock sources. One PWM cycle equals to 256 times the operational clock cycle. The OE bit switches the

functions of the external pins. When it is set to ‘1’, the external pins are used for the Stepper Motor Controller. Otherwise they are used as general purpose IO. OE1 switches PWM1 outputs and OE2 switches PWM2 outputs.

The CE bit starts/stops the operation of the PWM counter for PWM1 and PWM2. When this bit is set to ‘1’, the counter starts counting from ‘00H’. When it is reset, the counter stops. To help reduce switching noise from the PWM driver outputs, the output timing of PWM2 generator is delayed by one System Clock cycle from the PWM1 timing.

PWM Control

Address 0023H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OE2	OE1	P1	P0	CE	—	—	TST
R/W	R/W	R/W	R/W	R/W			R/W

Read/Write, default value 00000XX0B

Important :The TST bit should always be '0'

P1,P0	Operational Clock
00	System Clock
01	1/2 System Clock
10	1/4 System Clock
11	1/8 System Clock

5.2 Selector Logic

The Selector Logic controls the output of the motor drivers. The output signal can be switched between 0,1,PWM pulses and Hi-impedance state.

- Select registers

  By setting the contents of the Select registers, the outputs of the motor drivers can be switched between the four choices. P2, P1, P0, M2, M1 and M0 are used for this purpose.

  The BS bit has a special function. Only when the BS bit is set to '1', the modified settings in PWM1/PWM2 Compare and PWM1/PWM2 Select registers take effect at the end of the current PWM cycle. As long as the BS bit is reset, the changes of these settings do not have any effect. At the beginning of the next PWM cycle, the BS bit is reset automatically. A write operation to the BS bit cancels this reset operation if they occurs simultaneously.

PWM1 Select

Address 0027H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	P2	P1	P0	M2	M1	M0
		R/W	R/W	R/W	R/W	R/W	R/W

Default value XX000000B

PWM2 Select

Address 0028H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	BS	P2	P1	P0	M2	M1	M0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value X0000000B

P2,P1,P0	PWMnP output	M2,M1,M0	PWMnM output
000	L	000	L
001	H	001	H
01X	PWM pulses	01X	PWM pulses
1XX	High impedance	1XX	High impedance

Selector Test

Address 002DH

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value 00000010B

Important : This register is used only for device test

Important : Stored value should always be '02H'

6 Low Supply Voltage Interrupt

The Low Supply Voltage Interrupt controller compares the input voltage at the PW pin with its reference voltage. When the input voltage drops lower than the reference voltage, the controller signals an interrupt request to the core CPU.

6.1 Power Fail Control register

Power Fail Control

Address 002EH

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PD	—	—	TST	—	MS	INT	—
R/W			R/W		R/W	R/W	

Default value 1XX0X00XB

Important : The TST bit should always be '0'

Important : The TST bit is Read-Only for MB89PV940

The Power Fail Control register controls the operation of the Low Supply Voltage Interrupt controller.

When the PD bit is set to ‘1’, the controller goes into a low power state and its operation is stopped. Before entering Stop mode this bit must be set to ‘1’.

When the PD bit is reset to ‘0’, the controller starts its operation after a lead time. During this lead time, it does not sense the input voltage.

Lead time	Minimum	Maximum
	1.5*2**10/fosc	3.5*2**10/fosc

The INT bit is the interrupt flag. This bit is set when the controller detects the lower voltage at the input. Writing 0 to INT resets the flag and any read-modify-write operation performed this bit always results in reading ‘1’. The MS bit is the interrupt enable flag. When MS is ‘1’ and INT is set to ‘1’, the block signals an interrupt request.

The TST bit is used for device test. In user applications, this bit should always be set to ‘0’. The Read-Modify-Write instructions return ‘0’. For MB89PV940, it is recommended not to perform any Read-Modify-Write instructions on this register.

6.2 Band Gap Reference

The Band Gap Reference generates the reference voltage for the comparator in the Low Supply Voltage Interrupt controller. The comparator compares the input voltage at the PW pin with the reference voltage.

Reference Voltage	1.28V +/- 0.1V

7 IO port

MB89940 Series has four 8-bit general purpose IO ports. These ports share external pins with peripheral blocks with some exceptions. Those pin functions are switched by setting the internal registers of the peripheral blocks. Each port has its own data register and direction register for data transfer. When a shared pin is used as an input of a peripheral block, the port direction should be set as an input (inward) to cut off the output buffer of the port.

7.1 Port registers

Each port has an 8-bit Data register and an 8-bit Data Direction register except for Port4. The Data registers store the output data. The Data Direction registers specify the directions of the ports. The setting of the port directions can be made bit by bit. Therefore inputs and outputs can coexist in the same 8-bit port. A port pin serves as an output when the corresponding bit of the Data Direction register is set to '1'.

Port 4 has five open drain outputs. This port can not be used as inputs and it only has a 5-bit Data register.

Port 3 A/D Input Enable register is for disengaging the port function when the external pins are used for the A/D converter.

Register	Read/Write	Address	Default value
Port 0 Data register	Read/Write	0000H	XXXXXXXXB
Port 0 Data Direction register	Write	0001H	00000000B
Port 1 Data register	Read/Write	0002H	XXXXXXXXB
Port 1 Data Direction register	Write	0003H	00000000B
Port 2 Data register	Read/Write	000CH	00000000B
Port 2 Data Direction register	Write	000DH	00000000B
Port 3 Data register	Read/Write	000EH	XXXXXXXXB
Port 3 Data Direction register	Write	000FH	00000000B
Port 4 Data register	Read/Write	0010H	XXX11111B
Port 3 A/D Input Enable register	Read/Write	0011H	XXXXXX00B

7.2 Port access operation

- Output operation

  When a port pin is specified as an output, the corresponding bit of the Data register is output to the pin. A read access to the Data register reads the value at the port pin.

- Input operation

  When a port pin is specified as an input, the output buffer is cut off and the value at the pin is read by read access to the Data register. A write access to the Data register updates the content.

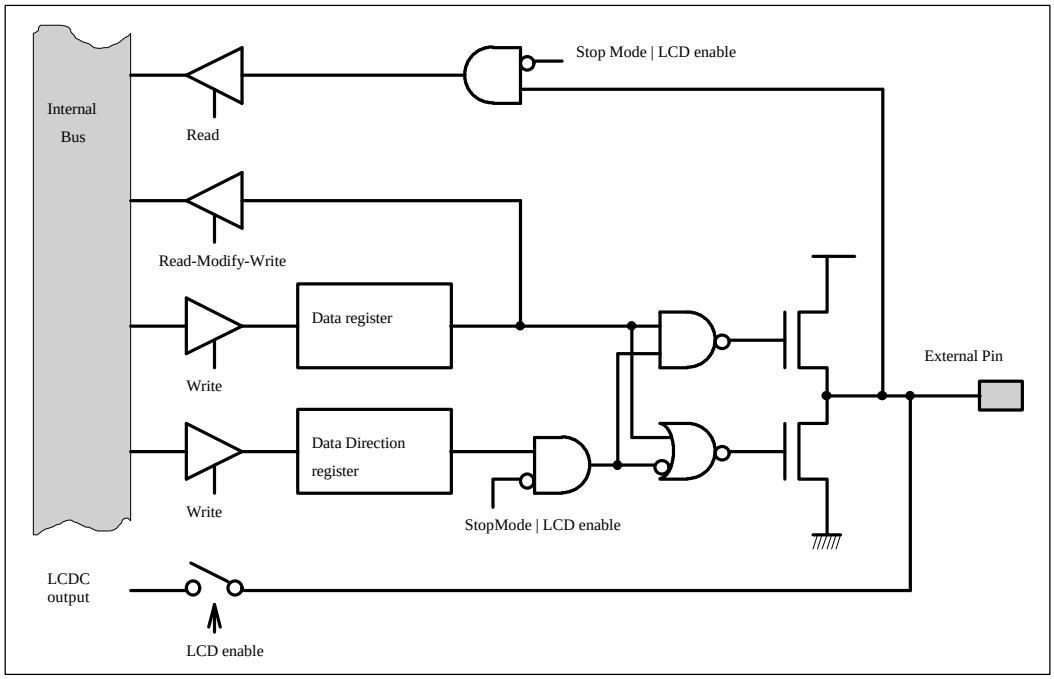
- Read-Modify-Write operation

  Any read-modify-write access to the Data register reads the content of the register regardless of the setting of the Data Direction register. (Even if port pins are specified as inputs)

  Logical operations and Bit operations perform read-modify-write access.

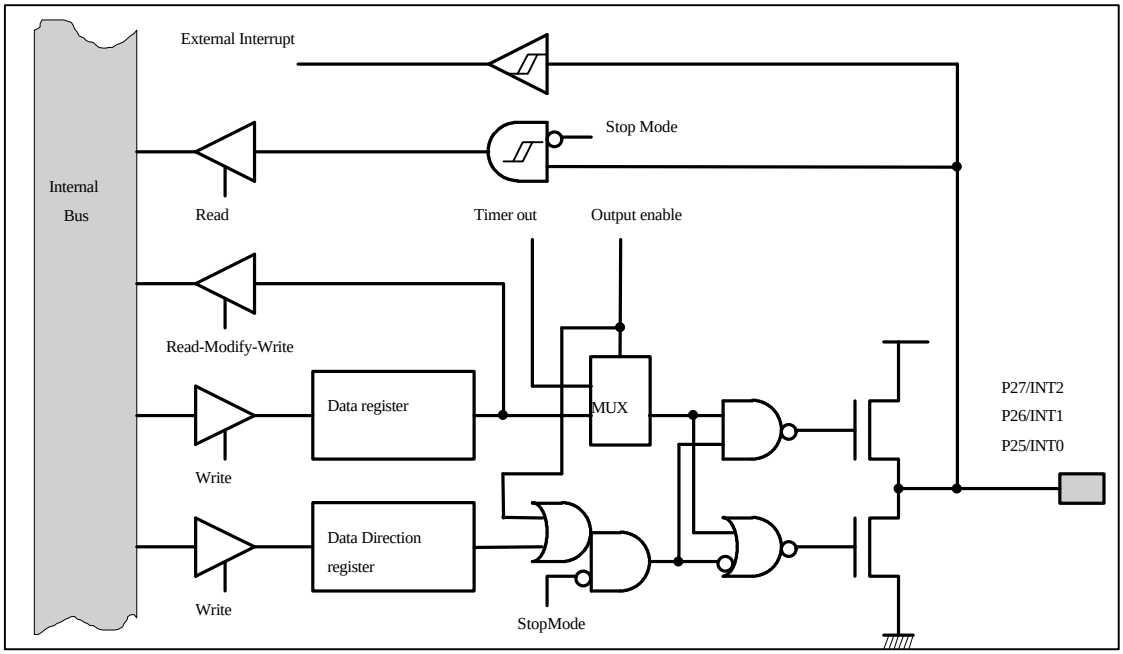
7.3 Port 0 and Port 1

Port 0 and Port 1 share their external pins with the LCD Driver/Controller. When LCD common/segment outputs are disabled, these pins are used for Port 0 and Port 1. Pull-up options are available for Port 1.

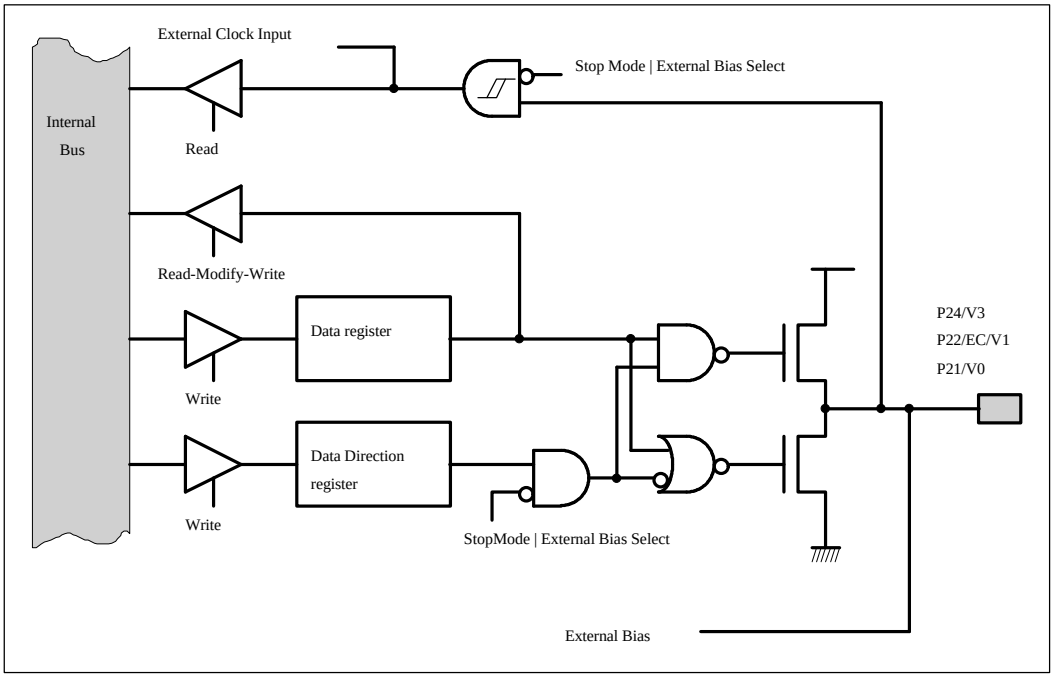


7.4 Port 2

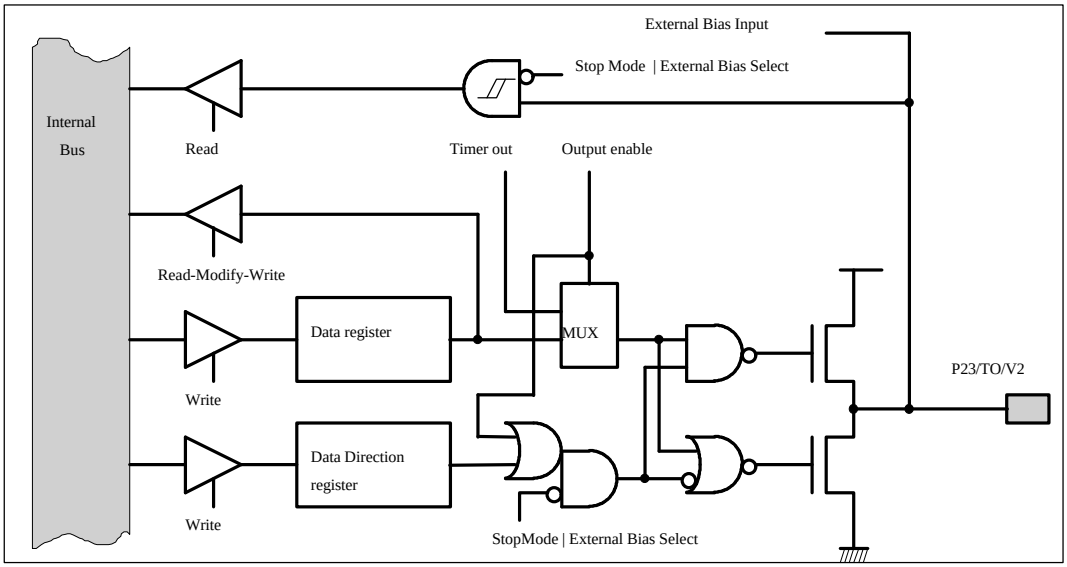
The bit 5 through 7 of Port 2 share their external pins with external interrupt inputs. When they are used for the port function, these external interrupt should be disabled.



The bit 2 of Port 2 shares its pin with the external clock input of the interval timer. When this pin is used for the timer, the corresponding bit of Data Direction register should be set inward (to '0').



The bit 3 of Port 2 shares its pin with the output from the interval timer. When the timer is configured to use this pin, the port function is disengaged from the external pin.



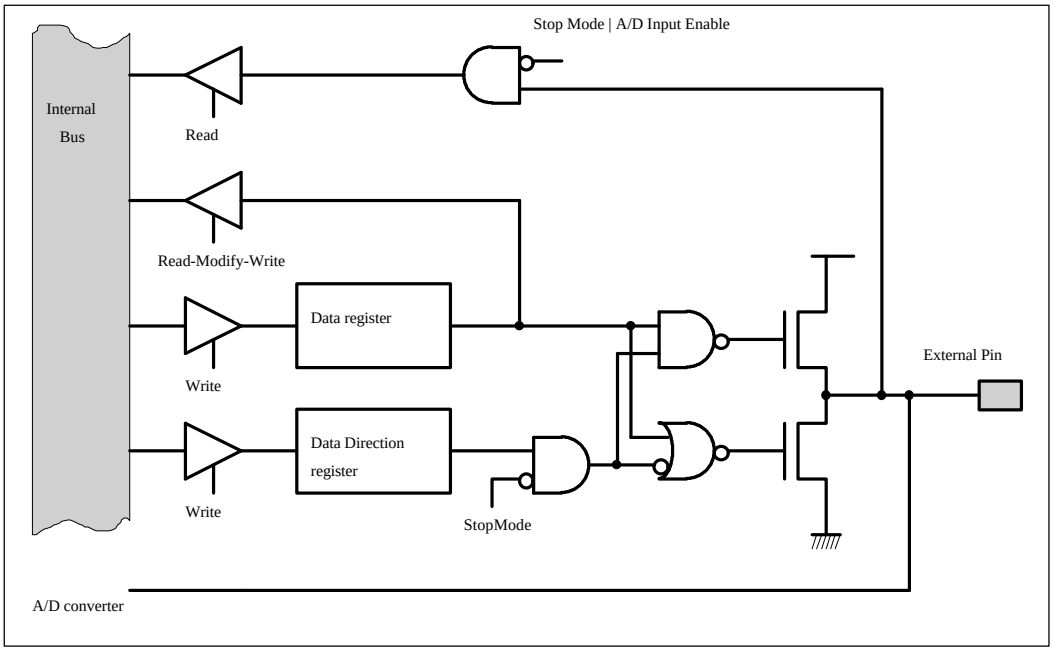
The external pins for P24 through P21(bit 4 through bit 1 of Port 2) can also be used for external LCD bias voltage inputs. When this bias input function is selected by the internal setting of the LCD Controller/Driver, the port function is disengaged from these external pins.

The bit 0 shares its pin with an LCD segment output. The use and block diagram of this bit is the same as described in the previous section.

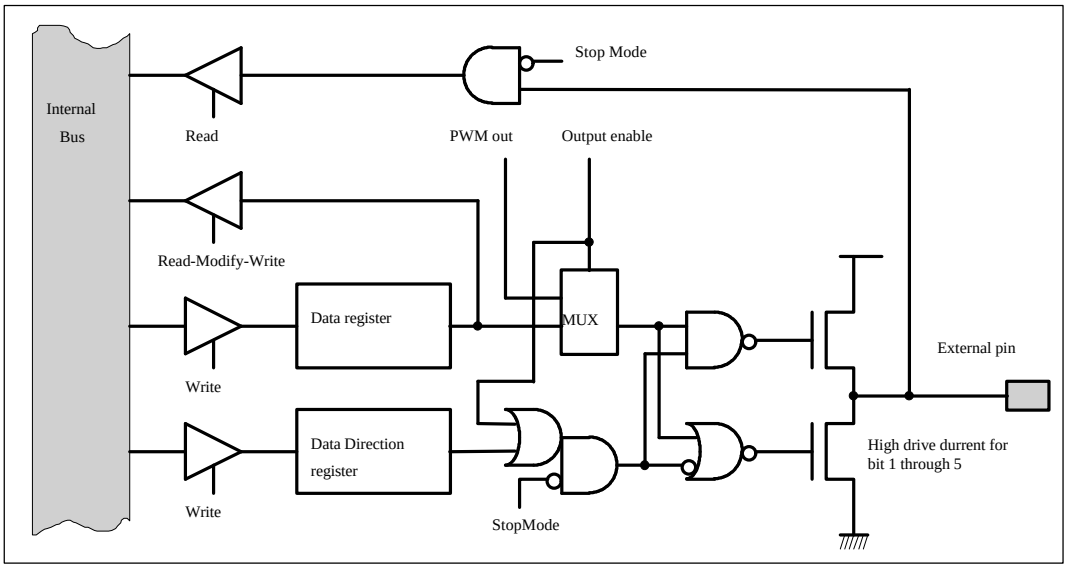
Pull-up options are available for Port 2.

7.5 Port 3

The bits 6 and 7 of the Port 3 share their pins with the A/D converter. When the external pin is used as general purpose IO, the corresponding bit of the A/D Input Enable register should be reset to '0'. When the bit 0 of the A/D Input Enable register is set to '1', the port function is disengaged from the external pin and this pin is used for the analog input of the A/D converter (channel 0). When the bit 1 of the A/D Input Enable register is set to '1', the port function is disengaged from the external pin and this pin is used for the analog input of the A/D converter (channel 1).



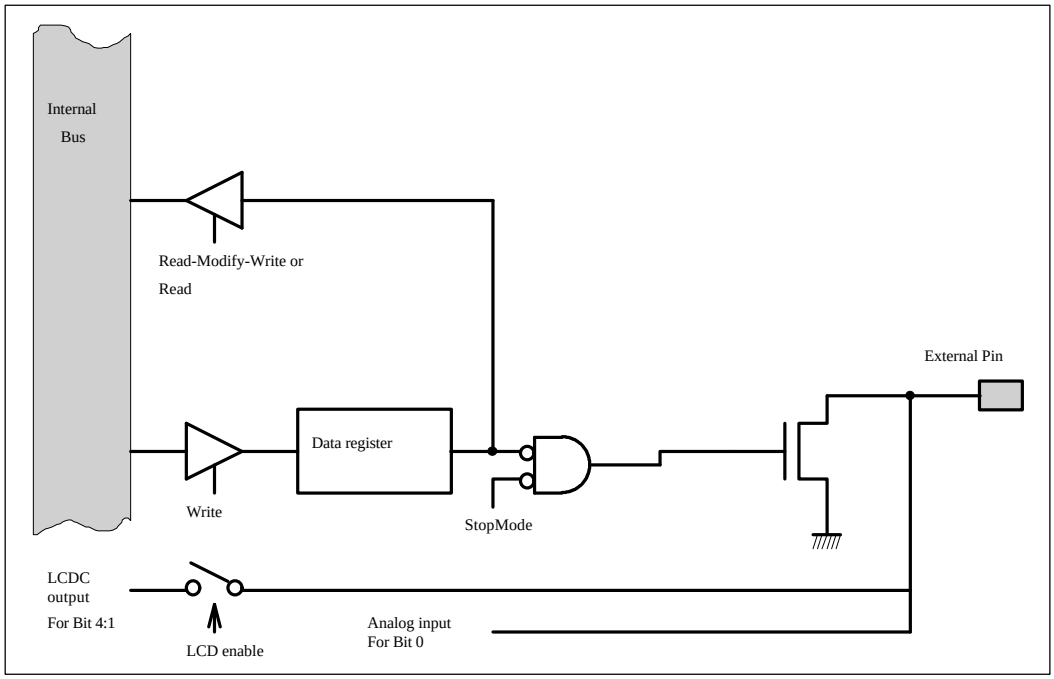
The bits 0 through 5 share their pins with PWM3, PWM4 and the Stepper Motor Controller. The functions of these pins can be selected by setting the internal registers of these peripheral blocks.



7.6 Port 4

Port 4 functions as a 5-bit open drain output. It shares its external pins with the LCD Drive/Controller and the Power Fail Detector. When these external pins are used for the peripheral blocks, the corresponding bit of the Data register should be set to '1'.

Reading the Data register returns the content of register. This is also the same for a Read-Modify-Write operation.



8 Interval Timer

The Interval Timer consists of two 8-bit counters and two sets of control and data registers. It can be configured as two 8-bit timers or one 16-bit timer. The Interval Timer generates an interrupt request signal. It can also generate a square waveform output signal. The sources of the operation clock for the two counters can be independently chosen. The data registers store the values indicating the upper limits of the count up operations for the counters.

8.1 Timer Control registers

Timer 1 Control

Address 0019H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T1IF	T1IE	T1O1	T1O0	T1C1	T1C0	T1SP	T1ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value X000XXX0B

Timer 2 Control

Address 0018H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2IF	T2IE			T2C1	T2C0	T2SP	T2ST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value X000XXX0B

The T1IF and T2IF bits are the interrupt flags. These bits are set when the corresponding counter reaches the upper limit stored in the Data register. Writing ‘0’ resets these bits. Any read-modify-write operation results in reading ‘1’. The T1IE and T2IE are the interrupt enable bits. When either of the interrupt flags is set and the corresponding enable bit is set, the Interval Timer signals an interrupt request.

The T1O1 and T1O0 bits control the TO external output. The TO output is connected to the output of a toggle flip-flip (T-FF). This T-FF flips when the Timer 2 counter reaches the upper limit thus creating a square waveform.

T1O1,T1O0	Operation
00	TO external pin can be used for the other functions.
01	Initial value for T-FF is set to ‘0’
10	Initial value for T-FF is set to ‘1’
11	TO external pin outputs the value of T-FF

The initial value for T-FF must be set while the both timers are stopped (T2ST=‘0’ and T1ST=‘0’). When T1O1 and T1O0 are set to ‘11’, the initial value is reflected to the output signal. The Interval Timer should be started after these settings.

The T1C1 and T1C0 bits determine which clock sources to be used for the Timer 1 counter.

T1C1,T1C0	Clock source
00	System clock/2**2
01	System clock/2**6

10	System clock/2**9
11	External clock from EC external pin

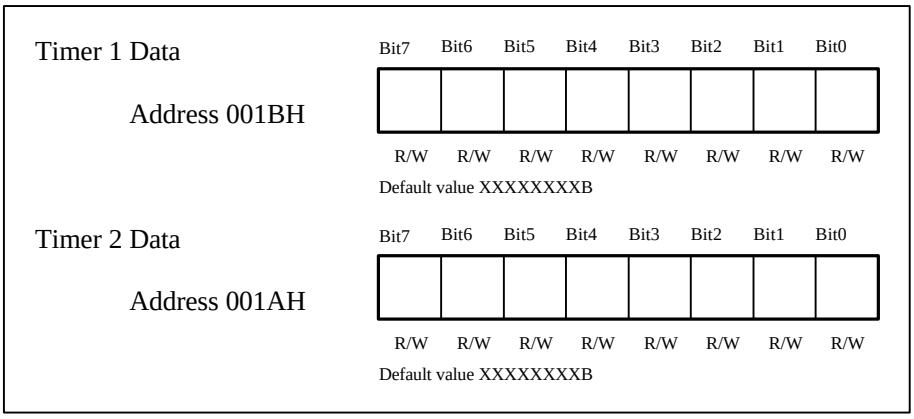
System clock : See section0

The T2C1 and T2C0 bits determine which clock sources to be used for Timer 2 counter. When these bits are set to '11', the Timer 2 counter is cascaded from the Timer 1 counter. Therefor the Interval Timer is configured as one 16-bit timer.

T2C1,T2C0	Clock source
00	System clock/2**2
01	System clock/2**6
10	System clock/2**9
11	Carry-out (upper-limit reached) signal from Timer 1

The T1SP and T2SP bits halt the timers. When one of these bits is set to '1', the corresponding timer halts count-up operation. When this bit is reset to '0', the timer continues the operation from the last state before the halt. The T1ST and T2ST starts/clears the timer. When one of these bits is set to '1', the corresponding counter starts counting from '0'. When this bit is reset, the counter stops.

8.2 Data registers



The Timer 1 Data register and Timer 2 Data register store the values of the upper limits for the two counters. Reading these registers returns the current timer values.

8.3 16-bit timer operation

When the two timers are configured as one 16-bit timer (When T2C1 and T2C0 = 11), the Timer 1 Control register controls the 16-bit timer operation.

The timer can be started by the T1ST bit and the overflow sets the T1IF bit. The clock source is determined by the T1C1 and T1C0 bits. The Timer 1 Data register stores the lower byte and the Timer 2 Data register stores the upper byte of the timer limit.

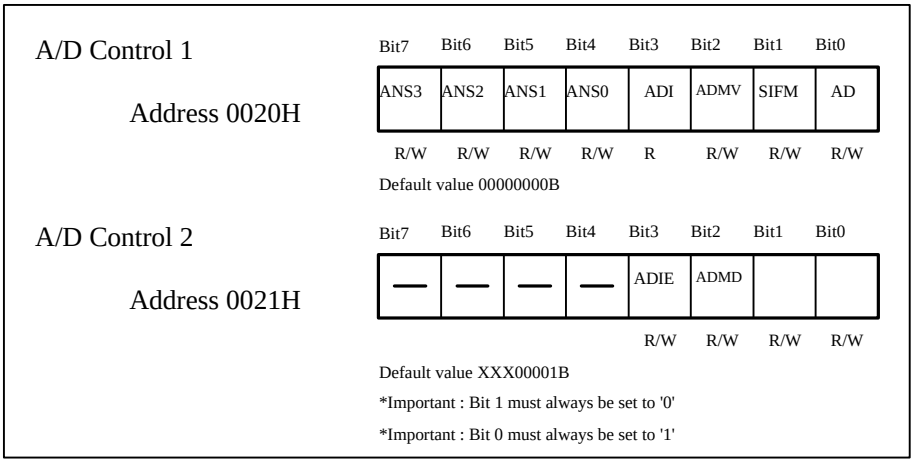
Reading the data registers returns the current timer values. However, it is recommended to read the upper byte twice in order to check if correct 16-bit data is obtained. This is because the carry from lower byte to the upper byte possibly occurs between two reads performed on the two registers.

9 A/D converter

The MB89940 Series employs the sequential-comparison method for its A/D converter. The 8-bit-precision A/D converter consists of the analog circuit including the voltage sampler, two control registers and one data register. It supports two analog input channels. The overall operation of the converter is supervised by software through the control registers and the data register stores the resultant value from the conversion.

The A/D converter also supports the sense mode operation. In this mode, the A/D converter simply judges whether the input voltage is higher/lower than the setting of the data register. The external input pins are shared with the general purpose port function. Refer to the section 0.

9.1 Control registers



■ A/D Control 1

The bits ANS3 through ANS0 are used for selecting the input channel of the A/D converter. While the ADMV bit is '1' (indicating conversion in process), these bit should not be re-written.

ANS3,ANS2,ANS1,ANS0	Input channel
0000	TEMPI (Channel 0)
0001	FUELI (Channel 1)
Other than above	Not supported

When the external input pins are used for the A/D converter the A/D Input Enable register should be set accordingly. (See also Section 0)

The ADI bit is the conversion complete flag. When this bit is '1', it indicates that the A/D conversion has been finished. When the A/D Converter is in the sense mode this bit has different function. When it is '1', it indicates that the specified condition (Refer to the definition of the SIFM bit) is met as a result of the sense mode operation. Writing '0' into this bit reset the flag. Writing '1' does not have any effect. Any Read-Modify-Write operation on

this bit always results in reading '1'. It is recommended that the ADI bit is reset prior to starting the A/D conversion and sense mode operation.

The ADMV bit indicates the status of the conversion process. While the A/D conversion or the sense mode operation is in process, this bit is set to '1'. Otherwise it is reset.

The SIFM bit is used for the sense mode operation. This bit indicates on which condition the ADI bit to be set. If the SIFM bit is set to '1', the ADI bit will be set on the condition that the input voltage is higher than the setting of the data register and vice-versa. This bit should not be modified while the ADMV bit is '1' (indicating operation in process).

Writing '1' into the AD bit starts the analog to digital conversion or starts the sense mode operation. Reading this bit always returns '0'.

The A/D Control 1 register is initialized when the MPU is in the Stop mode.

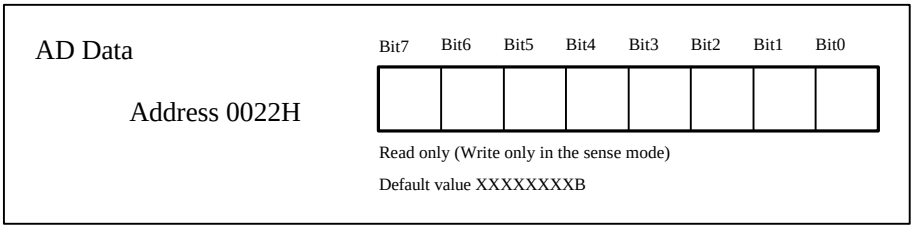
■ A/D Control 2

The ADIE bit is the interrupt enable flag. When this bit is set and ADI in A/D Control 1 is set, the A/D Converter requests an interrupt. Prior to setting the ADIE bit, it is recommended that the ADI bit in the A/D Control 1 is once reset.

The ADMD bit activates the sense mode operation. When this bit is set, the A/D converter is in the sense mode. This bit should not be modified while the A/D converter is in operation.

The A/D Control 2 register is initialized when the MPU is in the Stop mode.

9.2 Data register



The AD Data register stores the result value of the conversion. While the conversion is under its process, the data stored become unstable.

When in the sense mode, this register has different function. The AD Data register stores the reference voltage value being compared with the input voltage. Example of reference voltage values is shown below.

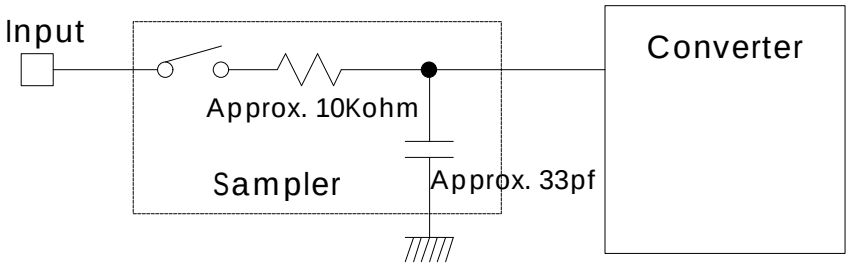
	Reference voltage					
	5.0V	4.0V	3.0V	2.0V	1.0V	0.0V
Data stored	FFH	CDH	9AH	66H	33H	00H

In the sense mode, the AD Data register becomes ‘write only’. This register should not be modified while the sense mode operation is under its process.

9.3 Conversion Time

The A/D converter requires 44 instruction cycles for the analog to digital conversion and 12 instruction cycles for the sense mode operation.

It should be also noted that the voltage sampler uses 8 instruction cycles for its sampling time. If the drive impedance of the external device connected to the A/D input is too high, the sampled voltage may not be accurate enough to guaranty the 8-bit precision. The figure below shows the equivalent circuit of the voltage sampler.



10 LCD Controller/Driver

The LCD Controller/Driver supports up to 17-segment and 4-common signal outputs. It consists of the display RAM, internal bias voltage generator, two control registers and control logic. The outputs of the LCD Controller/Driver can be directly connected to the LCD device.

10.1 LCD Control registers

LCDC Control 1

Address 0072H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		VSEL	BK	MS1	MS0	FP1	FP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value 00010000B

*Important : Bit 7 must always be set to '0'

*Important : Bit 6 must always be set to '0'

The VSEL bit selects the bias voltage source for the LCD drive waveform. When this bit is set to ‘1’, the internal bias voltage generator is used to generate the LCD drive waveform. Otherwise the external bias voltage inputs are used.

When the BK bit is set, the LCD Controller/Driver outputs the blanking waveform. Otherwise it outputs the display waveform in accordance with the contents of the display RAM.

The MS1 and MS0 bits selects the display operation mode. The choices are shown in the table below.

MS1,MS0	LCD display operation
00	LCD operation stops
01	1/2 duty operation
10	1/3 duty operation
11	1/4 duty operation

The FP1 and FP0 bits selects the LCD frame frequency. The choices are shown in the table below.

Note that clearing Time Base Timer alters the LCD frame time. The LCD display may flicker at this timing.

FP1,FP0	Frame frequency
00	1/2**13 Oscillation frequency/N
01	1/2**14 Oscillation frequency/N
10	1/2**15 Oscillation frequency/N
11	1/2**16 Oscillation frequency/N

N: Inverse of operation duty

LCDC Control 2

Address 0073H

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OE	C3			S3	S2	S1	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Default value 00XX000XB

The number of the segment outputs is software-programmable between 10 and 17. The S3, S2 and S1 bits specifies the number of segment outputs required.

S3,S2,S1	Segment output
000	SEG00-SEG16
001	SEG00-SEG15
010	SEG00-SEG14
011	SEG00-SEG13
100	SEG00-SEG12
101	SEG00-SEG11
110	SEG00-SEG10
111	SEG00-SEG09

The segment output pins not specified by this setting can be used for the port function.

The C3 bit also indicates whether the COM3 output is in use. When this bit is reset to '0', the external pin is not used for the LCDC and it can be used for the Port 4 function.

The OE bit indicates whether the all LCD driver outputs are in use. When this bit is reset to '0', it indicates the LCDC does not use all the segment and common outputs. And they are free for the other functions. However does not indicates whether the LCDC is in operation. The operation of the LCDC should be stopped by the MS1 and MS0 bits of the LCD Control 1 register.

10.2 Display RAM

The LCD Controller/Driver contains the 9-byte Display RAM. It stores the display data for the LCD panel. The bit map of the Display RAM is shown below.

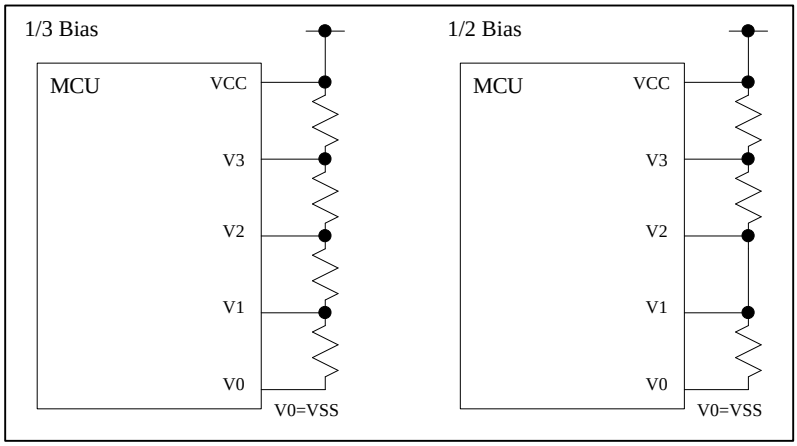
Address	COM3	COM2	COM1	COM0	Segment
0060H	Bit 3	Bit 2	Bit 1	Bit 0	SEG00
	Bit 7	Bit 6	Bit 5	Bit 4	SEG01
0061H	Bit 3	Bit 2	Bit 1	Bit 0	SEG02
	Bit 7	Bit 6	Bit 5	Bit 4	SEG03
0062H	Bit 3	Bit 2	Bit 1	Bit 0	SEG04
	Bit 7	Bit 6	Bit 5	Bit 4	SEG05
0063H	Bit 3	Bit 2	Bit 1	Bit 0	SEG06

	Bit 7	Bit 6	Bit 5	Bit 4	SEG07
0064H	Bit 3	Bit 2	Bit 1	Bit 0	SEG08
	Bit 7	Bit 6	Bit 5	Bit 4	SEG09
0065H	Bit 3	Bit 2	Bit 1	Bit 0	SEG10
	Bit 7	Bit 6	Bit 5	Bit 4	SEG11
0066H	Bit 3	Bit 2	Bit 1	Bit 0	SEG12
	Bit 7	Bit 6	Bit 5	Bit 4	SEG13
0067H	Bit 3	Bit 2	Bit 1	Bit 0	SEG14
	Bit 7	Bit 6	Bit 5	Bit 4	SEG15
0068H	Bit 3	Bit 2	Bit 1	Bit 0	SEG16
	Bit 7	Bit 6	Bit 5	Bit 4	

10.3 Bias Voltage

The LCD Controller/Driver supports 1/2-bias and 1/3-bias voltage waveforms. The bias voltages can be supplied through the four external pins or by the internal bias voltage generator. The internal voltage generator only supports 1/3-bias operation. In this case, the bias voltages are VSS, 1/3*VCC, 2/3*VCC and VCC. The bias current for this generator is cut off when the external bias voltage is selected or the LCD Controller/Driver is fully stopped (when Stop mode or MS1, MS0 = '00').

The external bias voltages should not be higher than VCC. Examples of the external bias voltage circuit are shown below.



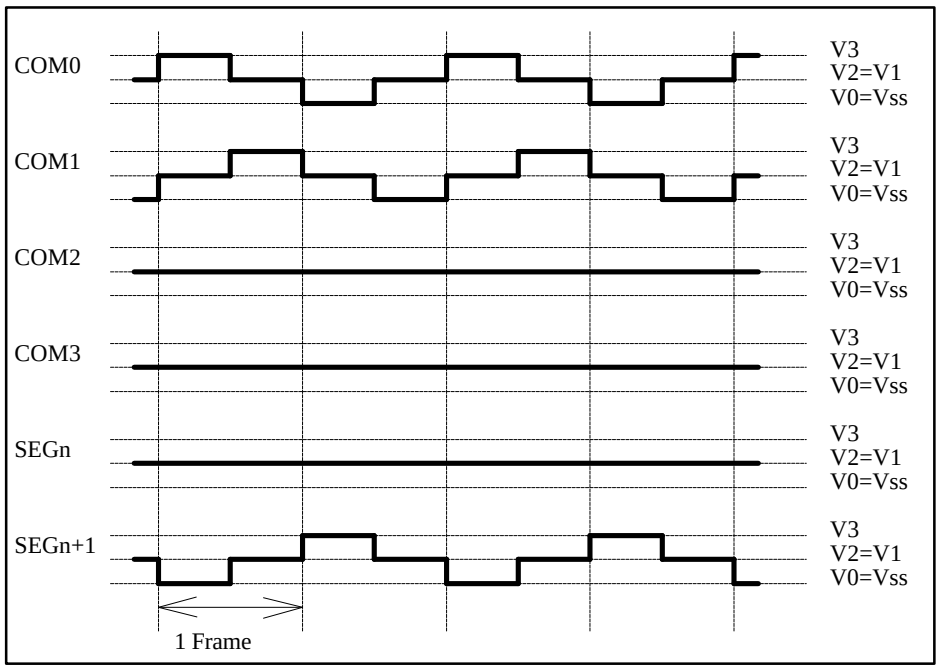
The LCD Controller/Driver supports the following combinations of the duty and bias voltage operations.

	1/2 Duty	1/3 Duty	1/4 Duty
1/2 Bias	Supported	N/A	N/A
1/3 Bias	N/A	Supported	Supported

The following figures show examples of LCD drive waveforms.

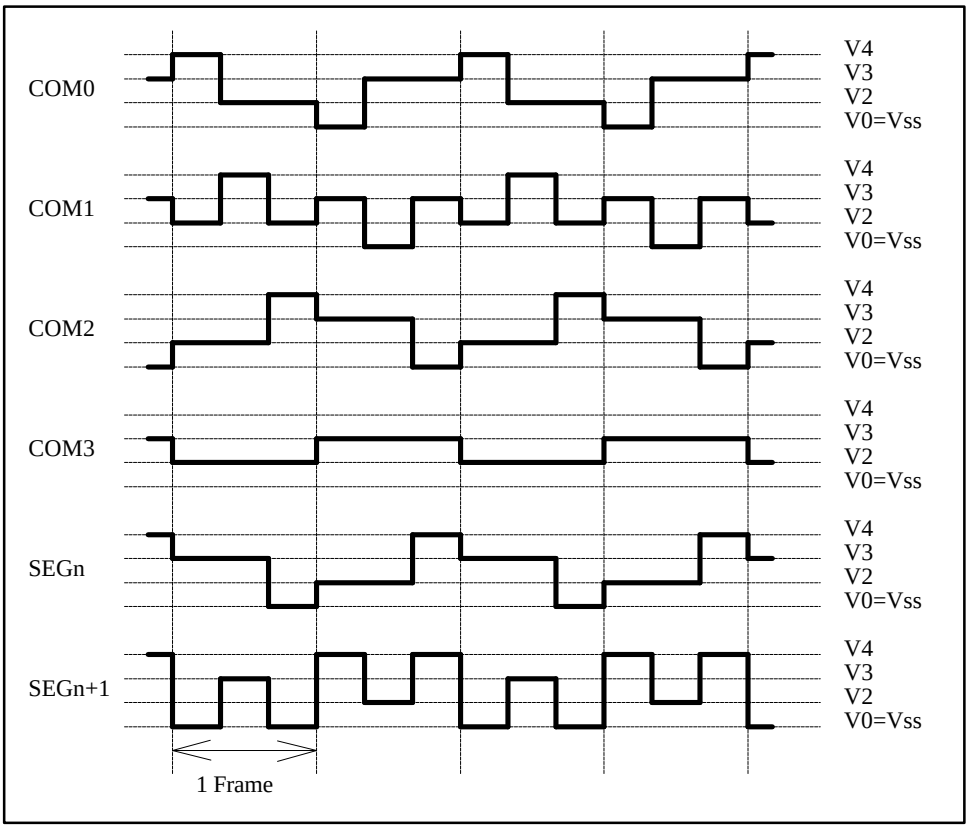
■ 1/2 Bias & 1/2 Duty

Contents of display RAM	COM3	COM2	COM1	COM0
SEGn	X	X	0	0
SEGn+1	X	X	0	1



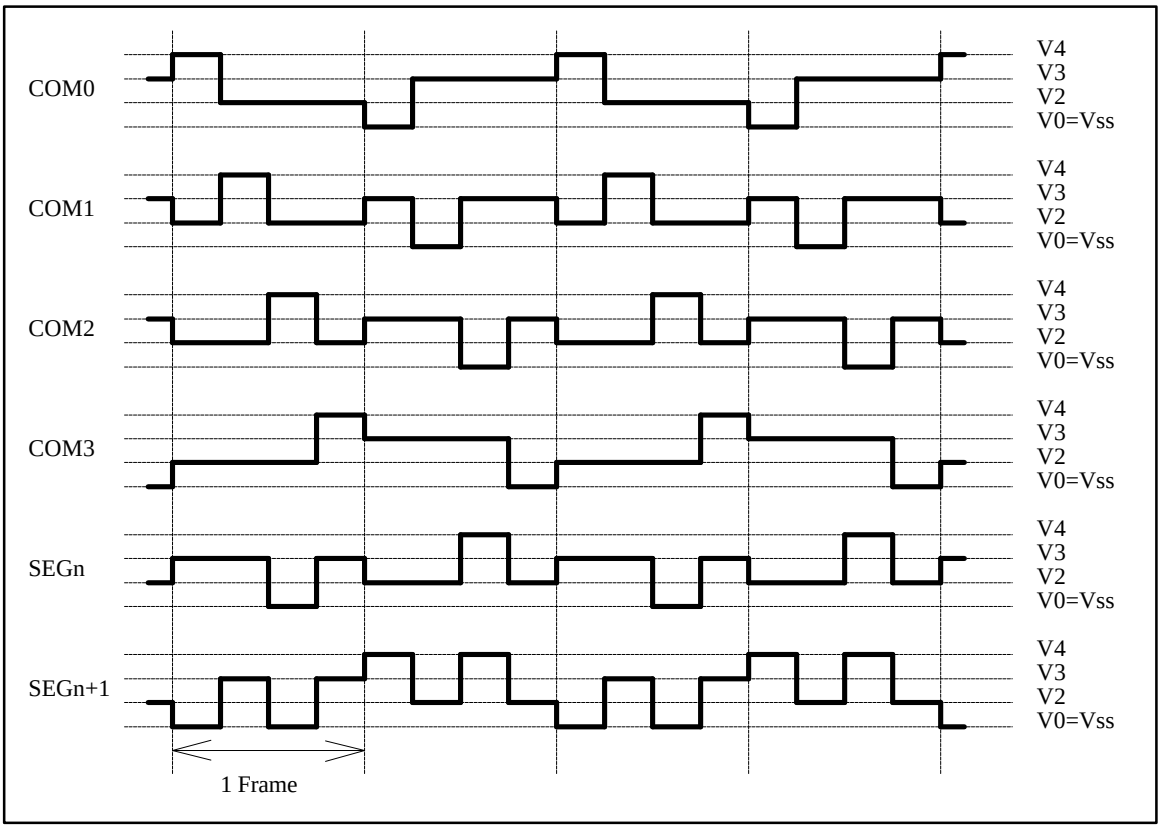
■ 1/3 Bias & 1/3 Duty

Contents of display RAM	COM3	COM2	COM1	COM0
SEGn	X	1	0	0
SEGn+1	X	1	0	1



■ 1/3 Bias & 1/4 Duty

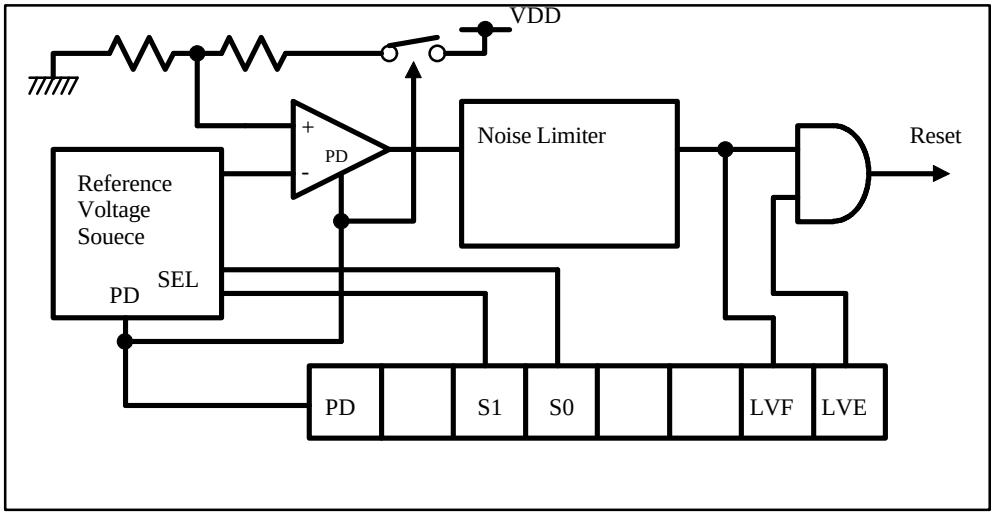
Contents of display RAM	COM3	COM2	COM1	COM0
SEGn	0	1	0	0
SEGn+1	0	1	0	1



11 Low Supply Voltage Reset

The MB89940 Series is capable of generating a reset pulse upon a low supply voltage condition. The Low Voltage Reset controller watches the supply voltage. While the supply voltage drops below the reference voltage, the controller asserts the reset signal. The Low Voltage Reset control register contains the selector bits for the reference voltage.

- Block Diagram



- Low Voltage Reset Control register

Low Voltage Reset Control

Address 000BH

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PDX		S1	S0	—	LVF	LVE	
R/W	R/W	R/W	R/W		R/W	R/W	R/W

Default value upon Power On Reset 0111X000B

When register contents are specified by option setting, writing to this register has no effect.

When the PDX bit is reset to ‘0’, the comparator and Reference Voltage Source go into a low power state and the operation of the controller is stopped. Before entering Stop mode, this bit must be reset to ‘0’.

The LVF bit is the low voltage flag. When a low supply voltage is detected, this bit is set. Writing ‘0’ into the LVF bit clears the flag and writing ‘1’ does not have any effect. Any Read-Modify-Write operation on this bit always results in reading ‘1’.

The LVE bit enables the reset output. If this bit is reset to ‘0’, the reset signal will not be asserted even on a low voltage condition. A write operation to this bit can be performed only once after the reset.

By setting S1 and S0 bits, the reference voltage can be selected between the three choices. Any reset other than Power On Reset does not set this register to the default value. The bits 6 and 0 are do not have any defined function.

S1	S0	Reference voltage
0	0	Reserved.
0	1	3.3 +/- 0.3V
1	0	3.6 +/- 0.3V
1	1	4.0 +/- 0.3V

The contents of Low Voltage Control register can be overridden by mask option. Refer to Appendix for more.

■ Start up operation

The Low Voltage Reset controller requires a lead time before starting its operation. After the PD bit of the Low Voltage Reset Control register is set, this lead time is taken and then the circuit starts the operation.

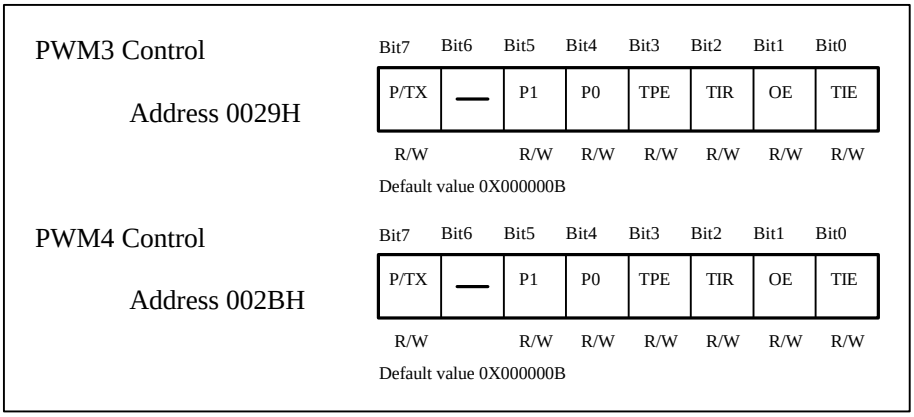
Lead time	Minimum	1.5*2**10/f_{osc}
	Maximum	3.5*2**10/f_{osc}

12 PWM Pulse Generators

The MB89940 Series contains two 8-bit precision PWM Pulse Generators for controlling indicator devices. Each PWM pulse generator operates independently and it consists of a Control register, Compare register, 8-bit counter and 8-bit equality comparator. These generators can also be used as 8-bit interval timers.

12.1 PWM Control registers

The operation of the PWM Pulse Generators are controlled by the PWM Control registers. They determine operational clock frequencies, start/stop the counters and enable/disable interrupt requests.



The P/TX bit switches the operation mode of the PWM Pulse Generator. When this bit is '0', the generator operates as an 8-bit interval timer (See section 0). Otherwise it operates as a PWM Pulse Generator. This bit should not be modified when the counter is in operation (TPE='1'). It is also recommended that the TIR and TIE bits are once reset prior to resetting the P/TX bit to '0'.

The P1 and P0 bits selects the source of the operation clock. The 8-bit counter operates with this operation clock. The choices are shown in the table below. These bits should not be modified while in operation.

P1,P0	Operation Clock	PWM cycle
00	$1/2^1$ System Clock	$1/2^9$ System Clock cycle
01	$1/2^2$ System Clock	$1/2^{10}$ System Clock cycle
10	$1/2^3$ System Clock	$1/2^{11}$ System Clock cycle
11	$1/2^4$ System Clock	$1/2^{12}$ System Clock cycle

The TPE bit starts/stops the operation of the counter. When this bit is set to '1', the counter starts counting from '00H'. And it continues count-up operation until the TPE bit is reset.

It should be noted that the first PWM cycle may have a shorter PWM pulse width by maximum one operation clock cycle. This is due to the asynchronous nature of the TPE write operation. If a TPE write is performed just before the rising edge of the operation clock, the PWM 'H' pulse width will be shorter by one operation clock.

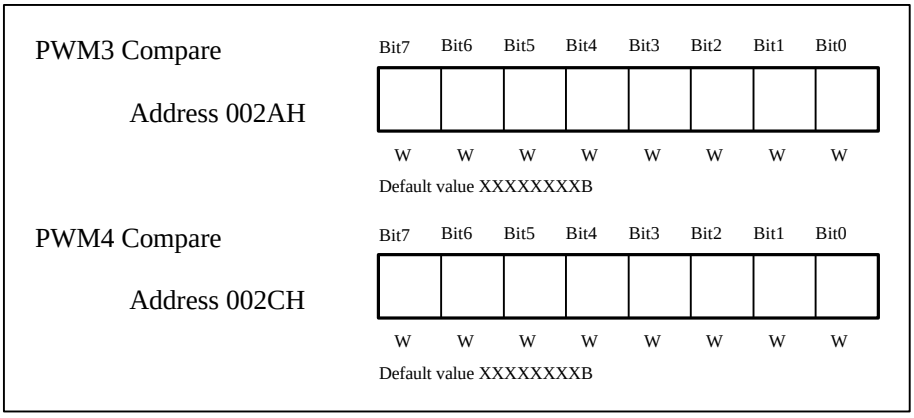
The TIR bit is the interrupt flag used in the 8-bit timer operation mode (P/TX='0'). The PWM Pulse Generator sets this flag when the value stored in the Compare register equals to the value of the 8-bit counter. (See section 0)

In normal operation mode (P/TX='1'), The TIR bit is not affected by the counter operation. Any Read-Modify-Write operation on this bit always results in reading '1'. Writing '0' in this bit clears the flag.

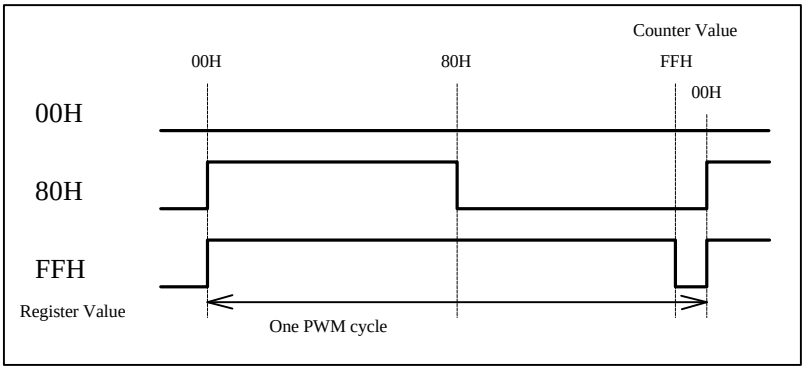
The OE bit controls the external output. When this bit is set, the external output is used for the PWM Pulse Generator. Otherwise it can be used for the port function.

The TIE bit is the interrupt enable flag used in the timer operation mode. (See section 0) When this bit is '1' and TIR bit is set, the generator signals an interrupt request to the core CPU. It is generally recommended that the TIR bit is once reset prior to enabling the interrupt request.

12.2 PWM Compare registers



The PWM Compare registers store the values defining the 'H' pulse width of the PWM signal. The following figure shows the relationship between the register value and the pulse width.



The PWM output stays logic-high until the counter value matches the registers value then changes to a logic-low. At the beginning of the next PWM cycle, the output becomes logic-high again. While in the Stop mode, the counter holds its operation and maintains the last state.

If the register value is modified while the counter is in operation, the modified value takes effect in the next interval.

12.3 Timer operation mode

When the P/TX bit is '0', the PWM Pulse Generator operates as an 8-bit interval timer.

In this operation mode, the value of the Compare register specifies the interval time. When the counter values matches the register value, the TIR bit is set and the counter is cleared then starts the next interval. If TIR bit is set and TIE bit is '1', the generator signals an interrupt request. The output signal flips at this timing therefor the generator outputs a square waveform. The equation for the interval time is as follows.

$T_{interval}$ = (Operation clock cycle time) * (Value of Compare register + 1)

It should be noted that the first interval time may be shorter by maximum one operation clock cycle. This is due to the asynchronous nature of the TPE write operation. If a TPE write is performed just before the rising edge of the operation clock, the interval time will be shorter by one operation clock.

If the register value is modified while the counter is in operation, the modified value takes effect in the next interval. While in the Stop mode, the counter holds its operation and maintains the last state.

13 On-Chip Voltage Regulator (MB89943)

MB89943 contains On-Chip Voltage Regulator for the internal 3V power supply. There are a few important features affecting the operation of the MCU.

13.1 Power On Reset

When power-on, the On-Chip Voltage Regulator requires a stabilization time additional to the oscillation stabilization time. This regulator stabilization time is dependent on the oscillation clock.

Regulator Stabilization Time	Tosc*2**19

Tosc:Oscillation clock cycle time

The external power supply voltage must reach the minimum operation voltage within the stabilization time.

The duration of the power on reset signal is lengthened by this stabilization time compared with other products(MB89PV940 and MB89P945).

13.2 Stop mode

In Stop mode, the voltage regulator is in standby maintaining a minimal power supply only for the data retention. Therefor all the peripheral blocks which contain analog circuit must be in power down mode.

An external event can reactivate the MCU but a recovery time is required on top of the oscillation stabilization time.

Regulator Recovery Time	Approx. 20us

Since the voltage regulator supplies minimal power in Stop mode, it is recommended that a limited number of external interrupt inputs are enabled in Stop mode.

For further details, please consult Fujitsu.

14 Instruction Set

Refer to the accompanied material.

15 Electrical characteristics

15.1 Absolute maximum ratings

Item	Symbol	Min	Max	Unit	Remark
Power supply voltage	VCC	V_{SS}-0.3	V_{SS}-6.5	V	
	AVCC	V_{SS}-0.3	V_{SS}-6.5	V	Should not exceed VCC
	DVCC	V_{SS}-0.3	V_{SS}-6.5	V	Should not exceed VCC
Input voltage	V_I	V_{SS}-0.3	V_{CC}-0.3	V	Except P3[1:5] and P4[4:1]
	V_{I2}	V_{SS}-0.3	DV_{CC}-0.3	V	P3[1:5]
	V_{I3}	V_{SS}-0.3	V_{SS}-6.5	V	P4[4:1]
Output voltage	V_{O1}	V_{SS}-0.3	V_{CC}-0.3	V	Except P3[1:5] and P4[4:1]
	V_{O2}	V_{SS}-0.3	DV_{CC}-0.3	V	P3[1:5]
	V_{O3}	V_{SS}-0.3	V_{SS}-6.5	V	P4[4:1]
Output low maximum current	V_{OL}		20	mA	Except P3[1:5]
Output low mean current	V_{OLAV}		4	mA	Except P3[1:5]
Output low mean current (Total)	$V_{OLTOTALAV}$		40	mA	Except P3[1:5]
Output low maximum current (Total)	$V_{OLTOTALMAX}$		100	mA	Except P3[1:5]
Output high current	V_{OH}		-20	mA	Except P3[1:5]
Output high mean current	V_{OHAV}		-4	mA	Except P3[1:5]
Output high mean current (Total)	$V_{OHTOTALAV}$		-20	mA	Except P3[1:5]
Output high maximum current (Total)	$V_{OHTOTALMAX}$		-50	mA	Except P3[1:5]
Output low maximum current	V_{OL}		50	mA	P3[1:5]
Output low mean current	V_{OLAV}		40	mA	P3[1:5]
Output low mean current (Total)	$V_{OLTOTALAV}$		100	mA	P3[1:5]
Output low maximum current (Total)	$V_{OLTOTALMAX}$		200	mA	P3[1:5]
Output high maximum current	V_{OH}		-50	mA	P3[1:5]
Output high mean current	V_{OHAV}		-40	mA	P3[1:5]
Output high mean current (Total)	$V_{OHTOTALAV}$		-100	mA	P3[1:5]
Output high maximum current (Total)	$V_{OHTOTALMAX}$		-200	mA	P3[1:5]
Power dissipation	P_D		300	mW	

Note : Exceeding the absolute maximum ratings may cause permanent damages on the product. Also the product should be used in the operation ranges described in DC Characteristics for maintaining the product reliability otherwise the reliability may deteriorate.

15.2 DC characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
Operating supply voltage range	V_{CC}, AV_{CC}, DV_{CC}		3.5		5.5	V	VCC=AVCC=DVCC
RAM data retention supply voltage range	$V_{CC,}$ AV_{CC}, DV_{CC}		3.0		5.5	V	VCC=AVCC=DVCC
Operating temperature range	T_A		-40		85	deg	
Input high voltage	V_{IH}		0.7* V_{CC}		V_{CC}+0.3	V	Other than below
	V_{IHS}		0.8* V_{CC}		V_{CC}+0.3	V	XRST,MODE,P2[7:0]
Input low voltage	V_{IL}		V_{SS}-0.3		0.3* V_{CC}	V	Other than below
	V_{ILS}		V_{SS}-0.3		0.2* V_{CC}	V	XRST,MODE,P2[7:0]
Open drain clamp voltage	V_D		V_{SS}-0.3		V_{CC}+0.3	V	P40
	V_{D2}		V_{SS}-0.3		V_{SS}+5.5	V	P4[4:1]
Output high voltage	V_{OH}	I_{OH}=-2.0mA	4.0			V	P1[7:0],P2[7:0],P30, P36,P37
	V_{OH2}	I_{OH}=-30mA	V_{CC}-0.5			V	P3[6:1] V_{CC}=DV_{CC}
Output low voltage	V_{OL}	I_{OL}=4.0mA			0.4	V	P1[7:0],P2[7:0],P37, P36,P30,P4[4:0]
	V_{OL2}	I_{OL}=30mA			0.5	V	P3[6:1] V_{SS}=DV_{SS}
Input leakage current	I_{IL1}	0V<V_I<V_{CC}, V_{CC}=DV_{CC}	-5		+5	uA	MODE,P1[7:0],P2[7:0],P3[7:0],P4[4:0] without pull-up option
Pull up resistor	R_{PULL}		25	50	100	K ohm	XRST,P1[7:2],P2[7:0] with pull-up option
LCD internal bias voltage resister.	R_{LCD}		50	100	200	K ohm	V0-V1,V1-V2,V2-V3

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
Power supply current	I_{CC}	fosc=8MHz,		12	20	mA	I_{CC} =I(V_{CC})+ I(DV_{CC}) MB89943,MB89PV940
		Tinst=500ns		12	20	mA	I_{CC} =I(V_{CC})+ I(DV_{CC}) MB89P945
	I_{CCS}	fosc=8MHz, Tinst=500ns in Sleep mode		3	7	mA	I_{CCS} =I(V_{CC})+ I(DV_{CC})
	I_{CCH}	In Stop mode T_A =25deg		5	10	uA	I_{CCH} =I(V_{CC})+ I(DV_{CC})
	I_A	fosc=8MHz A/D in operation		6	8	mA	I_A =I(AV_{CC})
	I_{AH}	fosc=8MHz A/D stopped		5	10	uA	I_{AH} =I(AV_{CC})
Input capacitance	C_{IN}	f_{IN}=1MHz		10		pF	
External Capacitor at VINT	C_{VINT}			0.1		uF	MB89943 only

T_{INST} : One instruction cycle time. Refer to section 0.

Preliminary information

15.3 DC/AC characteristic of A/D converter

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
Resolution					8	bit	
Conversion error					+/-1.5	LSB	
Nonlinearlity					+/-1.0	LSB	
Differential nonlinearlity					+/-0.9	LSB	
Zero reading voltage	V_{0T}		AV_{SS} -1.0$_{LSB}$	AV_{SS}+0.5$_{LSB}$	AV_{SS}+ 2.0$_{LSB}$	V	
Full scale reading voltage	V_{FST}		AV_{CC} -3.0$_{LSB}$	AV_{CC}-1.5$_{LSB}$	AV_{CC}	V	
Offset between analog input channels					0.5	LSB	
A/D conversion time					44	T_{INST}	
Sense mode conversion time					12	T_{INST}	
Analog input current	I_{AIN}				10	uA	
Analog input voltage range			0		AVCC	V	

T_{INST} : One instruction cycle time. Refer to section 0.

Terminology

- Conversion error : Absolute maximum conversion deviation with respect to the theoretical conversion line.
- Nonliniearlity : Relative maximum conversion deviation with respect to the theoretical conversion line connecting to the device-unique zero reading voltage and full scale reading voltage.
- Differential nonlinearlity : Maximum conversion deviation in any two adjacent reading voltages with respect to the theoretical LSB conversion step.
- Zero reading voltage : Maximum input voltage which results in the conversion value of '00H'.
- Full scale reading voltage: Minimum input voltage which results in the conversion value of 'FFH'.

15.4 DC characteristics of Low Supply Voltage Reset and Low Supply Voltage Interrupt

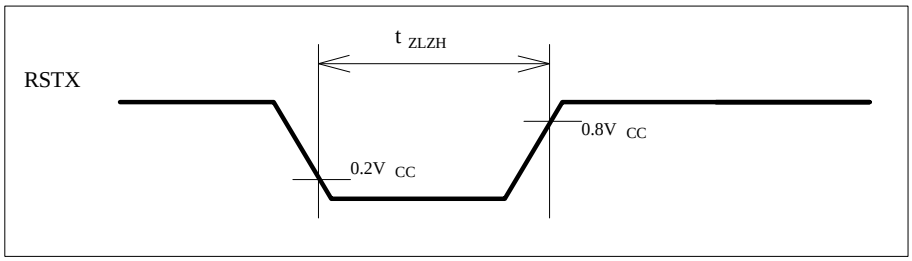
To be determined.

15.5 AC characteristics

15.5.1 Reset input timing

Item	Symbol	Condition	Min	Max	Unit	Remark
Reset low pulse width	t_{ZLZH}		16		T_{OSC}	

T_{OSC} : One oscillation clock cycle time

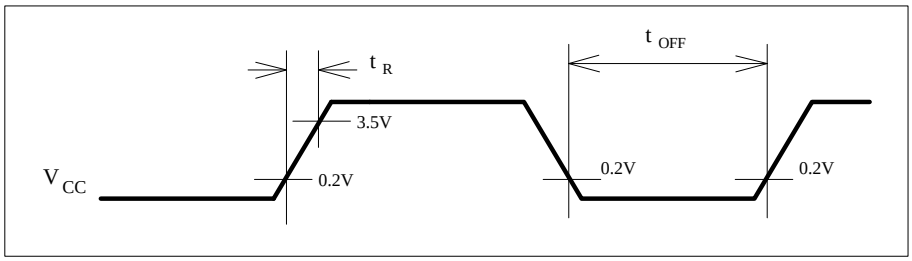


If Power-on reset option is not activated, the external reset signal must be kept asserted until the oscillation is stabilized.

15.5.2 Power on profile

Item	Symbol	Condition	Min	Max	Unit	Remark
Power supply voltage rising time	t_R			50	ms	MB89PV940 MB89P945
Power supply voltage rising time	t_R			2**19	T_{OSC}	MB89943
Power-off minimum period	t_{OFF}		1		ms	

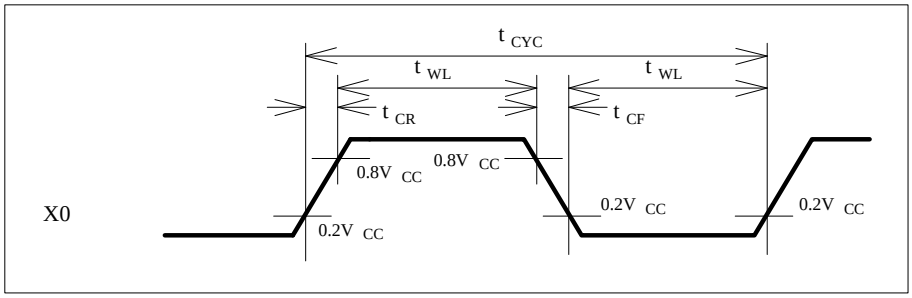
T_{OSC} : One oscillation clock cycle time



Power supply voltage should reach the minimum operation voltage within the specified default duration of the oscillation stabilization time. Refer to section 0.

15.5.3 Clock input timing

Item	Symbol	Condition	Min	Max	Unit	Remark
Clock frequency	f_{OSC}		1	8	MHz	
Clock cycle time	t_{CYC}		1000	125	ns	
Clock pulse width	t_{WH}, t_{WL}		20		ns	
Clock rising/falling time	t_{CR}, t_{CF}			10ns		

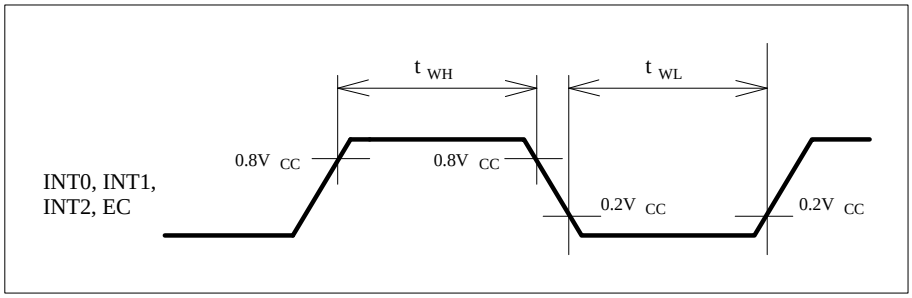


Preliminary information

15.5.4 Peripheral signal input timing

Item	Symbol	Condition	Min	Max	Unit	Remark
Peripheral input high pulse width	t_{WH}		2		T_{INST}	INT0,INT1,INT2,EC
Peripheral input low pulse width	t_{WL}		2		T_{INST}	INT0,INT1,INT2,EC

T_{INST} : one instruction cycle time



16 Package Dimensions

Refer to the accompanied material.

17 Appendix

17.1 Register Map

Address	Read/Write	Register	Comment
0000H	R/W	Port 0 Data register	
0001H	W	Port 0 Data Direction register	
0002H	R/W	Port 1 Data register	
0003H	W	Port 1 Data Direction register	
0004H			Reserved
0005H			Reserved
0006H			Reserved
0007H	R/W	System Clock Control	
0008H	R/W	Standby Control register	
0009H	R/W	Watchdog Timer Control Register	
000AH	R/W	Time Base Timer Control Register	
000BH	R/W	Low Voltage Reset Control	
000CH	R/W	Port 2 Data register	
000DH	R/W	Port 2 Data Direction register	
000EH	R/W	Port 3 Data register	
000FH	W	Port 3 Data Direction register	
0010H	R/W	Port 4 Data register	
0011H	R/W	Port 3 A/D Input Enable register	
0012H to 0017H			Reserved
0018H	R/W	Timer 2 Control register	
0019H	R/W	Timer 1 Control register	
001AH	R/W	Timer 2 Data register	
001BH	R/W	Timer 1 Data register	
001CH to 001FH			Reserved
0020H	R/W	A/D Control register 1	
0021H	R/W	A/D Control register 2	
0022H	R/W	A/D Data register	
0023H	R/W	PWM Control register	

0024H	W	PWM1 Compare register	
0025H			Reserved
0026H	W	PWM2 Compare register	
0027H	R/W	PWM1 Select register	
0028H	R/W	PWM2 Select register	
0029H	R/W	PWM3 Control register	
002AH	W	PWM3 Compare register	
002BH	R/W	PWM4 Control register	
002CH	W	PWM4 Compare register	
002DH	R/W	Selector Test register	
002EH	R/W	Power Fail Control register	
002FH	R/W	External Interrupt Control 1 register	
0030H	R/W	External Interrupt Control 2 register	
0031H to 005FH			Reserved
0060H to 0068H	R/W	LCD Display Data RAM	
0069H to 0071H			Reserved
0072H	R/W	LCD Control register	
0073H	R/W	LCD Control 2 register	
0074H to 007BH			Reserved
007CH	W	Interrupt Level Setting register 1	
007DH	W	Interrupt Level Setting register 2	
007EH	W	Interrupt Level Setting register 3	
007FH			Reserved

17.2 External pin state summary

Pin Name	Operation	Sleep	Stop SPL=0	Stop SPL=1	Reset
P0[7:0]	Input /output	Input /output	Hi-Z /output	Hi-Z	Hi-Z
P1[7:0]	Input /output	Input /output	Hi-Z /output	Hi-Z	Hi-Z
X0	oscillation input	oscillation input	Hi-Z	Hi-Z	oscillation input
X1	oscillation output	oscillation output	H output	H output	oscillation output
MODE	Input	Input	Input	Input	Input
RSTX	Input	Input	Input	Input	Input/ Output
P27/INT2	Input /output	Input /output	INT2 /output	Hi-Z	Hi-Z
P26/INT1	Input /output	Input /output	INT1 /output	Hi-Z	Hi-Z
P25/INT0	Input /output	Input /output	INT0 /output	Hi-Z	Hi-Z
P2[4:0]	Input /output	Input /output	Hi-Z /output	Hi-Z	Hi-Z
P3[7:0]	Input /output	Input /output	Hi-Z /output	Hi-Z	Hi-Z
P4[4:1]	Output	Output	Output	Hi-Z	Hi-Z
P40	Input /output	Input /output	Output	Hi-Z	Hi-Z
VINT	Output	Output	Output	Output	Output

17.3 Mask Option summary

For MB89P945 and MB89943, the following mask options are available.

Option	Description
Pull-up resistor	Internal pull-up resistors for P1[7:2], P2[7:0] external pins. If pull-up options are specified for P20 and P1[7:2], these pins should not be used for LCDC segment outputs. If pull-up options are specified for P2[4:1], these pins should not be used for LCDC external bias inputs. Any pull-up options are not available for MB89VP940.
Reset output	Reset output. When internal reset signal is generated, MB89940 series asserts the reset output signal. This option is always active for MB89PV940 and MB89943.
Power-on reset	Internal power-on reset. When power-on, a reset pulse is generated internally. This option is always active for MB89PV940 and MB89943.
Oscillation stabilization time	Default duration of the oscillation stabilization time. Refer to section 0. For MB89PV940, this option is always ‘11’. 00: 2**3/fosc 01: 2**14/fosc 10: 2**17fosc 11: 2**18/fosc
Low Voltage Reset	Specifies the contents of the Low Voltage Reset Control register. When this option is activated, software setting has not effect. Details to be found in the next section.

17.4 Option PROM (MB89P945)

For MB89P945, mask options are described in the option PROM area. The table below shows the bit map of the option PROM. The option data can be written by a standard EPROM programmer. Refer to the next section.

PROM Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0H	Unused	Unused	Unused	Reserved	Reset output 1:Active 0:Inactive	Power-on reset 1:Active 0:Inactive	Oscillation stabilization time 11:2^{18}Tosc 10:2^{17}Tosc 01:2^{14}Tosc 00:2^{3}Tosc	
3FF1H	P17 pull up 1:Inactive 0:Active	P16 pull up 1:Inactive 0:Active	P15 pull up 1:Inactive 0:Active	P14 pull up 1:Inactive 0:Active	P13 pull up 1:Inactive 0:Active	P12 pull up 1:Inactive 0:Active	Unused	Unused
3FF2H	P27 pull up 1:Inactive 0:Active	P26 pull up 1:Inactive 0:Active	P25 pull up 1:Inactive 0:Active	P24 pull up 1:Inactive 0:Active	P23 pull up 1:Inactive 0:Active	P22 pull up 1:Inactive 0:Active	P21 pull up 1:Inactive 0:Active	P20 pull up 1:Inactive 0:Active
3FF3H	Unused	Unused	Unused	Low Volt. PDX bit	Low Volt. S1 bit	Low Volt. S0 bit	Low Volt. LVE bit	Low Volt. 1:Register active 0:Option active
3FF4H	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused
3FF5H	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused
3FF6H	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused

Default values are all '1'.

Tosc : One oscillation clock cycle time.

When the bit 0 of '3FF3H' is '0', it activates the option setting for the Low Voltage Reset Control register. When this option is activated, software setting in the register has no effect.

17.5 Writing data in One Time PROM (MB89P945)

Using the EPROM adapter (provided by Fujitsu) and a standard EPROM programmer, user-defined data can be written into the One Time PROM and option PROM. The EPROM programmer should be set to '27C256' and electro-signature mode should not be used. When programming the data, the internal addresses are mapped as follows.