FUJITSU SEMICONDUCTOR
CONTROLLER MANUAL

CM25-10130-1E

F²MC-8L FAMILY
MICROCONTROLLERS
MB89950 SERIES
HARDWARE MANUAL

FUJITSU

PREFACE

The MB89950 series of microcontrollers are mid-range of microcontroller. They are general-purpose and high-speed products in the F^2MC-8L Family series of 8-bit single-chip microcontrollers operating at low voltages. It has UART, PWM, LCD controller and etc.

This manual covers the functions and operations of the MB89950 series of microcontrollers. Refer to the ***F^2MC-8L Family Software Manual*** for instructions.

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1. GENERAL

The MB89950 series of single-chip compact microcontroller using the F^{2}MC-8L core for which can operate at high-speeds and low voltages. They contain peripheral such as timers, UART, serial interfaces, and external interrupts, including a 168-pixel LCD controller/driver; they are best suited for use in LCD panels.

1.1 Features

- High-speed processing even at low voltages
  Minimum instruction execution time: 0.8 µs/5 MHz (V_{CC} = 5 V)

- F^{2}MC-8L family CPU core
  Instruction system most suited to controller
  - Multiplication and division instructions
  - 16-bit arithmetic operation
  - Instruction test and branch instruction
  - Bit manipulation instruction, etc.

- LCD controller/driver
  - Maximum 42 segment outputs × 4 common outputs
  - Built-in LCD driver split resistor

- Three-channel timer unit
  - 8-bit PWM timer: (usable as both reload timer and PWM timer)
  - 8-bit pulse width count timer: (usable as both reload timer)
  - 20-bit time-based counter

- Two serial interfaces
  - 8-bit synchronous serial interface (The transfer direction can be selected to communicate with various equipment.)
  - UART (5, 7, and 8-bit transfers possible)

- External-interrupt input: 2 channels
  - 2 channels can be used to clear the low-power consumption modes.
    (An edge-detection function is provided)

- Low-power consumption modes
  - Stop mode (Oscillation stops to minimize the current consumption.)
  - Sleep mode (The CPU stops to reduce current consumption to about 30% of normal.)

1.2 Product Series

Table 1–1 lists the types and functions of the MB89950 series of microcontrollers.

Table 1–1 Types and Functions of MB89950 Series of Microcontrollers

Model name	MB89951	MB89953	MB89P955	MB89PV950
Classification	Mass-produced product (Mask ROM product)		One-time programmable	Piggyback/Evaluation and development product
ROM capacity	4K × 8 bits (internal ROM)	8K × 8 bits (internal ROM)	16K × 8 bits (Internal PROM; writable by general-purpose writers)	32K × 8 bits (External ROM)
RAM capacity	128 × 8 bits	256 × 8 bits	512 × 8 bits	1024 × 8 bits
CPU function	Number of basic instructions:136 Instruction bit length:8 bits Instruction length:1 to 3 bytes Data bit length:1, 8, 16 bits Minimum instruction execution time:0.8 µs at 5 MHz (V_{CC} = 5 V) Interrupt processing time:7.2 µs at 5 MHz (V_{CC} = 5 V)			
Port	I/O port (N-ch open drain): 22 (also used as segment pin)*1 I/O port (N-ch open drain): 4 (two of them are also used as LCD bias pins) I/O port (CMOS): 7 (6 used as peripheral) Total: 33 (Maximum)			
PWM Timer	8-bit reload timer operation (toggle output possible) 8-bit resolution PWM operation Operation clock (pulse-width count timer output: 0.8 µs, 12.8 µs, 51.2 µs/5 MHz)			
Pulse-width Counter Timer	8-bit reload timer operation 8-bit pulse width measurement (continuous measurement, High- and Low-width measurement, and one-cycle measurement) Operation clock (0.8 µs, 3.2 µs, 25.6 µs/5 MHz)			
Serial I/O	8-bit length, selectable from least significant bit (LSB) first or most significant bit (MSB) first, transfer clock (external, 1.6 µs, 6.4 µs, 25.6 µs/5 MHz)			
UART	5-, 7-, 8-bit transfers possible, internal baud-rate generator (Max. 78125 bps/5 MHz)			
LCD controller/driver	Common output: 4 Segment output: 42 (max.) Operation mode: 1/2 bias and 1/2 duty, 1/3 bias and 1/3 duty, 1/3 bias and 1/4 duty LCD controller display RAM capacity: 42 × 4 bits LCD driver split resistor: built-in (external resistor selectable)			
External Interrupt	2 (edge selectable: one serving as pulse-width count timer input)			
Standby Mode	Sleep mode, stop mode			
Package	FPT-64-M09			MQP-64C-P01
Operation Voltage *2	2.2 V to 6.0 V		2.7 V to 6.0 V	
EPROM	not applicable			MBM27C256A-25 (LCC package)

*1 Mask Option.

*2 Varies according to conditions such as frequency.

1.3 Block Diagram

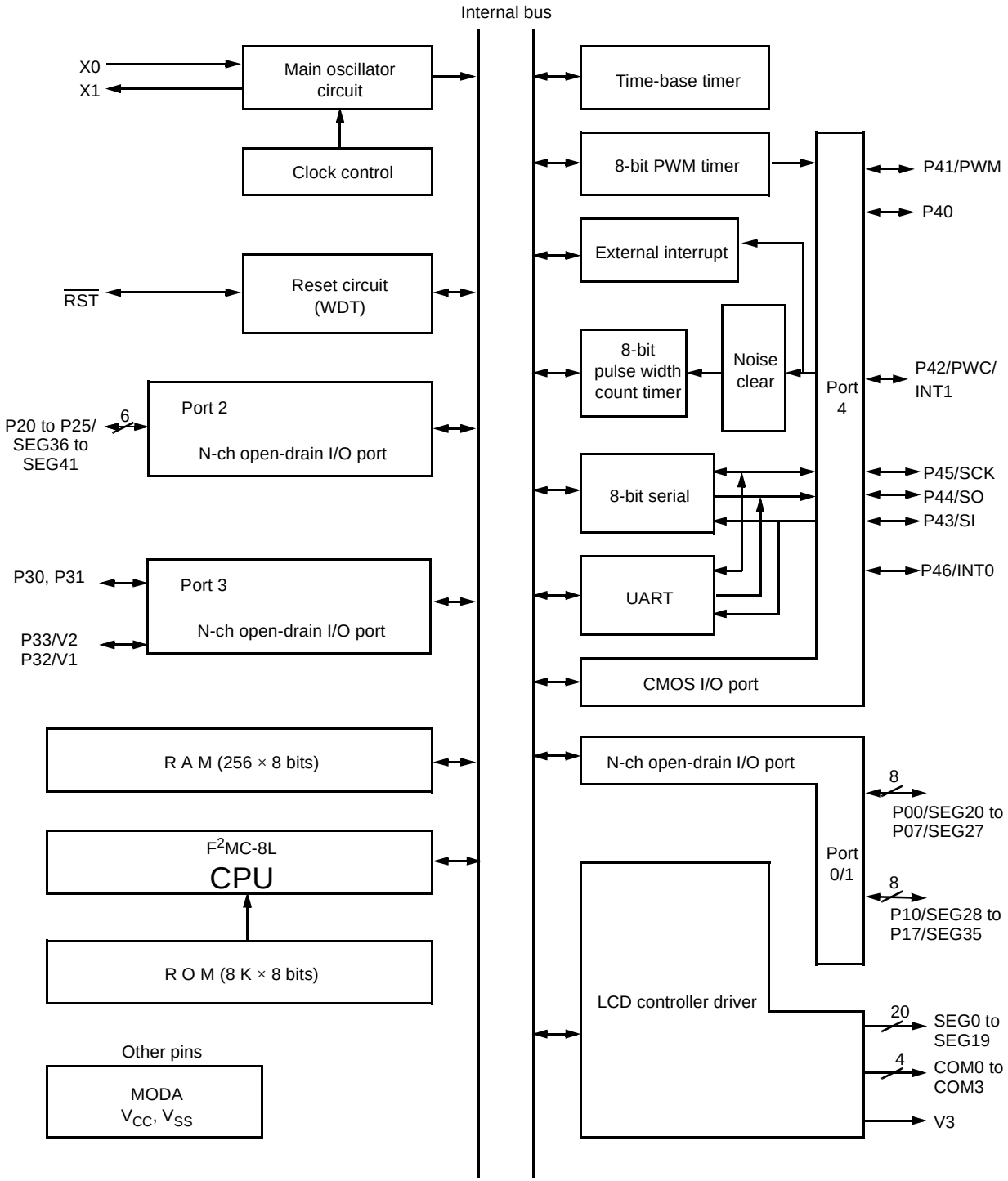


Fig. 1.1 Block Diagram (MB89953)

1.4 Pin Assignment

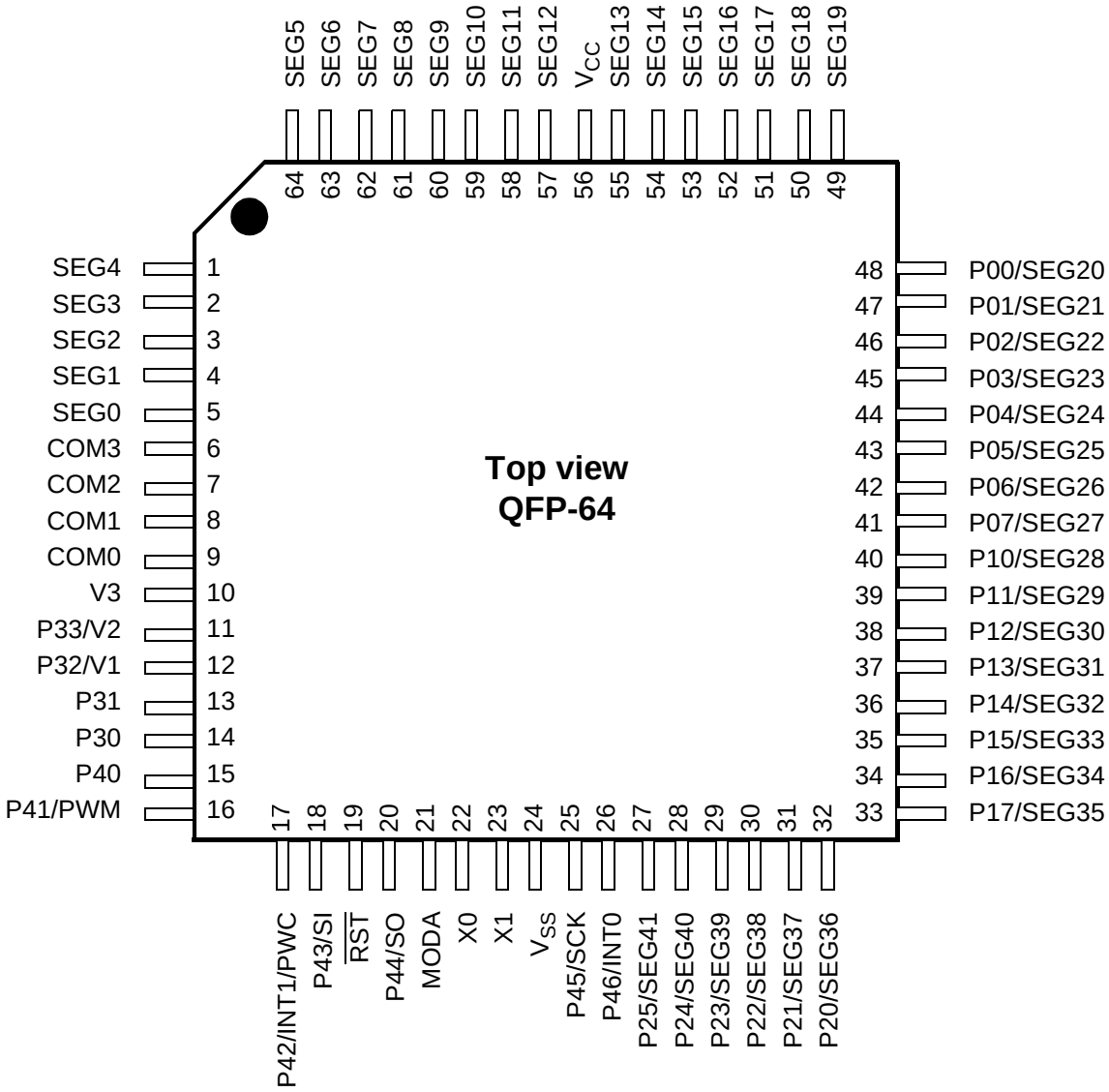


Fig. 1.2 Pin Assignment of MB89953 and MB89P955 (QFP-64, pitch: 0.65 mm)

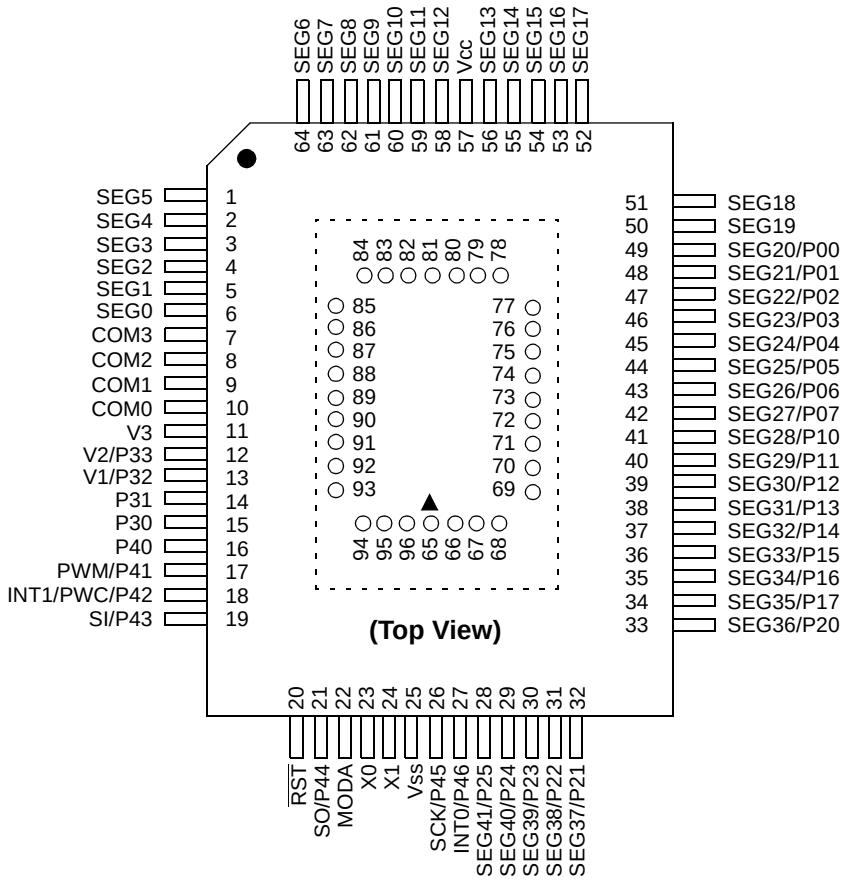


Fig. 1.3 Pin Assignment of MB89PV950 (MQFP-64, pitch: 0.8 mm)

Pin assignment on package top (MB89PV950 only)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	Vpp	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	Vss	88	A10	96	Vcc

N.C.: Non connection pin. Keep open.

1.5 Pin Description

Table 1–2 lists the pin functions and shows the Fig. 1.4 input/output circuits.

Table 1–2 Pin Description

Pin No		Pin Name	Circuit	Function
0.65	0.8			
22	23	X0	A	Clock oscillator pins
23	24	X1		
21	22	MODA	B	Operation-mode select pins This pin is connected directly to V_{SS} with pull down resistor.
19	20	$\overline{RST}$	C	Reset I/O pin This pin consists of an N-ch open-drain output with a pull-up resistor and hysteresis input. A Low level is put out from this pin. A “LOW” voltage on this port generates a RESET condition.
48 to 41	49 to 42	P00/SEG20 to P07/SEG27	D	N-channel open-drain type general-purpose I/O ports Also serve as LCDC controller segment outputs. Switching between port output and segment output is performed by the mask option every 8 bits.
40 to 33	41 to 34	P10/SEG28 to P17/SEG35	D	N-channel open-drain type general-purpose I/O ports Also serve as LCDC controller segment outputs. Switching between port output and segment output is performed by the mask option.
32 to 27	33 to 28	P20/SEG36 to P25/SEG41	D	N-channel open-drain type general-purpose I/O ports Also serve as LCDC controller segment outputs. Switching between port output and segment output is performed by the mask option.
14 to 11	15 to 12	P30 to P31	F	N-channel open-drain type general-purpose I/O ports
12 to 11	13 to 12	P32/V1 to P33/V2	D	N-channel open-drain type general-purpose I/O ports Also serve as LCDC controller power supply.
15	16	P40	E	General-purpose I/O ports A pull-up resistor option is provided.
16	17	P41/PWM	E	General-purpose I/O port Serves as PWM timer toggle output (PWM). A pull-up resistor option is provided.
17	18	P42/PWC/ INT1	E	General-purpose I/O port Also serves as pulse-width count timer input (PWC) and external interrupt input (INT1). The PWC and INT1 inputs are hysteresis type. A pull-up resistor option is provided.
18	19	P43/SI	E	General-purpose I/O port Also serves as serial I/O and UART data input (SI). The SI input is hysteresis type. A pull-up resistor option is provided.
20	21	P44/SO	E	General-purpose I/O port Also serves as serial I/O and UART data output (SO). A pull-up resistor option is provided.
25	26	P45/SCK	E	General-purpose I/O port Also serves as serial I/O and UART clock input/output (SCK). The SCK input is hysteresis type. A pull-up resistor option is provided.

Table 1–2 Pin Description *(Continued)*

Pin No		Pin Name	Circuit	Function
0.65	0.8			
26	27	P46/INT0	E	General-purpose input port Also serves as external-interrupt input (INT0). The input is hysteresis type. A pull-up resistor option is provided.
5 to 1 64 to 57 55 to 49	6 to 1 64 to 58 56 to 50	SEG0 to SEG19	G	For LCDC controller segment ouput
9 to 6	7 to 10	COM0 TO COM3	G	For LCDC controller common output
10	11	V3	-	For LCD driver power supply
56	57	Vcc	-	Power Pin
24	25	Vss	-	Power (GND) Pin

Table 1–3 Pin Description for External ROM

• External EPROM pins (for MB89PV950)

Pins No.	Pin Name	I/O	Function
66	Vpp	O	For High-level output
67	A12	O	For address output
68	A7		
69	A6		
70	A5		
71	A4		
72	A3		
73	A2		
74	A1		
75	A0		
77	O1	I	For data input
78	O2		
79	O3		
80	Vss	O	For power supply (GND)
82	04	I	For data input
83	O5		
84	O6		
85	O7		
86	O8		
87	$\overline{CE}$	O	For ROM output enable The High level is output in standby mode.
88	A10	O	For address output
89	$\overline{OE}$	O	For ROM output enable. The Low level is always output.
91	A11	O	For address output
92	A9		
93	A8		
94	A13	O	For address output
95	A14		
96	Vcc	O	For EPROM power supply

Table 1–3 Pin Description for External ROM *(Continued)*

• External EPROM pins (for MB89PV950)

Pins No.	Pin Name	I/O	Function
65 76 81 90	N.C.	—	For internal connection Keep open.

Fig. 1.4 I/O Circuits

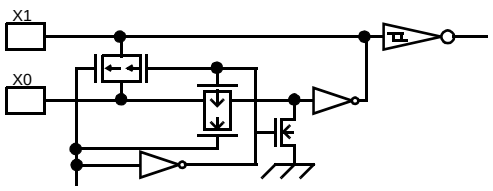
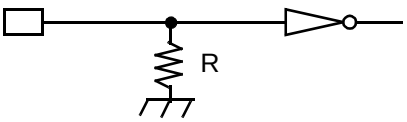
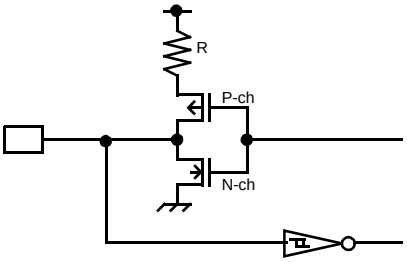
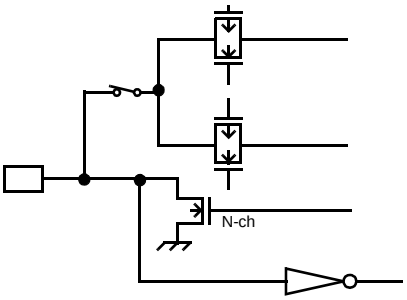
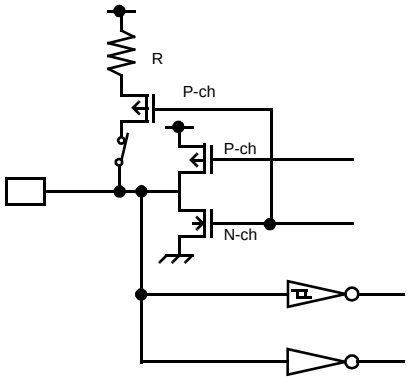
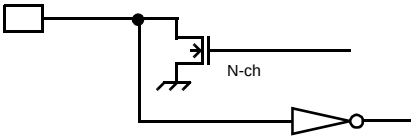
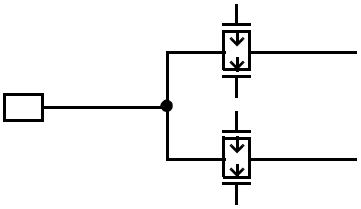
Classification	Circuit	Remarks
A	 Standby control signal	• Crystal oscillator • Feedback resistor: About 1 MΩ/ 5 V (1 to 5 MHz)
B		• CMOS input • Pull down resistor (N-ch)
C		• Output pull-up resistor (P-ch): • About 50 MΩ (5 V) • Hysteresis input
D		• N-ch open-drain output • CMOS input • The segment output is optional.

Fig. 1.4 I/O Circuits *(Continued)*

Classification	Circuit	Remarks
E		• CMOS output • CMOS input • Hysteresis input (peripheral input) • The pull-up resistor is optional.
F		• N-ch open-drain output • CMOS input
G		• LCDC output

1.6 Handling Devices

(1) Preventing latch-up

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium to high-voltage pins or if higher than the voltage which shows on Absolute Maximum Ratings is applied between V_{CC} and V_{SS}.

When latch-up occurs, supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

(2) Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down resistor.

(3) Power Supply Voltage Fluctuations

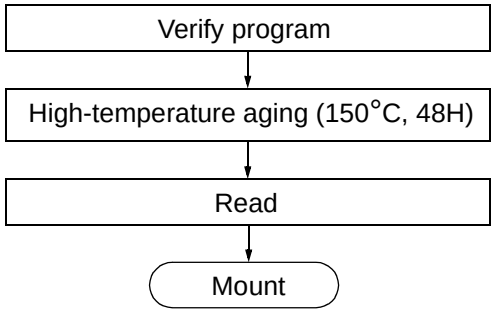
Although V_{CC} power supply voltage is assured to operate within the rated, a rapid change to the IC is therefore cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied of the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P. value) will be less that 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

(4) Precaution When Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (option selection) and release from stop mode.

(5) Recommended Screening Conditions

The OTPROM product should be screened by high-temperature aging before mounting.



The programming test cannot be performed for all bits of the preprogrammed OTPROM product due to its characteristics. Consequently, 100% programming yielding cannot be ensured.

2. HARDWARE CONFIGURATION

This chapter describes each block of the CPU hardware.

CPU

2.1 CPU

This section describes the memory space and register composing CPU hardware.

2.1.1 Memory Space

F^2MC-8L CPU has a memory space of 64 Kilobytes. All I/O, data, and program areas are located in this space. The I/O area is near the lowest address and the data area is immediately above it. The data area can be divided into register, stack, and direct-address areas according to the applications. The program area is located near the highest address, and the tables of interrupt and reset vectors and vector-call instructions are at the highest address in this area. Fig.2.1 shows the structure of the memory space for the MB89950 series of microcontrollers.

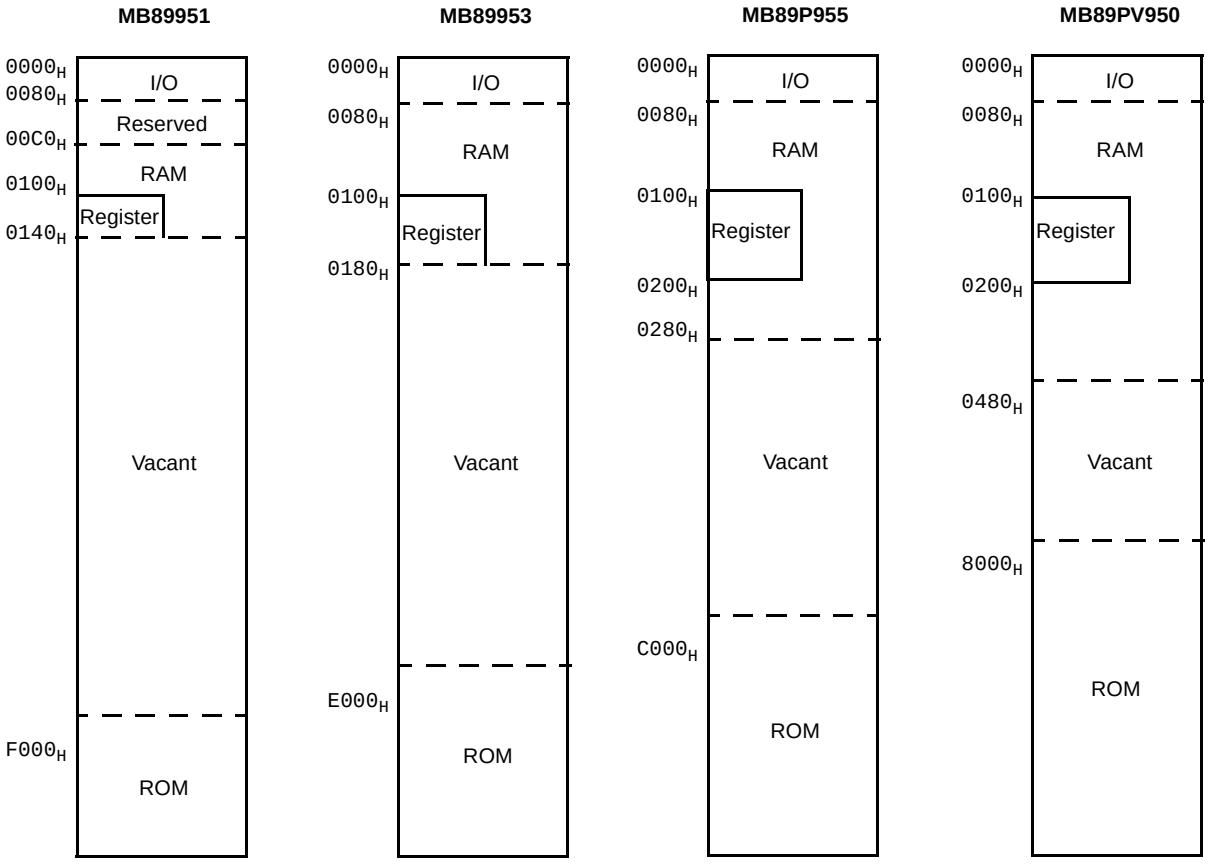


Fig. 2.1 Memory Space of MB89950 Series Microcontrollers

CPU

(1) I/O area

This area is where various peripherals such as control and data registers are located. The memory map for the I/O area is given in APPENDIX A.

(2) RAM area

This area is where the static RAM is located. Addresses from 0100_H to $017F_H$ (0100_H to $013F_H$ in MB89951, 0100_H to $01FF0_H$ in MB89P955 and MB89PV950) are also used as the general-purpose register area. One can access these registers through register-related instructions or just treat them as ordinary RAM.

(3) ROM area

This area is where the internal ROM is located. Addresses from $FFC0_H$ to $FFFF_H$ are also used for the table of interrupt, reset and vector-call instructions. Table 2–1 shows the correspondence between each interrupt number or reset and the table addresses to be referenced for the MB89950 series of microcontrollers.

Table 2–1 Table of Reset and Interrupt Vectors

	Table address	
	Upper data	Lower data
CALLV #0	$FFC0_H$	$FFC1_H$
CALLV #1	$FFC2_H$	$FFC3_H$
CALLV #2	$FFC4_H$	$FFC5_H$
CALLV #3	$FFC6_H$	$FFC7_H$
CALLV #4	$FFC8_H$	$FFC9_H$
CALLV #5	$FFCA_H$	$FFCB_H$
CALLV #6	$FFCC_H$	$FFCD_H$
CALLV #7	$FFCE_H$	$FFCF_H$

	Table address	
	Upper data	Lower data
Interrupt #B	$FFE4_H$	$FFE5_H$
Interrupt #A	$FFE6_H$	$FFE7_H$
Interrupt #9	$FFE8_H$	$FFE9_H$
Interrupt #8	$FFEA_H$	$FFEB_H$
Interrupt #7	$FFEC_H$	$FFED_H$
Interrupt #6	$FFEE_H$	$FFEF_H$
Interrupt #5	$FFF0_H$	$FFF1_H$
Interrupt #4	$FFF2_H$	$FFF3_H$
Interrupt #3	$FFF4_H$	$FFF5_H$
Interrupt #2	$FFF6_H$	$FFF7_H$
Interrupt #1	$FFF8_H$	$FFF9_H$
Interrupt #0	$FFFA_H$	$FFFB_H$
Reset mode	-----	$FFFD_H$
Reset vector	$FFFE_H$	$FFFF_H$

Note: $FFFC_H$ is already reserved. When using $FFFD_H$ in the reset mode, write 00_H.

CPU

2.1.2 Arrangement of 16-bit Data in Memory Space

When the MB89950 series of microcontrollers handle 16-bit data, the data written at the lower address is treated as the upper 8-bit data and that written at the next address is treated as the lower 8-bit data as shown in Fig. 2.2.

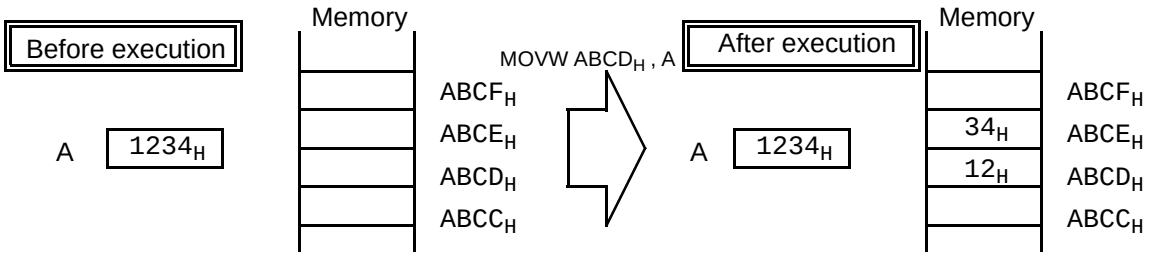
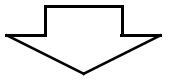


Fig. 2.2 Arrangement of 16 bit Data in Memory Space

This is the same when 16 bits are specified by the operand during execution of an instruction. Bits closer to the OP code are treated as the upper byte and those next to it are treated as the lower byte. This is also the same when the memory address or 16-bit immediate data is specified by the operand.

[Example]

```
MOV A, 5678H      ; Extended address
MOV A, #1234H     ; 16-bit immediate data
```




```
XXXXH XX XX
XXXXH 60 56 78   ; Extended address
XXXXH E4 12 34   ; 16-bit immediate data
XXXXH XX
```

Fig. 2.3 Arrangement of 16 bit Data during Execution of Instruction

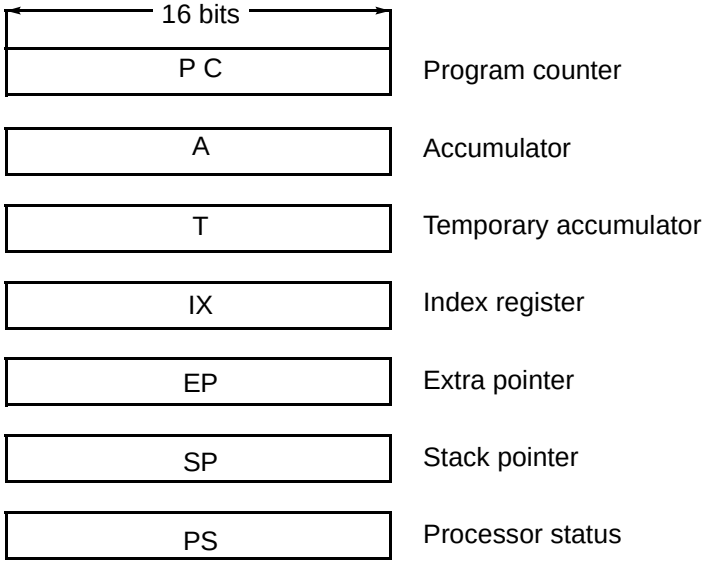
Data saved in the stack by an interrupt is also treated in the same manner.

CPU

2.1.3 Internal Registers in CPU

The MB89950 series of microcontrollers have dedicated registers in the CPU and general-purpose registers in memory. The types of dedicated registers are as follows.

- Program counter (PC) — 16-bit length register indicating the location where instructions are stored.
- Accumulator (A) — 16-bit length register storing results of operations temporarily. The lower one byte is used to execute 8-bit data processing instructions.
- Temporary accumulator (T) — 16-bit length register where the operations are performed between this register and the accumulator. The lower one byte is used to execute 8-bit data processing instructions.
- Index register (IX) — 16-bit length register for index modification.
- Extra pointer (EP) — 16-bit length register for indicating memory address.
- Stack pointer (SP) — 16-bit length register indicating stack area.
- Processor status (PS) — 16-bit length register where register pointers and condition codes are stored.



CPU

The 16 bits of the processor status (PS) can be divided into 8 upper bits for a register bank pointer (RP) and 8 lower bits for a condition code register (CCR). (See Fig. 2.4.)

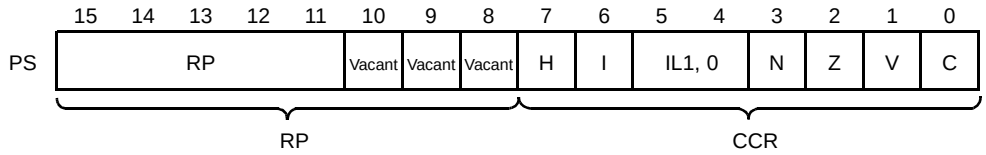


Fig. 2.4 Structure of Processor Status

The RP indicates the address of the current register bank. The relationship between the contents of the RP and the real addresses is as shown in Figure 2.5.

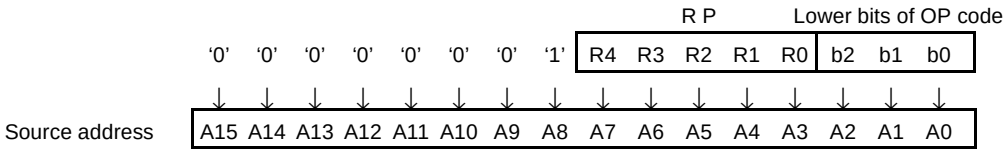


Fig. 2.5 Rule for Translating Real Addresses at General-purpose Register Area

The CCR has bits indicating the results of operations and transfer data contents, and bits controlling the CPU operation when an interrupt occurs.

- H-flag H-flag is set when a carry or a borrow out of bit 3 into bit 4 is generated as a result of operations; it is cleared in other cases. This flag is used for decimal-correction instructions.

- I-flag An interrupt is enabled when this flag is 1 and is disabled when it is 0. The I-flag is 0 at reset.

- IL1 and IL0 These bits indicate the level of the currently-enabled interrupt. The CPU executes interrupt processing only when an interrupt with a value smaller than the value indicated by this bit is requested.

IL1	IL0	Interrupt level	High and low
0	0	1	High ↕ low = No interrupt
0	1		
1	0	2	
1	1	3	

- N-flag The N-flag is set when the most significant bit is 1 as a result of operations; it is cleared when the MSB is 0.

CPU

- Z-flag Z-flag is set when zero is the result of operations; it is cleared in other cases.
- V-flag V-flag is set when a two's complement overflow occurs as a result of operations; it is reset when an overflow does not occur.
- C-flag C-flag is set when a carry or a borrow out of bit 7 is generated as a result of operations; it is cleared in other cases. When the shift instruction is executed, the value of the C-flag is shifted out.

• General-purpose register..... 8-bit length register where data are stored.
8-bit general-purpose registers are provided in the register banks in the memory for storing data. Eight registers are provided per bank for and up to 16 banks can be used for MB89953 (8 banks are provided in MB89951, 32 banks are provided in MB89P955 and MB89PV950).
The register bank pointer (RP) indicates the currently-used bank.

Note: The register banks are as follows depend on RAM area.

MB89951	0100_H to $013F_H$	8 banks
MB89953	0100_H to $017F_H$	16 banks
MB89P955	0100_H to $01FF_H$	32 banks
MB89PV950	0100_H to $01FF_H$	32 banks

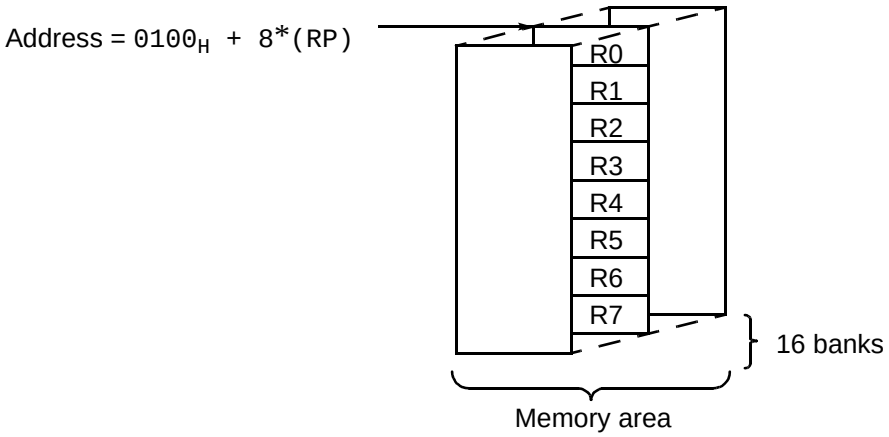


Fig. 2.6 Register Bank Configuration

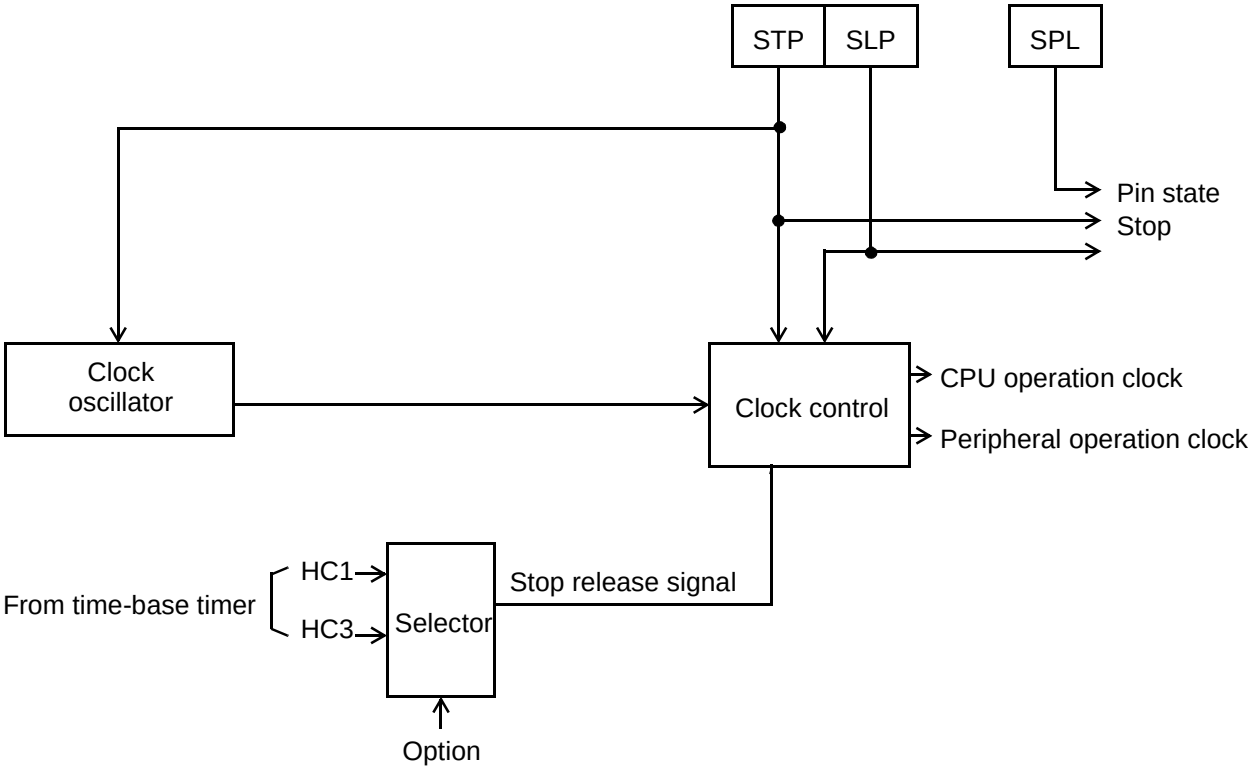
CPU

2.1.4 Clock Control Block

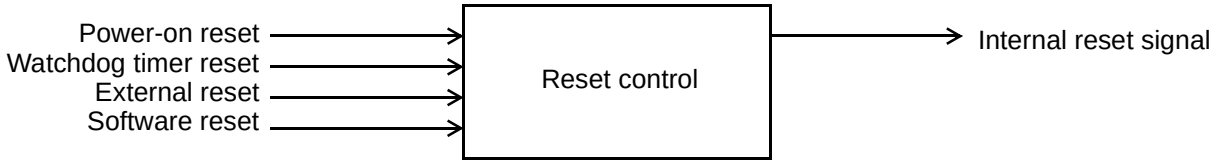
This block controls the standby operation and software reset.

(1) Machine clock control block diagram

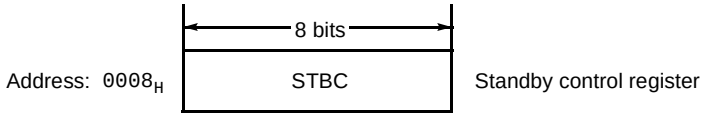
(a) Machine clock control section



(b) Reset control section



(2) Register list



CPU

(3) Description of registers

The detail of each register is described below.

Address: 0008_H STBC

(a) Standby control register (STBC)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0008_H	STP	SLP	SPL	RST	—	—	—	—
	(W)	(W)	(R/W)	(W)				
				(Initial value) $0001XXXX_B$				

[Bit 7] STP: Stop bit
This bit is used to specify switching CPU to the stop mode.

0	No operation
1	Stop mode

This bit is cleared at reset or stop cancellation.

0 is always read when this bit is read.

[Bit 6] SLP: Sleep bit
This bit is used to specify switching the CPU to the sleep mode.

0	No operation
1	Sleep mode

This bit is cleared at reset, sleep cancellation or stop cancellation.

0 is always read when this bit is read.

[Bit 5] SPL: Pin state specifying bit
This bit is used to specify the external pin state in the stop mode.

0	Holds pin state and level immediately before stop mode
1	High impedance

This bit is cleared at reset.

[Bit 4] RST: Software reset bit
This bit is used to specify the software reset.

0	Generates 4-cycle reset signal
1	No operation

1 is always read when this bit is read.

CPU

(4) Description of operation

(a) Low-power consumption mode

This chip has three operation modes shown in the table below. The sleep mode and stop mode reduce the power consumption. The system clock can be selected out of three according to the system condition to minimize power consumption.

Table 2–2 Operating Mode of Low-power Consumption Modes

Oscillation mode	Clock pulse	Each operating clock pulse (5 MHz clock)			Wake-up source in each mode
		CPU	Time-base timer	Each peripheral	
RUN	Oscillates	2.5 MHz	2.5 MHz	2.5 MHz	Various interrupt requests
SLEEP		Stops			
STOP	Stop		Stops	Stops	External interrupt

- The SLEEP mode stops only the operating clock pulse of the CPU; other operations are continued.
- The STOP mode stops the oscillation. Data can be held with the lowest power consumption in this mode.

a. SLEEP mode

- Switching to Sleep mode
  - Writing 1 at the SLP (bit 6) of the STBC register switches the mode to SLEEP mode.
  - The SLEEP mode is the mode to stop clock pulse operating the CPU; only the CPU stops and the peripherals continue to operate.
  - If an interrupt is requested when 1 is written at the SLP (bit 6), instruction execution continues without switching to the SLEEP mode.
  - In the SLEEP mode, the contents of registers and RAM immediately before entering the SLEEP mode are held.
- Canceling SLEEP mode
  - The SLEEP mode is canceled by inputting the reset signal or requesting an interrupt.
  - When the reset signal is input during the SLEEP mode, the CPU is switched to the reset state and the SLEEP mode is canceled.
  - When an interrupt level higher than 11 is requested from a peripheral during the SLEEP mode, the SLEEP mode is canceled.
  - When the I flag and IL bit are enable after canceling, the CPU executes the interrupt processing like an ordinary interrupt. When they are disabled, the CPU starts processing the next instruction given before entering the SLEEP mode.

CPU

b. STOP mode

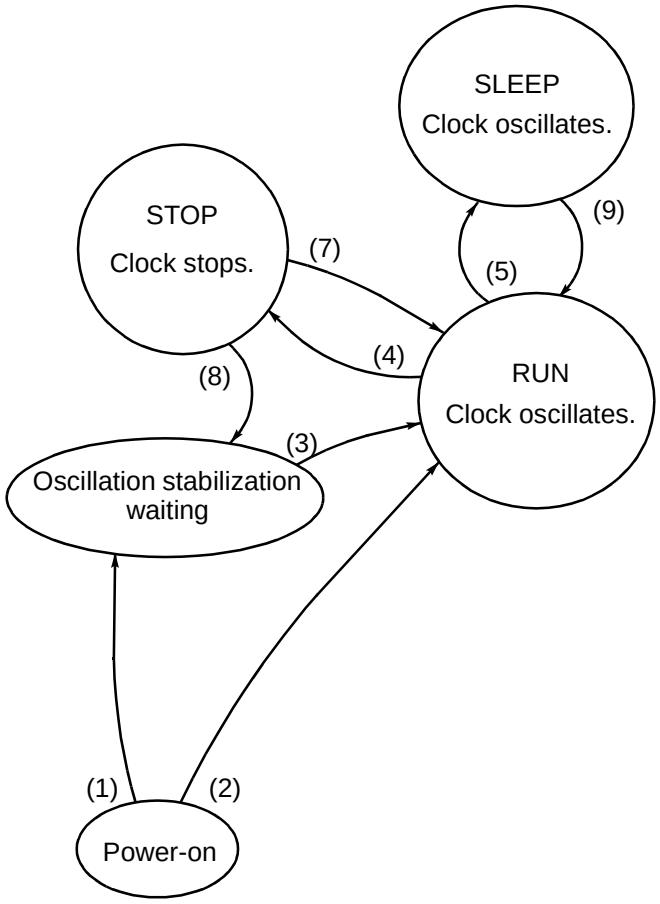
- Switching to STOP mode
  - Writing 1 at the STP (bit 7) of the STBC register switches the mode to STOP mode.
  - The STOP mode stops clock oscillation and the CPU and all peripherals stop.
  - The input/output pins and output pins in the STOP mode can be controlled by the SPL (bit 5) of the STBC register so that they are held in the state immediately before entering the STOP mode, or so that they enter in the high-impedance state.
  - If an interrupt is requested when 1 is written at the STP (bit 7), instruction execution continues without switching to the STOP mode.
  - In the STOP mode, the contents of registers and RAM immediately before entering the STOP mode are held.
- Canceling STOP mode
  - The STOP mode is canceled either by inputting the reset signal or by requesting an interrupt.
  - When the reset signal is input during the STOP mode, the CPU is switched to the reset state and the STOP mode is canceled.
  - When an interrupt higher than level 11 is requested from the external interrupt circuit during the STOP mode, the STOP mode is canceled.
  - When the I flag and IL bit are enabled after canceling, the CPU executes the interrupt processing like an ordinary interrupt. When they are disabled, the CPU starts processing the next instruction given before entering the STOP mode.
  - The oscillation stabilization time can be selected from the two types in Table 2–3 as options.
  - If the STOP mode is canceled by inputting the reset signal, the CPU is switched to the oscillation stabilization state. Therefore, the reset sequence is not executed unless the oscillation stabilization time is elapsed. The oscillation stabilization time corresponds to the optionally selected oscillation stabilization time of the main clock. However, when Power-on reset unavailable is selected by the mask option, the CPU is not switched to the oscillation stabilization state even if the STOP mode is canceled by inputting the reset signal.

Table 2–3 Selection of Oscillation Stabilization Time

Oscillation stabilization time	Oscillation stabilization time at 5 MHz	Remarks
About $2^{18}/f_{CH}$	About 52.4 ms	For crystal oscillator
About $2^{14}/f_{CH}$	About 3.28 ms	For crystal oscillator

CPU

(b) State transition diagram



(1) When power-on reset available selected
(2) When power-on reset unavailable selected
(3) After oscillation stabilizing
(4) Set STP bit to 1.
(5) Set SLP bit to 1.
(7) External reset when power-on reset unavailable selected
(8) External reset or interrupt when power-on reset available selected
(9) External reset or interrupt

CPU

(c) Reset

There are four types of reset depending on the source shown in Table 2–4.

Table 2–4 Sources of Reset

Reset name	Description
External-pin reset	When setting external-reset pin to Low
Software reset	When writing 0 at RST (bit 4) of STBC
Watchdog reset	When watchdog timer overflows
Power-on reset	When turning power on

When the power-on reset or reset during the stop state is used, the oscillation stabilization time is needed after the oscillator starts operating. The time-base timer controls this stabilization time. Consequently, the operation does not start immediately even after canceling the reset.

However, if Power-on reset is not selected by the mask option, no oscillation stabilization time is required in any state after external pins have been released from the reset.

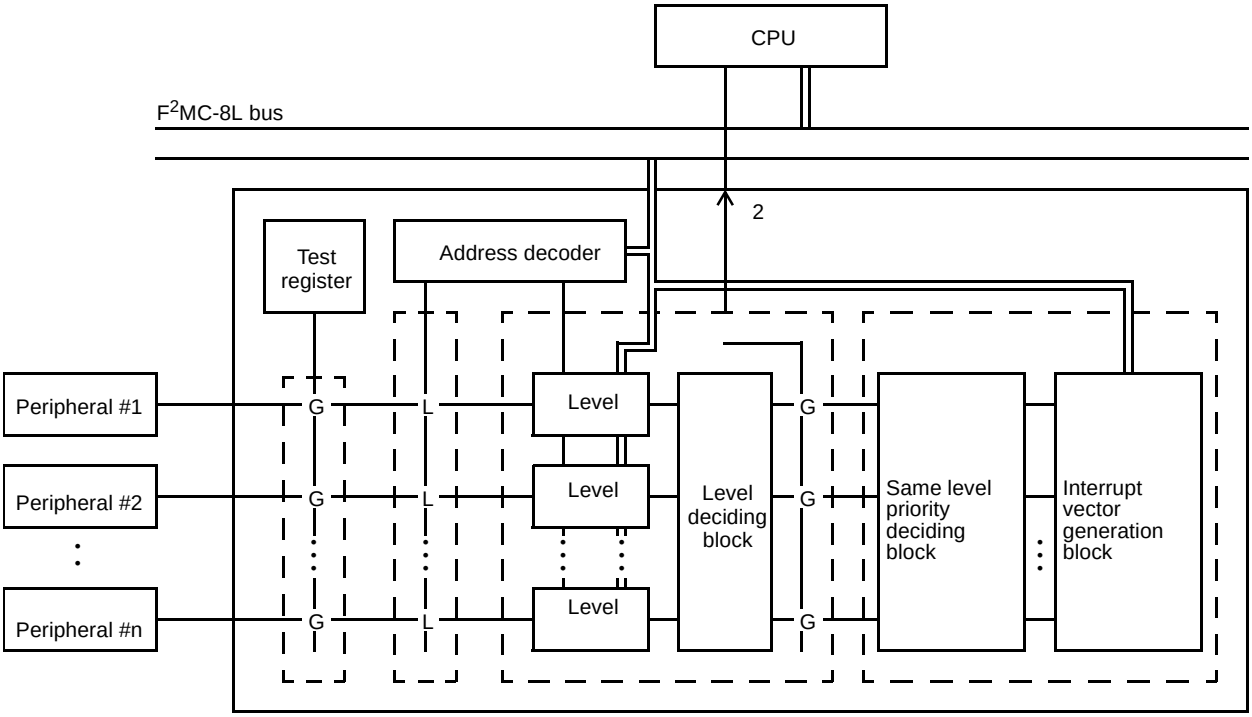
Note: A longer time than the optionally-specified oscillation stabilization time should be allowed for reset at power-on of Power-on reset unavailable products. In other cases, the time is based on theorist timing given in the ***MB89950 SERIES DATA SHEET*** "AC characteristics."

CPU

2.1.5 Interrupt Controller

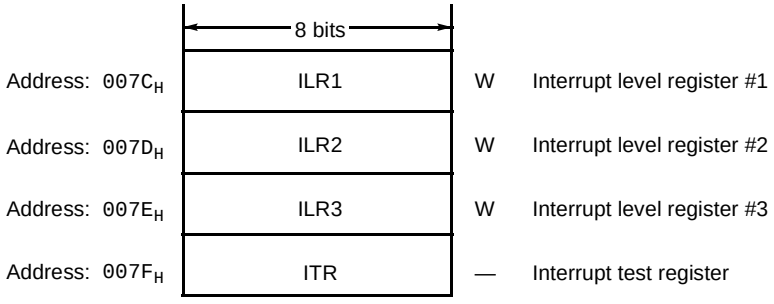
The interrupt controller for the F^{2}MC-8L family is located between the CPU and each peripheral. This controller receives interrupt requests from the peripherals, assigns priority to them. When the interrupt controller transfers the priority to the CPU, it also decides the priority of same-level interrupts.

(1) Block diagram



(2) Register list

Interrupt controller consists of interrupt-level registers (ILR1, 2, and 3) and interrupt-test register (ITR).



CPU

Address: $007C_H$ ILR1

Address: $007D_H$ ILR2

Address: $007E_H$ ILR3

Address: $007F_H$ ITR

(3) Description of registers

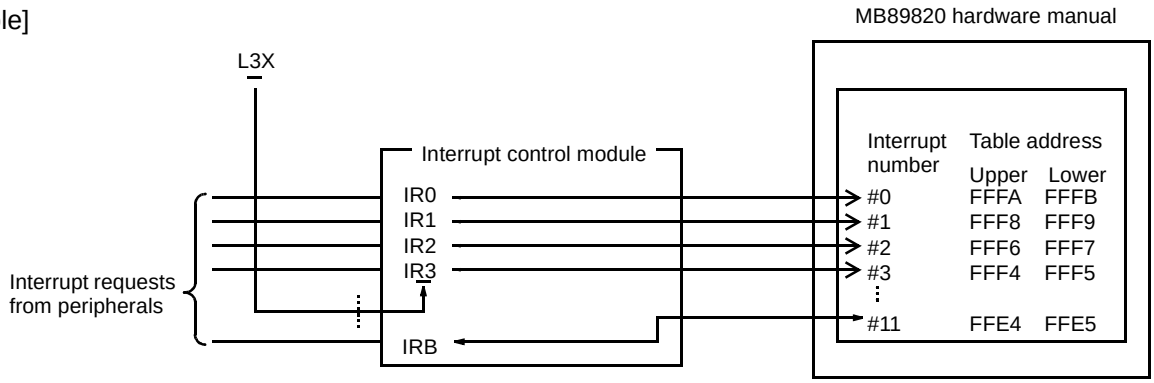
The details of each register is described below.

(a) Interrupt level register 1 to 3 (ILRx: Interrupt Level Register x)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $007C_H$	L31	L30	L21	L20	L11	L10	L01	L00
Address: $007D_H$	L71	L70	L61	L60	L51	L50	L41	L40
Address: $007E_H$	LB1	LB0	LA1	LA0	L91	L90	L81	L80
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)
(Initial value)	11111111_B							

The ILRx sets the interrupt level of each peripheral. The digits in the center of each bit correspond to the interrupt numbers.

[Example]



[Bits 7 and 6][Bits 5 and 4][Bits 3 and 2][Bits 1 and 0]Lx1, Lx0: Interrupt level setting bit

Lx1	Lx0	Required interrupt level
0	X	1
1	0	2
1	1	3 (None)

When an interrupt is requested from a peripheral, the interrupt controller transfers the interrupt level based on the value set at the 2 bits of the ILRx corresponding to the interrupt to the CPU.

Address: $007C_H$ ILR1

Address: $007D_H$ ILR2

Address: $007E_H$ ILR3

Address: $007F_H$ ITR

(b) Interrupt test register (ITR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $007F_H$	—	—	—	—	—	—	*	*
							(—)	(—)
(Initial value)	$XXXXXX00_B$							

The ITR is used for testing. Do not access it.

CPU

(4) Description of operation

The functions of interrupt controllers are described below.

(a) Interrupt functions

The MB89950 series of microcontrollers have 7 inputs for interrupt requests from the peripherals. The interrupt level is set by 2-bit registers corresponding to each input. When an interrupt is requested from a peripheral, the interrupt controller receives it and transfers the contents of the corresponding level register to the CPU. The interrupt to the device is processed as follows:

(1) An interrupt source is generated inside a peripheral.
(2) If an interrupt is enabled after referring to the interrupt-enable bit inside the peripheral, an interrupt request is output from the peripheral to the interrupt controller.
(3) After receiving this interrupt request, the interrupt controller determines the priority of simultaneously-requested interrupts and then transfers the interrupt level for the applicable interrupt to the CPU.
(4) The CPU compares the interrupt level requested from the interrupt controller with the IL bit in the processor status register.
(5) As a result of the comparison, if the interrupt level has priority over the current interrupt processing level, the contents of the I-flag in the same processor status register are checked.
(6) As a result of the check in step (5), if the I-flag is enabled for an interrupt, the contents of the IL bit are set to the required level. As soon as the currently-executing instruction is terminated, the CPU performs the interrupt processing and transfers control to the interrupt-processing routine.
(7) When an interrupt source is cleared by software in the user's interrupt processing routine, the CPU terminates the interrupt processing.

Fig. 2.7 outlines the interrupt operation for the MB89950 series of microcontrollers.

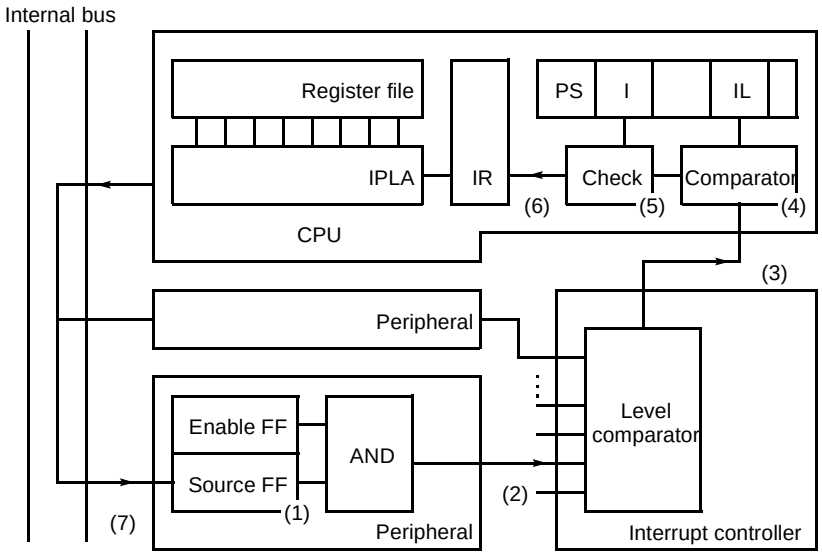


Fig. 2.7 Interrupt-processing Flowchart

Peripherals

2.2 Peripherals

2.2.1 I/O Ports

- The MB89950 series of microcontrollers have five parallel ports (33 pins). Ports 0 and 1 serve as 8-bit I/O ports; port 2 serves 6-bit I/O port; port 3 serves as 4-bit I/O ports; port 4 serves as 7-bit I/O port.
- Ports 0, 1, 2, 3 and 4 are also used as peripherals.

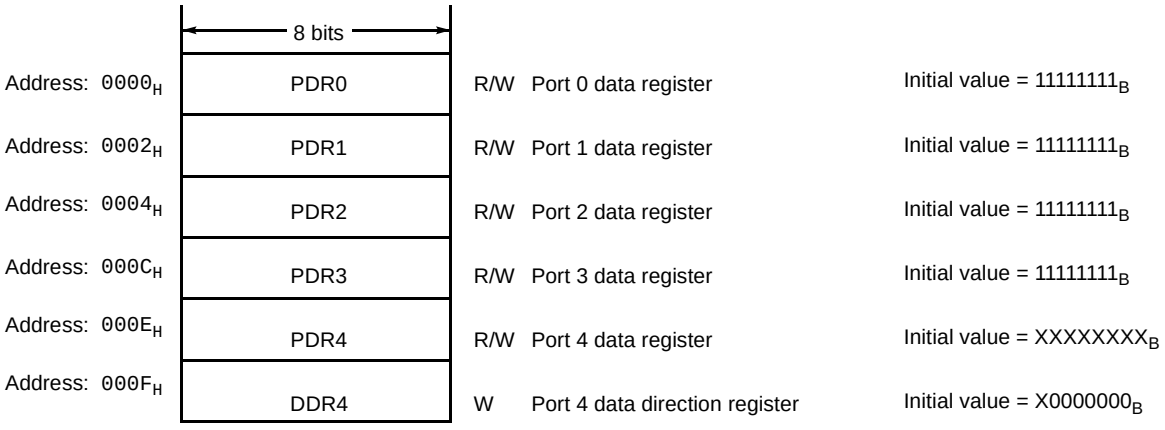
(1) List of port functions

Table 2–5 List of Port Functions

Pin	Input Type	Output Type	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P00 to P07	CMOS	N-ch open drain	Parallel port 0	P07	P06	P05	P04	P03	P02	P01	P00
			Segment output	SEG 27 ——— SEG20							
P10 to P17	CMOS	N-ch open drain	Parallel port 1	P17	P16	P15	P14	P13	P12	P11	P10
			Segment port 1	SEG 35 ——— SEG28							
P20 to P25	CMOS	N-ch open drain	Parallel port 2	—	—	P25	P24	P23	P22	P21	P20
				—	—	SEG41 ——— SEG36					
P30 to P33	CMOS	N-ch open drain	Parallel port 3	—	—	—	—	P33	P32	P31	P30
			LCD voltage	—	—	—	—	V2	V1	—	—
P40 to P45	CMOS	CMOS push-pull	Parallel port 4	—	P46	P45	P44	P43	P42	P41	P40
	Hysteresis		Timer serial/external interrupt	—	INT0	SCK	SO	SI	PWC /INT1	PWM	—

(2) Register list

I/O port consists of the following registers.



Peripherals

(3) Description of functions

The function of each port is described below.

P00 to P07: N-ch open-drain type input/output ports (also used as segment output)

P10 to P17: N-ch open-drain type input/output ports (also used as segment output)

P20 to P25: N-ch open-drain type input/output ports (also used as segment output)

- Operation for output port
  The value written at the PDR is output to the pin. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other.

- Operation for input port
  When using these ports as input ports, set 1 at the PDR and turn the output transistor off. The value of the pin can always be read when the PDR is read. When the segment output is selected by the LCD controller port/segment select bit, the input data is always read as 0.

- Operation for segment output
  When using these ports as segment outputs, the segment output must be selected by the mask option. When segment output is selected using the LCD controller port/segment select bit, these ports can be used as segment outputs.

- State at reset
  At reset, these ports serve as port inputs. The PDR is initialized to 1 and the output transistor is turned off at all bits.

- State in stop mode
  For segment output, the output state when the CPU enters the stop mode is held. For port output, the pins states in stop mode are controlled by SPL bit in standby control register (STBC).
  When SPL=0, pin states before entering stop mode are held.
  When SPL=1, port pins go high impedance in stop mode.

Peripherals

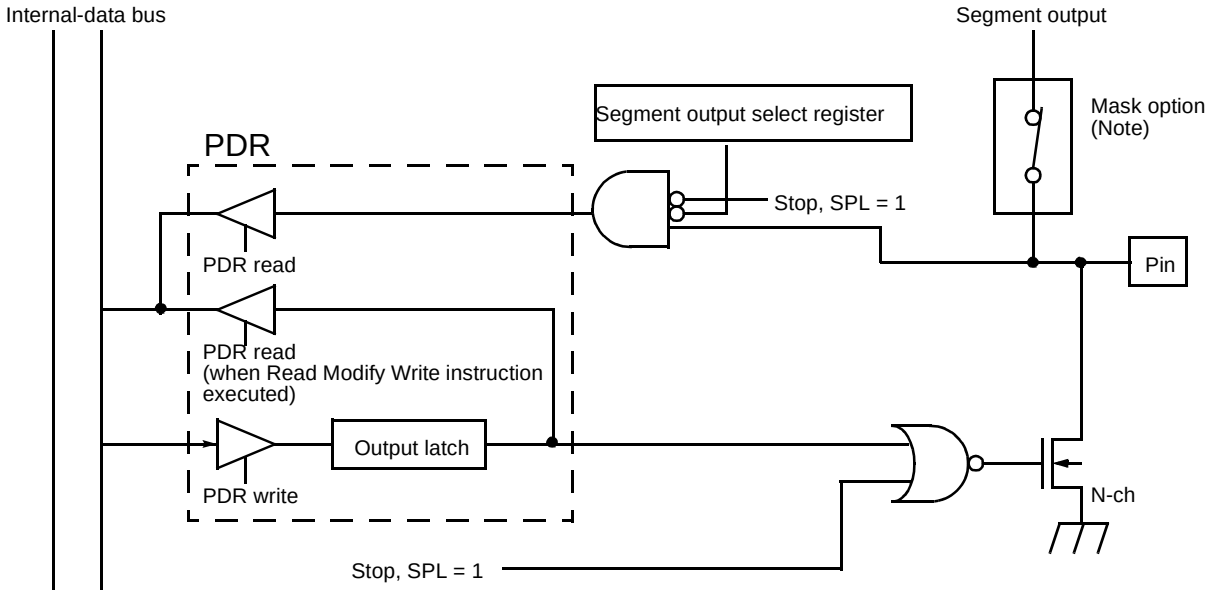


Fig. 2.8 Ports 0, 1 and 2

Note: Selection of segment output using the mask option is available only for mass-produced products. The mask option must be consistent with LCD segment output select register (SEGR).

Peripherals

P30, P31: N-ch open-drain output, CMOS input
P32, P33: N-ch open-drain type input/output ports
(also used as LCD controller power supply V1,V2)

- Operation for output port
  The value written at the PDR is output to the pin. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other.

- Operation for input port
  When using these ports as input ports, set 1 at the PDR and turn the output transistor off. The value of the pin can always be read when the PDR is read. When V1/V2 is selected by PSEL bit of LCDR, the input data is always read as 0.

- Operation for V1 and V2
  The PSEL bit in LCDR (see page 2-60) must be cleared in order to choose P32/P33 as LCD controller power supply.

- State at reset
  At reset, these ports serve as LCD controller power supply. The PDR is initialized to 1 and the output transistor is turned off at all bits. Since PSEL bit of LCDR will be reset to zero (see page 2-60), therefore P32/P33 will be configured to V1/V2 right after reset.

- State in stop mode
  If P32/P33 is chosen as V1/V2 and stop mode is triggered, the voltage at those pins before stop mode will be held. For port output, the pins states in stop mode are controlled by SPL bit in standby control register (STBC).
  When SPL=0, pin states before entering stop mode are held.
  When SPL=1, port pins go high impedance in stop mode.

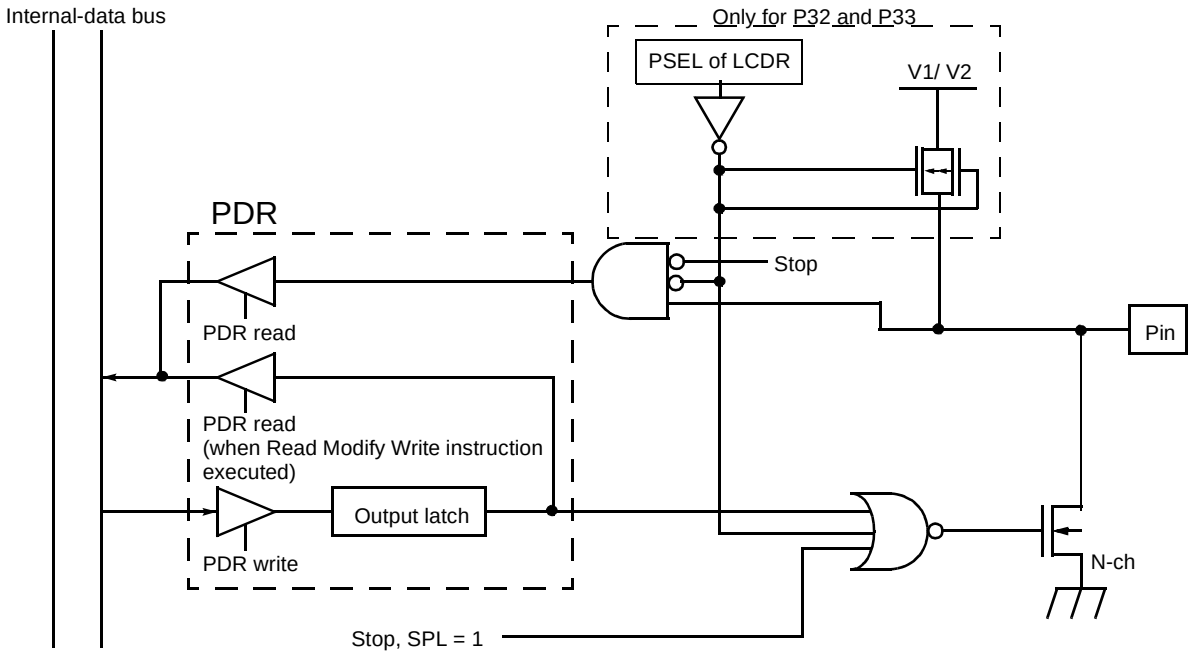

Internal-data bus
Only for P32 and P33
PSEL of LCDR
V1/ V2
PDR
Stop
PDR read
Pin
PDR read
(when Read Modify Write instruction
executed)
Output latch
PDR write
N-ch
Stop, SPL = 1

Fig. 2.9 Port 3

Peripherals

P40 to P46: CMOS type I/O ports
(also used as peripheral input and output)

- Switching input and output
  This port has a data-direction register (DDR) and a port-data register (PDR) for each bit. Input and output can be set independently for each bit. The pin with the DDR set to 1 is set to output, and the pin with the DDR set to 0 is set to input. When the peripheral output bit is enabled, these ports are set to output irrespective of the DDR setting conditions.
- Operation for output port (DDR = 1)
  The value written at the PDR is output to the pin where the DDR is set to 1. When the PDR is read, usually, the value of the pin is read instead of the contents of the output latch. However, when the Read Modify Write instruction is executed, the contents of the output latch are read irrespective of the DDR setting conditions. Therefore, the bit-processing instruction can be used even if input and output are mixed with each other. When data is written to the PDR, the written data is held in the output latch irrespective of the DDR setting conditions.
- Operation for input port (DDR = 0)
  When used as the input port, the output impedance goes High. Therefore, when the PDR is read, the value of the pin is read.
- Peripheral output operation
  When using as the peripheral output, setting is performed by the peripheral output enable bit (See the description of each peripheral). The peripheral output enable bit has priority in switching input and output. Even if the output from each peripheral is enabled, the read value of the port is effective, so the peripheral output value can be checked.
- Peripheral input operation
  The pin value at a port with the peripheral input function is always input for the peripheral input irrespective of the setting of the DDR and peripheral. Set the DDR to input when using an external signal for the peripheral input.
- State when reset
  When reset, the DDR is initialized to 0 and the output impedance goes High at all bits. When reset, the PDR is not initialized. Therefore, set the value of the PDR before setting the DDR to output.
- State in stop mode
  With the SPL bit of the standby-control register set to 1, the output impedance goes High in stop mode irrespective of the value of the DDR.

Peripherals

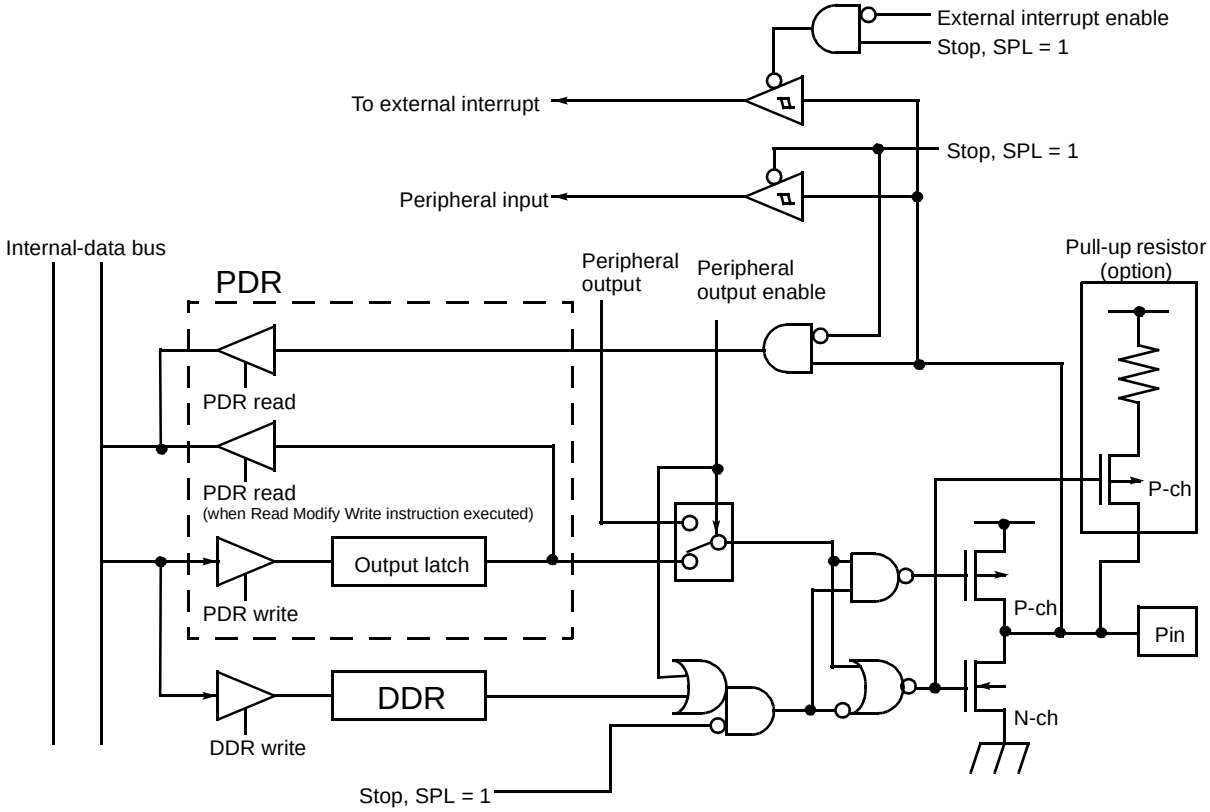


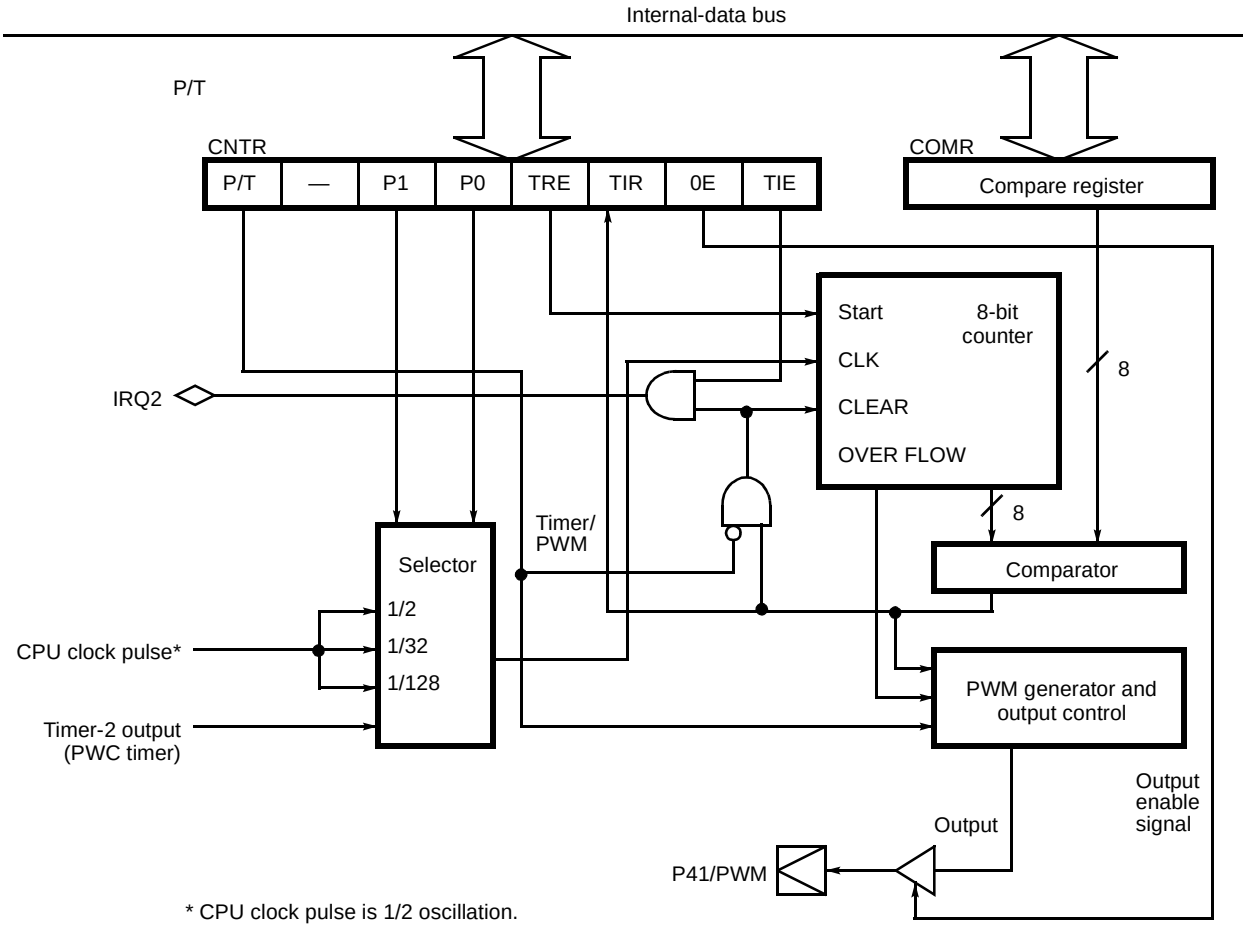
Fig. 2.10 Port 4

Peripherals

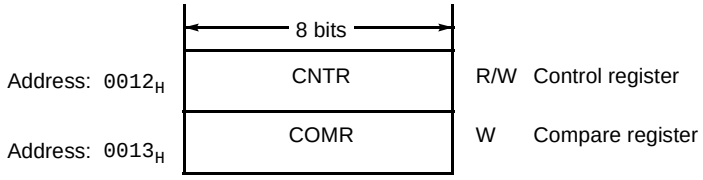
2.2.2 8-bit PWM Timer (Timer 1)

- This timer can be used as an 8-bit timer or PWM control circuit with 8-bit resolution.
- Four kinds of clock frequency can be selected.

(1) Block diagram



(2) Register list



Peripherals

Address: 0012H CNTR

Address: 0013H COMR

(3) Description of registers

(a) Control register (CNTR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0012_H	P/T	—	P1	P0	TPE	TIR	OE	TIE
	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
				(Initial value) $0X000000_B$				

[Bit 7] P/T: Timer/PWM operation mode switching bit

The operation is performed as the timer when bit 7 is set to 0, and as the

0	Timer
1	PWM control circuit

When switching, set channel to stop counting (TPE = 0), interrupt disabled (TIE = 0) and interrupt request flag cleared (TIR = 0).

[Bits 5 and 4] P1 and P0: Clock-pulse select bits

Clock pulses from the prescaler or WT0 output of timer 2 (pulse-width count timer) can be selected using P1 and P0.

P1	P0	Clock cycle
0	0	Internal clock pulse 1 instruction cycle
0	1	Internal clock pulse 16 instruction cycles
1	0	Internal clock pulse 64 instruction cycles
1	1	Timer 2 cycle

Note that these bits must not be rewritten when the counter is operating (TPE = 1).

[Bit 3] TPE: Counting enable bit

When these bits are set to 1, the timer or PWM control circuit starts operation.

0	Stops counting
1	Starts counting

[Bit 2] TIR1: PWM channel interrupt request flag bit

Bit 2 goes to 1 when an interrupt source occurs. To clear the generated interrupt source, write 0 at this bit. The meaning of bit to be read is as follows:

0	Values of counter and COMR do not match.
1	Values of counter and COMR match.

Peripherals

Note that 1 is always read when the Read Modify Write instruction is executed.

The meaning of each bit to be written is as follows:

0	Clears this bit
1	Does not change this bit nor affect other bits

Note: In the PWM operation mode, neither the read nor write values of these bits have any meaning.

[Bit 1] OE: Output signal control bit

When bit 1 is 1, the port serves as the PWM timer output. In the timer operation mode, a signal that is reversed each time the values of the counter and the compare register match is output. In the PWM operation mode, a PWM signal is output.

0	General-purpose ports (P41)
1	Counter/PWM output pins (PWM)

Even if the DDR of P41 is set for input (bit 1 of DDR4 is set to 1), when this bit is 1, it serves as the counter/PWM output pin.

[Bit 0] TIE: Interrupt enable bit (Timer mode)

If bit 0 is set to 1, an interrupt occurs when the values of the counter and the compare register match.

0	Disables counter interrupt output
1	Enables counter interrupt output

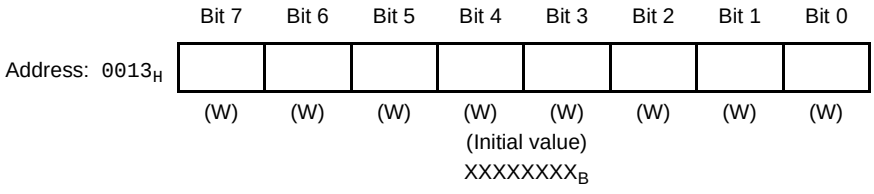
However, in the PWM operation mode, an interrupt does not occur irrespective of the value of this bits.

Address: 0012H CNTR

Address: 0013H COMR

(b) Compare register (COMR)

This register holds the value to be compared with the counter value in the timer operation mode, and also clears the counter when the value agrees with the counter value. In the PWM operation mode, the High pulse width can be specified by this register value.



Peripherals

(4) Description of operation

(a) Timer function

Setting the P/TX bit of the CNTR to 0 gives the timer-operation mode. When the TPE bit of the CNTR is set to 1, the counter starts incrementing from 00_H. When the value of the counter agrees with that of the COMR, the counter is cleared on the next count clock pulse and incrementing restarts. Therefore, the TIR bits are set and the output pin is reversed (but, when the TPE bit is 0, the output pin is fixed at Low level) in cycles of the count clock pulses when 00_H is written at the COMR, or in cycles 256 times longer than those of the count clock pulses when FF_H is written.

If the value of the COMR is rewritten in the timer-operation mode, it becomes effective from the next cycle (when the value of the counter is 00_H, the value of the COMR is transferred to the comparator latch).

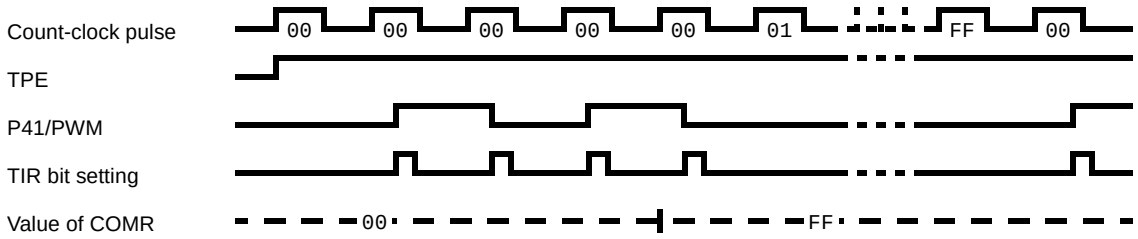


Fig. 2.11 Timer Operation

If the TIE bit of the CNTR is set to 1, an interrupt occurs when the values of the counter and COMR match. During interrupt processing, the TIR bit is used as the interrupt flag. The TIR bit is set irrespective of the value of the TIE bit. However, if the values of the counter and COMR match, the TIR bit is set to 1 even after an interrupt is disabled.

Writing 0 at the TIR bit permits clearing of the interrupt source or the TIR bit. When the Read Modify Write instruction is read, the TIR bit is set so that 1 can always be read to prevent erroneous clearing.

By using P0 and P1 bit in CNTR, 1 out of 4 clock sources can be selected for the counter.

Peripherals

(b) PWM operation

Setting the P/TX bit of the CNTR to 1 gives the PWM operation mode. The COMR specifies the duty of the output pulse. Pulses can be output with 1/256 resolution and a duty of 0% to 99.6%.

When 0 (00_H) is written at the COMR, the duty of the PWM output pulse is 0%; when 128 (80_H) is written, the duty is 50%, and when 255 (FF_H) is written, it is 99.6%.

The value of COMR is transferred to the comparator latch when the value of the counter is 00_H. If the value of the COMR is rewritten in the PWM operation mode, it becomes effective from the next cycle.

At starting (counter = 00), output is high. When the counter matches the compare register, output goes low.

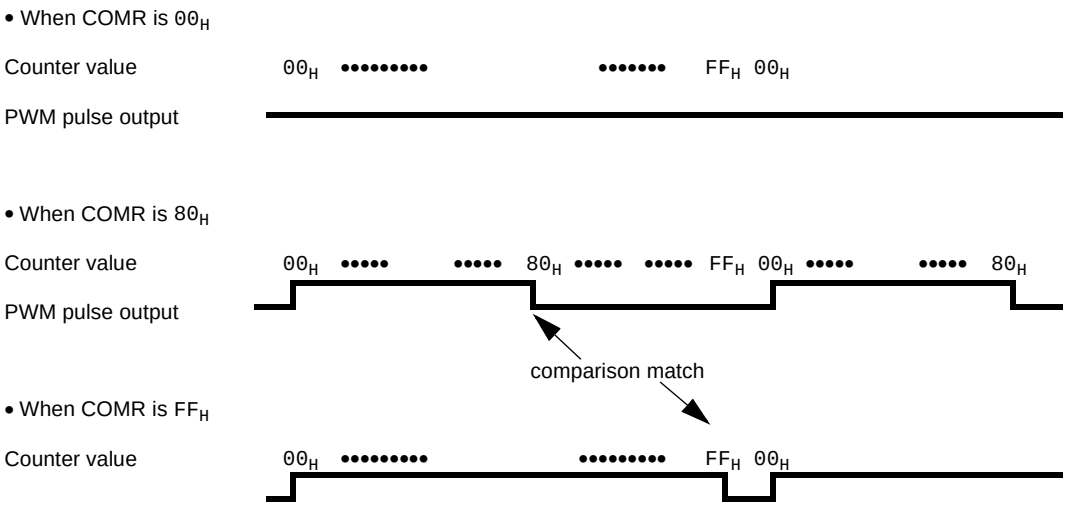


Fig. 2.12 PWM Pulse Output

In the PWM operation mode, the values at the TIR bit of the CNTR have no meaning. No interruption occurs even if the TIE bit are 1.

The cycle of the PWM pulse can be changed by switching the count clock pulse.

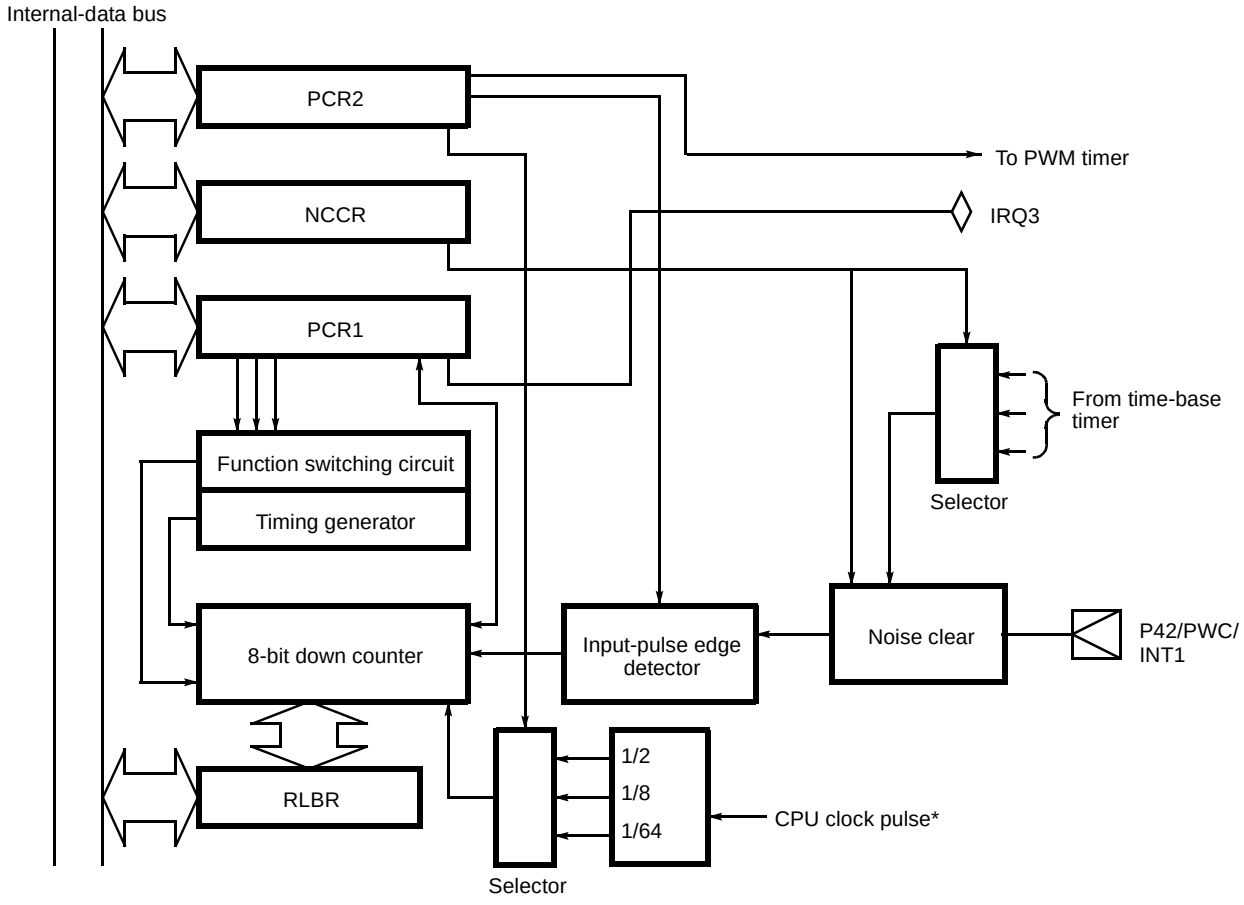
The count clock pulse can be selected from three clock pulses of the prescaler and the clock pulse of the internal timer by the clock pulse select bits P1 and P0 of the CNTR.

Peripherals

2.2.3 Pulse-width Count Timer (Timer 2)

- This timer has timer and pulse-width measurement functions.
- The timer function has two modes: reload timer and one-shot.
- In the reload timer mode, the set values are counted down repeatedly.
- In the one-shot mode, counting down is started from the set values and stops at the first underflow.
- The pulse-width measurement function enables measurement of High, Low, or one-cycle widths of pulses input from pins.
- For inputting from pins, the 5-bit noise-clearing circuit is selectable.

(1) Block diagram



* The CPU clock pulse is an oscillation-divided pulse.

Peripherals

(2) Register list

	8 bits		
Address: 0014_H	PCR1	R/W	Pulse-width control register 1
Address: 0015_H	PCR2	R/W	Pulse-width control register 2
Address: 0016_H	RLBR	R/W	Reload buffer register
Address: 0017_H	NCCR	R/W	Noise-clear control register

(3) Description of registers

Address: 0014_H PCR1

Address: 0015_H PCR2

Address: 0016_H RLBR

Address: 0017_H NCCR

(a) Pulse-width control register 1 (PCR1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0014_H	EN	—	IE	—	—	UF	IR	BF
	(R/W)	(R/W)	(R/W)			(R/W)	(R/W)	(R)
				(Initial value) $000XX000_B$				

[Bit 7] EN: Count enable bit

At the timer function, when 1 is written at this bit, the value of the data register is loaded to start counting down. When 0 is written, counting down stops. At the pulse-width measurement function, when 1 is written at this bit, the measurement-enable state is set. Under this condition, counting down is started when the edge of the measured pulse is detected. When 0 is written at this bit during measurement, counting down stops; the count is not transferred to the reload buffer register (RLBR).

	Timer function	Pulse-width measurement function
0	Count disable	Pulse-width measurement stop/disable
1	Count enable/start	Pulse-width measurement enable/start

[Bit 5] IE: Interrupt request enable bit

When bit 5 is 1, an interrupt request is output when the interrupt request flags (UF, IR, and BF) are set.

0	Interrupt disabled
1	Interrupt enabled

[Bit 2] UF: Underflow interrupt request bit

Bit 2 indicates whether the timer underflowed. The meaning of each bit to be read is as follows:

0	No underflow
1	Underflow occurred

Peripherals

1 is always read when the Read Modify Write instruction is executed.

The meaning of each bit to be written is as follows:

0	Clears this bit
1	Unchanges this bit and other bits unaffected

[Bit 1] IR: Measurement-end interrupt request bit
When the IE bit (bit 5) of the PCR1 is 1, an interrupt occurs at the end of pulse-width measurement.

The meaning of each bit to be read is as follows:

0	Pulse-width measurement not terminated
1	Pulse-width measurement terminated

1 is always read when the Read Modify Write instruction is executed.

The meaning of each bit to be written is as follows:

0	Clears this bit
1	Unchanges this bit and other bits unaffected

[Bit 0] BF: Buffer-full flag
When the IE bit (bit 5) of the PCR1 is 1, an interrupt occurs when any measured value is found in the RDBR. This bit is set at the end of pulse-width measurement and cleared when data in the buffer is read.

The meaning of each bit to be read is as follows:

0	Pulse-width measured value not found
1	Pulse-width measured value found

Address: 0014_H PCR1

Address: 0015_H PCR2

Address: 0016_H RLBR

Address: 0017_H NCCR

(b) Pulse-width control register 2 (PCR2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0015_H	FC	RM	TO	—	C1	C0	W1	W0
	(R/W)	(R/W)	(R/W)		(R/W)	(R/W)	(R/W)	(R/W)
				(Initial value)				
				$000X0000_B$				

[Bit 7] FC: Function select bit
Bit 7 is used to select the timer and pulse-width measurement functions.

0	Timer function
1	Pulse-width measurement function

One should not change the function select bit when timer function is enabled (EN=1).

Peripherals

[Bit 6] RM: Timer mode select bit

In the timer function, bit 6 is used to select the timer mode.

0	Reload timer mode
1	One-shot timer mode

The mode should be changed only when the operation is stopped (when the EN bit (bit 7) of the PCR1 is 0).

[Bit 5] TO: Timer output bit

The value of bit 5 is inverted each time the counter underflows. Bit 5 is a write bit; it must not be rewritten when the EN bit (bit 7) of the PCR1 is 1.

[Bits 3 and 2] C1 and C2: Count clock pulse select bits

Setting is performed as shown below using a combination of bits 3 and 2. These bits are irrelevant to the value of the FC bit (bit 7).

C1	C0	Count clock pulse
0	0	Internal clock pulse 1 instruction cycle
0	1	Internal clock pulse 4 instruction cycles
1	0	Internal clock pulse 32 instruction cycles
1	1	Do not set.

[Bits 1 and 0] W1 and W0: Measured pulse select bits

Setting is performed as shown below using a combination of bits 1 and 0. These bits are ignored when the timer is in operation (FC = 0).

W1	W0	Measured pulse width
0	0	High level
0	1	Low level
1	0	Rising-to-rising
1	1	Falling-to-falling

Address: 0014_H PCR1

Address: 0015_H PCR2

Address: 0016_H RLBR

Address: 0017_H NCCR

(c) Reload buffer register (RLBR)

At the timer function, the RLBR is a read-and-write reload register. At pulse-width measurement, it is a read-only data buffer register for holding the measured values. In this case, writing is impossible. The BF bit (bit 0) of the PCR1 is cleared by reading data.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0016_H								
Timer function ⇒	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Pulse-width measurement function ⇒	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
				(Initial value)				
				$XXXXXXXX_B$				

Peripherals

Address: 0014_H PCR1

Address: 0015_H PCR2

Address: 0016_H RLBR

Address: 0017_H NCCR

(d) Noise-clear control register (NCCR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0017_H	—	—	—	—	—	—	NCS1	NCS0
							(R/W)	(R/W)
							(Initial value)	
							------00_B	

[Bits 1 and 0] NCS1 and NCS0: Sampling clock pulse select bits

The sampling clock pulse of the noise-clearing circuit is selected as shown

NCS1	NCS0	Clock pulse selected	Clock cycle at 5MHz	Noise pulse width
0	0	No noise clear	-	-
0	1	Oscillation clock pulse × 4	0.8 [µs]	4.0 [µs]
1	0	Oscillation clock pulse × 32	12.8 [µs]	64 [µs]
1	1	Oscillation clock pulse × 128	51.2 [µs]	256 [µs]

(4) Description of operation

(a) Timer function

The timer function has the following two modes.

a. Reload timer mode

Each time the counter underflows, the value written at the RLBR is reloaded to continue counting down. In this mode, when the counter underflows, the interrupt request flag UF (bit 2) is set. An interrupt request is also output when the IE bit (bit 5) is set to 1. Each time the timer underflows, the value of the TO bit (bit 5) is inverted.

b. One-shot mode

Counting stops at an underflow. In this mode, when the counter underflows, the underflow interrupt request flag UF (bit 2) is set and the EN bit (bit 7) is automatically set to 0 to stop counting.

In both modes, counting starts when 1 is written at the EN bit (bit 7) and stops when 0 is written.

Peripherals

(b) Pulse-width measurement function

a. Measurement start

Writing 1 at the EN bit (bit 7) and FC bit (bit 7) causes the counter to enter the operation-enabled state. In this condition, counting starts when the edge of the measured pulse input is detected. At the pulse-width measurement function, counting down is started from FF_H.

b. Measurement end and measured value

When measurement is terminated, the measured value is transferred to the buffer, and the measurement-end flag IR (bit 1) and buffer-full flag BF (bit 0) are set. causing the counter to re-enter the operation-enabled state. At this time, an interrupt request is output when the IE bit (bit 5) is set to 1. When the previous measured value cannot be read after continuous pulse-width measurement, it is held by continuing to set the BF flag. The new measured value is discarded.

c. Long pulse

When the counter underflows during measurement, the UF bit (bit 2) is set to 1 to continue counting. In this case, an interrupt request is also output when the IE bit (bit 5) is set to 1.

d. Measurement stop

Measurement stops when 0 is written at the EN bit (bit 7).

e. Calculation of pulse width

The count value when measurement is terminated is transferred as the measured value to the buffer. Therefore, the pulse width should be calculated using the following equation.

Pulse width = [(256 – count value) + (Number of TO counts inverted × 256)] × one cycle width of count clock pulse

f. Others

The counter remains in the operation-enabled state even after the end of measurement, so continuous pulse-width measurement is possible. Measurement of a High pulse width is started from the changing edge of the input pulse. If the EN bit is enabled (EN = 1) when the input pulse is already High, counting is performed after the next rising edge.

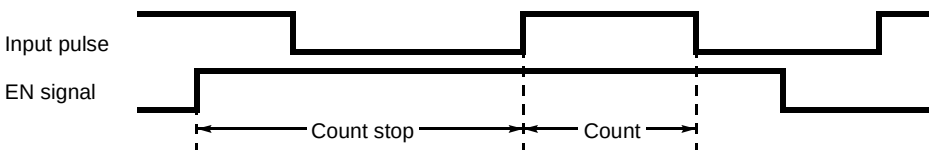


Fig. 2.13 Measurement of High Pulse Width

Peripherals

(c) Noise-clearing circuit operation

Figure 2.15 shows the operation of the noise-clearing circuit. The PWC input is sampled by the clock pulse selected by the clock pulse select bits (NCS1 and NCS0) of the noise-clear control register. Integrating the sampled signal clears the noise. The maximum width of cleared noise is as follows:

Nw = Sampling clock cycle × 5

When noise clearing is prohibited, the PWC input is input directly to the pulse-width count timer.

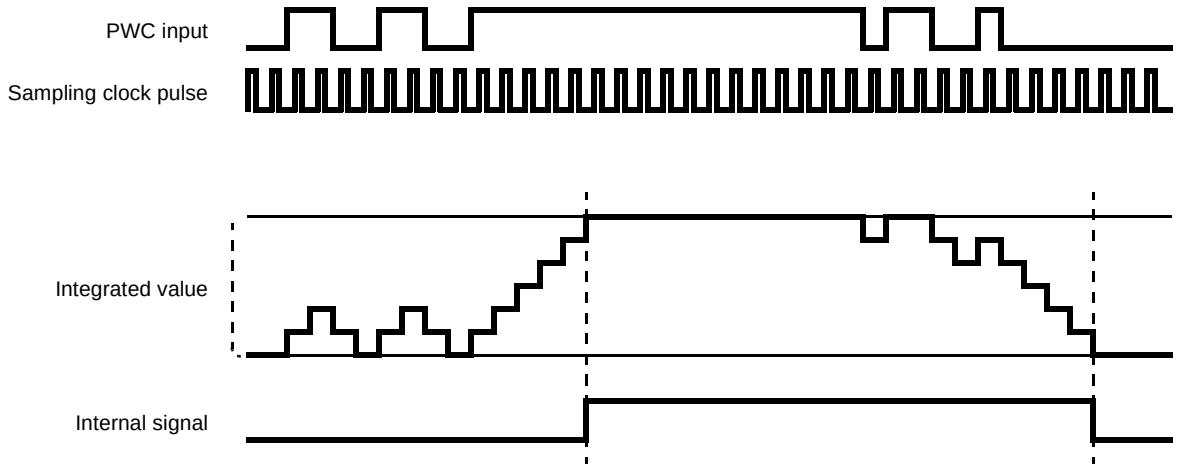


Fig. 2.14 Operation of Noise Clearing Circuit

(5) Usage precautions

(a) Do not rewrite the value of PCR2 when the EN bit is 1 (during timer operation and pulse-width measurement).

(b) At mode switching (FC bit rewriting), the state of each flag does not change. Clear each flag immediately after the mode is switched.

(c) Read the measured value before the next underflow. When the value is read after an underflow, the TO bit is inverted, sometimes disabling calculation of the correct measured value.

(d) When the previous measured value is not read after continuous pulse-width measurement, it is held without transferring the new value to the buffer.

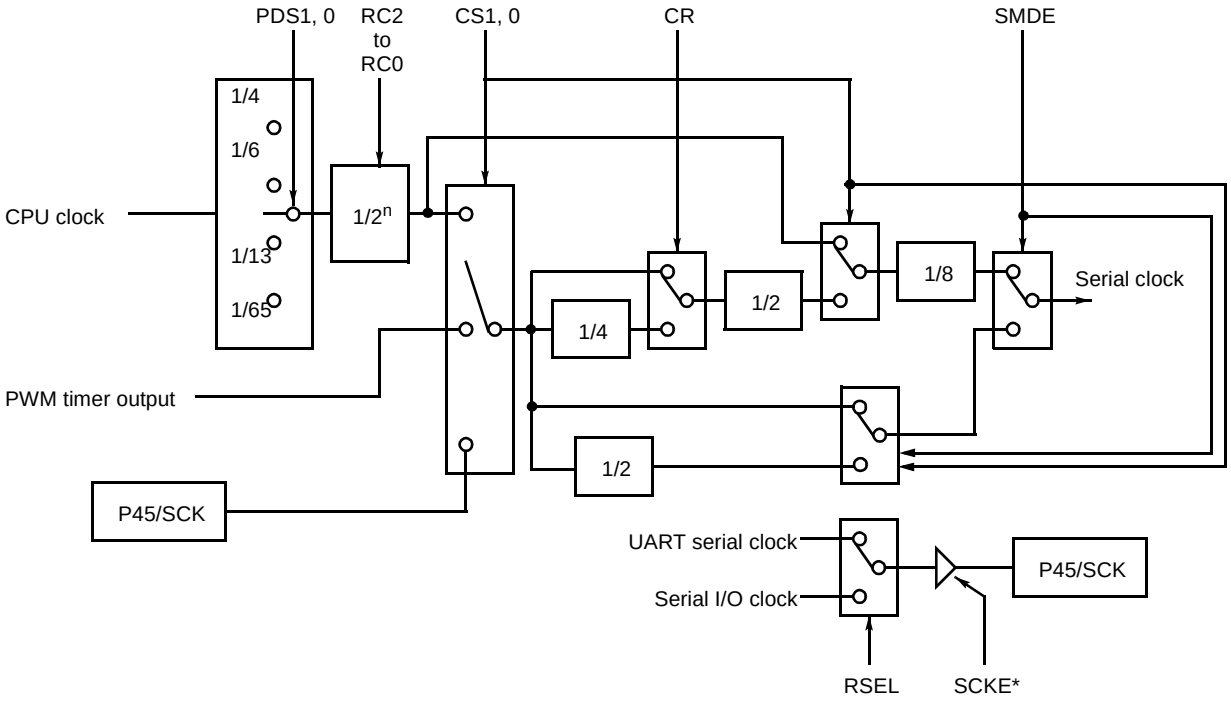
Peripherals

2.2.4 UART

- Full-duplex double buffers
- CLK synchronous and asynchronous data transfer
- 8 baud rates (for internal clock)
  The baud rate can also be freely selected by external clock input or input from the internal timer.
- Variable data length
- NRZ transfer format
- Two data and clock pins can be switched for use.
- The data and clock input/output polarities can be inverted.

(1) Block diagram

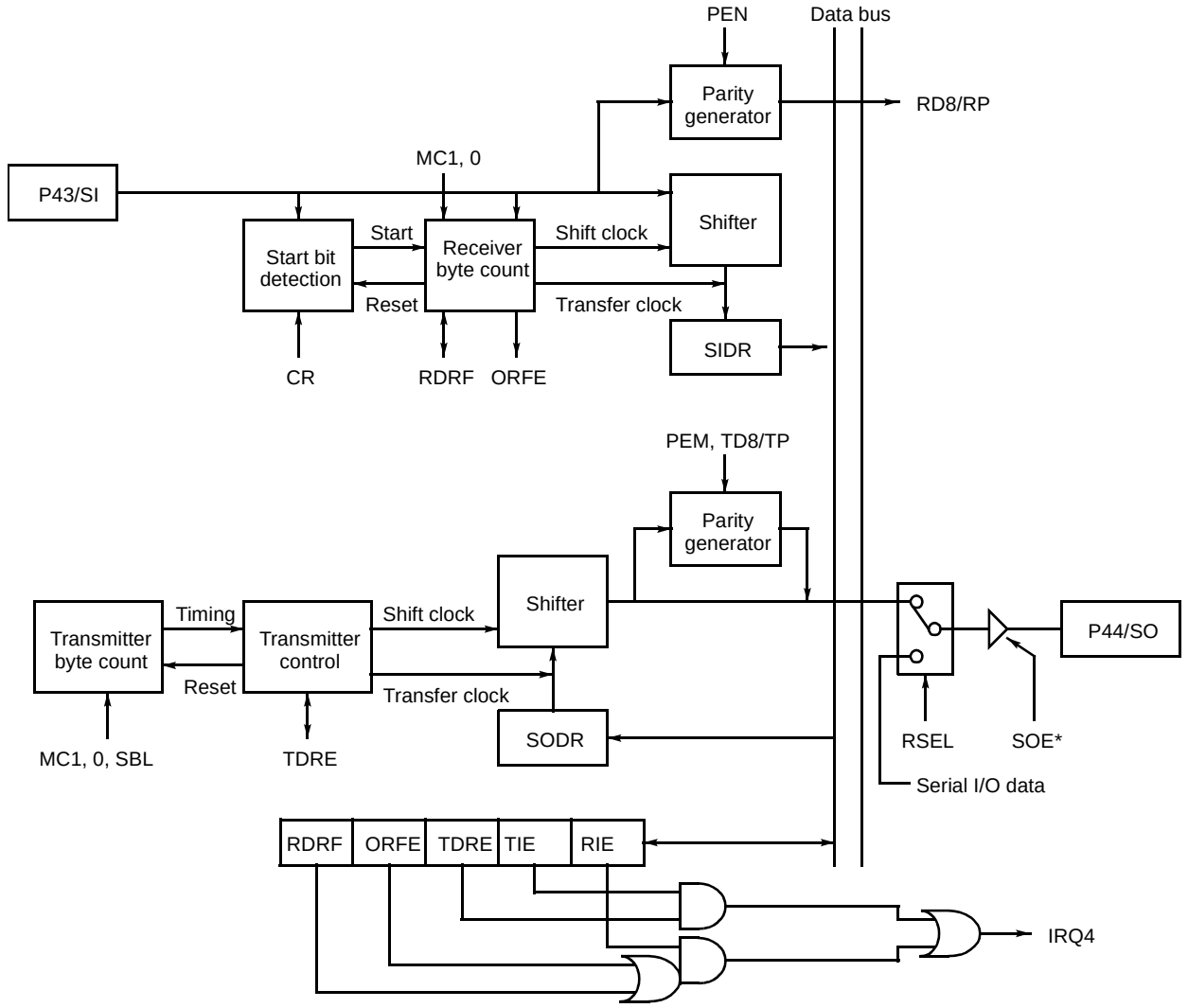
(a) Baud rate generator and serial clock generator



* At switching between port output and serial clock output, the SCKE bit of the UART is valid when the RSEL bit is 0; the SCKE bit of the serial I/O is valid when the RSEL bit is 1.

Peripherals

(b) Data transmitter/receiver



* At switching between port output and serial data output, the SOE bit of the UART is valid when the RSEL bit is 0; the SOE bit of the serial I/O is valid when the RSEL bit is 1.

Peripherals

(2) Register list

		8 bits		
Address:	0020_H	SMC1	R/W	Serial mode control register 1
Address:	0021_H	SRC	R/W	Serial rate control register
Address:	0022_H	SSD	R/W	Serial status and data register
Address:	0023_H	SIDR	R	Serial input data register
Address:	0023_H	SODR	W	Serial output data register
Address:	0024_H	SMC2	R/W	Serial mode control register 2

(3) Description of registers

(a) Serial mode control register 1 (SMC1)

Address: 0020_H SMC1

Address: 0021_H SRC

Address: 0022_H SSD

Address: 0023_H SIDR

Address: 0023_H SODR

Address: 0024_H SMC2

This register is used to select the UART operation mode.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0020_H	PEN	SBL	MC1	MC0	SMDE	—	SCKE	SOE
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)		(R/W)	(R/W)
				(Initial value) $00000\text{-}00_B$				

[Bit 7] PEN: Parity enable

Bit 7 is used to determine whether to append a parity bit (when transmitting) or to detect it (when receiving) for serial data input/output.

0	No parity (Initial value)
1	Parity (Odd or even parity is set by TD8/TP of the SSD register.)

[Bit 6] SBL: Stop bit length

Bit 6 is used to determine the stop bit length of transmit data. At the receiving end, only the first bit of the stop bit is recognized; second and later bits are ignored.

0	2-bit length (Initial value)
1	1-bit length

Peripherals

[Bits 5 and 4] MC1 and MC0: Mode control

Bits 5 and 4 are used to select the transfer mode (data length).

MC1	MC2	Mode	Data Length
0	0	0	5 (4)
0	1	1	8 (7)
1	0	reserved	reserved
1	1	3	9 (8)

(Initial value)
Values in parentheses indicate the data length with parity.

[Bit 3] SMDE:

0	Synchronous transfer (Initial value)
1	Asynchronous transfer

[Bit 1] SCKE: SCLK enable

When 1 is written at bit 1, the UART serial clock output pin is switched to the port to output an external synchronous clock pulse.

If the mode in which a synchronous clock pulse is input from the outside is set by the CS1 and CS0 bits of the SRC register, the value can also be read from the port as the input pin.

0	Functions as general-purpose input/output port that does not output serial clock pulse When the port is set to input (DDR = 0), it also functions as a serial clock input pin. (Initial value)
1	Functions as UART serial clock input/output port

In the external clock input mode, set this bit to 0.
This bit is valid when the RSEL bit of the SMC2 is 0.

[Bit 0] SOE: Serial output enable

When 1 is written at bit 0, the port is switched to the UART serial data output pin to enable serial data output.

0	Functions as port that does not output serial data (Initial value)
1	Functions as UART serial data output port (SOUT)

This bit is valid when the RSEL bit of the SMC2 is 0.

Peripherals

Address: 0020_H SMC1

Address: 0021_H SRC

Address: 0022_H SSD

Address: 0023_H SIDR

Address: 0023_H SODR

Address: 0024_H SMC2

(b) Serial rate control register (SRC)

This register is used to control the data transfer speed (baud rate) of the UART.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0021_H	—	—	CR	CS1	CS0	RC2	RC1	RC0
			(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
			(Initial value) --011000_B					

[Bit 5] CR: Clock rate

Bit 5 is used to select the asynchronous transfer clock rate. However, when the CS1 and CS0 bits are 11_B, the 1/8 clock rate is selected irrespective of the value of the CR bit.

0	1/16 of clock input (Initial value)
1	1/64 of clock input

Note: The synchronous transfer clock rate is as follows irrespective of the value of the CR bit:

Clock source — PWM timer, dedicated baud rate generator 1/2
— External clock, dedicated baud rate generator 1/1

Note that the dedicated baud rate generator may select the clock rate according to the CR value.

[Bits 4 and 3] CS1 and CS0: Clock select

Bits 4 and 3 are used to select the clock input of the UART port. If the external or internal clock is selected as clock input, the baud rate is a 1/16 or 1/64 clock frequency according to the value of the CR bit (initial value: 11_B). For details, see (4) of Description of operation.

[Bits 2 to 0] RC2 to RC0:

Bits 2 to 0 are needed only when generating a serial clock pulse with the dedicated baud rate generator. The baud rate can be selected from eight kinds by these bits (initial value: 000_B). For the baud rate setting, see (4) of Description of Operation.

Peripherals

Address: 0020_H SMC1

Address: 0021_H SRC

Address: 0022_H SSD

Address: 0023_H SIDR

Address: 0023_H SODR

Address: 0024_H SMC2

(c) Serial status and data register (SSD)

This register is used to indicate the current status of the UART port. When the data communication length is 9 bits, the most significant data (bit 8) is included.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0022_H	RDRF	ORFE	TDRE	TIE	RIE	—	TD8 /TP	RD8 /RP
	(R)	(R)	(R)	(R/W)	(R/W)		(R/W)	(R)
				(Initial value) 00100-1X_B				

[Bit 7] RDRF:
The RDRF flag is used to indicate the data status of the serial input data register (SIDR).

0	Empty (Initial value)
1	Contains data

When the SIDR register is read after reading the SSD register with the RDRF flag set to 1, the RDRF flag is cleared. When this flag is set to 1, the receiver interrupt request is output.

[Bit 6] ORFE:
The ORFE flag is used to indicate that an overrun or framing error has occurred. This flag is initialized to 0 at reset.

0	Normal (Initial Value)
1	Error

If this flag is set, data is not transferred from the receive shift register to the SIDR register.

When the SIDR register is read after reading the SSD register with the ORFE flag set to 1, the ORFE flag is cleared. When this flag is set to 1, the receiver interrupt request is output.

The status of input data is specified by the RDRF and ORFE flags as follows:

RDRF	ORFE	SIDR data status
0	0	Empty
0	1	Framing error (If new data is input under this condition, RDRF is not set.)
1	0	Normal data
1	1	Overrun (previous data remains)

Peripherals

[Bit 5] TDRE:

The TDRE flag is used to indicate the status of the serial output data register (SODR).

0	Contains data
1	Empty (Initial value)

If SODR (Serial Output Data Register) is empty, and newly written data to SODR, SODR will be driven out of the serial output pin (P44/SO).

When the TDRE flag is set to 1, a transmitter interrupt request is output.

[Bit 4] TIE: Transmitter interrupt request enable bit

Bit 4 is used to enable the transmitter interrupt request.

0	Disables interrupt (Initial value)
1	Enables interrupt

[Bit 3] RIE: Receiver interrupt request enable bit

Bit 3 is used to enable the receiver interrupt request.

0	Disables interrupt (Initial value)
1	Enables interrupt

[Bit 1] TD8/TP:

When parity is not provided, bit 1 is treated as bit 8 of the SODR register. When parity is provided, this bit is used to determine whether the parity of serial output data is even or odd.

0	Odd parity
1	Even parity (Initial value)

[Bit 0] RD8/RP:

When parity is not provided, bit 0 is treated as bit 8 of the SIDR register. When parity is provided, this bit is used to determine whether the parity of serial input data is even or odd (Initial value: undefined).

0	Odd parity
1	Even parity

Peripherals

Address: 0020_H SMC1
Address: 0021_H SRC
Address: 0022_H SSD
Address: 0023_H SIDR
Address: 0023_H SODR
Address: 0024_H SMC2

Address: 0020_H SMC1
Address: 0021_H SRC
Address: 0022_H SSD
Address: 0023_H SIDR
Address: 0023_H SODR
Address: 0024_H SMC2

(d) Serial input data register (SIDR)
Serial output data register (SODR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIDR Address: 0023_H								
	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)

The SIDR register is used for input of serial data (Initial value: undefined).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SODR Address: 0023_H								
	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)

The SODR register is used for output of serial data (Initial value: undefined).

(e) Serial mode control register 2 (SMC2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0024_H	—	—	PSEN	—	RSEL	—	PDS1	PDS0
	—	—	(R/W)	—	(R/W)	—	(R/W)	(R/W)
	(Initial value) --1-0-00_B							

[Bit 5] PSEN:
Bit 5 is used to determine whether to start or stop the operation of the baud rate generator.

0	Stops operation
1	Starts operation (Initial value)

[Bit 3] RSEL:
Bit 3 is used to select whether either the UART or serial I/O to output data and clock.

0	UART (Initial value)
1	Serial I/O

[Bits 1 and 0] PDS1 and PDS0:

Bits 1 and 0 are used to select the division of the divider at the front of the baud rate generator.

PDS1	PDS0	
0	0	Select 4 dividing (Initial value)
0	1	Select 6 dividing
1	0	Select 13 dividing
1	1	Select 65 dividing

Peripherals

(4) Description of operation

(a) Operation modes

The UART has the operation modes listed in Table 2–6; they can be switched by setting the value at the serial mode control register 1 (SMC1).

Table 2–6 Operation Modes of UART

Mode	Parity	Data Length	Clock Mode	Stop Bit Length
0	Provided	4	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	5	Asynchronous/synchronous	1 bit or 2 bits
1	Provided	7	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	8	Asynchronous/synchronous	1 bit or 2 bits
3	Provided	8	Asynchronous/synchronous	1 bit or 2 bits
	Not provided	9	Asynchronous/synchronous	1 bit or 2 bits

However, the stop bit length can be specified only for the transmitter channel. The 1-bit length is always specified for the receiver channel.

(b) Interrupt occurrence and flag setting conditions

The UART has three flags and two interrupt sources.
The three flags are ORFE, RDRF, and TDRE. The ORFE flag is an overrun/framing error flag which is set when an error occurs at receiving. The RDRF flag indicates that the receive data is ready at the SIDR register. The TDRE flag indicates that writing to the transmit data register (SODR) is enabled. The two interrupt sources are one for receiving, and one for transmitting. At receiving, an interrupt is requested by the RDRF or ORFE flag. At transmitting, an interrupt is requested by the TDRE flag.

a. Receiving in modes 0, 1, and 3

Both the RDRF (receive data register full) and ORFE (overrun/framing error) flags are set when receiving and transfer are completed and the last stop bit is detected. An interrupt request is then output to the CPU. When the RDRF flag is active, the received data is transferred to the serial data input register (SIDR).

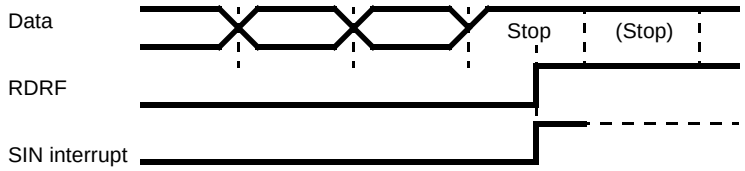


Fig. 2.15 RDRF Flag Set Timing

Peripherals

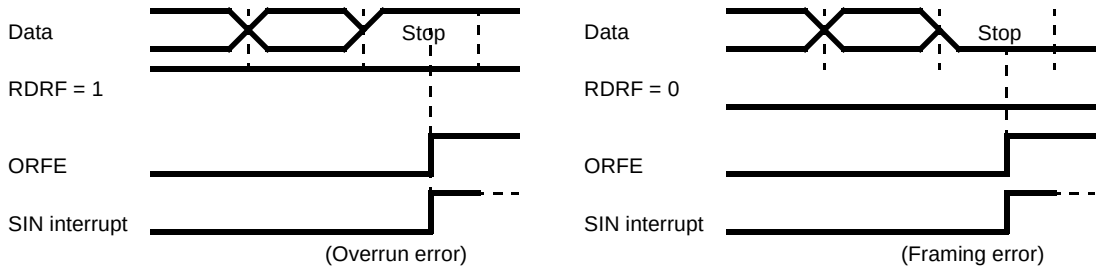
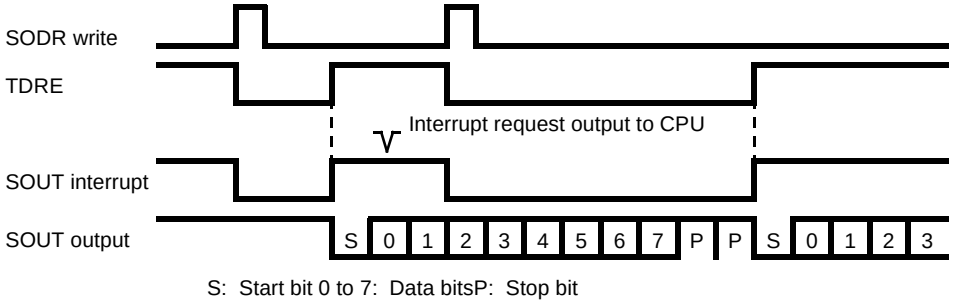


Fig. 2.16 ORFE Flag Set Timing

b. Transmission

When the next data is ready to write after data written to the SODR (serial output data register) is transferred to the interrupt shift register, the TDRE (transmit data register empty) flag is set and an interrupt request is output to the CPU.

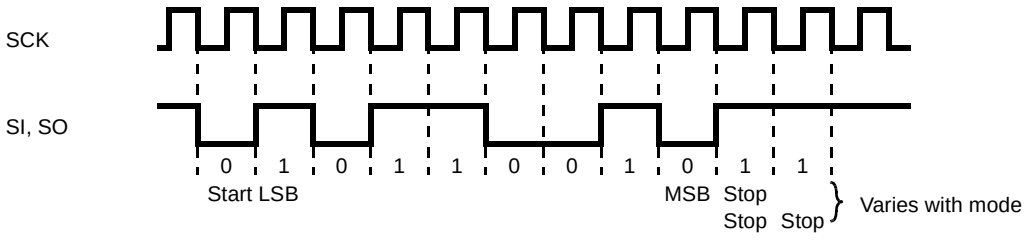


S: Start bit 0 to 7: Data bitsP: Stop bit

Fig. 2.17 TDRE Flag Set Timing

(c) Transfer data format

The UART can handle only NRZ (non-return-to-zero)-type data. The relationship between transmitter/receiver clocks and data is shown in the figure below.



Transmitted data is 01001101_B (mode 1) or 101001101_B (mode 3)

Fig. 2.18 Transfer Data Format (Synchronous Transfer)

Peripherals

As shown in the figure, data transfer starts from the start bit (Low-level data), the data bit length specified by the LSB first is transferred, and transfer ends at the stop bit (High-level data).
In asynchronous transfer, the relationship between SCK and SI is not as shown in the above figure. In addition, at asynchronous transfer, the relationship is not as shown in the above diagram even when SCK is set to input.

(d) Transfer clock selection

The transfer clock can be selected from the external clock (SCK pin), PWM timer, and the dedicated baud rate generator. This selection is done by the CS0, CS1, and CR bits of the serial rate control register (SRC). The division ratios are listed in Table 2–7.

Table 2–7 Clock Division Ratio

CS1	CS0	Clock Input	CR	Asynchronous	Sychronous
0	0	External clock	0	1/16	1/1
			1	1/64	
0	1	PWM timer	0	1/16	1/2
			1	1/64	
1	0	Dedicated baud rate generator	0	1/16	1/2
			1	1/64	
1	1		---	1/8	1/1

When using the dedicated baud rate generator, select the input clock of the baud rate generator by PDS1 and PDS0 of the SMC2. indicates the input clocks to be used and the division, and Table 2–9 indicates the reference baud rates.

Table 2–8 Input Clock of Baud Rate Generator

PDS1	PDS0	Division	Clock
0	0	1/4	CPU operation
0	1	1/6	CPU operation
1	0	1/13	CPU operation
1	1	1/65	CPU operation

Peripherals

Table 2–9 Selection of Baud Rate (When Dedicated Baud Rate Generate Used)

RC2	RC1	RC0	Division ratio	Baud rate (bps)			Remarks
				4.9152 MHz	5 MHz		Clock
				1/4	1/4	1/65	PDS division
				1/64	1/8	1/16	CS,CR division
0	0	0	2^0	9600	78125	2404	
0	0	1	2^1	4800	39063	1202	
0	1	0	2^2	2400	19531	601	
0	1	1	2^3	1200	9766	300	
1	0	0	2^4	600	4883	150	
1	0	1	2^5	300	2441	75	
1	1	0	2^6	150	1221	38	
1	1	1	2^7	75	610	19	

(e) Selection of input/output signal

The UART shares the data and clock input/output with the serial I/O. Therefore, the output signal selected by the RSEL bit is output. At switching between port output and peripheral output, the peripheral enable bit selected by the RSEL bit becomes valid.

- When the RSEL bit is 0, UART is selected.
- When the RSEL bit is 1, serial I/O is selected.

(5) Precautions for UART

- After canceling register initialization by reset, 11 shift clocks are required to initialize the internal control section.
- When using the external clock, the minimum pulse width is as follows:

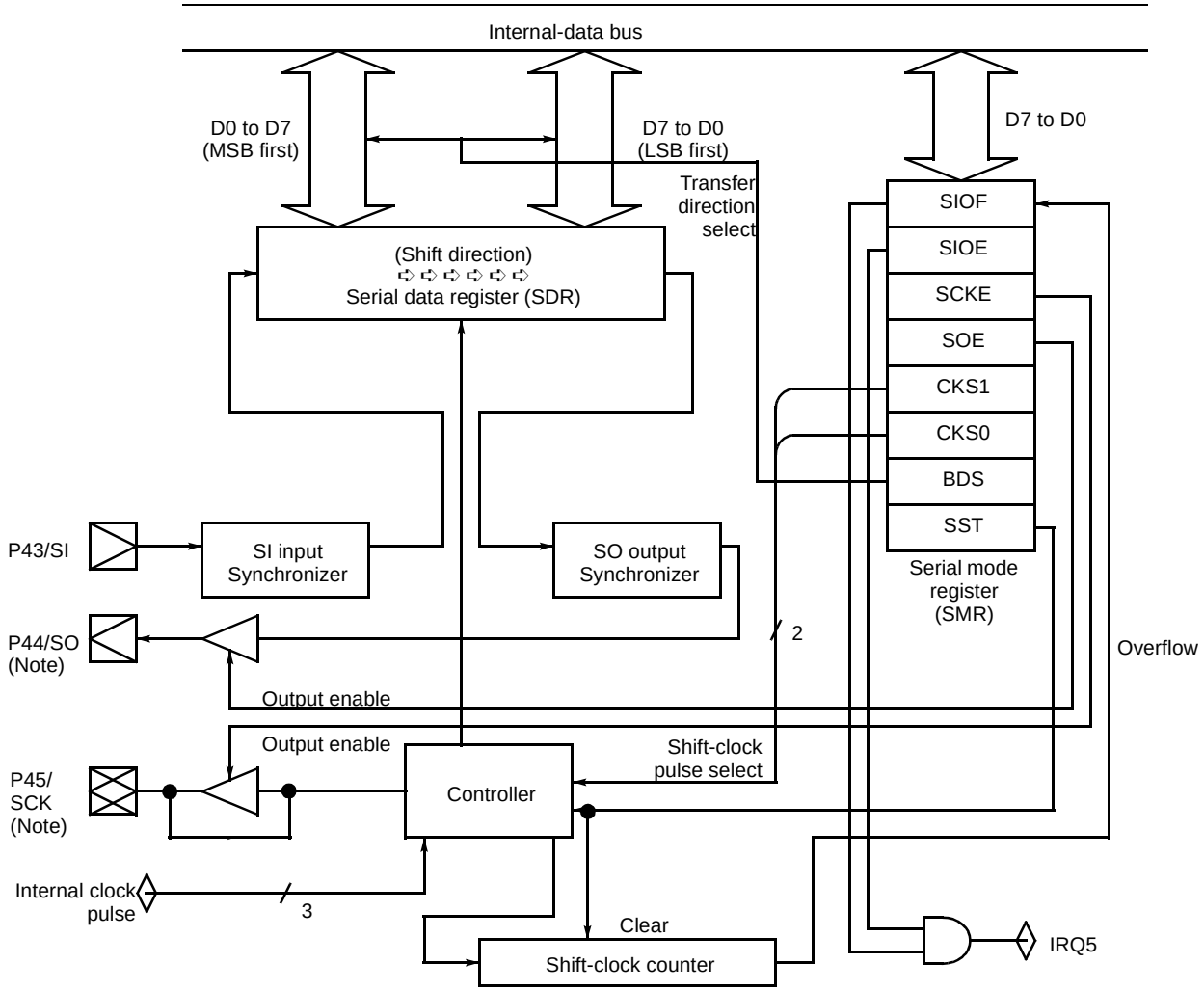
  CPU operating clock cycle $\times$ 4

Peripherals

2.2.5 8-bit Serial I/O

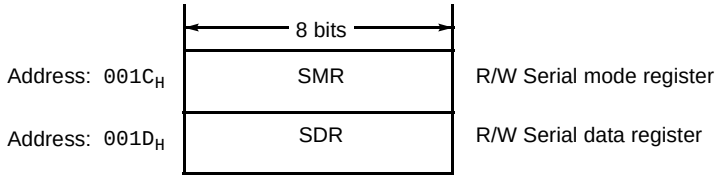
- 8-bit serial data synchronous transfer.
- LSB first or MSB first can be selected for data transfer.
- The 4 shift-clock mode can be selected (three internal and one external).

(1) Block diagram



Note: The SO and SCK outputs serve as UART outputs. They can be used as the outputs of the serial I/O when the RSEL bit of the SMC2 in the UART is 1.

(2) Register list



Peripherals

Address: $001C_H$ SMR

Address: $001D_H$ SDR

(3) Description of registers

The detail of each register is described below.

(a) Serial-mode register (SMR)

The SMR is used to control serial I/O.

Address: $001C_H$

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIOF	SIOE	SCKE	SOE	CKS1	CKS0	BDS	SST
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
(Initial value) 00000000_B							

[Bit 7] SIOF: Serial I/O interrupt-request flag

This bit is used to indicate the serial I/O transfer state.
The meaning of each bit when reading is as follows:

0	Serial data transfer not terminated
1	Serial data transfer terminated

Note that 1 is always read when the Read Modify Write instruction is read.
If this bit is set when an interrupt is enabled (SIOE = 1), an interrupt request is output to the CPU.

The meaning of each bit when writing is as follows:

0	Clears this bit
1	Unchanges this bit and other bits unaffected

The end-of-transfer decision may be made by either the SST bit (bit 0) of the SMR or by this bit.

[Bit 6] SIOE: Serial I/O interrupt-enable bit

This bit is used to enable a serial I/O interrupt request.

0	Serial I/O interrupt-output disabled
1	Serial I/O interrupt-output enabled

[Bit 5] SCKE: Shift-clock output-enable bit

This bit is used to control the shift-clock I/O pins.

0	General-purpose port pin (P45) or SCK input pin
1	SCK (shift clock) output pin

When using the P45/SCK pin as an external clock, always set the DDR4 to input (bit 5 of DDR4 = 0).

This bit is valid when the RSEL bit of the SMC2 in the UART is 1.

Peripherals

[Bit 4] SOE: Serial-data output-enable bit

This bit is used to control the output pin for serial I/O.

0	General-purpose port pin (P44)
1	SO (serial data) output pin

When using P43/SI pin as SI pin, always set the DDR4 to input (bit 3 of DDR4 = 0).

This bit is valid when the RSEL bit of the SMC2 in the UART is 1.

[Bits 3 and 2] CKS1 and CKS0: Shift-clock select bits

These bits are used to select the serial shift-clock modes.

CKS1	CKS0	Mode	(Clock rate)	SCK
0	0	Internal shift-clock mode	(2 instruction cycle)	Output
0	1	Internal shift-clock mode	(8 instruction cycle)	Output
1	0	Internal shift-clock mode	(32 instruction cycle)	Output
1	1	External shift-clock mode	(SCK)	Input

[Bit 1] BDS: Transfer direction select bit

At serial data transfer, this bit is used to decide the transfer direction: from the least significant bit first (LSB first) or from the most significant bit first (MSB first).

0	LSB first
1	MSB first

Note that when this bit is rewritten after writing data to the SDR, the data become invalid.

[Bit 0] SST: Serial I/O transfer-start bit

This bit is used to start serial I/O transfer. The bit is automatically cleared to 0 when transfer is terminated.

0	Stops serial I/O transfer
1	Starts serial I/O transfer

Before starting transfer, ensure that transfer is stopped (SST = 0).

Address: $001C_H$ SMR

Address: $001D_H$ SDR

(b) Serial-data register (SDR)

This 8-bit register is used to hold serial I/O transfer data. (Note: Do not write data to this register during the serial I/O operation.)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $001D_H$								
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
				(Initial value)				
				$XXXXXXXX_B$				

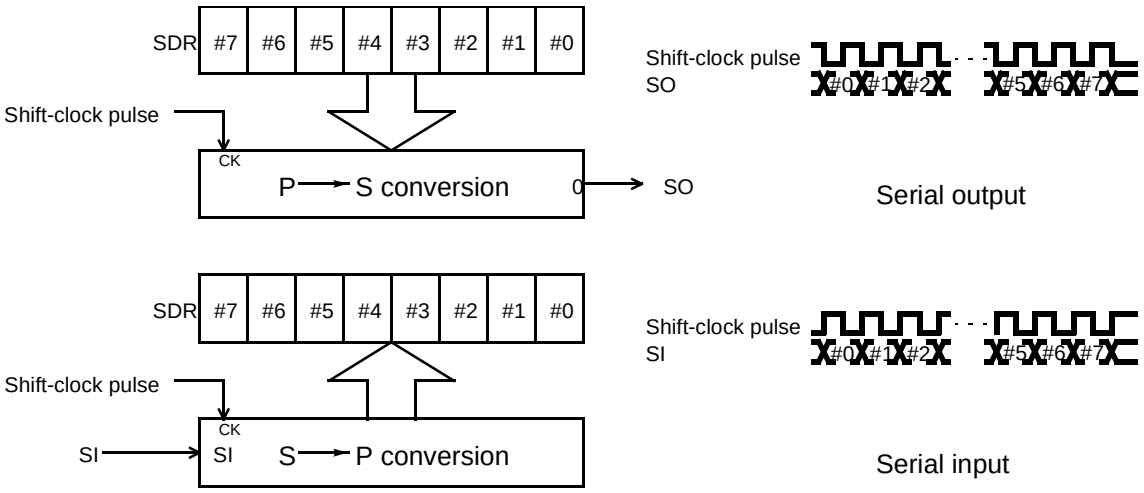
Peripherals

(4) Description of operation

The operation of 8-bit serial I/O is described below.

(a) Outline

This module consists of the serial-mode register (SMR) and serial-data register (SDR). At serial output, data in the SDR is output in bit serial to the serial output pin (SO) in synchronization with the falling edge of a serial shift-clock pulse generated from the internal or external clock. At serial input, data is input in bit serial from the serial input pin (SI) to the SDR at the rising edge of a serial shift-clock pulse.



(b) Operation modes

The serial I/O has three internal shift-clock modes and one external shift-clock mode according to the type of shift-clock, which are specified by the SMR. Mode switching or clock selection should be made with serial I/O stopped (SST bit of SMR = 0).

a. Internal shift-clock mode

Operation is performed by the internal clock. A shift-clock pulse with a duty of 50% is output at the SCK pin as a synchronous timing output. Data is transferred bit-by-bit at every clock pulse.

b. External shift-clock mode

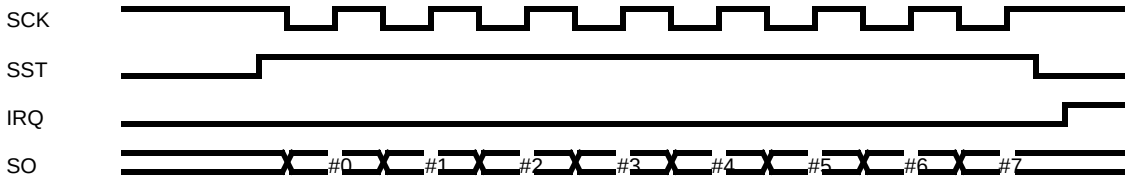
Data is transferred bit-by-bit at every clock pulse in synchronization with the external shift-clock pulse input from the SCK pin. The transfer speed can be from DC to 1 (2 instruction cycles). When one instruction cycle is 1 μs (at 5 MHz oscillation), the transfer speed can be up to 500 kHz.

Do not write data to the SMR and SDR during the serial I/O operation in either mode.

Peripherals

(c) Interrupt functions

This module can output an interrupt request to the CPU. To output an interrupt request, set the SIOE bit (bit 6) of the SMR to 1 to enable an interrupt and then set the interrupt flag SIOF bit (bit 7) of the SMR after 8-bit data transfer is terminated.

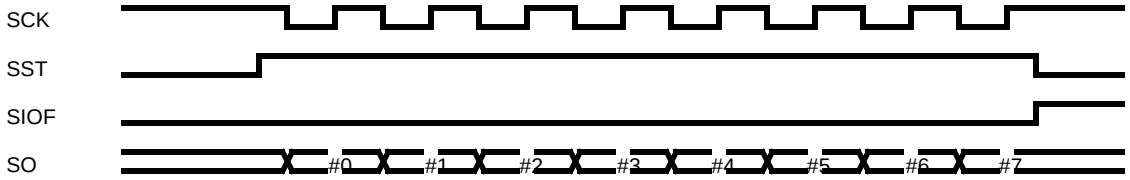


(d) Shift start/stop timing

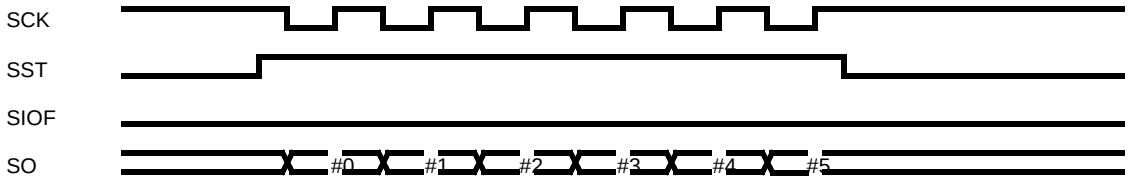
Data transfer starts when 1 is written at the SST bit (bit 0) of the SMR, and stops when 0 is written. When data transfer is terminated, the SST bit is automatically cleared to 0, which stops the operation.

a. Internal shift-clock mode (LSB first)

[When transfer terminated]

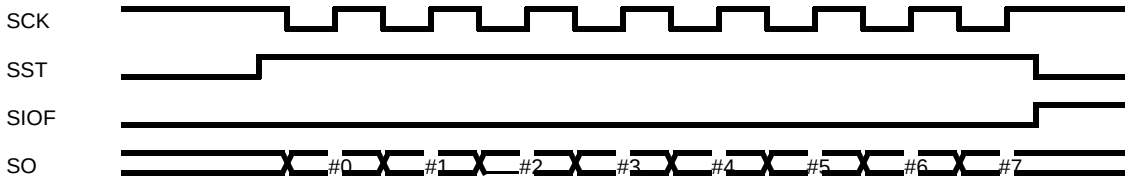


[When transfer suspended]



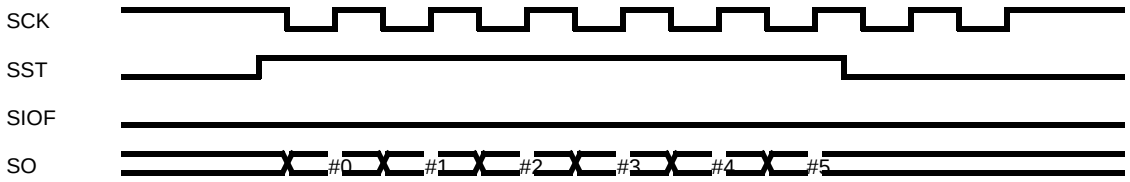
b. External shift-clock mode (LSB first)

[When transfer terminated]



Peripherals

[When transfer suspended]



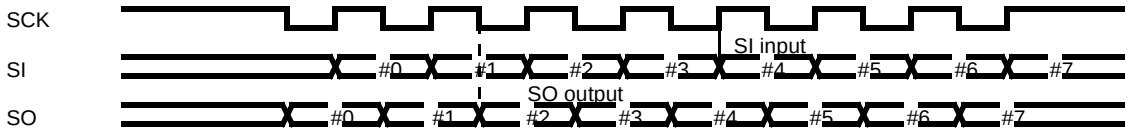
Note: When data is written at the SDR, the output data changes at the falling edge of the external-clock pulse.

Fig. 2.19 Shift Start/Stop Timing

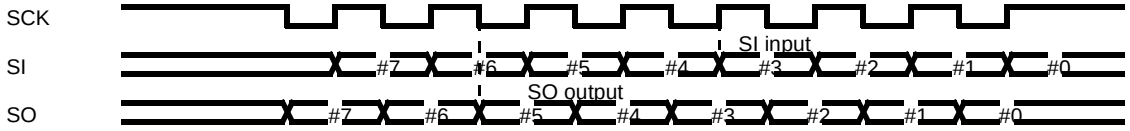
(e) Input/output shift timing

Data is output from the serial output pin (SO) at the falling edge of the shift-clock pulse, and is input from the serial input pin (SI) to the SDR at the rising edge of the shift-clock pulse.

a. LSB first (BDS = 0)



b. MSB first (BDS = 1)



DI7 to DI0 indicate input data, and DO7 to DO0 indicate output data.

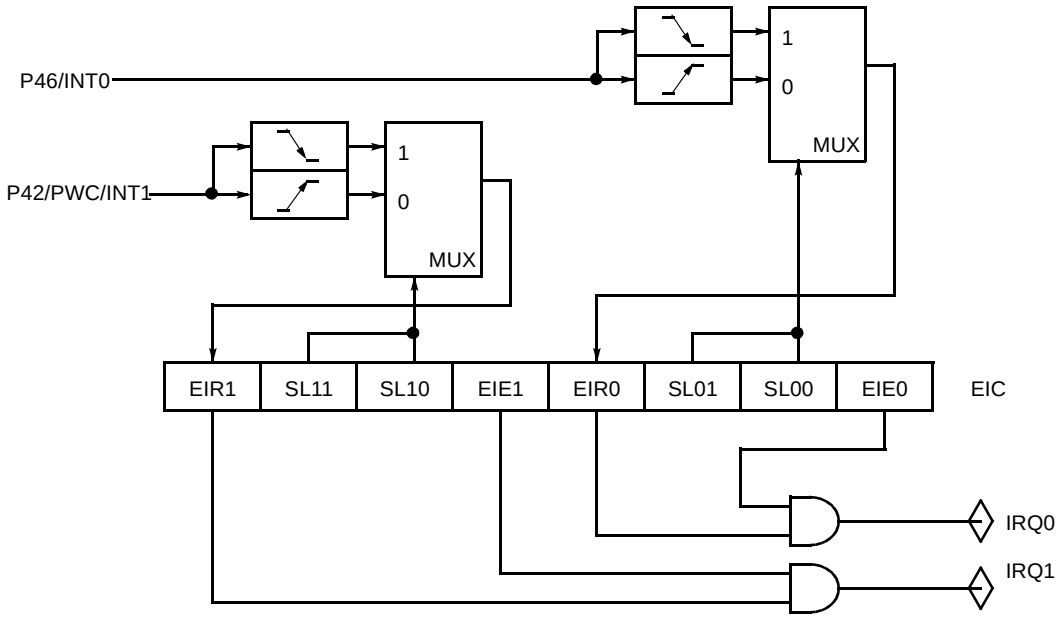
Fig. 2.20 Input/Output Shift Timing

Peripherals

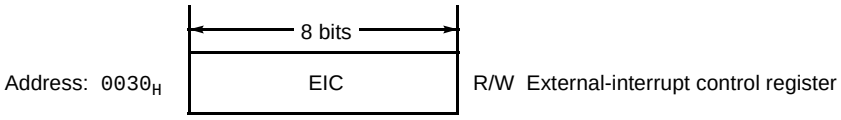
2.2.6 External Interrupt

- The edges of external-interrupt sources can be detected to set the corresponding flag.
- An interrupt can be generated at the same time the flag is set.
- The interrupts can release the STOP or SLEEP mode.

(1) Block diagram



(2) Registers



(3) Description of registers

(a) External-interrupt control register (EIC)

The EIC controls interrupts by the INT pins.

Address: 0030_H EIC

Address: 0030_H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIR1	SL11	SL10	EIE1	EIR0	SL01	SL00	EIE0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
(Initial value) 00000000_B							

Peripherals

[Bit 7] EIR1: External-interrupt request flag

When the edge specified by the SL11 and SL10 bits is input to the INT1 pin, bit 7 is set to 1. When the EIE1 bit is 1, an interrupt request (IRQ1) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT1 pin
1	Specified edge input to INT1 pin (IRQ1 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	Clears this bit
1	Unchanges this bit and other bits unaffected

[Bits 6 and 5] SL11 and SL10: Edge-polarity mode select bits

These bits are used to control the input edge polarity mode of the INT1 pin.

SL11	SL10	
0	0	No edge detected
0	1	Rising edge
1	0	Falling edge
1	1	Both-edge mode

[Bit 4] EIE1: Interrupt-enable bit

This bit is used to enable an external-interrupt request by the INT1 pin.

0	Disables interrupt request
1	Enables interrupt request by EIR1 setting

[Bit 3] EIR0: External-interrupt request flag

When the edge specified by the SL01 and SL00 bits is input to the INT0 pin, bit 3 is set to 1. When the EIE0 is 1, an interrupt request (IRQ0) is output if this bit is set.

The meaning of each bit to be read is as follows:

0	Specified edge not input to INT pin
1	Specified edge input to INT pin (IRQ0 is output.)

1 is always read when the Read Modify Write instruction is read.

The meaning of each bit to be written is as follows:

0	Clears this bit
1	Unchanges this bit and other bits unaffected

Peripherals

[Bits 2 and 1] SL01 and SL00: Edge-polarity mode select bits

Bit 2 and bit 1 are used to control the input edge polarity mode of the INT0 pin.

When internal pull-up resistors option is chosen for P42 or P46, only falling edge can wake up the CPU from stop mode or sleep mode.

SL01	SL00	
0	0	No edge detected
0	1	Rising edge
1	0	Falling edge
1	1	Both-edge mode

[Bit 0] EIE0: Interrupt-enable bit

Bit 0 is used to enable an external-interrupt request by the INT0 pin.

0	Disables interrupt request
1	Enables interrupt request by EIR0 setting

(4) Precautions for external-interrupt circuit

When enabling an interrupt after clearing reset, always clear the interrupt flag simultaneously. An interrupt request is output immediately when the interrupt flags (EIR0, EIR1) are set to 1.

Peripherals

2.2.7 LCD Controller/driver

The LCD controller/driver consists of the display controller that generates segment and common signals according to the display data and memory data, and the segment and common drivers that can drive the LCD panel directly.

- Direct LCD driving
- 4 common outputs (COM0 to COM3) and 42 segment outputs (SEG0 to SEG41)
- 21-byte display data memory
- 1/2, 1/3, or 1/4 selected as duty.
- SEG20 to SEG41 can be used as general-purpose ports (option).

(1) Block diagram

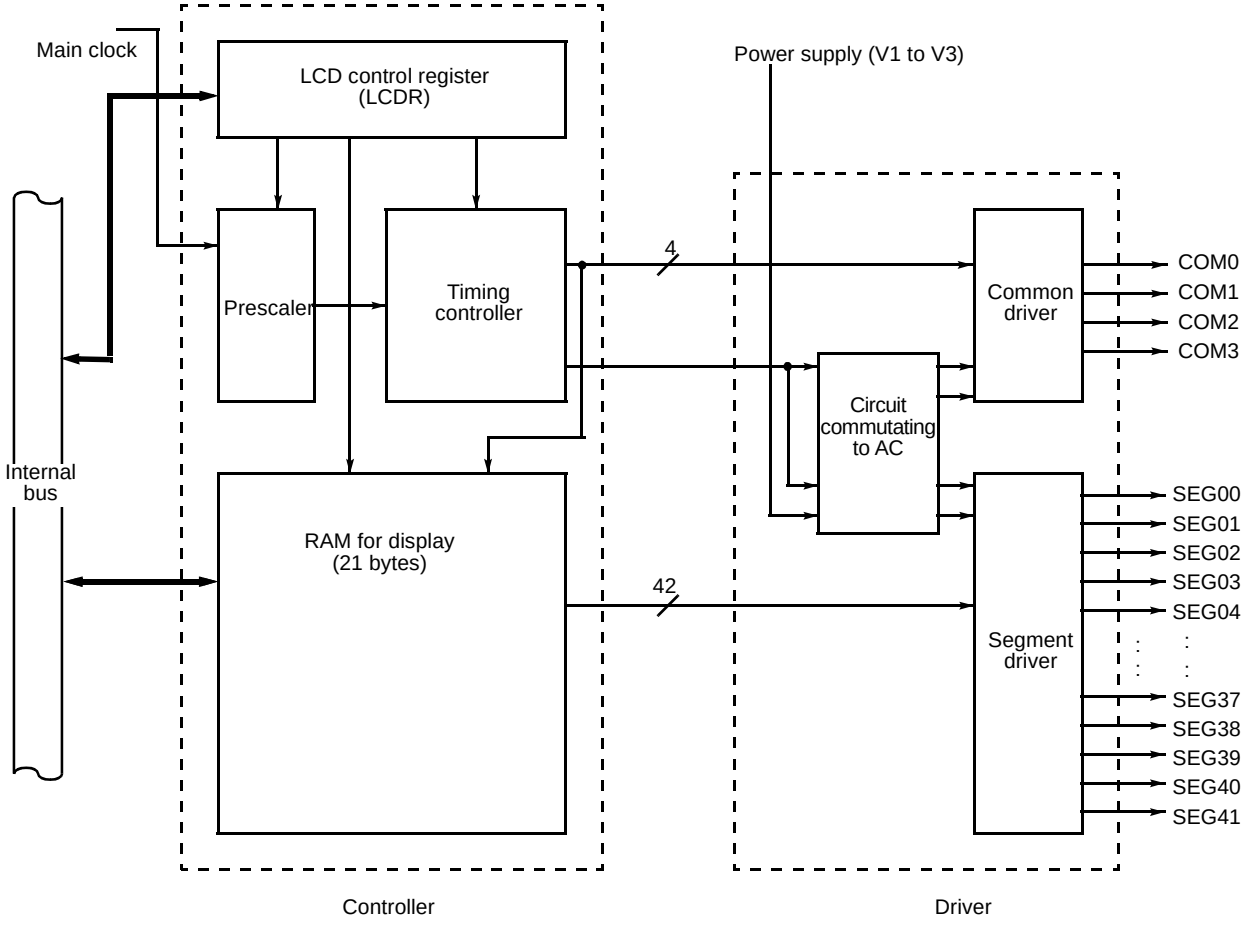
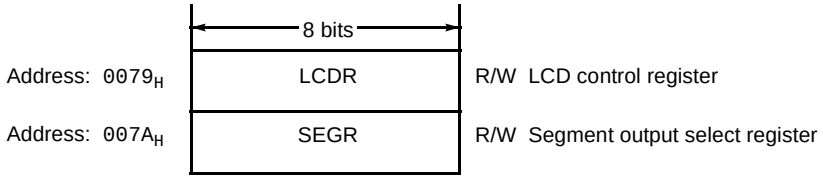


Fig. 2.21 LCD Controller /Driver Block Diagram

Peripherals

(2) Registers



(3) Description of registers

The detail of LCD control register is described below.

Address: 0079H LCDR

Address: 007AH SEGR

(a) LCD control register (LCDR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0079H	—	PSEL	VSEL	BK	MS1	MS0	FP1	FP0
		(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
				(Initial value)				
				x0010000B				

[Bits 7]: Always write 0.

[Bit 6] PSEL:
This bit is used to select LCD voltage V1, V2 and P32, P33.

1	Select P32 and P33
0	Select V1 and V2 (Initial value)

[Bit 5] VSEL: Drive power control bit
This bit is used to control LCD drive power.

0	Connection of internal resistor for divided voltage enters off state
1	Connection of internal resistor for divided voltage enters on state

[Bit 4] BK: Display or display blanking select bit
This bit is used to select display or display blanking. The segment output in display blanking is an non-conforming waveform.

0	Display
1	Display blanking

Peripherals

[Bits 3 and 2] MS1 and MS0: Display mode select bit

These bits are used to select display mode. The mode is set according to the following table.

MS1	MS0	Display mode	Number of time divisions: N
0	0	LCD stop	—
0	1	1/2 duty output mode	2
1	0	1/3 duty output mode	3
1	1	1/4 duty output mode	4

[Bits 1 and 0] FP1 and FP0 (Frame Period 1 and 0): Clock cycle select bit

These bits are used to select the LCD clock cycle. The frame frequency is shown below. Calculate the optimum frame frequency and set the register according to the LCD module.

FP1	FP0	Frame frequency	
0	0	$f_{CH}/(2^{11} \times N)$	610 Hz (N = 4)
0	1	$f_{CH}/(2^{12} \times N)$	305 Hz (N = 4)
1	0	$f_{CH}/(2^{13} \times N)$	153 Hz (N = 4)
1	1	$f_{CH}/(2^{14} \times N)$	76 Hz (N = 4)

N: Number of time divisions
f_{CH}: Clock frequency (5 MHz)

Address: 0079H LCDR

Address: 007AH SEGR

(b) Segment output select register (SEGR)

Address: $007A_H$

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG00
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
	(Initial value)						
	-0000000_B						

[Bits 6 to 0] SEG15 to SEG00: Port/segment output select bit

0	Selects port function
1	Selects segment output

SEG00: Selection bit for P00/SEG20 to P07/SEG27
SEG10: Selection bit for P10/SEG28 to P13/SEG31
SEG11: Selection bit for P14/SEG32 and P15/SEG33
SEG12: Selection bit for P16/SEG34
SEG13: Selection bit for P17/SEG35
SEG14: Selection bit for P20/SEG36 to P23/SEG39
SEG15: Selection bit for P24/SEG40 to P25/SEG41

Note: The setting of this register MUST be consistent with the mask option. This register cannot override the mask option.

Peripherals

(4) RAM for display

The LCD controller/driver contains the 21 × 8-bit RAM for generating a segment output signal. The data of this RAM is automatically read in synchronization with the common signal select timing and the waveform corresponding to this data is output from the segment output pin.

42 segment signals correspond to 21 locations of the display RAM. Each location bit is in synchronization with the common signal select timing: bits 0 and 4 with COM0, bits 1 and 5 with COM1, bits 2 and 6 with COM2, and bits 3 and 7 with COM3. If the value of each bit is 1, the signal is converted to LCD voltage and if it is 0, the signal is converted to non-LCD and is output. However, at reset, COM0 to COM3 and SEG0 to SEG19 go Low, and SEG20 to SEG41 go high impedance because they also serve as I/O ports.

The waveform is output from the segment pins irrespective of the CPU operation. Therefore, reading and writing from and to the display RAM are possible in any timing.

When using SEG20 to SEG41 as general-purpose output ports, the 11 upper bytes ($006E_H$ to 0078_H) are usually used as RAM.

Address	COM3	COM2	COM1	COM0	Segment	
064H	b3	b2	b1	b0	SEG00	
	b7	b6	b5	b4	SEG01	
065H	b3	b2	b1	b0	SEG02	
	b7	b6	b5	b4	SEG03	
:	:	:	:	:	:	
:	:	:	:	:	:	
06DH	b3	b2	b1	b0	SEG18	
	b7	b6	b5	b4	SEG19	
06EH	b3	b2	b1	b0	SEG20	
	b7	b6	b5	b4	SEG21	
06FH	b3	b2	b1	b0	SEG22	
	b7	b6	b5	b4	SEG23	Multiplexed with port 0
070H	b3	b2	b1	b0	SEG24	
	b7	b6	b5	b4	SEG25	
071H	b3	b2	b1	b0	SEG26	
	b7	b6	b5	b4	SEG27	
072H	b3	b2	b1	b0	SEG28	
	b7	b6	b5	b4	SEG29	
073H	b3	b2	b1	b0	SEG30	
	b7	b6	b5	b4	SEG31	Multiplexed with port 1
074H	b3	b2	b1	b0	SEG32	
	b7	b6	b5	b4	SEG33	
075H	b3	b2	b1	b0	SEG34	
	b7	b6	b5	b4	SEG35	
076H	b3	b2	b1	b0	SEG36	
	b7	b6	b5	b4	SEG37	
077H	b3	b2	b1	b0	SEG38	
	b7	b6	b5	b4	SEG39	Multiplexed with port 2
078H	b3	b2	b1	b0	SEG40	
	b7	b6	b5	b4	SEG41	

Peripherals

(5) Operation

First, write the data to be displayed to display RAM. Then, set the value corresponding to the LCD panel to be used to LCDR (LCD control register). The LCD drive waveform is output according to the data in the display RAM, when the clock pulse is supplied.

The display drive output has a 2-frame AC waveform. The combination of bias and duty shown below may be possible. Note that the combination of 1/3 bias and 1/2 duty should not be used. Examples of waveforms are shown on the following pages.

	1/2 duty	1/3 duty	1/4 duty
1/2 bias	◎	×	×
1/3 bias	×	◎	◎

◎ : Recommended mode
× : Application disabled

In the 1/2 duty mode, the COM2 and COM3 output waveforms are non-selective level. The COM3 output waveform is also a non-conforming waveform at 1/3 duty.

When LCD operation is terminated, both common and segment produce waveforms at L level. However, when SEG20 to SEG41 are specified as general-purpose port by the mask option, segment data are not output.

Peripherals

(6) LCD drive output waveform

(a) Waveform at 1/2 bias and 1/2 duty

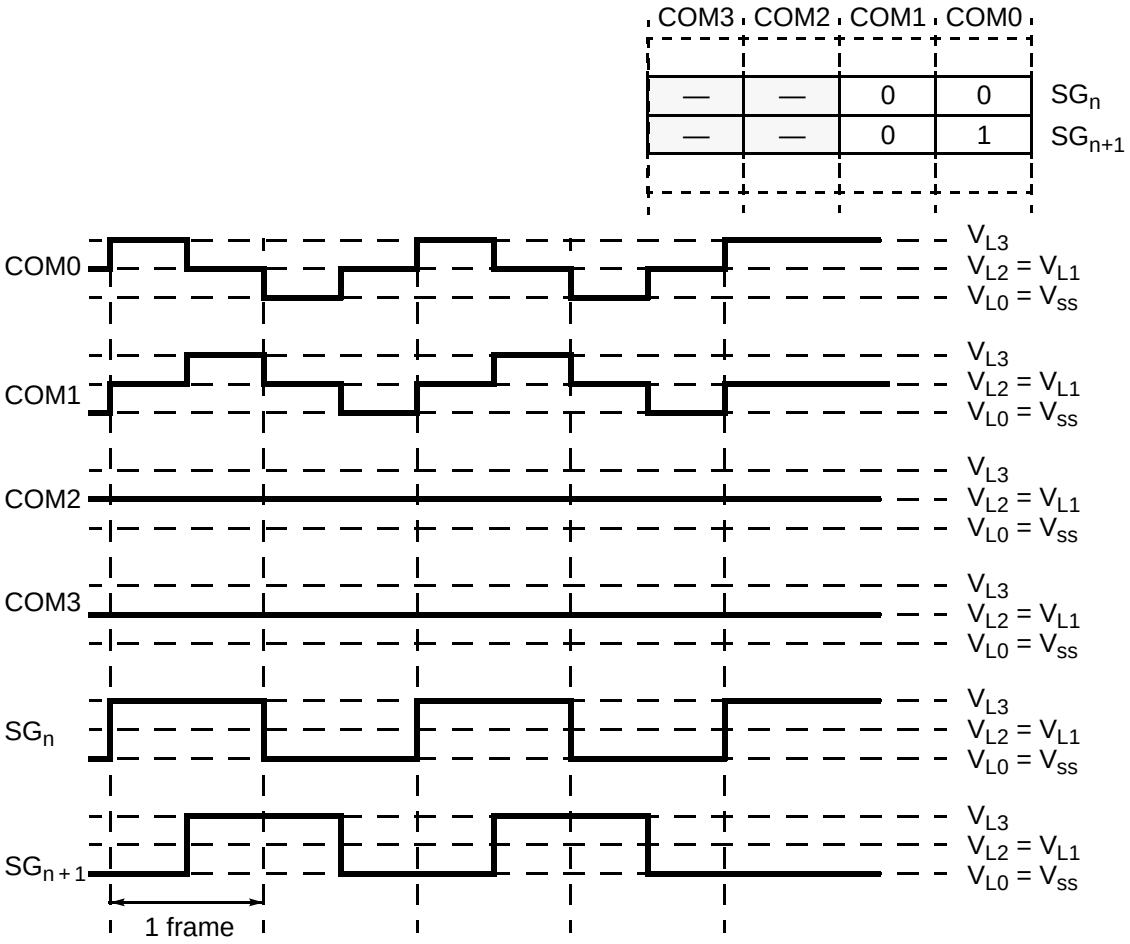


Fig. 2.22 Example of Waveform at Pin Corresponding to the RAM Data for Display

(b) Waveform at 1/3 bias and 1/3 duty

COM3	COM2	COM1	COM0	
—	1	0	0	SG_n
—	1	0	1	SG_{n+1}

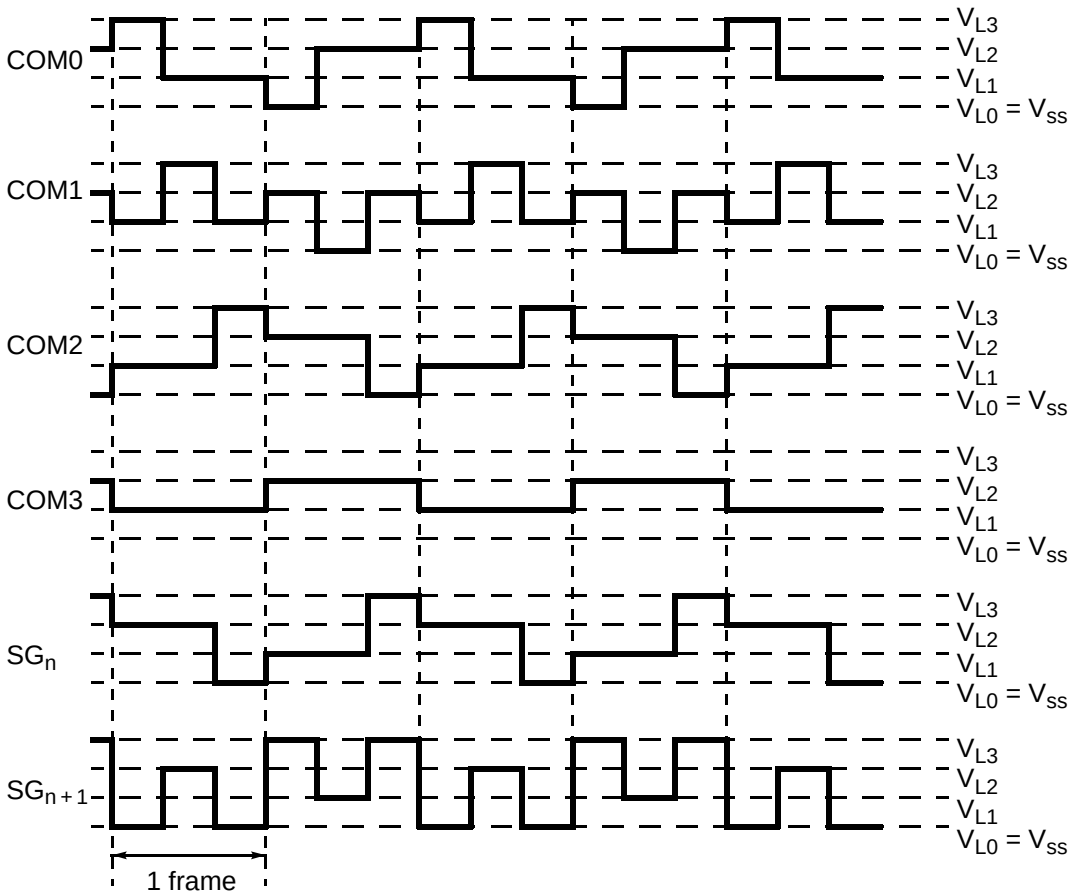


Fig. 2.23 Example of Waveform at Pin Corresponding to the RAM Data for Display

Peripherals

(c) Waveform at 1/3 bias and 1/4 duty

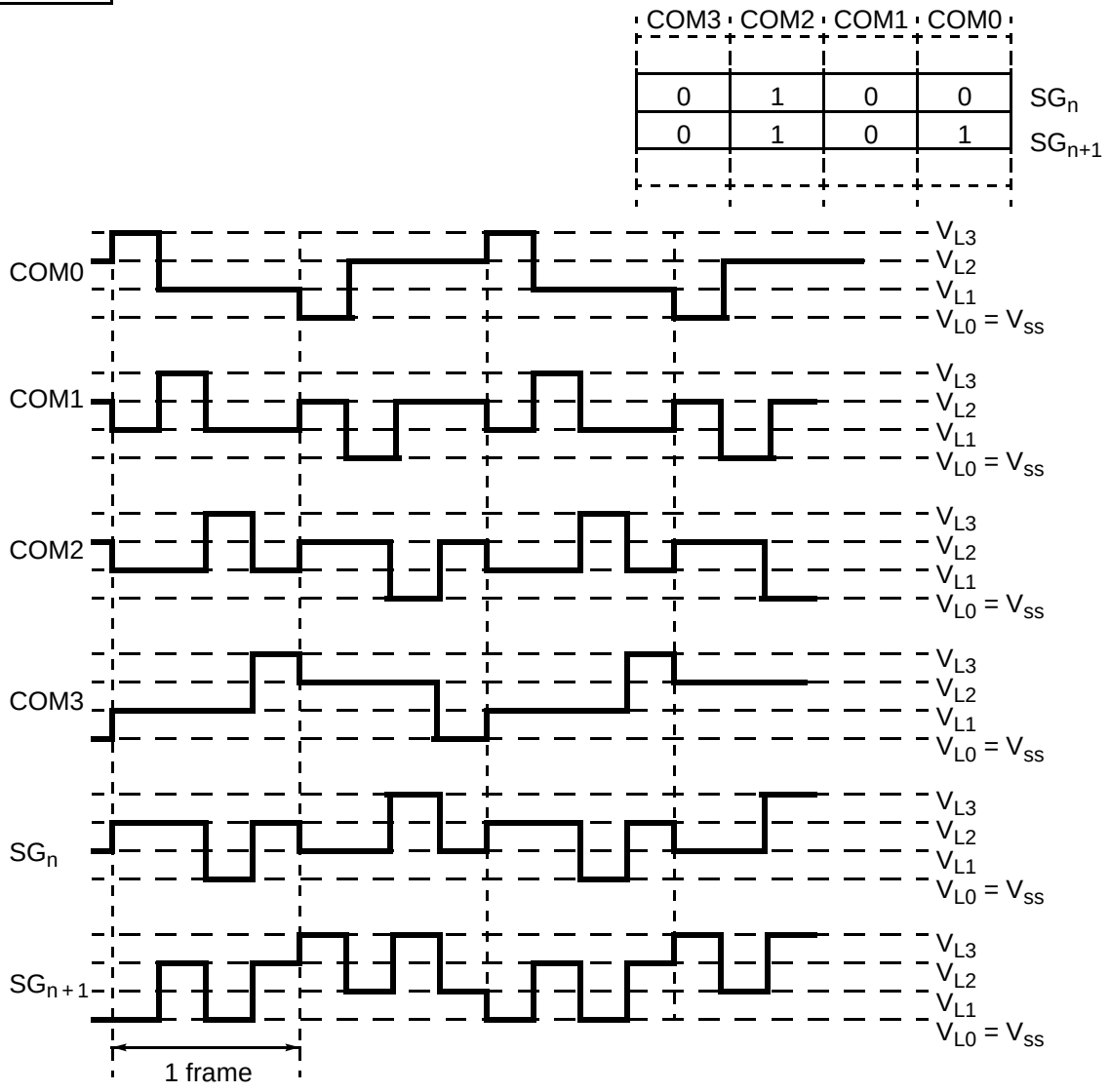


Fig. 2.24 Example of Waveform at Pin Corresponding to the RAM Data for Display

Peripherals

(7) Voltage setting at power pins (V3, V2 and V1) for driving LCD

Set the voltages at the LCD power pins (V3, V2 and V1) as shown below.

	V3	V2	V1
1/2 bias	V_{LCD}	1/2 V_{LCD}	1/2 V_{LCD}
1/3 bias	V_{LCD}	2/3 V_{LCD}	1/3 V_{LCD}

V_{LCD} : LCD operating voltage

A connection example for supply power to drive the LCD is shown in Fig. 2.25.

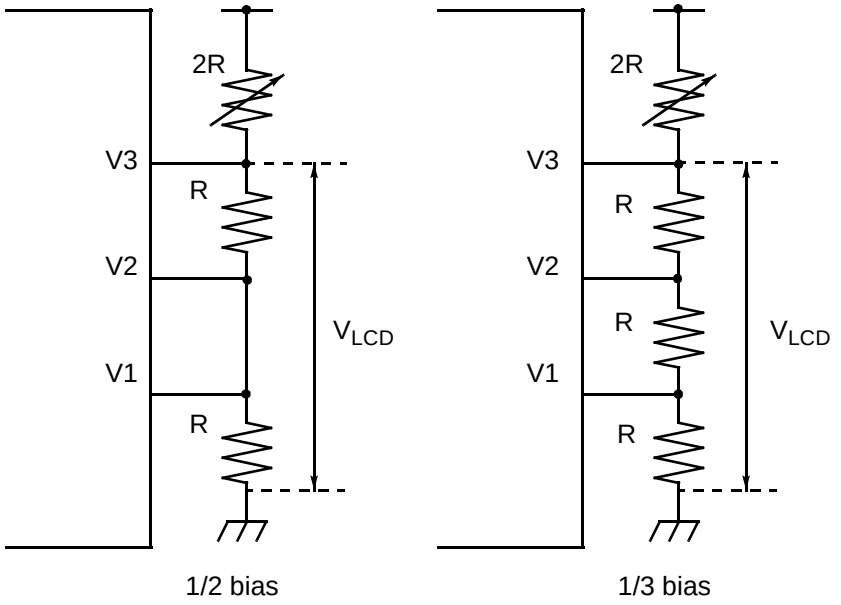


Fig. 2.25 Connection Examples for Supply Power for Driving LCD

Note: To set a 1/2 bias when using the external dividing resistor (ladder circuit), short-circuit the pins V2 and V1.

Built-in voltage dividing resistor

The built-in voltage dividing resistors are connected as shown in Fig. 2.26. Writing 1 at the VSEL bit connects the built-in voltage dividing resistors. Therefore, write 1 at the VSEL bit to connect the resistors and set 0 to disconnect the resistors.

The built-in voltage dividing circuit is connected to the V_{SS} through the transistor within chip. Therefore, the current flowing into the resistor can be cut when the LCD stops.

Peripherals

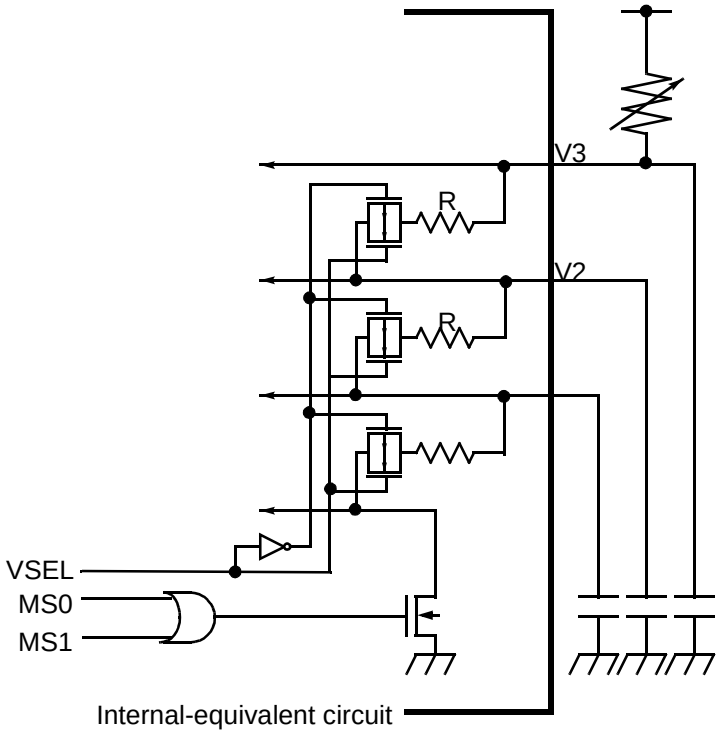


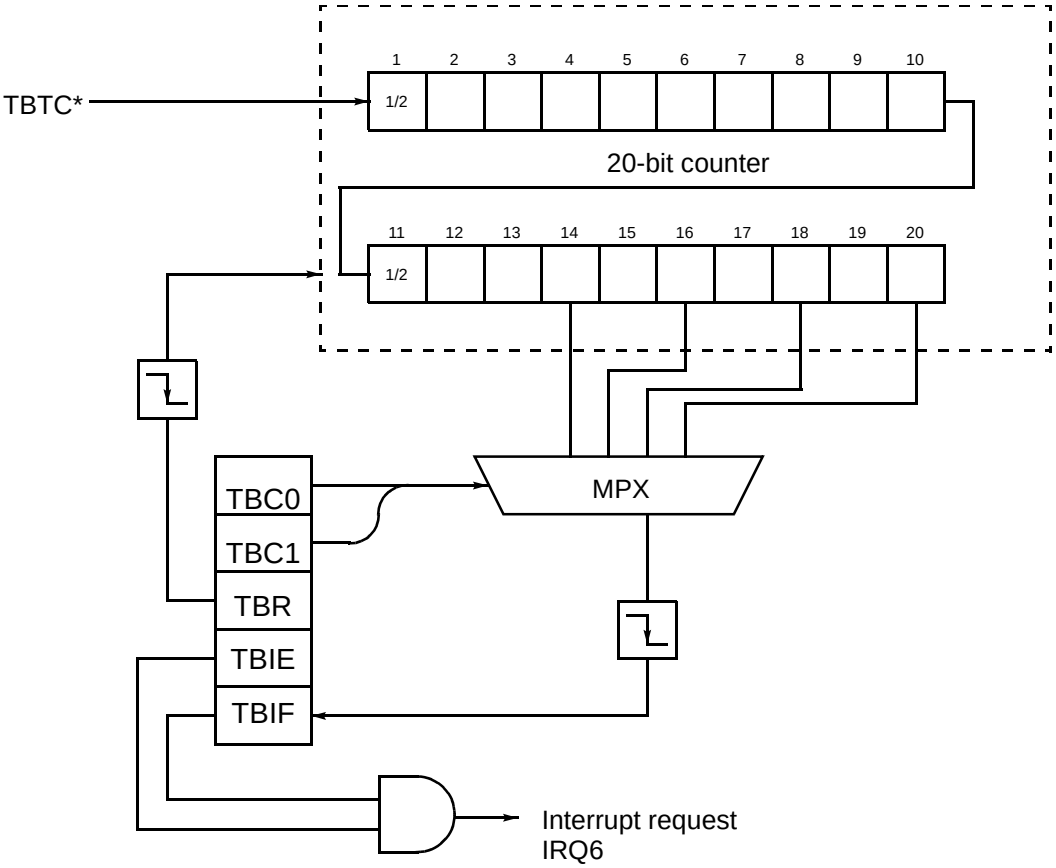
Fig. 2.26 Built-in Voltage Dividing resistors

Peripherals

2.2.8 Time-base Timer

- This timer has a 20-bit binary counter and uses a clock pulse with 1/2 oscillation of the main clock.
- Can be selected from four interval times
- This function cannot be used when the main clock is stopped.

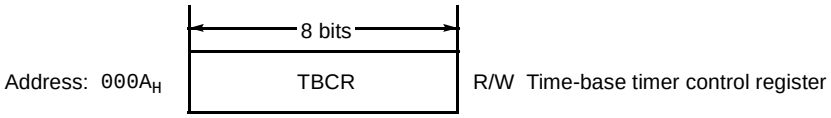
(1) Block diagram



* TBTC is a clock pulse with 1/2 oscillation of the main clock oscillation.

(2) Register list

The time-base timer has one time-base timer control register (TBCR).



Peripherals

Address: $000A_H$ TBCR

(3) Description of registers

The detail of time-base timer control register (TBCR) is described below.

(a) Time-base timer control register (TBCR)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: $000A_H$	—	—	—	TBIE	TBIF	TBR	TBC1	TBC0
				(R/W)	(R/W)	(W)	(R/W)	(R/W)
				(Initial value) $XXX00000_B$				

[Bit 4] TBIE: Interval-timer interrupt enable bit

This bit is used to enable an interrupt by the interval timer.

0	Disables interval interrupt
1	Enables interval interrupt

[Bit 3] TBIF: Interval timer overflow bit

When writing, this bit is used to clear the interval timer overflow flag.

0	Clears interval timer overflow flag
1	No operation

When reading, this bit indicates that an interval timer overflow has occurred.

0	No interval timer overflow
1	Interval timer overflow

During Read Modify Write instruction, 1 is always read. If the TBIF bit is set to 1 when the TBIE bit is 1, an interrupt request is output. This bit is cleared upon reset.

[Bit 2] TBR: Time-base timer clear bit

This bit is used to clear time-base timer.

0	Clears time-base timer
1	No operation

This bit is always read 1.

[Bits 1 and 0] TBC1, TBC0: Interval time specification bits

These bits are used to specify interval timer cycle

TBC1	TBC0	Interval time	Value at f_{CH} = 5 MHz
0	0	$2^{15}/f_{CH}$	6.55 [ms]
0	1	$2^{17}/f_{CH}$	26.21 [ms]
1	0	$2^{19}/f_{CH}$	104.86 [ms]
1	1	$2^{21}/f_{CH}$	0.42 [s]

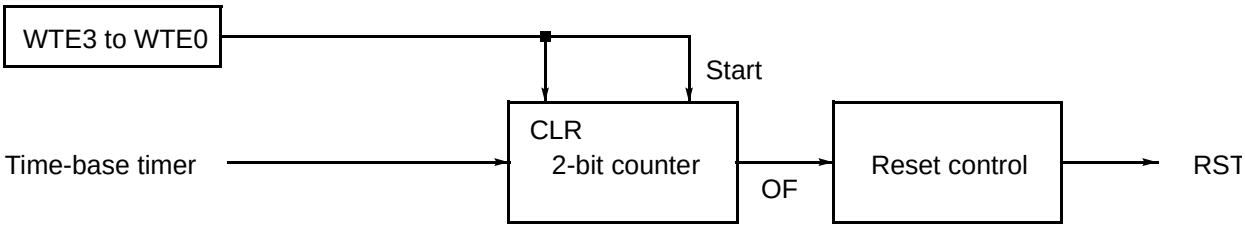
f_{CH}: clock frequency

Peripherals

2.2.9 Watchdog Timer Reset

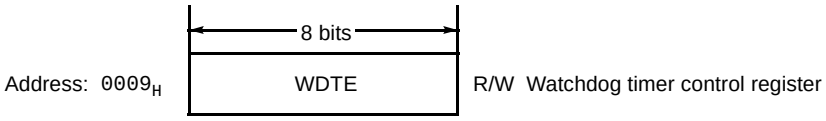
A watchdog reset is generated using the output of the time-based timer as a clock pulse.

(1) Block diagram



(2) Registers

The watchdog timer reset has one watchdog timer control register (WDTE).



(3) Description of register

The detail of the watchdog timer control register (WDTE) is described below.

Address: 0009_H WDTE

(a) Watchdog timer control register (WDTE)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0009_H	—	—	—	—	WTE3	WTE2	WTE1	WTE0
					(W)	(W)	(W)	(W)
					(Initial value)			
					$XXXXXXXX_B$			

[Bits 3 to 0] WTE3 to WTE0: Watchdog timer control bits
These bits are used to control the watchdog timer.

First write only after reset

0101	Starts watchdog timer
Other than the above	No operation

Second and later write

0101	Clears watchdog timer counter
Other than the above	No operation

The watchdog timer can be stopped only by reset. These bits are read 1111.

Peripherals

(4) Description of operation

The watchdog timer enables the detection of program malfunction.

(a) Starting watchdog timer

The watchdog timer starts when 0101 is written at the watchdog timer control bits.

(b) Clearing watchdog timer

When 0101 is written at the watchdog timer control bits after start, the watchdog timer is cleared. The counter of the watchdog timer is cleared when changing to the standby mode (STOP, SLEEP, WATCH).

(c) Watchdog timer reset

If the watchdog timer is not cleared within the time given in the table below, a watchdog timer reset occurs to reset the chip internally.

	Time-base timer cycle $1/2^{21}f_{CH}$
Minimum time	Approx. 419 ms
Maximum time	Approx. 839 ms

f_{CH} = 5 MHz

(d) Stopping watchdog timer

Once started, the watchdog timer will not stop until a reset occurs.

3. OPERATION

The operation of MB89950 is described below.

3.1 Clock Pulse Generator

The MB89950 series of microcontrollers contain the system clock pulse generator. The crystal oscillator is connected to the X0 and X1 pins to generate clock pulses. Clock pulses can also be supplied internally by inputting externally-generated clock pulses to the X0 pin. The X1 pin should be kept open.

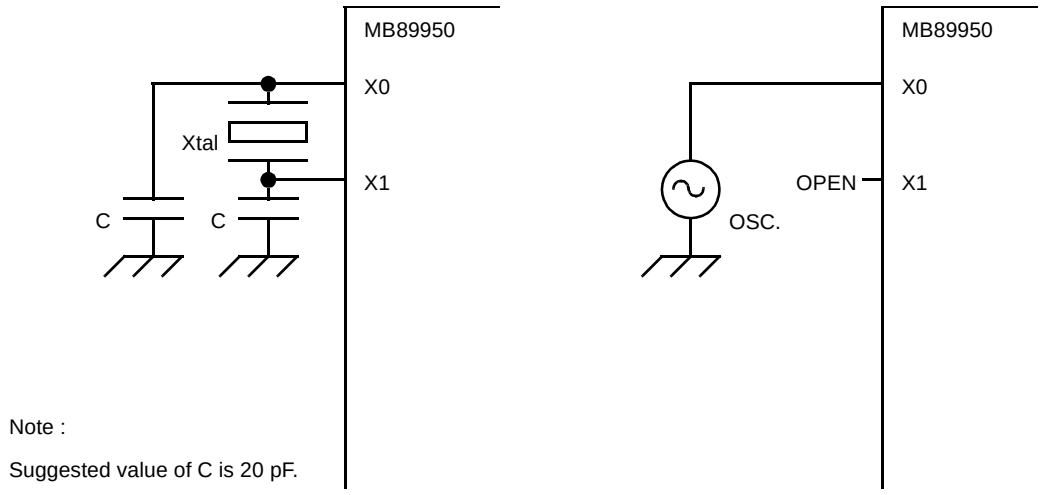


Fig. 3.1 Clock Pulse Generator

3.2 Reset

The detail of reset operation and reset sources are described below.

3.2.1 Reset Operation

When reset conditions occur, the MB89950 series of microcontrollers suspend the currently-executing instruction to enter the reset state. The contents written at the RAM do not change before and after reset. However, if a reset occurs during writing of 16-bit long data, data is written to the upper bytes and may not be written to lower bytes. If a reset occurs around write timing, the contents of the addresses being written are not assured.

When the reset conditions are cleared, the MB89950 series of microcontrollers are released from the reset state and start operation after fetching the mode data from address $FFFD_H$, the upper bytes of the reset vectors from address $FFFE_H$, and the lower bytes from address $FFFF_H$, in that order. Fig. 3.2 shows the flowchart for the reset operation.

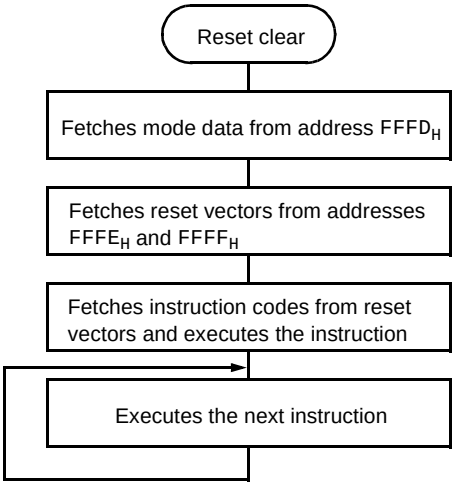


Fig. 3.2 Outline of Reset Operation

Fig. 3.3 indicates the structure of data to be stored in addresses $FFFD_H$, $FFFE_H$, and $FFFF_H$.

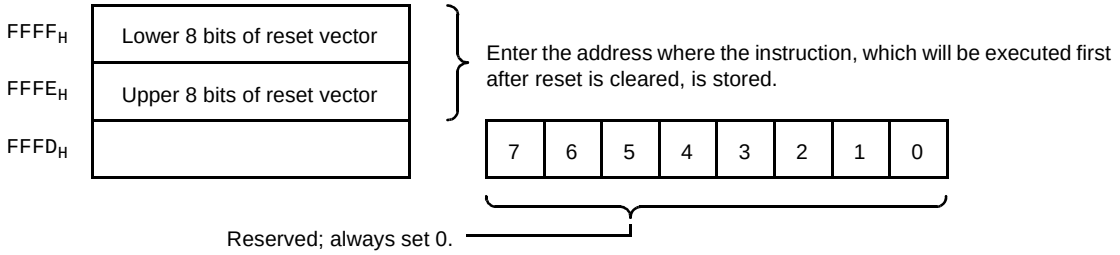


Fig. 3.3 Reset Vector Structure

3.2.2 Reset Sources

The MB89950 series of microcontrollers have the following reset sources.

(1) External pin	When a Low level is input to the RST pin
(2) Specification by software	When 0 is written at the RST bit of the standby-control register
(3) Power-on	Power on when the power-on reset option is selected
(4) Watchdog function	When the watchdog function is enabled by the watchdog-control register and reaccess to this register is not obtained within the specified time

When the stop mode is cleared by reset or power-on reset (optionally selected), operation is started after elapse of the oscillation stabilization time.

For details, see page 2-9.

3.3 Interrupt

If the interrupt controller and CPU are ready to accept interrupts when an interrupt request is received from the internal peripherals or an external-interrupt, the CPU finished the currently-executing instruction and executes the interrupt-processing program. Fig. 3.4 shows the interrupt-processing flowchart.

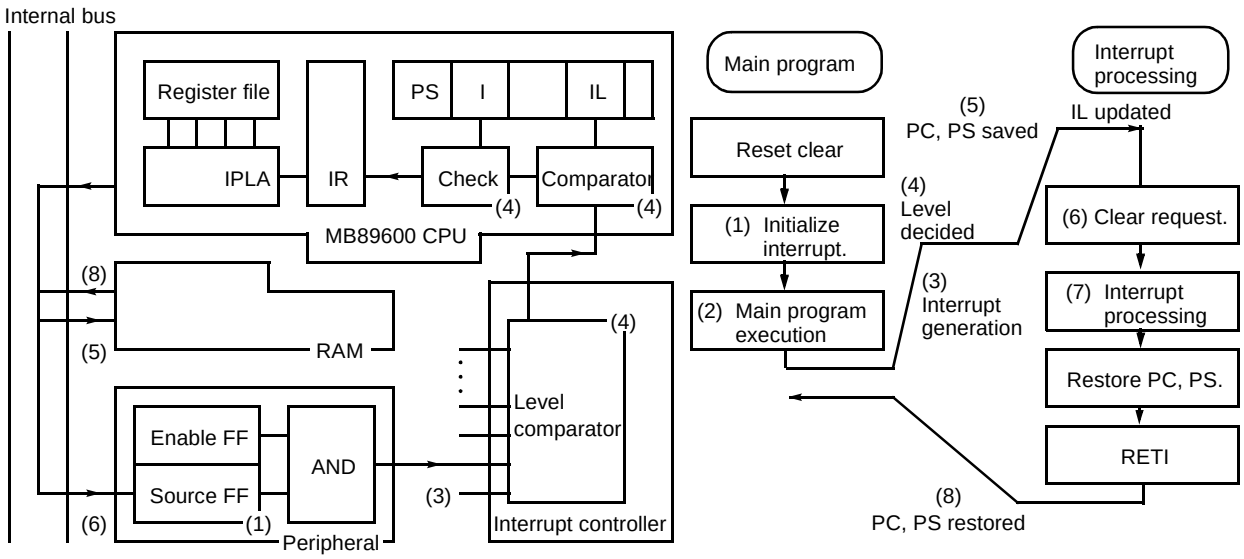


Fig. 3.4 Interrupt-processing Flowchart

All interrupts are disabled right after reset. Therefore, the main program (1) should initialize interrupts . Each peripheral generating interrupts and the interrupt-level-setting registers (ILR1 to ILR3) in the interrupt controller corresponding to these interrupts should be initialized. The levels of all interrupts can be set by the interrupt-level-setting registers (ILR1 to ILR3) from address 007CH to 007EH in the interrupt controller. The interrupt level can be set from 1 to 3, where 1 indicates the highest level, and 2 the second highest level. Level 3 indicates that no interrupt occurs. The interrupt request of this level cannot be accepted. After setting the peripherals, the main program executes various controls (2). Interrupts are generated from the peripherals (3). The highest-priority interrupt requests are identified from those occurring at the same time by the interrupt controller and are transferred to the CPU. The CPU then checks the current interrupt level and the status of the I-flag (4), and starts the interrupt processing.

The CPU performs the interrupt processing to save the contents of the current PC and PS in the stack (5) and fetches the entry addresses of the interrupt program from the interrupt vectors. After updating the IL value in the PS to the required one, the CPU starts executing the interrupt-processing routine.

Clear the interrupt sources (6) and process the interrupts in the user's interrupt-processing routine. Finally, the CPU restores the PC and PS values from the stack (8) by the RETI instruction; and then return to the interrupted instruction.

Note: Unlike the F^2MC-8 family, A and T are not saved in the stack at the interrupt time.

Table 3–1 lists the relationships between each interrupt source and interrupt vector.

Table 3–1 Interrupt Sources and Interrupt Vectors

Interrupt Source	Upper vector address	Lower vector address
IRQ0 (External interrupt 0)	$FFFA_H$	$FFFB_H$
IRQ1 (External interrupt 1	$FFF8_H$	$FFF9_H$
IRQ2 (8-bit PWM timer)	$FFF6_H$	$FFF7_H$
IRQ3 (Pulse-width count timer)	$FFF4_H$	$FFF5_H$
IRQ4 (UART)	$FFF2_H$	$FFF3_H$
IRQ5 (8-bit serial I/O)	$FFF0_H$	$FFF1_H$
IRQ6 (Interval timer)	$FFEE_H$	$FFEF_H$
IRQ7 (Unused)	$FFEC_H$	$FFED_H$
IRQ8 (Unused)	$FFEA_H$	$FFEB_H$
IRQ9 (Unused)	$FFE8_H$	$FFE9_H$
IRQA (Unused)	$FFE6_H$	$FFE7_H$
IRQB (Unused)	$FFE4_H$	$FFE5_H$

3.4 Low-power Consumption Modes

The MB89950 series of microcontrollers have two standby modes: sleep and stop to reduce the power consumption. Writing to the standby control register (STBC) gives a transition to these two standby modes. See section 2.1.4 for setting and releasing each mode.

Whether or not an oscillation stabilization period is required at release from each low-power consumption mode depends on the mask option of the power-on reset (See page 2-9).

Table 3–2 Low-power Consumption Mode at Each Clock Mode

Function		Operation mode		
		RUN	SLEEP	STOP
Main clock		Operate	Operate	Stop
CPU	Instruction	Operate	Stop	Stop
	ROM	Operate	Hold	Hold
	RAM			
Peripheral	I/O	Operate	Hold	Hold
	Timer-base timer	Operate	Operate	Stop
	8-bit PWM	Operate	Operate	Stop
	Pulse width counter	Operate	Operate	Stop
	8-bit SIO	Operate	Operate	Stop
	UART	Operate	Operate	Stop
	LCDC	Operate	Operate	Stop
	External Interrupt	Operate	Operate	Operate
	Watchdog timer	Operate	Operate	Stop

3.5 Pin States For Sleep, Stop, and Reset

The state of each pin of the MB89950 series of microcontrollers at sleep, stop and reset is as follows:

(1) Sleep — The pin state immediately before the sleep state is held.

(2) Stop — The pin state immediately before the stop state is held when the stop mode is started and bit 5 of the standby-control register (STBC) is set to 0; the impedance of the output and input/output pins goes High when the bit is set to 1.

(3) Reset — The impedance of all I/O and peripheral pins (excluding pins for pull-up option) goes High.

Table 3–3 Pin State of MB89950

Pin name	Normal	Sleep	Stop SPL=0	Stop SPL=1	Reset
COM0 to COM3	COM outputs	COM outputs	Low level outputs	Low level outputs	Low level output
SEG00 to SEG19	Segment outputs	Segment outputs	Low level outputs	Low level outputs	Low level output
P00/SEG20 to P07/SEG27 P10/SEG28 to P17/SEG35 P20/SEG36 to P25/SEG41	Port I/O /Peripheral output	Port I/O /Peripheral output	Port I/O /Peripheral output = Low	High impedance*1 /Peripheral output = Low	High impedance*1
X0	Input for oscillation	Input for oscillation	High impedance*1	High impedance*1	Input for oscillation
X1	Output for oscillation	Output for oscillation	High output	High output	Output for oscillation
MODA	Mode input	Mode input	Mode input	Mode input	Mode input
RST	Reset input	Reset input	Reset input	Reset input	Reset input*2
P30,P31	Port I/O	Port I/O	Port I/O	High impedance*1	High impedance
P32/V1, P33/V2	Port/LCD bias	Port/LCD bias	Port/LCD bias	High impedance*4 /LCD bias	High impedance*5
V3	Input	Input	Input	Input	Input
P40 to P46/INT0	Port/Peripheral I/O	Port/Peripheral I/O	Port/Peripheral I/O	High impedance*1,*3	High impedance*1

*1 The internal input level is fixed to prevent leakage due to open input . Pins for which the pull-up option is selected, enter the pull-up state.

*2 The reset pin may serve as the output depending on the option setting.

*3 For P42 and P46, when edge detection for the external interrupt is selected, only the external interrupt can be input even in the stop mode (SPL = 1).

*4 Whether the pins behave as I/O port or LCD bias depends on the PSEL bit of LCDR (see page 2-60).

*5 These pins are selected as LCD bias after reset. To turn P32 and P33 to ports after reset, set PSEL bit of LCDR to 1 afterwards.

4. INSTRUCTIONS

4.1 Legend

Symbol	Meaning
ext	Extended addressing (addresses 0000 to FFFF)
dir	Direct addressing (addresses 0000 to 00FF)
dir : n	Direct bit addressing (bit position: n = 0 to 7)
rel	Relative addressing (8 bits)
#	Immediate addressing, vector addressing
AH	Upper byte of A
AL	Lower byte of A
TL	Lower byte of T
@	Register indirect addressing Index (with offset) Extra pointer, accumulator
Ri	Memory registers R0 to R7
d8	Immediate data (8 bits)
d16	Immediate data (16 bits)
vct	Vector number (0 to 7
off	Offset (-128 to 127)
MOD	Remainder

Flag (NZVC)

+: Changed by execution of instruction

•: Not changed

R: Reset by execution of instruction

S: Set by execution of instruction

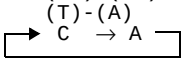
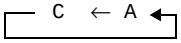
4.2 Transfer Instructions

No	Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP Code
1	MOV dir,A	3	2	(dir) ← (A)	-	-	-	- - - -	45
2	MOV @IX+off,A	4	2	((IX)+off) ← (A)	-	-	-	- - - -	46
3	MOV ext,A	4	3	(ext) ← (A)	-	-	-	- - - -	61
4	MOV @EP,A	3	1	((EP)) ← (A)	-	-	-	- - - -	47
5	MOV Ri,A	3	1	(Ri) ← (A)	-	-	-	- - - -	48 to 4F
6	MOV A,#d8	2	2	(A) ← d8	AL	-	-	+ + - -	04
7	MOV A,dir	3	2	(A) ← dir	AL	-	-	+ + - -	05
8	MOV A,@IX+off	4	2	(A) ← ((IX)+off)	AL	-	-	+ + - -	06
9	MOV A,ext	4	3	(A) ← (ext)	AL	-	-	+ + - -	60
10	MOV A,@A	3	1	(A) ← ((A))	AL	-	-	+ + - -	92
11	MOV A,@EP	3	1	(A) ← ((EP))	AL	-	-	+ + - -	07
12	MOV A,Ri	3	1	(A) ← (Ri)	AL	-	-	+ + - -	08 to 0F
13	MOV dir,#d8	4	3	(dir) ← d8	-	-	-	- - - -	85
14	MOV @IX+off,#d8	5	3	((IX)+off) ← d8	-	-	-	- - - -	86
15	MOV @EP,#d8	4	2	((EP))← d8	-	-	-	- - - -	87
16	MOV Ri,#d8	4	2	(Ri) ← d8	-	-	-	- - - -	88 to 8F
17	MOVW dir,A	4	2	(dir) ←(AH),(dir+1)← (AL)	-	-	-	- - - -	D5
18	MOVW @IX+off,A	5	2	((IX)+off)←(AH),((IX)+off+1)←(AL)	-	-	-	- - - -	D6
19	MOVW ext,A	5	3	(ext) ← (AH),(ext+1)←(AL)	-	-	-	- - - -	D4
20	MOVW @EP,A	4	1	((EP)) ← (AH),((EP)+1)← (AL)	-	-	-	- - - -	D7
21	MOVW EP,A	2	1	(EP) ← (A)	-	-	-	- - - -	E3
22	MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + - -	E4
12	MOVW A,dir	4	2	(AH)←(dir),(AL)←(dir+1)	AL	AH	dH	+ + - -	C5
24	MOVW A,@IX+off	5	2	(AH)←((IX)+off),(AL)←((IX)+off+1)	AL	AH	dH	+ + - -	C6
25	MOVW A,ext	5	3	(AH)←(ext),(AL)←(ext+1)	AL	AH	dH	+ + - -	C4
26	MOVW A,@A	4	1	(AH)←((A)),(AL)← ((A)+1)	AL	AH	dH	+ + - -	93
27	MOVW A,@EP	4	1	(AH)←((EP)),(AL) ←((EP)+1)	AL	AH	dH	+ + - -	C7
28	MOVW A,EP	2	1	(A) ←(EP)	-	-	dH	- - - -	F3
29	MOVW EP,#d16	3	3	(EP)←d16	-	-	-	- - - -	E7
30	MOVW IX,A	2	1	(IX)←(A)	-	-	-	- - - -	E2
31	MOVW A,IX	2	1	(A) ← (IX)	-	-	dH	- - - -	F2
32	MOVW SP,A	2	1	(SP)← (A)	-	-	-	- - - -	E1
33	MOVW A,SP	2	1	(A) ← (SP)	-	-	dH	- - - -	F1
34	MOV @A,T	3	1	((A)) ← (T)	-	-	-	- - - -	82
35	MOVW @A,T	4	1	((A)) ← (TH),((A)+1) ← (TL)	-	-	-	- - - -	83
36	MOVW IX,#d16	3	3	(IX)← d16	-	-	-	- - - -	E6
37	MOVW A,PS	2	1	(A) ← (PS)	-	-	dH	- - - -	70
38	MOVW PS,A	2	1	(PS)← (A)	-	-	-	+ + + +	71
39	MOVW SP,#d16	3	3	(SP)← d16	-	-	-	- - - -	E5
40	SWAP	2	1	(AH) ⇔ (AL)	-	-	AL	- - - -	10
41	SETB dir:n	4	2	(dir):n ← 1	-	-	-	- - - -	A8 to AF
42	CLRB dir:n	4	2	(dir):n ← 0	-	-	-	- - - -	A0 to A7
43	XCH A,T	2	1	(AL) ⇔ (TL)	AL	-	-	- - - -	42
44	XCHW A,T	3	1	(A) ⇔ (T)	AL	AH	dH	- - - -	43
45	XCHW A,EP	3	1	(A) ⇔ (EP)	-	-	dH	- - - -	F7
46	XCHW A,IX	3	1	(A) ⇔ (IX)	-	-	dH	- - - -	F6
47	XCHW A,SP	3	1	(A) ⇔ (SP)	-	-	dH	- - - -	F5
48	MOVW A,PC	2	1	(A) ← (PC)	-	-	dH	- - - -	F0

Notes

1. In byte transfer to A, T u A is only for low bytes.
2. Operands for two or more operand instructions should be stored in the order designated in Mnemonic (Opposite order to F^{2}MC-8 family).

4.3 Operation Instructions

No	Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP Code
1	ADDC A,Ri	3	1	(A) ← (A)+(Ri)+C	-	-	-	+ + + +	28 to 2F
2	ADDC A,#d8	2	2	(A) ← (A)+d8+C	-	-	-	+ + + +	24
3	ADDC A,dir	3	2	(A) ← (A)+(dir)+C	-	-	-	+ + + +	25
4	ADDC A,@IX+off	4	2	(A) ← (A)+((IX)+off)+C	-	-	-	+ + + +	26
5	ADDC A,@EP	3	1	(A) ← (A)+((EP))+C	-	-	-	+ + + +	27
6	ADDCW A	3	1	(A) ← (A)+(T)+C	-	-	dH	+ + + +	23
7	ADDC A	2	1	(AL)← (AL)+(TL)+C	-	-	-	+ + + +	22
8	SUBC A,Ri	3	1	(A) ← (A)-(Ri)-C	-	-	-	+ + + +	38 to 3F
9	SUBC A,#d8	2	2	(A) ← (A)-d8-C	-	-	-	+ + + +	34
10	SUBC A,dir	3	2	(A) ← (A)-(dir)-C	-	-	-	+ + + +	35
11	SUBC A,@IX+off	4	2	(A) ← (A)-((IX)+off)-C	-	-	-	+ + + +	36
12	SUBC A,@EP	3	1	(A) ← (A)-((EP))+C	-	-	-	+ + + +	37
13	SUBCW A	3	1	(A) ← (T)-(A)-C	-	-	dH	+ + + +	33
14	SUBC A	2	1	(AL)← (TL)-(AL)-C	-	-	-	+ + + +	32
15	INC Ri	4	1	(Ri)← (Ri)+1	-	-	-	+ + + -	C8 to CF
16	INCW EP	3	1	(EP)← (EP)+1	-	-	-	- - - -	C3
17	INCW IX	3	1	(IX)← (IX)+1	-	-	-	- - - -	C2
18	INCW A	3	1	(A) ← (A)+1	-	-	dH	+ + - -	C0
19	DEC Ri	4	1	(Ri)← (Ri)-1	-	-	-	+ + + -	D8 to DF
20	DECW EP	3	1	(EP)← (EP)-1	-	-	-	- - - -	D3
21	DECW IX	3	1	(IX)← (IX)-1	-	-	-	- - - -	D2
22	DECW A	3	1	(A) ← (A)-1	-	-	dH	+ + - -	D0
12	MULU A	19	1	(A) ← (AL)*(TL)	-	-	dH	- - - -	01
24	DIVU A	21	1	(A) ← (T)/(AL), MOD”(T)	dL	00	00	- - - -	11
25	ANDW A	3	1	(A) ← (A) ∩ (T)	-	-	dH	+ + R -	63
26	ORW A	3	1	(A) ← (A) ∪ (T)	-	-	dH	+ + R -	73
27	XORW A	3	1	(A) ← (A) ⊕ (T)	-	-	dH	+ + R -	53
28	CMP A	2	1	(TL)-(AL)	-	-	-	+ + + +	12
29	CMPW A	3	1	(T)-(A)	-	-	-	+ + + +	13
30	RORC A	2	1		-	-	-	+ + - +	03
31	ROLC A	2	1		-	-	-	+ + - +	02
32	CMP A,#d8	2	2	(A)-d8	-	-	-	+ + + +	14
33	CMP A,dir	3	2	(A)- dir	-	-	-	+ + + +	15
34	CMP A,@EP	3	1	(A)-((EP))	-	-	-	+ + + +	17
35	CMP A,@IX+off	4	2	(A)-((IX)+off)	-	-	-	+ + + +	16
36	CMP A,Ri	3	1	(A)-(Ri)	-	-	-	+ + + +	18 to 1F
37	DAA	2	1	decimal adjust for addition	-	-	-	+ + + +	84
38	DAS	2	1	decimal adjust for subtraction	-	-	-	+ + + +	94
39	XOR A	2	1	(A) ← (AL) ⊕ (TL)	-	-	-	+ + R -	52
40	XOR A,#d8	2	2	(A) ← (AL) ⊕ d8	-	-	-	+ + R -	54
41	XOR A,dir	3	2	(A) ← (AL) ⊕ (dir)	-	-	-	+ + R -	55
42	XOR A,@EP	3	1	(A) ← (AL) ⊕ ((EP))	-	-	-	+ + R -	57
43	XOR A,@IX+off	4	2	(A) ← (AL) ⊕ ((IX)+off)	-	-	-	+ + R -	56
44	XOR A,Ri	3	1	(A) ← (AL) ⊕ (Ri)	-	-	-	+ + R -	58 to 5F
45	AND A	2	1	(A) ← (AL) ∩ (TL)	-	-	-	+ + R -	62
46	AND A,#d8	2	2	(A) ← (AL) ∩ d8	-	-	-	+ + R -	64
47	AND A,dir	3	2	(A) ← (AL) ∩ (dir)	-	-	-	+ + R -	65
48	AND A,@EP	3	1	(A) ← (AL) ∩ ((EP))	-	-	-	+ + R -	67
49	AND A,@IX+off	4	2	(A) ← (AL) ∩ ((IX)+off)	-	-	-	+ + R -	66
50	AND A,Ri	3	1	(A) ← (AL) ∩ (Ri)	-	-	-	+ + R -	68 to 6F
51	OR A	2	1	(A) ← (AL) ∪ (TL)	-	-	-	+ + R -	72
52	OR A,#d8	2	2	(A) ← (AL) ∪ d8	-	-	-	+ + R -	74
53	OR A,dir	3	2	(A) ← (AL) ∪ (dir)	-	-	-	+ + R -	75
54	OR A,@EP	3	1	(A) ← (AL) ∪ ((EP))	-	-	-	+ + R -	77
55	OR A,@IX+off	4	2	(A) ← (AL) ∪ ((IX)+off)	-	-	-	+ + R -	76
56	OR A,Ri	3	1	(A) ← (AL) ∪ (Ri)	-	-	-	+ + R -	78 to 7F
57	CMP dir,#d8	5	3	(dir) - d8	-	-	-	+ + + +	95
58	CMP @EP,#d8	4	2	((EP))- d8	-	-	-	+ + + +	97
59	CMP @IX+off,#d8	5	3	((IX)+off) - d8	-	-	-	+ + + +	96
60	CMP Ri,#d8	4	2	(Ri) - d8	-	-	-	+ + + +	98 to 9F
61	INCW SP	3	1	(SP)← (SP) + 1	-	-	-	- - - -	C1
62	DECW SP	3	1	(SP)← (SP) - 1	-	-	-	- - - -	D1

4.4 Branch Instructions

No	Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP Code
1	BZ/BEQ rel	3	2	if Z=1 then PC←PC+rel	-	-	-	- - - -	FD
2	BNZ/BNE rel	3	2	if Z=0 then PC←PC+rel	-	-	-	- - - -	FC
3	BC/BLO rel	3	2	if C=1 then PC←PC+rel	-	-	-	- - - -	F9
4	BNC/BHS rel	3	2	if C=0 then PC←PC+rel	-	-	-	- - - -	F8
5	BN rel	3	2	if N=1 then PC←PC+rel	-	-	-	- - - -	FB
6	BP rel	3	2	if N=0 then PC←PC+rel	-	-	-	- - - -	FA
7	BLT rel	3	2	if V⊕N=1 then PC←PC+rel	-	-	-	- - - -	FF
8	BGE rel	3	2	if V⊕N=0 then PC←PC+rel	-	-	-	- - - -	FE
9	BBC dir:b,rel	5	3	if (dir:b)=0 then PC←PC+rel	-	-	-	- + - -	B0 to B7
10	BBS dir:b,rel	5	3	if (dir:b)=1 then PC←PC+rel	-	-	-	- + - -	B8 to BF
11	JMP @A	2	1	(PC)←(A)	-	-	-	- - - -	E0
12	JMP ext	3	3	(PC)←ext	-	-	-	- - - -	21
13	CALLV #vct	6	1	vector call	-	-	-	- - - -	E8 to EF
14	CALL ext	6	3	subroutine call	-	-	-	- - - -	31
15	XCHW A,PC	3	1	(PC)←(A), (A)←(PC)+1	-	-	dH	- - - -	F4
16	RET	4	1	return from subroutine	-	-	-	- - - -	20
17	RETI	6	1	return from interrupt	-	-	-	restore	30

4.5 Other Instructions

No	Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP Code
1	PUSHW A	4	1	SP ← SP-2(SP) ← A	-	-	-	- - - -	40
2	POPW A	4	1	A ← (SP) SP ← SP + 2	-	-	dH	- - - -	50
3	PUSHW IX	4	1	SP ← SP-2(SP) ← IX	-	-	-	- - - -	41
4	POPW IX	4	1	IX ← (SP) SP ← SP + 2	-	-	-	- - - -	51
5	NOP	1	1	NO OPERATION	-	-	-	- - - -	00
6	CLRC	1	1	C ← 0	-	-	-	- - - R	81
7	SETC	1	1	C ← 1	-	-	-	- - - S	91
8	CLRI	1	1	I ← 0	-	-	-	- - - -	80
9	SETI	1	1	I ← 1	-	-	-	- - - -	90

4.6 F²MC-8L Family Instruction Map

H / L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,#d8	MOVW A,PS	CLRI	SETI	CLRB dir:0	BBC dir:0,r	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir:1	BBC dir:1,r	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir:2	BBC dir:2,r	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir:3	BBC dir:3,r	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8	[redacted]	XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir:4	BBC dir:4,r	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir:5	BBC dir:5,r	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	MOV @IX+d,A	XOR A,@IX+d	AND A,@IX+d	OR A,@IX+d	MOV @IX+d,#d	CMP @IX+d,#d	CLRB dir:6	BBC dir:6,r	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir:7	BBC dir:7,r	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir:0	BBS dir:0,r	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir:1	BBS dir:1,r	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir:2	BBS dir:2,r	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir:3	BBS dir:3,r	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir:4	BBS dir:4,r	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir:5	BBS dir:5,r	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir:6	BBS dir:6,r	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir:7	BBS dir:7,r	INC R7	DEC R7	CALLV #7	BLT rel

5. MASK OPTIONS

Table 5–1 Mask Options

No.	Model	MB89953	MB89P95x	MB89PV950
	Specification method	Select when ordering mask	Set by EPROM	Fixed
1	Port pull-up resistor P40 to P46	Can be selected for each pin	Can be selected for each pin	No pull up resistor
2	Port/Segment output P00 to P07, P10 to P17, P20 to P25	Can be selected for every 8 to 1 pins*2	Port/Segment output *3	Port/Segment output *3
3	Power-on reset Power-on reset available Power-on reset unavailable	Can be selected	Can be selected	Power-on reset available
4	Selection of main clock oscillation stabilization time (at 5 MHz)*1 About $2^{18}/f_{ch}$ (about 52.4 ms) About $2^{14}/f_{ch}$ (about 3.28 ms)	Can be selected	Can be selected	$2^{18}/f_{ch}$
5	Reset pin output Reset output available Reset output unavailable	Can be selected	Can be selected	Reset output available

*1 The main clock oscillation stabilization time is generated by dividing the main clock oscillation. Since the oscillation cycle is unstable immediately after oscillation starts, the time in this table is only a guide.

*2 Port/segment output switching should be specified in the same manner as the port allocation set by the segment output select register in the LCD controller described on page 2-61.

*3 When those pins are used as ports, applied voltage should never be higher than V3.

Table 5–2 Recommended port/segment mask option combinations

Number of segments	Number of I/O ports *1	Mask Options						
		P00/SEG20 to P07/SEG27	P10/SEG28 to P13/SEG31	P14/SEG32 to P15/SEG33	P16/SEG34	P17/SEG35	P20/SEG36 to P23/SEG39	P24/SEG40 to P25/SEG41
42	11	X	X	X	X	X	X	X
41	12	X	X	X	X	O	X	X
40	13	X	X	X	O	O	X	X
38	15	X	X	O	O	O	X	X
34	19	X	O	O	O	O	X	X
26	27	O	O	O	O	O	X	X
40	13	X	X	X	X	X	X	O
22	31	O	O	O	O	O	O	X
20	33	O	O	O	O	O	O	O

X = Mask option is selected for LCD segment outputs

O = Mask option is selected for port outputs

*1 This column of numbers assume that all the multiplexed peripherals are disabled.

If any customer want to choose the mask option combination which is not shown in Table 5–2, please inform Fujitsu for special testing arrangement.

APPENDIX

Appendix A I/O Map

Addresses 00_H to $7F_H$

Address	Read/Write	Register	Description of register
00_H	(R/W)	PDR0	Port-0 data register
01_H			
02_H	(R/W)	PDR1	Port-1 data register
03_H			
04_H	(R/W)	PDR2	Port-2 data register
05_H			
06_H			
07_H			
08_H	(R/W)	STBC	Standby control register
09_H	(R/W)	WDTC	Watchdog timer control register
$0A_H$	(R/W)	TBCR	Time-base timer control register
$0B_H$			
$0C_H$	(R/W)	PDR3	Port-3 data register
$0D_H$			
$0E_H$	(R/W)	PDR4	Port-4 data register
$0F_H$	(W)	DDR4	Port-4 data direction register
10_H			
11_H			
12_H	(R/W)	CNTR	PWM timer control register
13_H	(W)	COMR	PWM timer compare register
14_H	(R/W)	PCR1	PWC pulse width control register 1
15_H	(R/W)	PCR2	PWC pulse width control register 2
16_H	(R/W)	RLBR	PWC reload buffer register
17_H	(R/W)	NCCR	PWC noise reduction control register
18_H			
19_H			
$1A_H$			
$1B_H$			
$1C_H$	(R/W)	SMR	Serial mode register
$1D_H$	(R/W)	SDR	Serial data register
$1E_H$			
$1F_H$			
20_H	(R/W)	SMC1	UART serial mode control register 1
21_H	(R/W)	SRC	UART serial rate control register
22_H	(R/W)	SSD	UART serial status/data register

(continued)

(continued)

Address	Read/Write	Register	Description of register
23_H	(R/W)	SIDR/SODR	UART serial data register
24_H	(R/W)	SMC2	UART serial mode control register 2
25_H			
26_H			
27_H			
28_H			
29_H			
$2A_H$			
$2B_H$			
$2C_H$			
$2D_H$			
$2E_H$			
$2F_H$			
30_H	(R/W)	EIC1	External interrupt 1 control register 1
31_H to 63_H			
64_H to 78_H	(R/W)	VRAM	Display data RAM
79_H	(R/W)	LCDR	LCD control register
$7A_H$	(R/W)	SEGR	Segment output select register
$7B_H$			
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$	—	ITR	Interrupt test register

Note:— indicates the vacant area, it is not used

Appendix B Writing EPROM

Functions equivalent to the MBM27C256A can be used in the MB89P955 EPROM mode. Accordingly, the user can write data with a general-purpose EPROM writer by using a dedicated adapter. Note that the electrical signature mode is not supported.

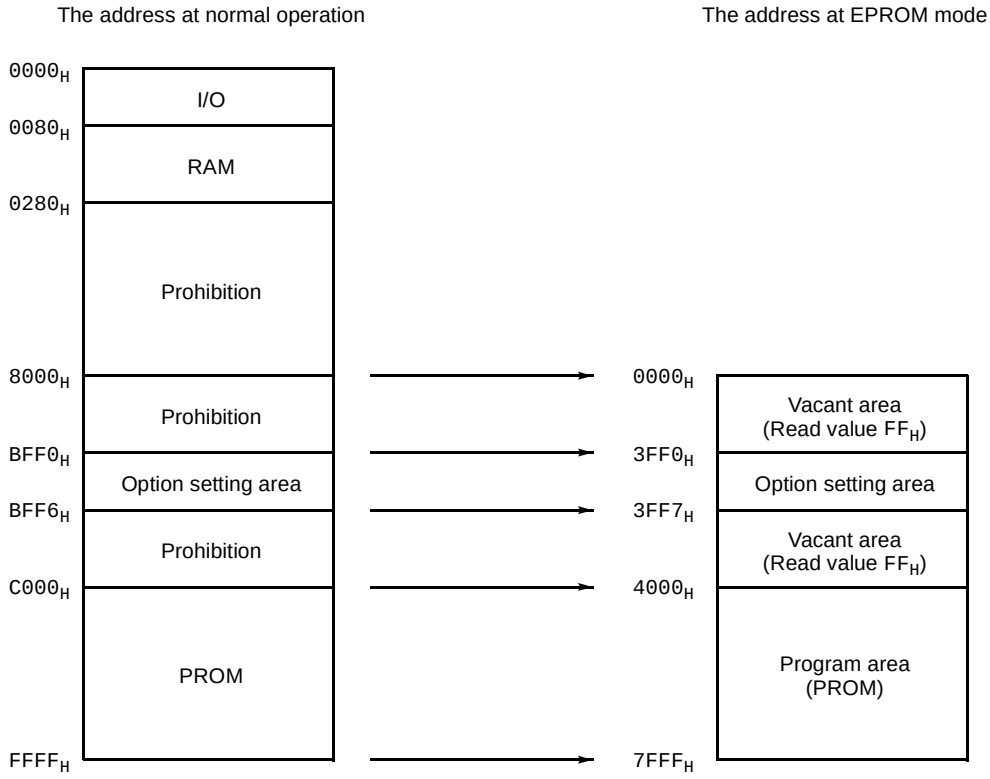
• Writing procedure

(1) Set the EPROM writer for the MBM27C256A.

(2) Load program data from 4000_H to $7FFF_H$ of the EPROM writer (Note that $0C000_H$ to $0FFFF_H$ in the operation mode are equivalent to 4000_H to $7FFF_H$ in the EPROM mode).
Load option data from $3FF0_H$ to $3FF6_H$ of the EPROM writer (See Bit Map on the next page for the correspondence to each option).

(3) Write the data with the EPROM writer.

The memory space in the EPROM mode is shown below.



• ROM writer adapter (by SUN HAYATO)

Package number	Adapter model number
FPT-64P-M09	ROM-64QF2-28DP-8L3

• Bit Map for PROM Option

	7	6	5	4	3	2	1	0
$3FF0_H$	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Oscillation stabilization time 1: $2^{18}/f_{ch}$ 0: $2^{14}/f_{ch}$	Reset pin Output 1:Available 0:Unavailable	Power-on Reset 1:Available 0:Unavailable	Vacant Readable/ Writable	Vacant Readable/ Writable
$3FF1_H$	Vacant Readable/ Writable	P46 Pull-up 1:Unavailable 0:Available	P45 Pull-up 1:Unavailable 0:Available	P44 Pull-up 1:Unavailable 0:Available	P43 Pull-up 1:Unavailable 0:Available	P42 Pull-up 1:Unavailable 0:Available	P41 Pull-up 1:Unavailable 0:Available	P40 Pull-up 1:Unavailable 0:Available
$3FF2_H$	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable
$3FF3_H$	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable
$3FF4_H$	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable
$3FF5_H$	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable
$3FF6_H$	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable	Vacant Readable/ Writable

Note: Initial value is 1 at each bit

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel:(044)754-3753
Fax:(044)754-3329

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel:(408)922-9000
Fax:(408)432-9044/9045

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel:(06103)690-0
Fax:(06103)690-122

Asia Pacific

FUJITSU MICROELECTONICS ASIA PTE. LIMITED
No. 51 Bras Basah Road,
Plaza By The Park,
#06-04 to #06-07
Singapore 189554
Tel:336-1600
Fax:336-1609

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