Addendum and Corrections of the Hardware Manual HM90495-draftv1-6

Version : hm90495-draftV1-6-corr-x1-00

1. UART 0/1 clock

If clock input output SCK0/SCK1 is used, some conflicts may occur. This problem will be fixed with MB90V495G and MB90F497G version.

2. CAN Interface

Under very certain circumstances, it possibly may happen that the CPU reads wrong data from the CAN-RAM if the CAN Macro itself has access to the CAN RAM as well. This may lead to wrong CAN data reception or CPU register corruption. This problem will be fixed in MB90V495G and MB90F497G version.

The following entries contains all known errors of the Hardware Manual of MB90495 series.

Chapter 11. Watch Timer

Figure: 11.2-1 Configuration of the Watch Timer Control Register (WTC) (Page 257)

			Interval time
WTC2	WTC1	WTC0	Sub osc. 32.768KHz
0	0	0	31.25ms
0	0	1	62.5ms
0	1	0	125ms
0	1	1	250ms
1	0	0	500ms
1	0	1	1s
1	1	0	2s
1	1	1	4s

Chapter 17 CAN

Chapter 17.4.4 Bit Timing Register (BTR) (page 387)

Old:

For correct operation, the following conditions should be met.

BT >= 8TQ
TSEG2 >= RSJW + 2TQ*1
TSEG1 >= delay time*2 + RSJW

*1) 2TQ: Data processing time
*2) Delay time: Twice as long as the sum of the bus propagation, input comparator and output driver delay

New:

For correct operation of the CAN controller, the following conditions should be met:

Devices with "G" suffix:

For 1 <= PSC <= 63:
TSEG1 >= 2TQ
TSEG1 >= RSJW
TSEG2 >= 2TQ
TSEG2 >= RSJW

For PSC = 0:
TSEG1 >= 5TQ
TSEG2 >= 2TQ
TSEG2 >= RSJW

Devices without "G" suffix:

For 1 <= PSC <= 63:
TSEG1 >= RSJW
TSEG2 >= RSJW + 2TQ

For PSC = 0:
TSEG1 >= 5TQ
TSEG2 >= RSJW + 2TQ

In order to meet the Bit Timing requirements defined in the CAN Specification, additional conditions have to be met, e.g. the propagation delay has to be considered.

Chapter 8 UART1:

8.1 Overview of UART1 (page 188)

In the description : ... (Multiprocessor mode) is only available for the master system.

In the table 8.1-1:

Old:

Transfer mode: clock synchronous (using start and stop bits)

New:

Transfer Mode: clock synchronous

Chapter 8.0 Uart1 (p. 195)

There is a typo in the table **8.4.3-1 'function of each bit of status register 1 (SSR1)'**. For the bits PE, ORE and FRE it is mentioned that to clear this bits the RFC bit in the SMR1 register has to be set to '0'.

Correction:

The REC bit in the SCR1 register has to be set.

Chapter 12. 16bit I/O Timer

The FRT Timer Control Status register includes 3 clock select bits, CLK2, CLK1, CLK0. These clock selection bits enable one of eight clock sources to be selected.

Old: The 16-bit free-run timer consists of a 16-bit up counter, control register and prescaler. The values output from this timer counter are used as the base timer for input capture.
• Four counter clocks are available.
Internal clock: $\phi/4$, $\phi/16$, $\phi/64$, $\phi/256$

Should be replaced with:

The 16-bit free-run timer consists of a 16-bit up counter, control register and prescaler. The values output from this timer counter are used as the base timer for input capture.

• Eight counter clocks are available.

Internal clock: ϕ, ϕ/2, ϕ/4, ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128

Chapter 21 Interrupts

Chapter 21.4.5 Hardware Interrupts (page450)

Interrupt handling time:

incorrect formula:

Old:

Θ = 24 + 6 + Z

Θ = 11 + 6 + Z

New:

Θ = 24 + 6 * Z

Θ = 11 + 6 * Z

Power On : Port behaviour

When the external reset, RSTX, is not asserted during Power On, pins on port 0 and 1 will be in an undefined state. Pins on port 2, 3, 4, 5 and 6 enter High-Z upon Power on reset.

To make sure that all ports are High-Z, the external reset RSTX must be kept asserted for the entire power on reset period.

If the external reset gets disasserted during the power on reset period, the pins on port 0 and 1 will become undefined.

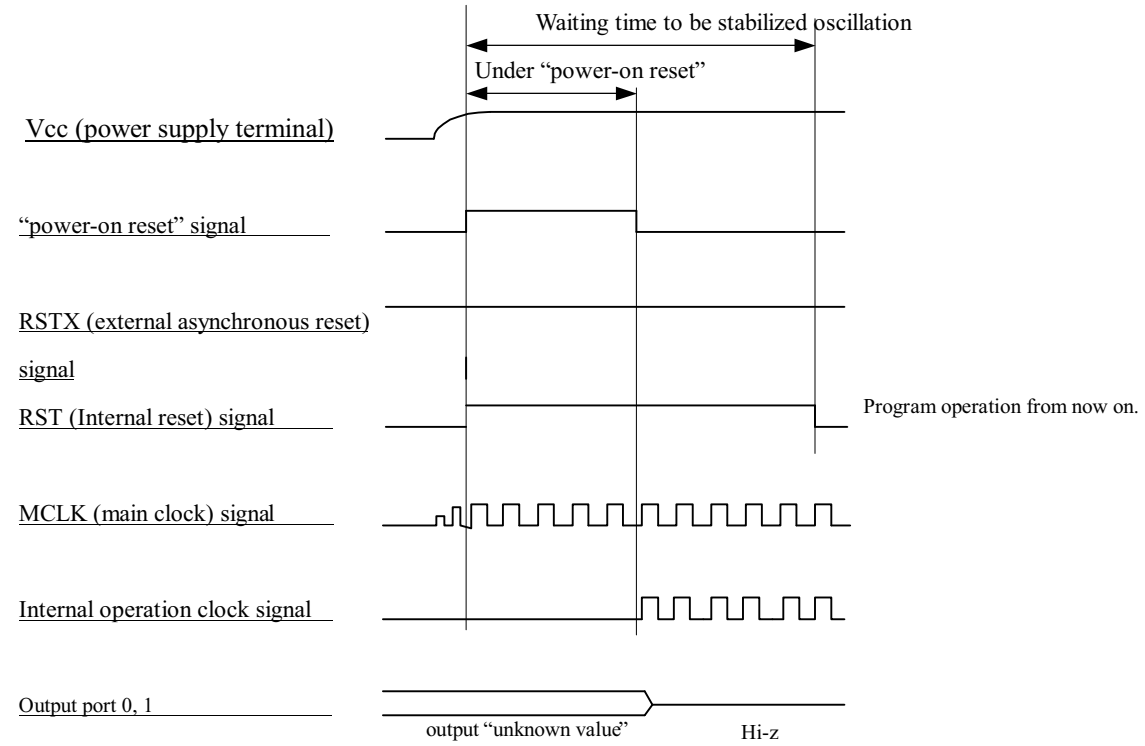
Output “unknown value” , when the power supply is turned on If F^2MC-16LX is used.

Note:
Output “unknown value” of pin 00 to pin 7 and pin 10 to pin 17 terminal, when the power supply Is turned on.

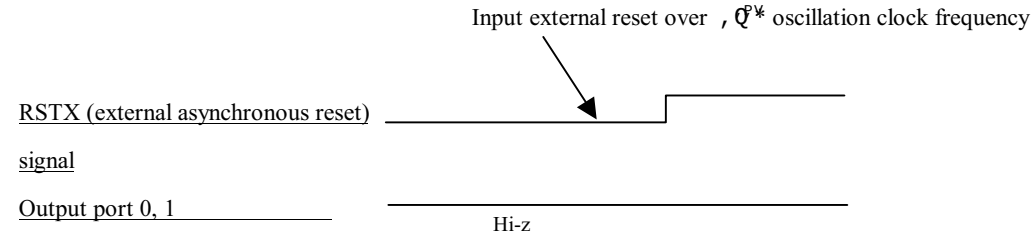
Pin 00 to pin 07 and pin 10 to pin 17 terminal become “unknown value” (output “H”, “L” level or output “Hi-z”) under “power-on reset” (stabilized times (2¨ * oscillation clock frequency) of clamping circuit for internal power supply), when the power supply is turned on, and when “power-on reset” function operates and RSTX terminal is “H” level.
If you want to output “Hi-z” under “power-on reset”, it is applied reset input “ “L” level “ from external and so pin 00 to pin 07 and pin 10 to pin 17 terminal become “Hi-z” condition during the time.

It shows timing chart in detail the next page.

Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)



How to output “Hi-z” under “power-on reset”



Timing chart

Under “power-on reset” 2^{17} * oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation 2^{17} * oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz)

Chapter 21 Interrupts and EIIOS Function

Figure 23.1 1-2. Interrupt Control Registers (p. 436)

Bits 4 and 5, S0 and S1 are read Only bits.

R/W: Read/write
R: Write-only
- : Not used
X: Undefined
: Initial value

The above is incorrect and should read:

R/W: Read/write
R: Read-only
- : Not used
X: Undefined
: Initial value

Register ICCS Extended Intelligent IO Service Status register

Bit 4, ICCS_IF should read:

After data transfer, the buffer address pointer is not updated.
0 IOA update/fixed selection bit
1 After data transfer, the I/O register address pointer is updated. (*2)

Chapter 22 Setting a mode

Figure 22.3-3 Correspondence between access areas and physical addresses in different modes (page 475)

wrong address for lower external bus area mentioned.

old:

0037FFh

0010FFh

New:

0037FFh

002000

Chapter 22.4.3 Detailed Register Settings, page 478

[bit9, 8] LMR1, LMR0

Old:

These bits determine the automatic wait function for external access to the area 001100h to 7FFFFFh. (002100h to 7FFFFFFh for MB90V495)

New:

These bits determine the automatic wait function for external access to the area 002000h to 7FFFFFh. (002100h to 7FFFFFFh for MB90V495)

(3) Bus Control select Register, page 480

[bit 9] LMBS

old:

In 16-bit external area data bus mode, this bit controls the bus size for external access to the area 001100h to 7FFFFFh. (002100h to 7FFFFFFh for MB90V495)

New:
In 16-bit external area data bus mode, this bit controls the bus size for external access to the area 002000h to 7FFFFFh. (002100h to 7FFFFFFh for MB90V495)

Chapter 4 Clocks

Chapter 4.1 Clocks (page 80)

The max. oscillation clock is 16MHz.

Old:

Note
Although an oscillation clock of 3 MHz to 32 MHz can be generated when the operating voltage is 5 V, the maximum operating frequency for the CPU and peripheral functions is 16 MHz. …

Correction:

Note
Although an oscillation clock of 3 MHz to 16 MHz can be generated when the operating voltage is 5 V, the maximum operating frequency for the CPU and peripheral functions is 16 MHz. …

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